Finite State Machines
4190.309
2008 Fall Semester

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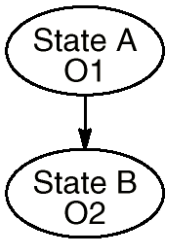
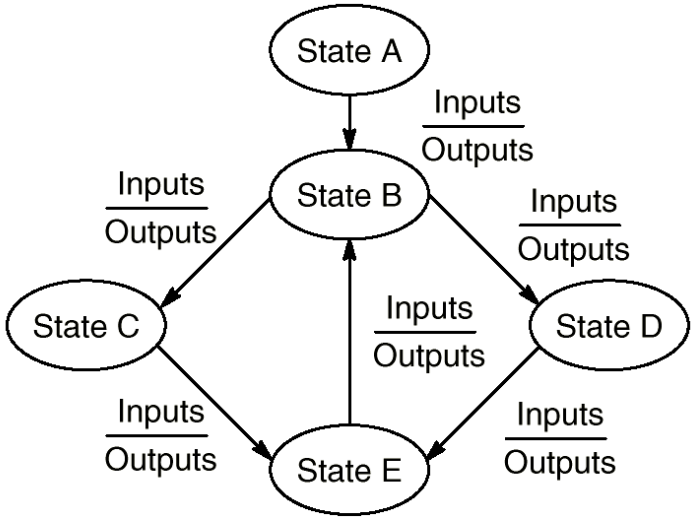
What is state machine?

- A state is a set of values measured at different parts of the circuit.
- A state machine is a digital device that traverses through a predetermined sequence of states in an orderly fashion.
- A synchronous state machine distinguishes state by the clock.

State diagram

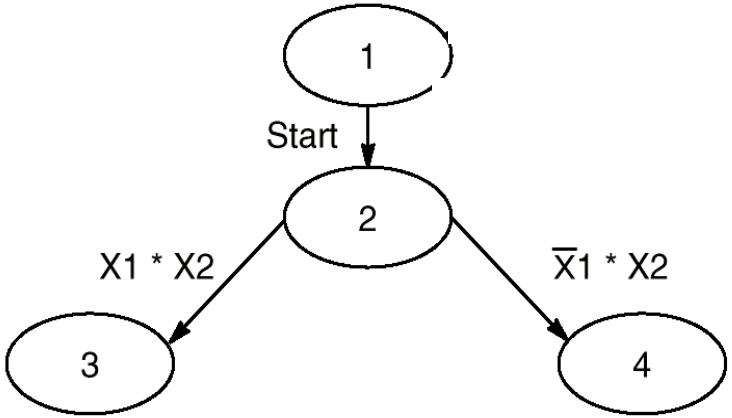
- Mealy model
- Moore model output





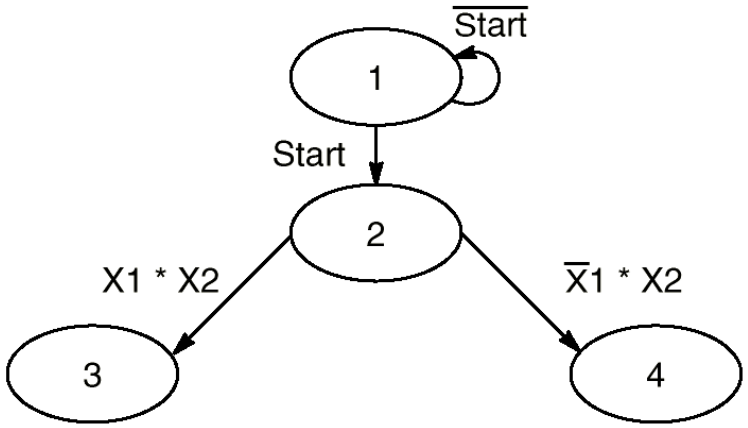
State diagram (2)

- Asynchronous state diagram
  - State machine remains forever in State 1 unless Start becomes active.



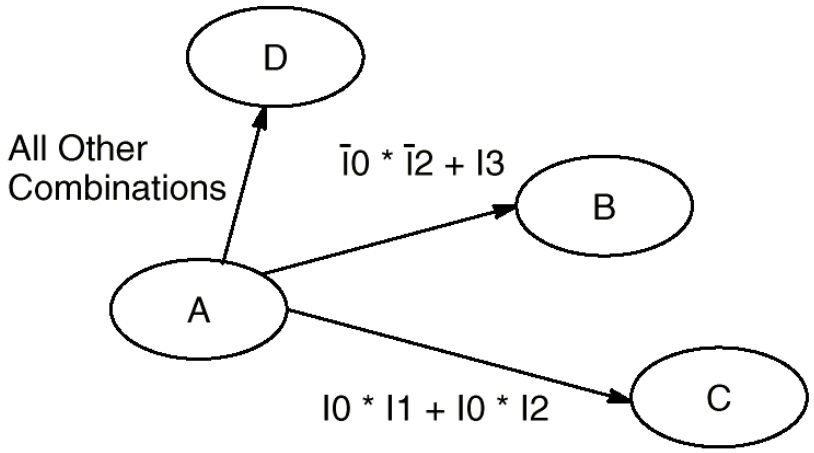
State diagram (3)

- Synchronous state machine
  - State transition has to be made in every clock cycle.
  - The sum of branch conditions has to be 1.



State diagram (4)

- Branch condition example



State transition table

- Format of state transition table

Present State	Inputs	Next State	Outputs Generated
S0 – Sn	I0 – Im	S0 – Sn	O0 – Op

State assignment

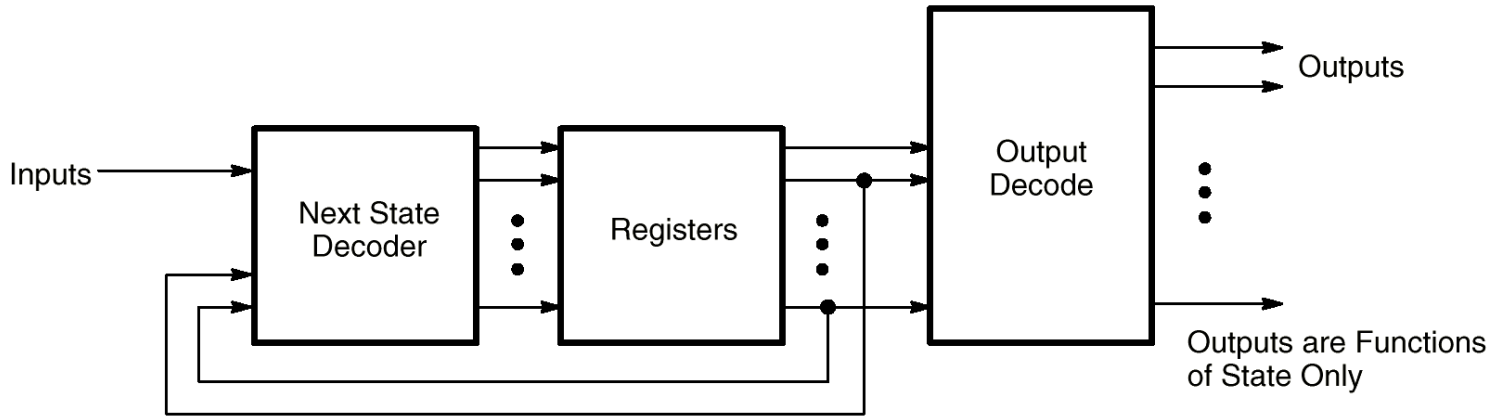
- State encoding
  - Identify each state by a unique name
- Non-redundant encoding
  - Binary encoding
  - Gray code encoding
- Redundant encoding
  - One-hot encoding
  - BCD encoding

One-hot encoding

- Use of n-bit code for n states
  - S1: 0000000001
  - S2: 0000000010
  - S3: 0000000100

Model of state machines

- Moore Model

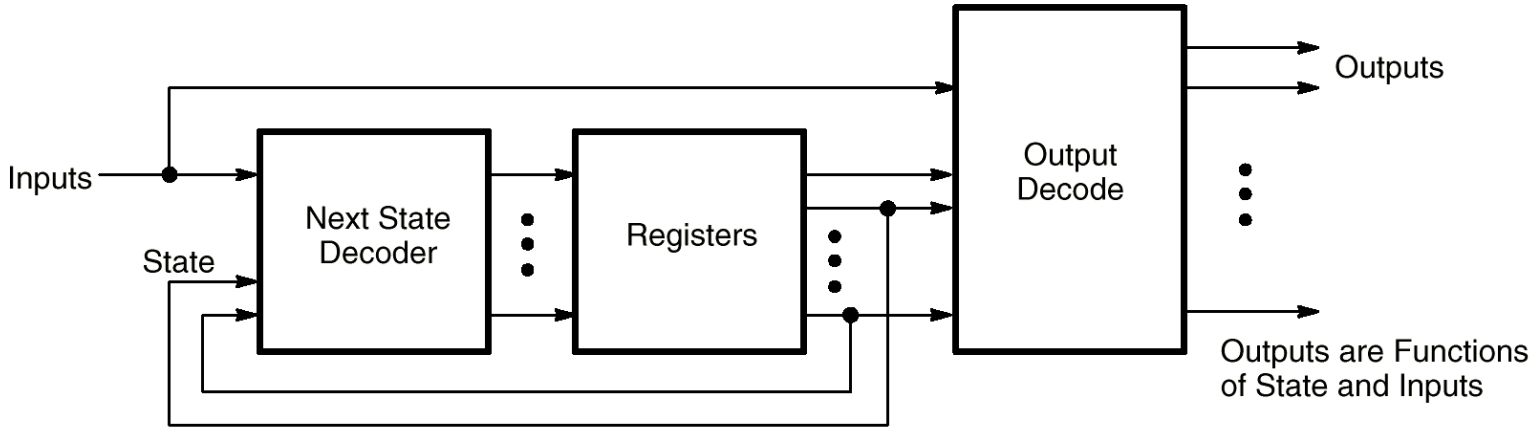


Example

- Design a clock-enable DFF with a primitive DFF

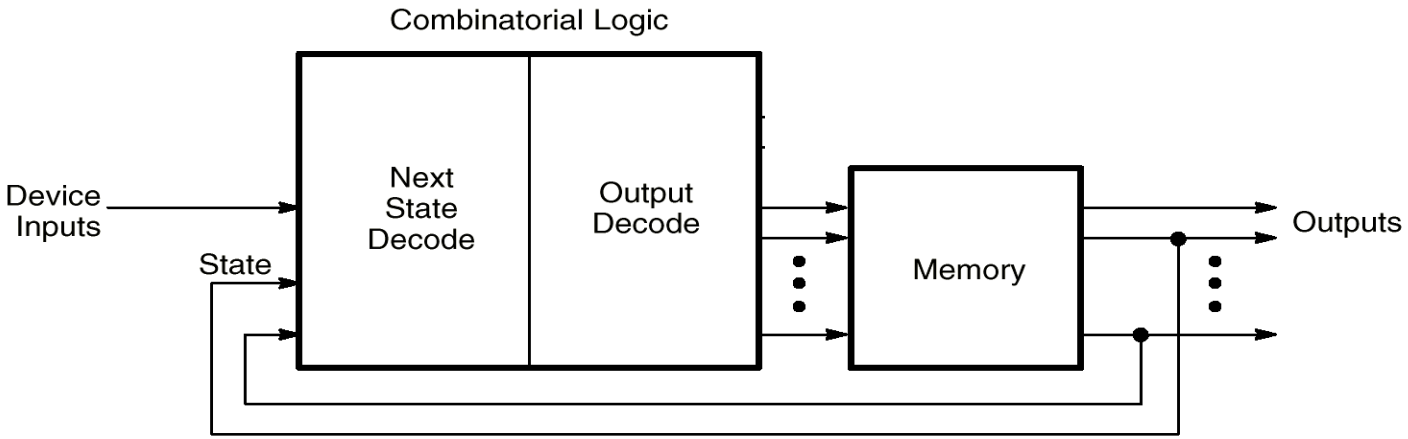
Model of state machines (2)

- Mealy model



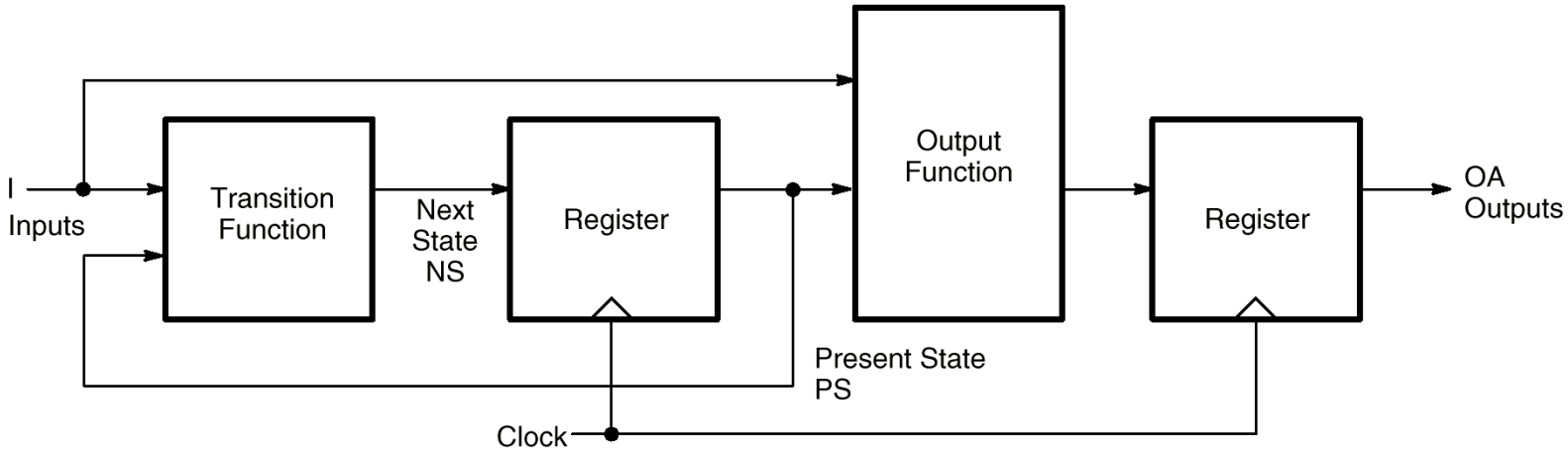
Model of state machines (3)

- Basic model



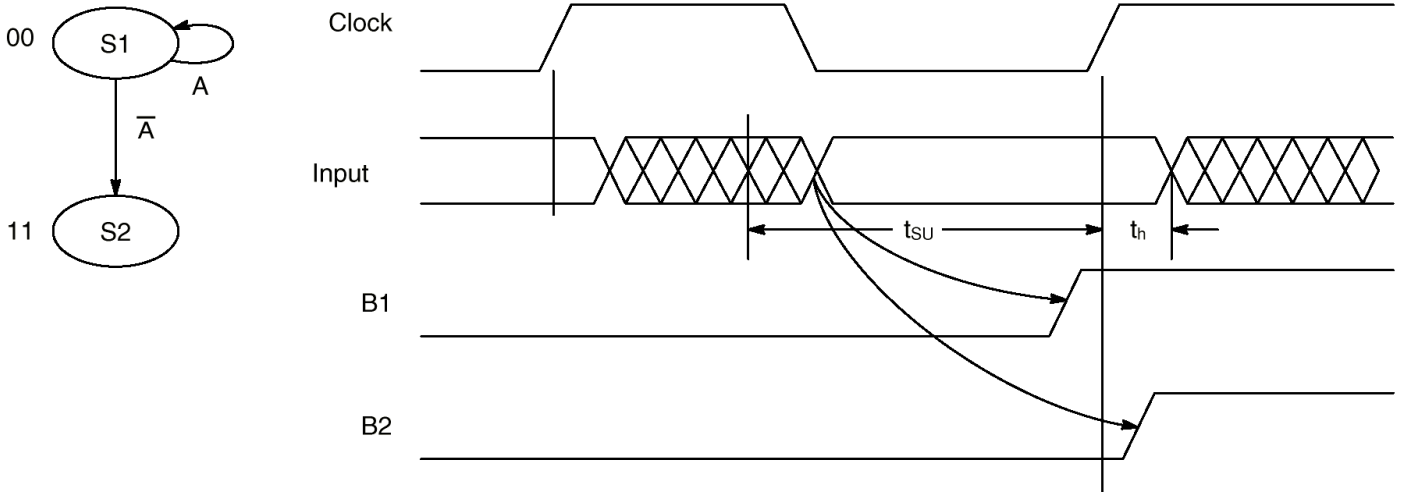
Output synchronization

- Prevent from glitch
- Increase output delay



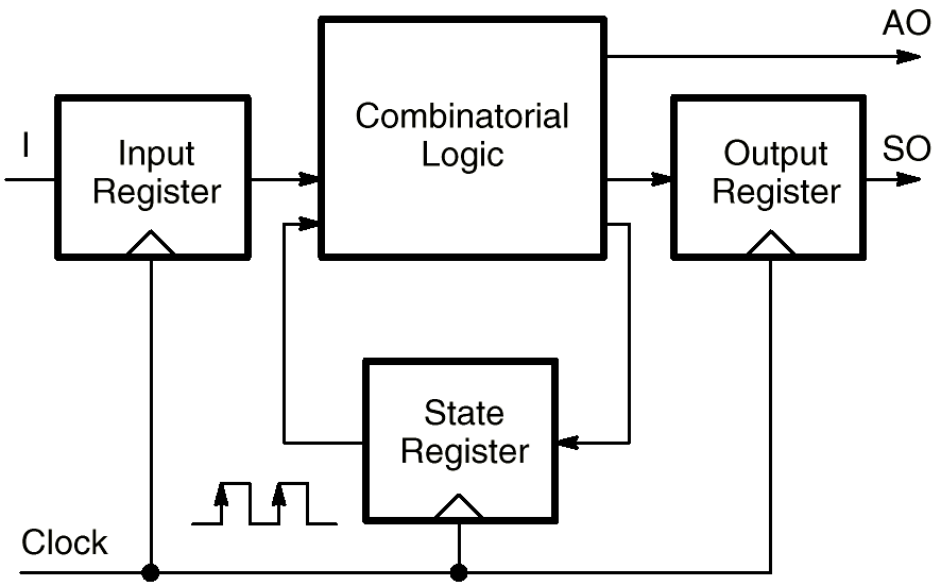
Input synchronization

- Prevent from timing fault
- Increase delay

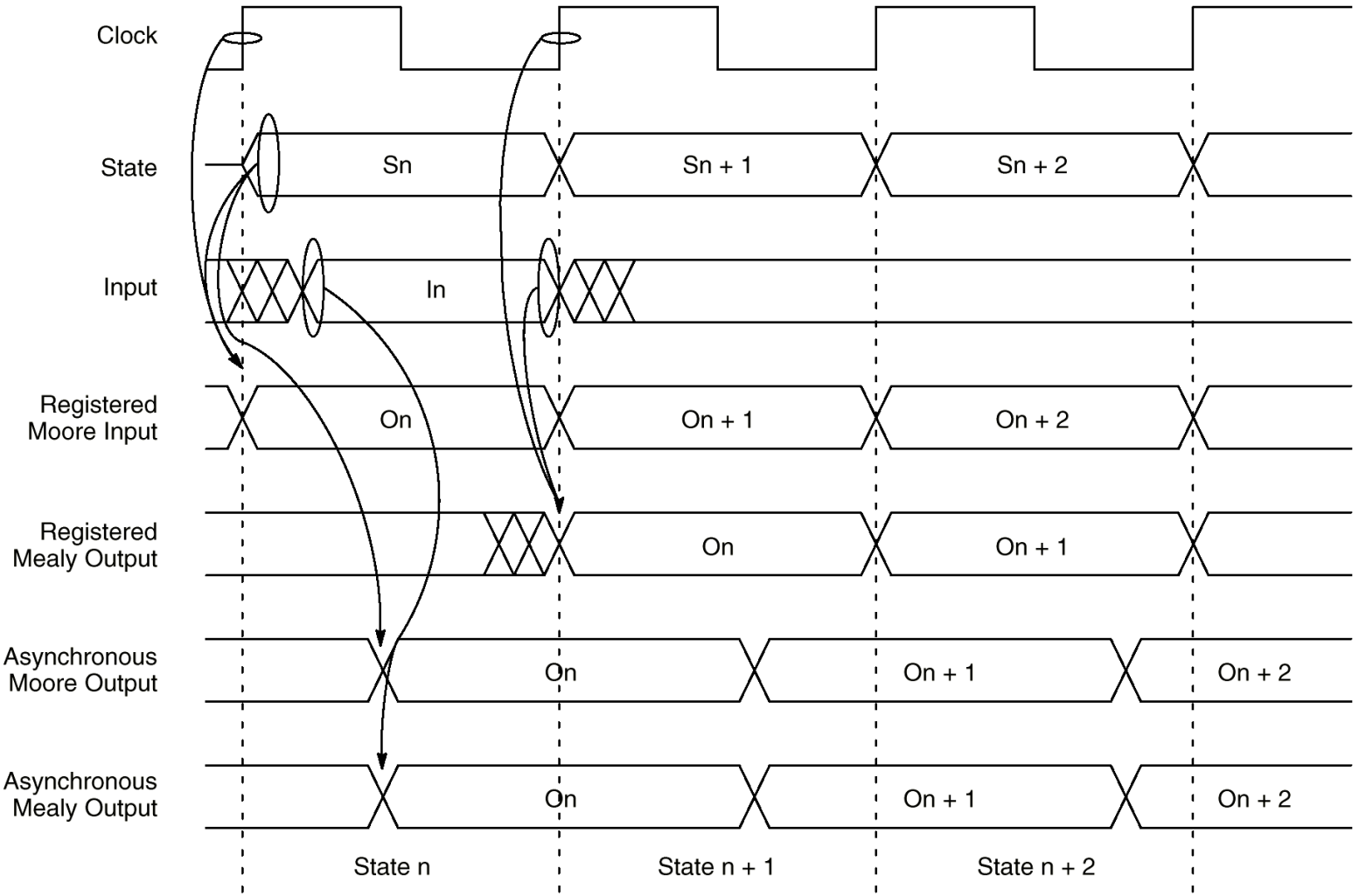


Generic synchronous state machine

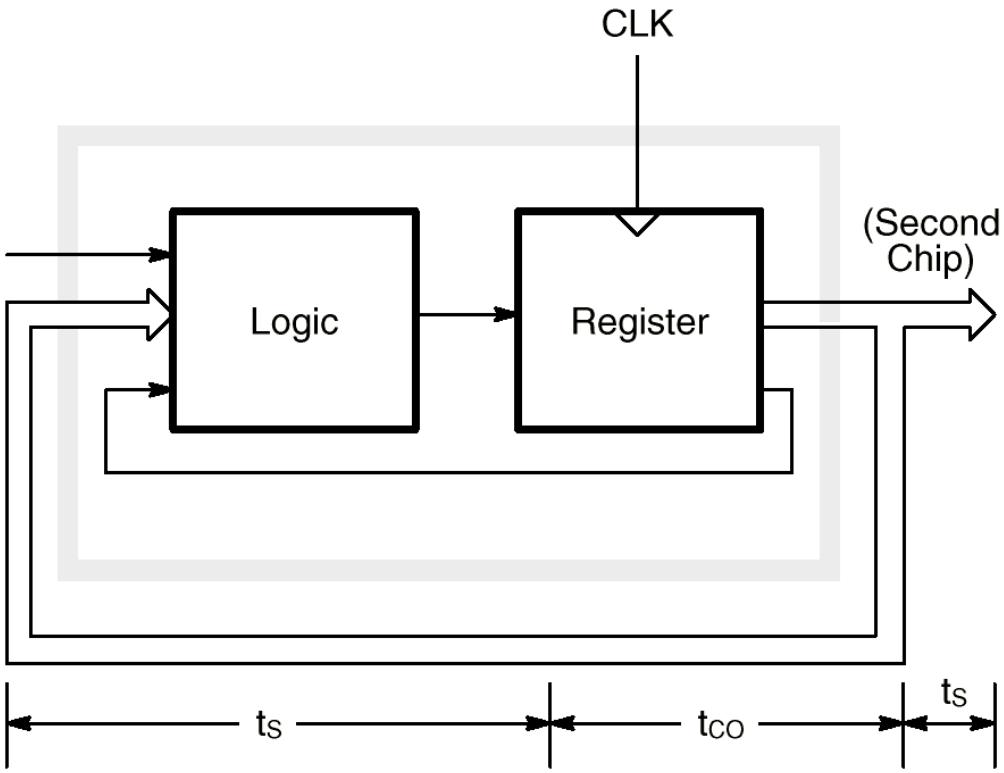
- I/O synchronization registers



Timing diagram



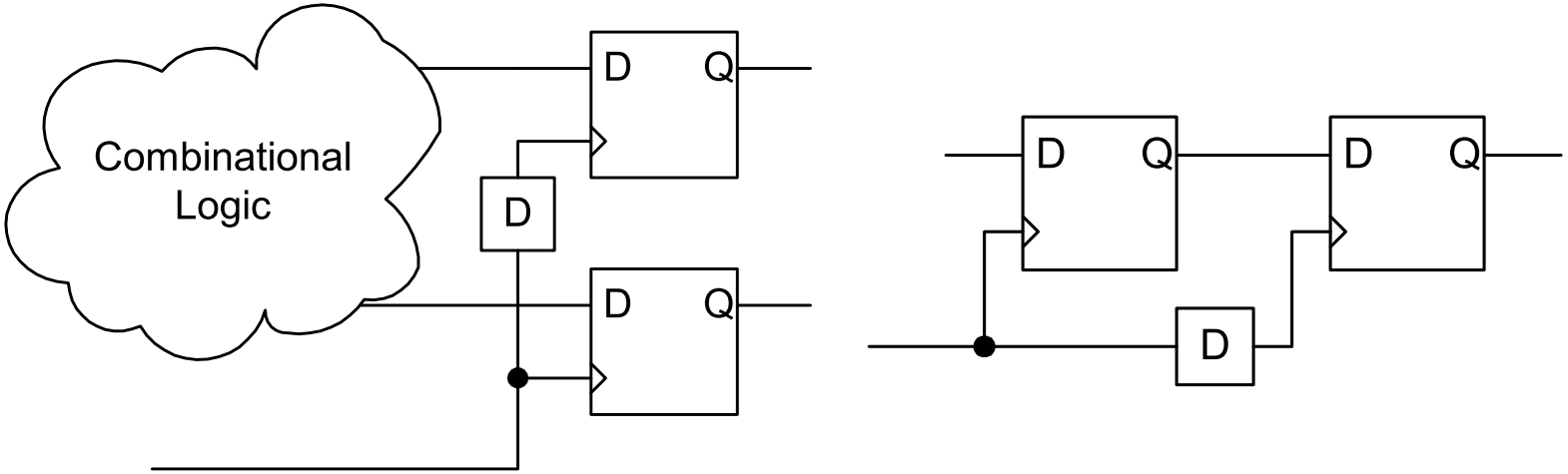
Maximum operating frequency



f_{MAX} External: $1/(t_S + t_{CO})$

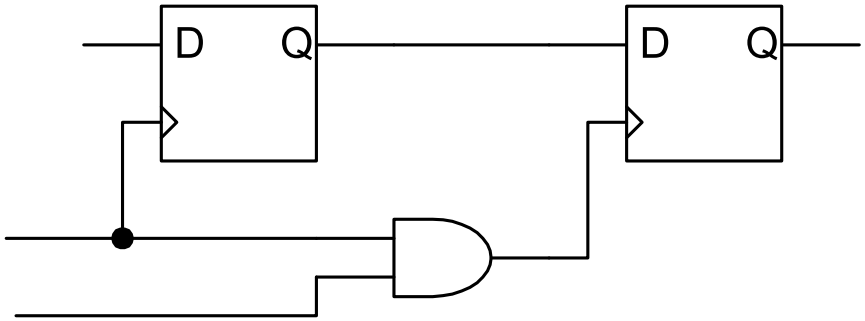
Clock skew

- Timing fault



Clock skew (2)

- Clock skew is caused by
  - Net delay
  - Artificial delay



Rule of thumb

- Never introduce signal transition that is not synchronized the clock in the synchronous state machines.

Note: Some figures are from Publication # 90005, Rev. A, Amendment/0, Issue Date: June 1993 and Publication # 90004, Rev. A, Amendment/0, Issue Date: February 1996 from Advanced Micro Devices.