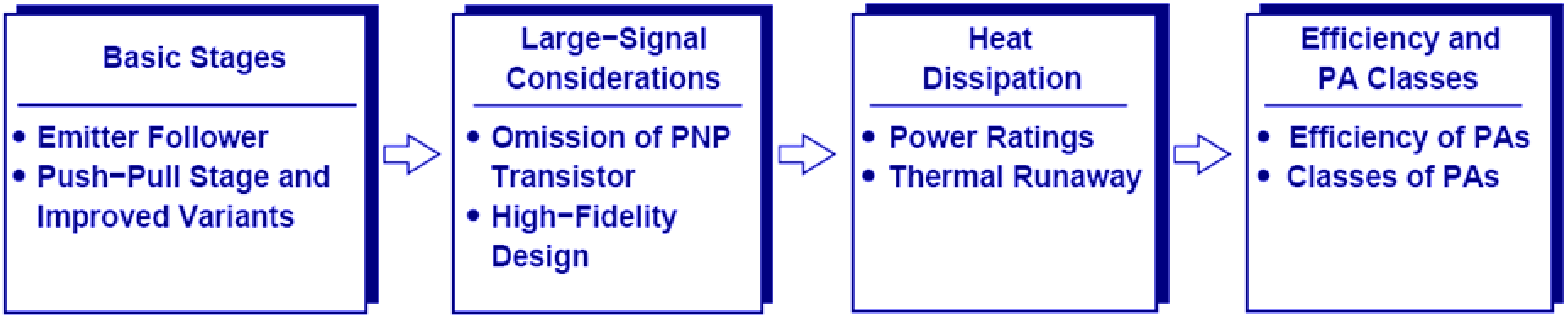
Chapter 13 Output Stages and Power Amplifiers

- 13.1 General Considerations
- 13.2 Emitter Follower as Power Amplifier
- 13.3 Push-Pull Stage
- 13.4 Improved Push-Pull Stage
- 13.5 Large-Signal Considerations
- 13.6 Short Circuit Protection
- 13.7 Heat Dissipation
- 13.8 Efficiency
- 13.9 Power Amplifier Classes

Why Power Amplifiers?

- Drive a load with high power.
- Cellular phones need 1W of power at the antenna.
- Audio systems deliver tens to hundreds of watts of power.
- Ordinary Voltage/Current amplifiers are not suitable for such applications

Chapter Outline



Basic Stages

- Emitter Follower
- Push-Pull Stage and Improved Variants

Large-Signal Considerations

- Omission of PNP Transistor
- High-Fidelity Design

Heat Dissipation

- Power Ratings
- Thermal Runaway

Efficiency and PA Classes

- Efficiency of PAs
- Classes of PAs

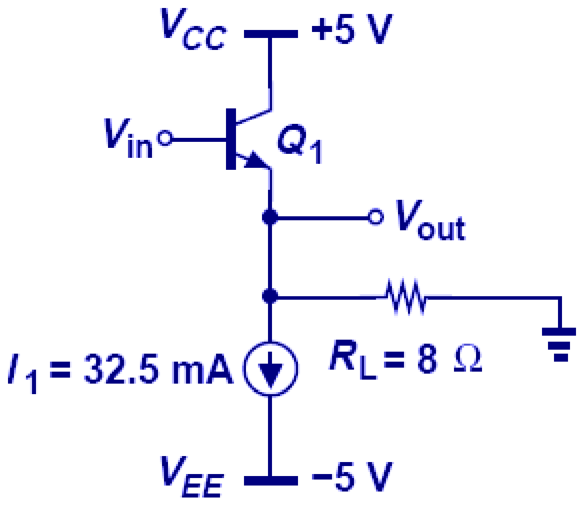
Power Amplifier Characteristics

- **Experiences low load resistance.**
- **Delivers large current levels.**
- **Requires large voltage swings.**
- **Draws a large amount of power from supply.**
- **Dissipates a large amount of power, therefore gets “hot”.**

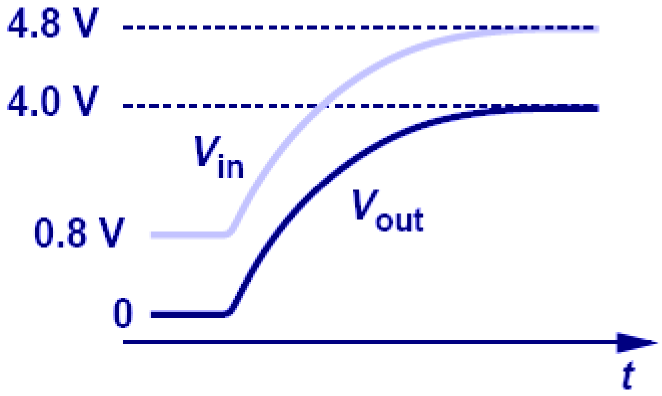
Power Amplifier Performance Metrics

- **Distortion - Linearity**
- **Power Efficiency**
- **Voltage Rating – Transistor Breakdown voltage**

Emitter Follower Large-Signal Behavior I



(a)



(b)

$$A_v = R_L / (R_L + 1/g_m)$$

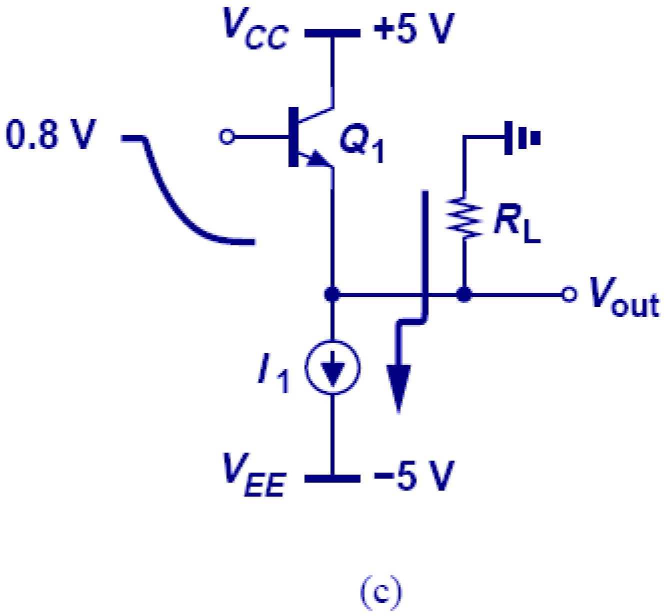
$$\text{For } R_L = 8\ \Omega,$$

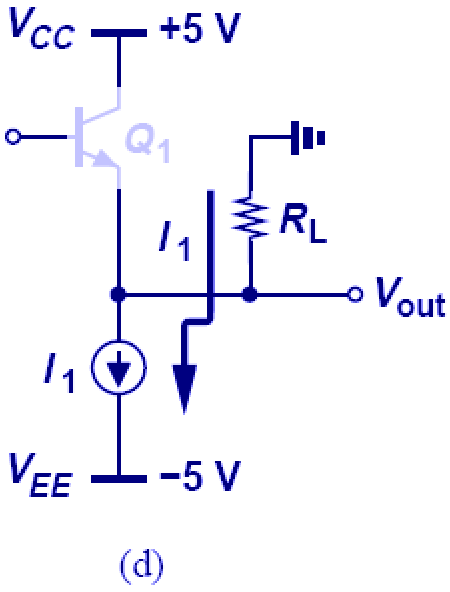
$$1/g_m = 0.8\ \Omega,\ \text{thus, } I_C = 32.5\ \text{mA}$$

- **As V_{in} increases V_{out} also follows and Q_1 provides more current.**

- **For V_{in}=4.8V, V_{out}=4.0V, I_L=500mA, I_{E1}=532.5mA**

Emitter Follower Large-Signal Behavior II



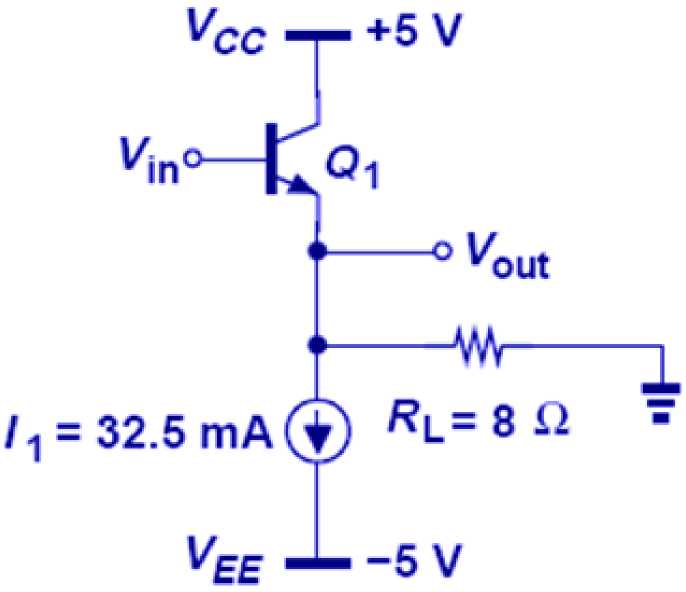


- However, as V_{in} decreases, V_{out} also decreases, shutting off Q_1 and resulting in a constant V_{out}.

- For V_{in}=0.8V, V_{out}=0V, I_L=0mA, I_{E1}=32.5mA
- For V_{in}=0.7V, V_{out}=-0.1V, I_L=12.5mA, I_{E1}=20mA
- When all current (32.5mA) flows to the load, V_{out}=-0.26V

Example 13.1: Emitter Follower

- $V_{in}=0.5V$, $V_{out}=?$



$$V_{in}-V_{BE1}=V_{out}\ ,\ \ \frac{V_{out}}{R_L}+I_1=I_{C1}$$

$$V_{BE1}=V_T\ln(I_{C1}/I_S)$$

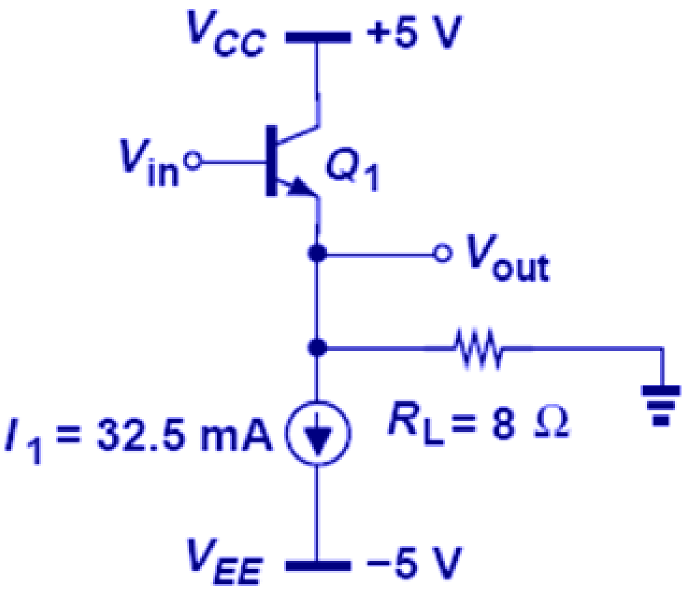
$$V_{in}-V_T\ln\left[\left(\frac{V_{out}}{R_L}+I_1\right)\frac{1}{I_S}\right]=V_{out}$$

For $V_{in}=0.5\ V$

$\Rightarrow V_{out}\approx -211$ mV by a few iterations

Example 13.1: Emitter Follower

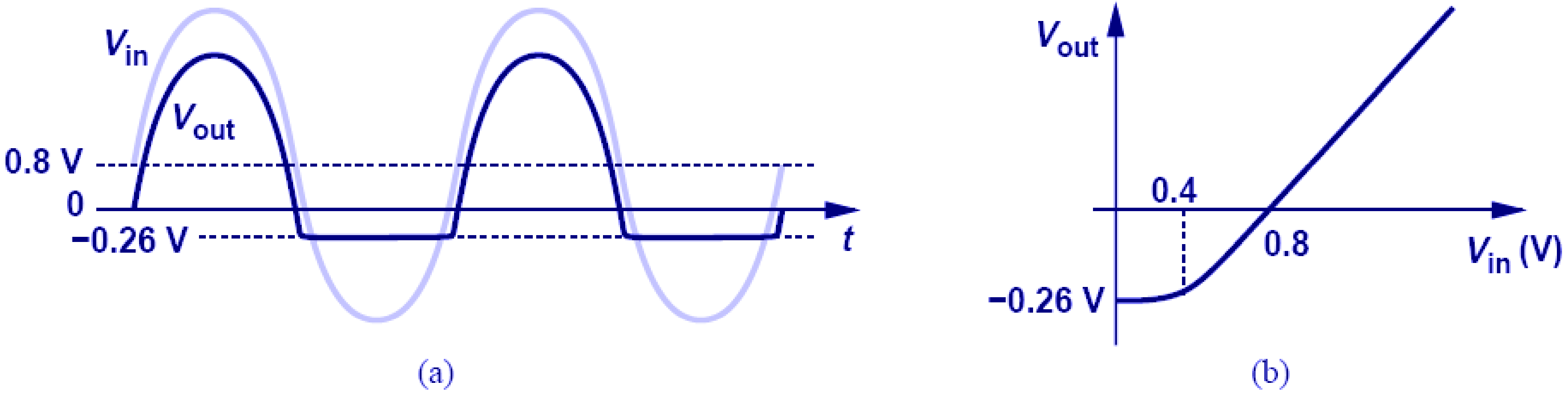
- For what V_{in}, Q_1 carries only 1% of I_1?



$$V_{in} = V_T \ln\frac{I_{C1}}{I_S} + \left(I_{C1} - I_1\right)R_L$$

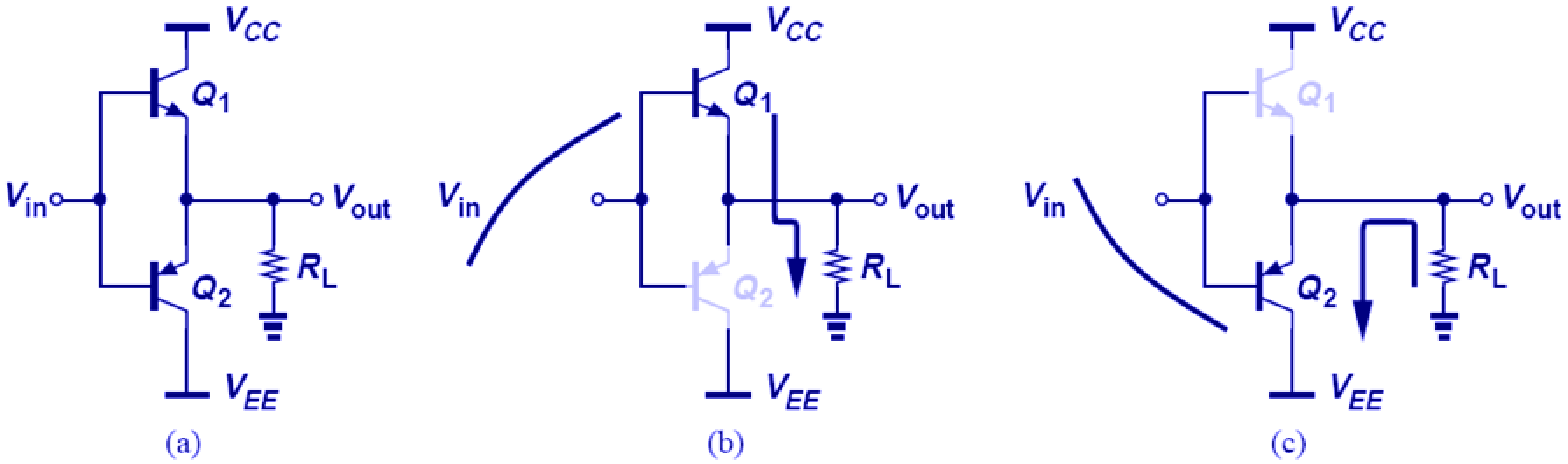
$$\boxed{\begin{array}{l}\text{For } I_{C1} \approx 0.01 \cdot I_1 \\ \Rightarrow V_{in} \approx 390\text{ mV}\end{array}}$$

Linearity of an Emitter Follower



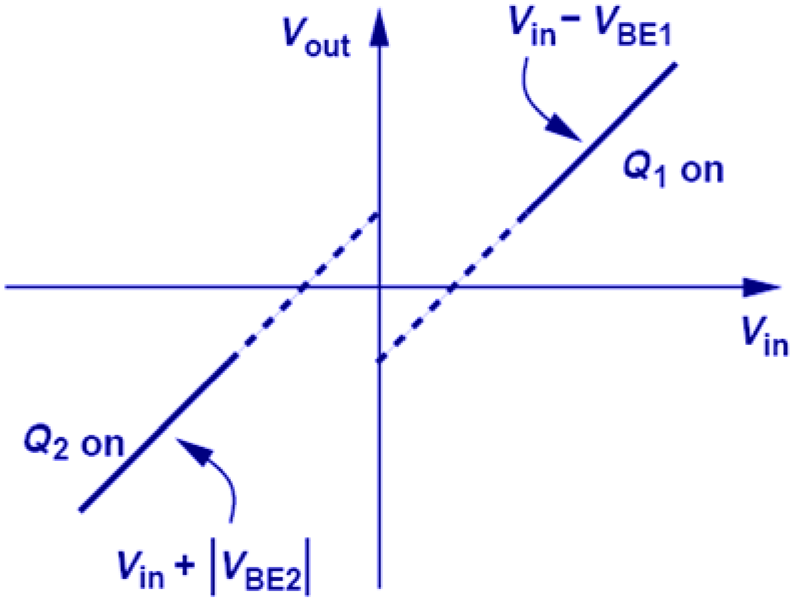
- **As V_{in} decreases the output waveform will be clipped, introducing nonlinearity in I/O characteristics.**

Push-Pull Stage



- As V_{in} increases, Q_1 is on and pushes current into R_L.
- As V_{in} decreases, Q_2 is on and pulls current out of R_L.

Example 13.2: I/O Characteristics for Large V_{in}

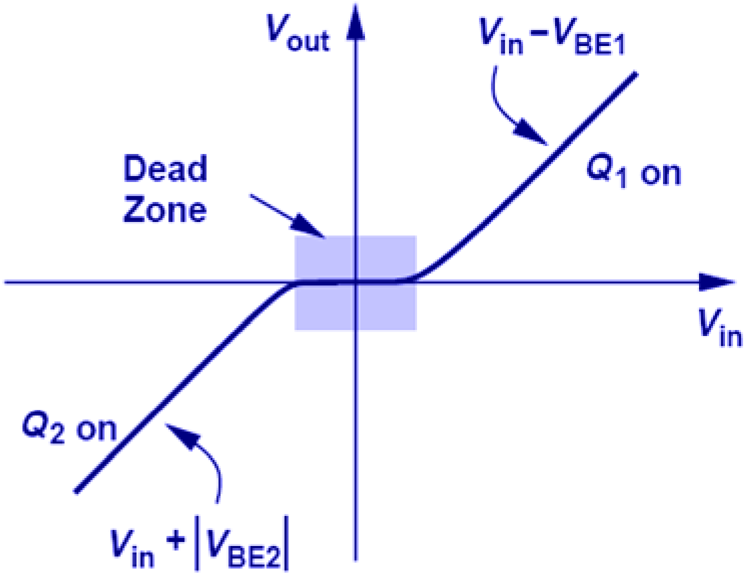


$V_{out} = V_{in} - V_{BE1}$ for large $+V_{in}$

$V_{out} = V_{in} + |V_{BE2}|$ for large $-V_{in}$

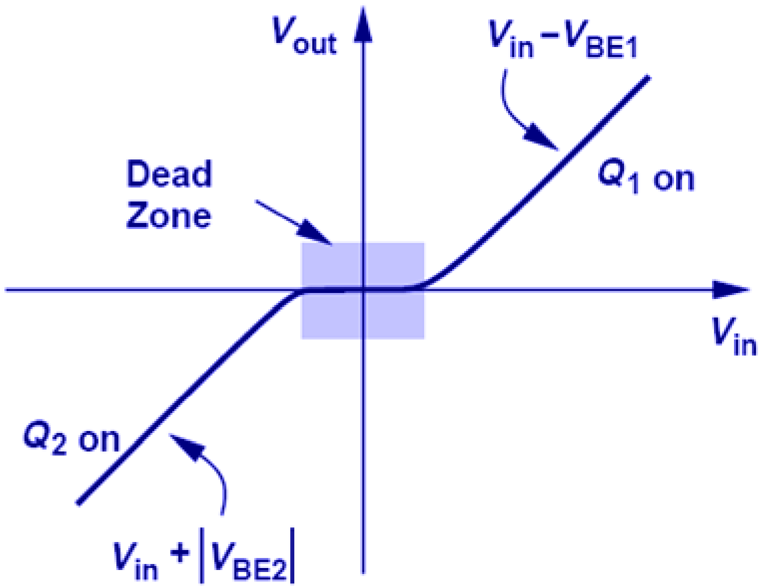
- **For positive V_{in}, Q_1 shifts the output down and for negative V_{in}, Q_2 shifts the output up.**

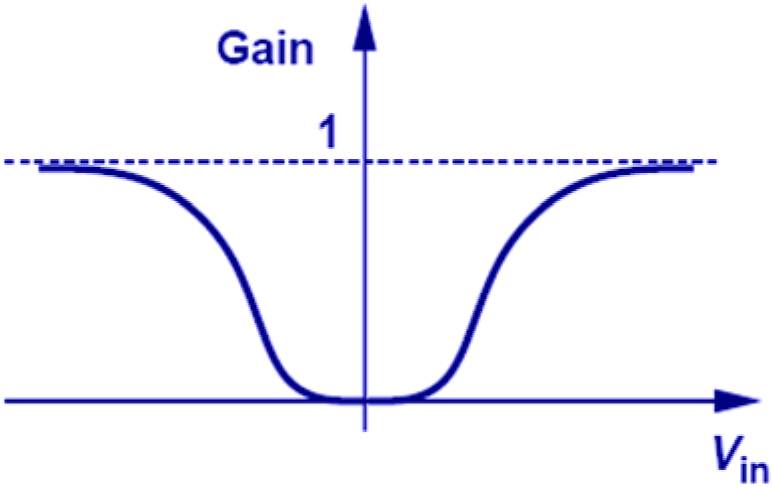
Overall I/O Characteristics of Push-Pull Stage



- However, for small V_{in}, there is a “dead zone” (both Q_1 and Q_2 are off) in the I/O characteristic, resulting in gross nonlinearity.

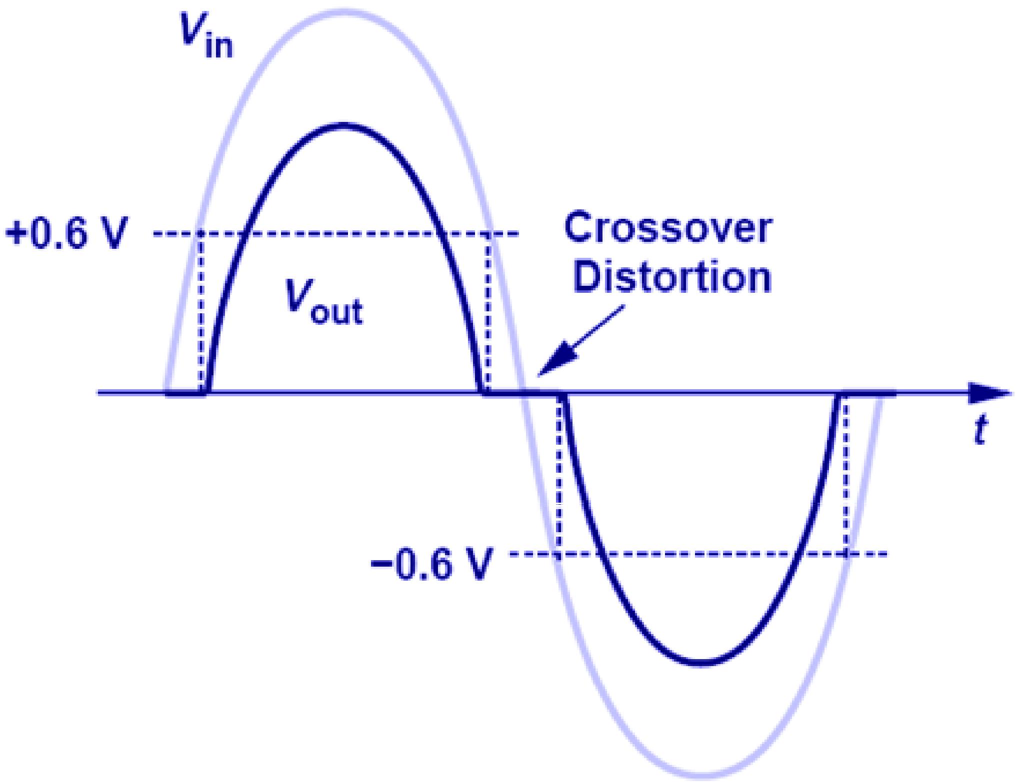
Example 13.3: Small-Signal Gain of Push-Pull Stage





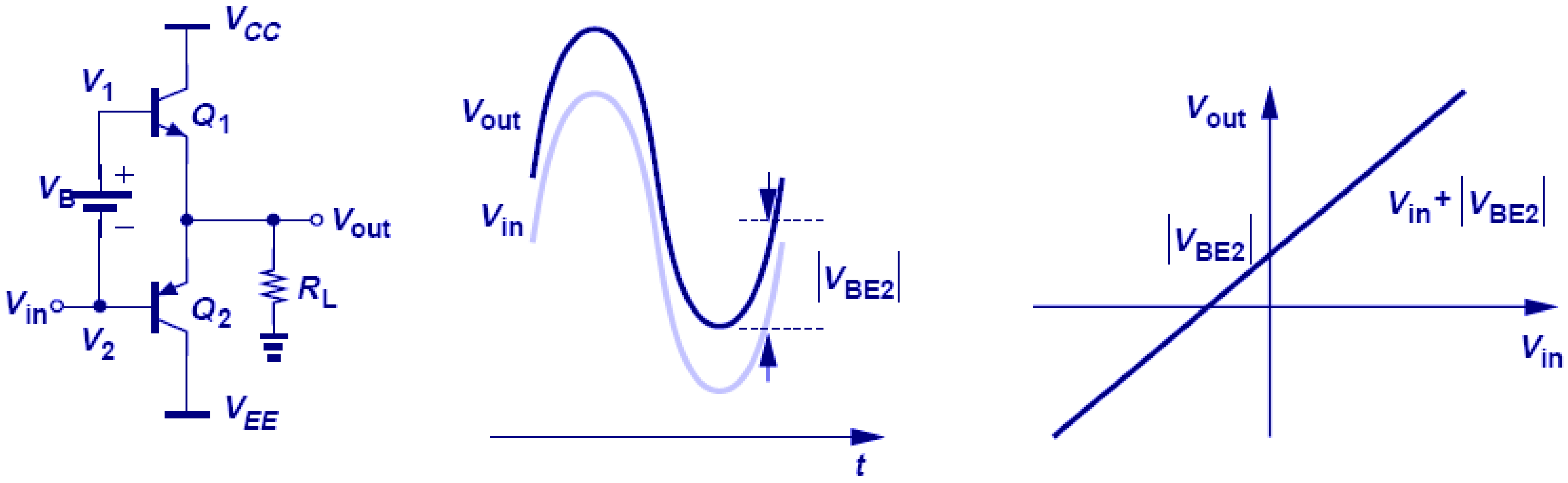
- The push-pull stage exhibits a gain that tends to unity when either Q_1 or Q_2 is on.
- When V_{in} is very small, the gain drops to zero.

Example 13.4: Sinusoidal Response of Push-Pull Stage



- For large V_{in}, the output follows the input with a fixed DC offset, however as V_{in} becomes small the output drops to zero and causes “Crossover Distortion.”

Improved Push-Pull Stage

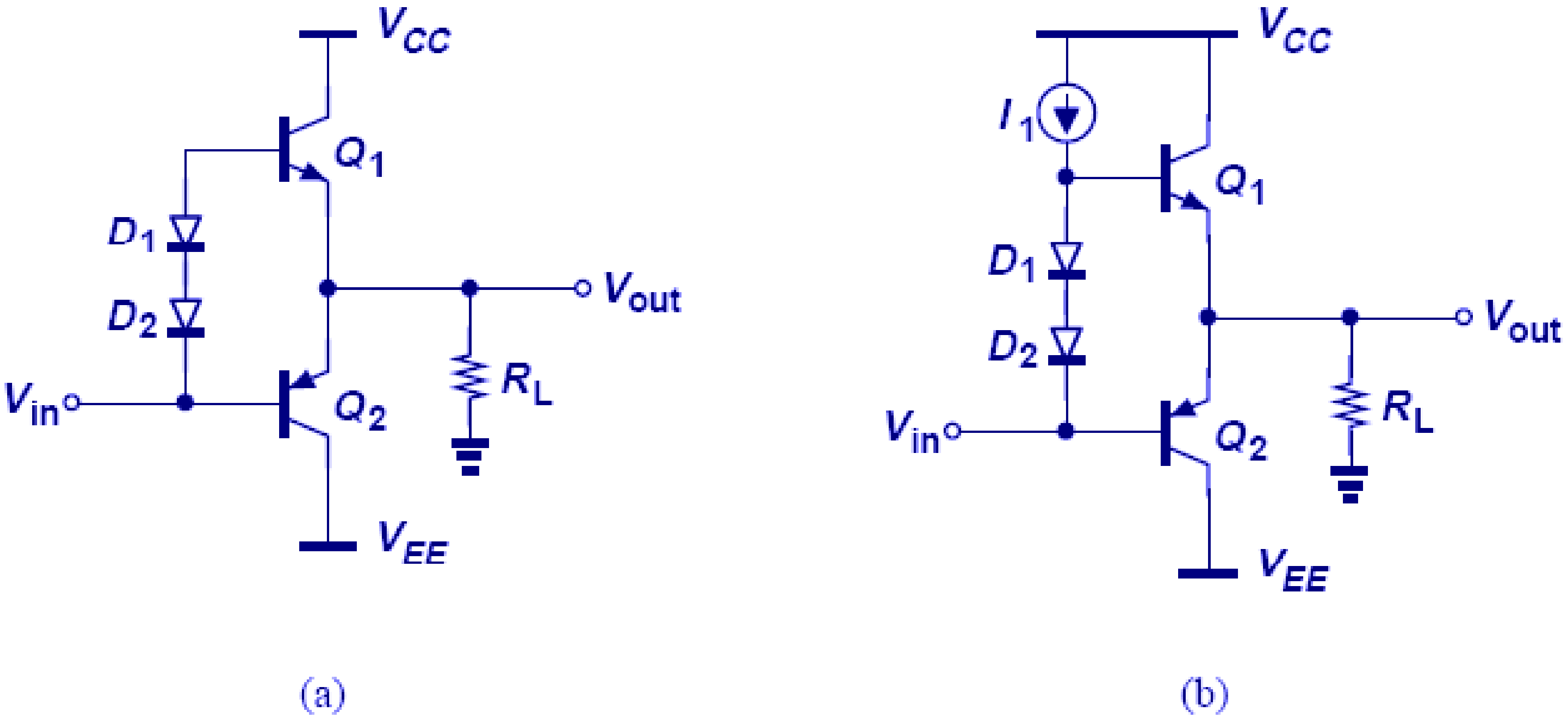


(a) (b) (c)

$$V_B = V_{BE1} + |V_{BE2}|$$

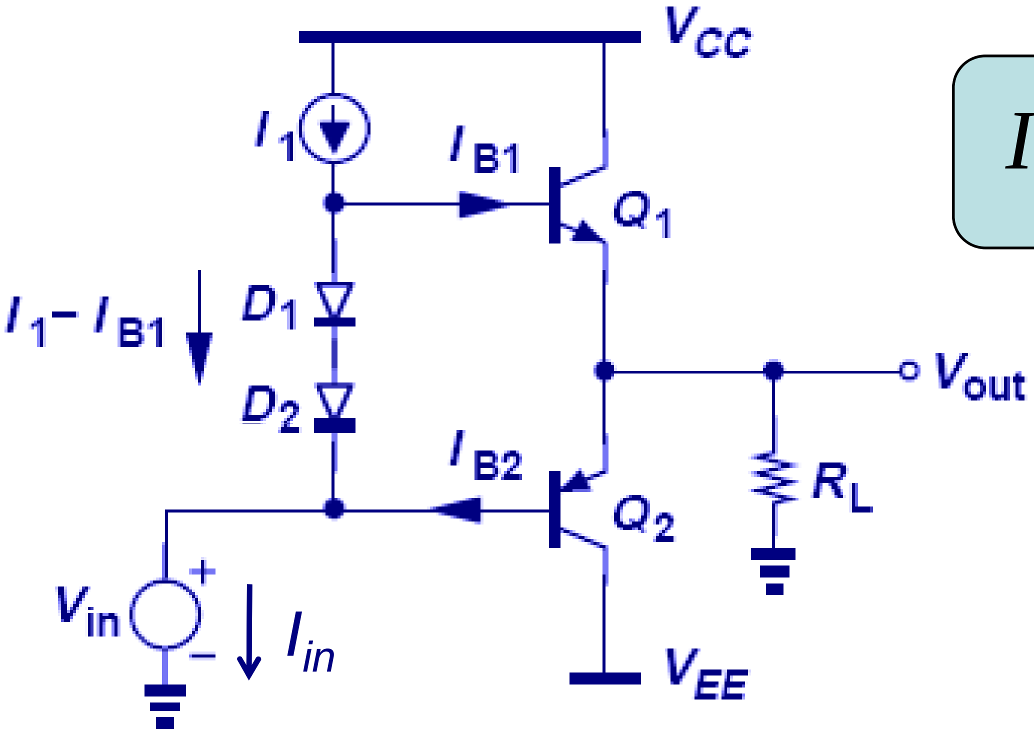
- **With a battery of V_B inserted between the bases of Q_1 and Q_2, the dead zone is eliminated.**

Implementation of V_B



- **Since $V_B = V_{BE1} + |V_{BE2}|$, a natural choice would be two diodes in series.**
- **I_1 in figure (b) is used to bias the diodes and Q_1.**

Example 13.6: Current Flow I

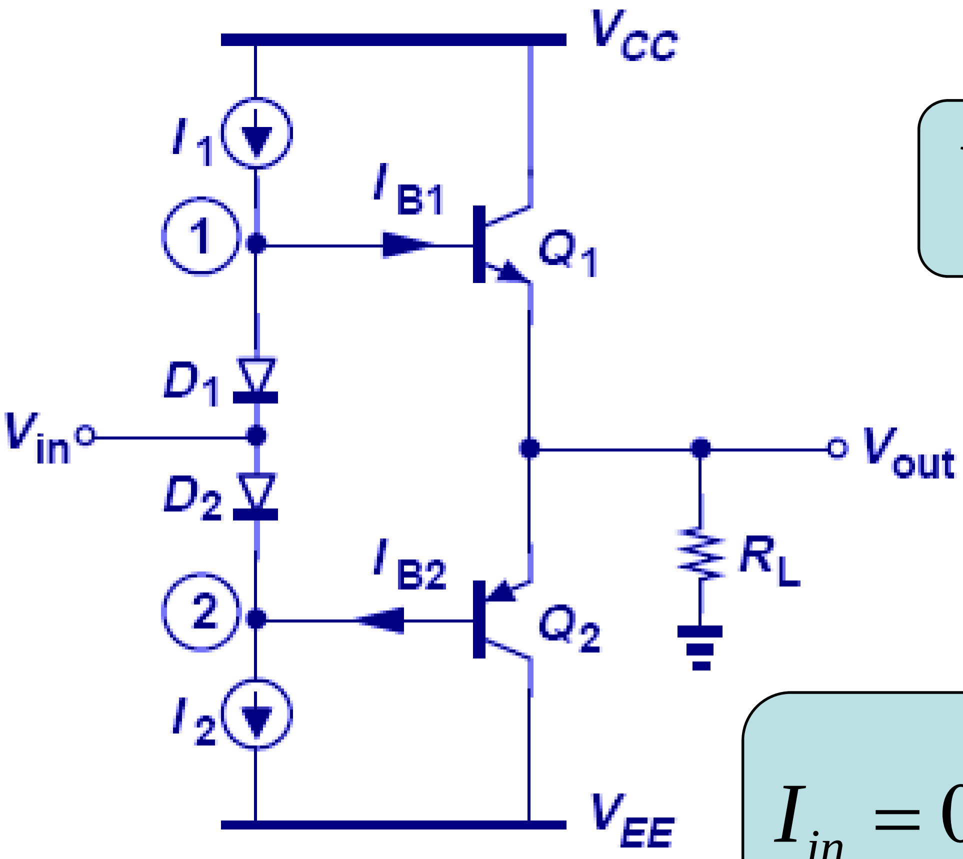


$$I_{in} = I_1 - I_{B1} + |I_{B2}|$$

Usually $I_{B1} \neq |I_{B2}|$ unless $V_{out} = 0$

I_{in} flows even when $V_{out} = 0$.

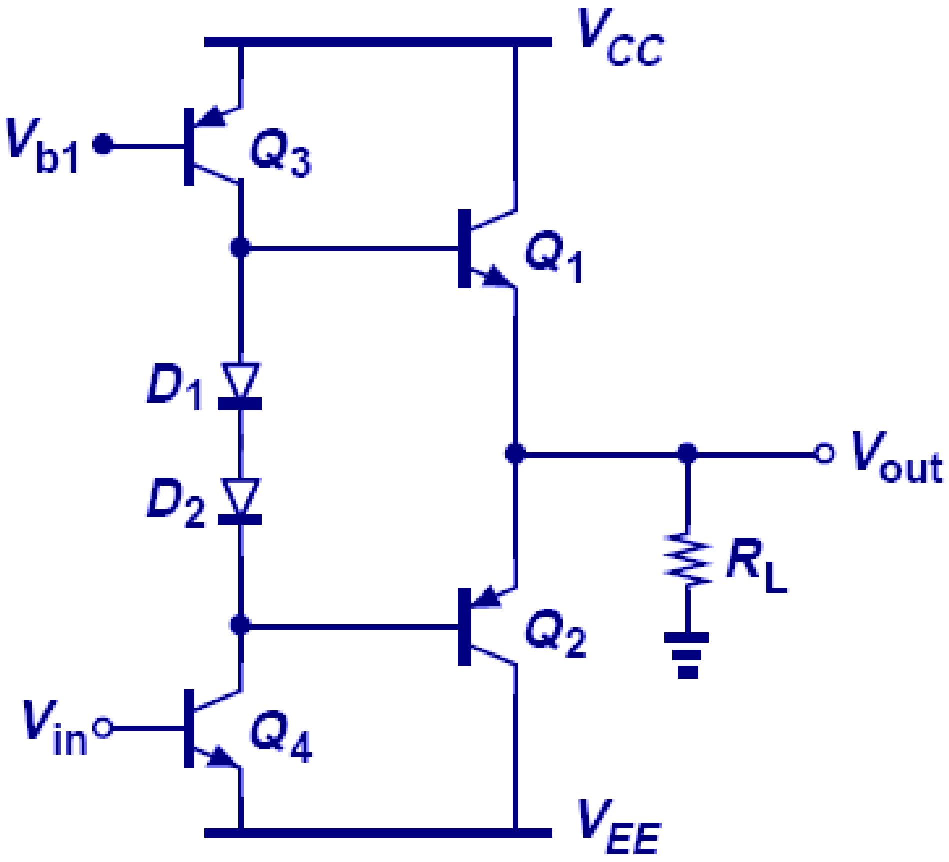
Example 13.8: Current Flow II



$$V_{D1} \approx V_{BE} \longrightarrow V_{out} \approx V_{in}$$

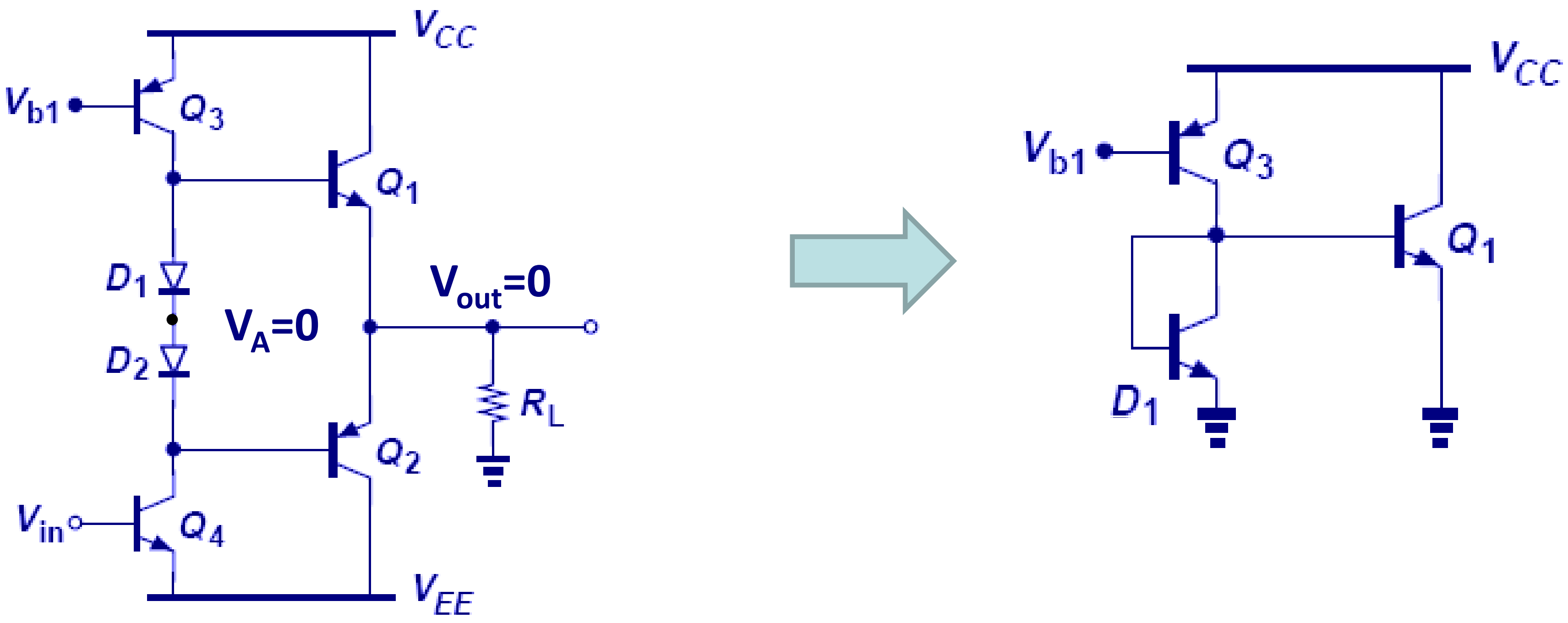
$$I_{in} = 0 \text{ when } V_{out} = 0 \text{ if } I_1 = I_2$$

Addition of CE Stage



- **A CE stage (predriver) is added to provide voltage gain from the input to the bases of Q_1 and Q_2.**

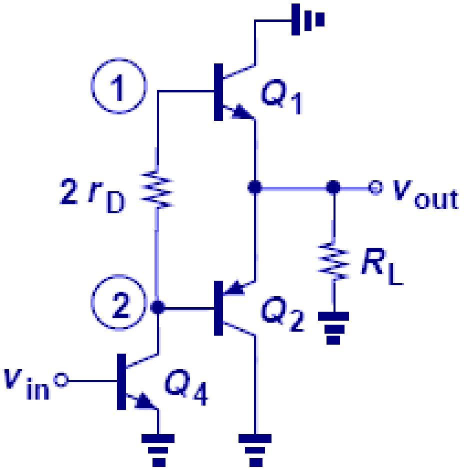
Bias Point Analysis

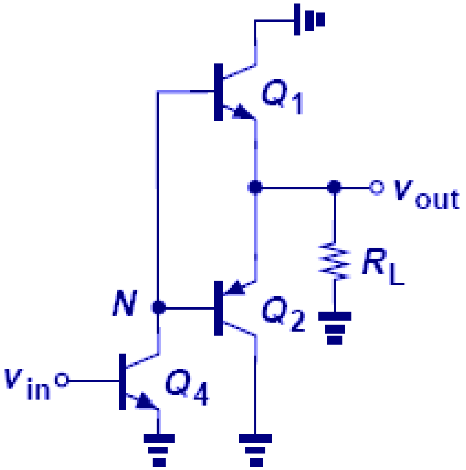


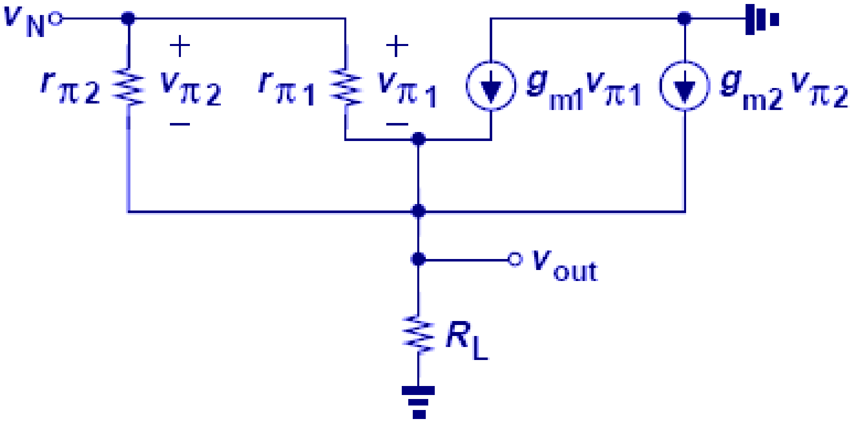
- **For bias point analysis for V_{out}=0, the circuit can be simplified to the one on the right, which resembles a current mirror.**

$$I_{C1} = \frac{I_{S,Q1}}{I_{S,D1}} \cdot \left| I_{C3} \right|$$

Small-Signal Analysis



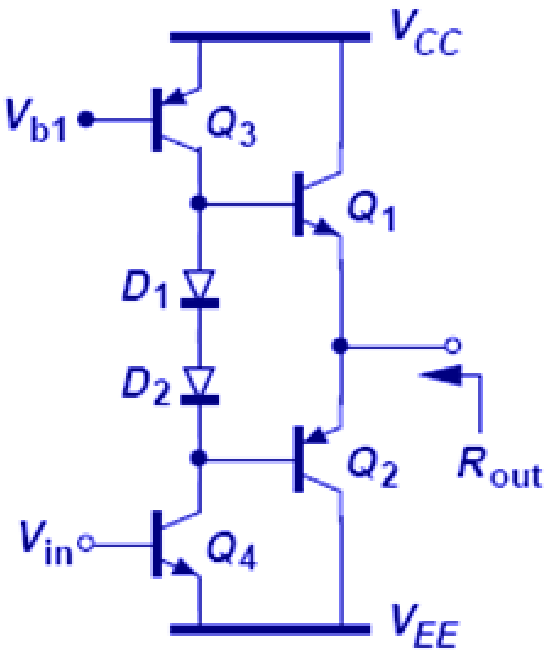


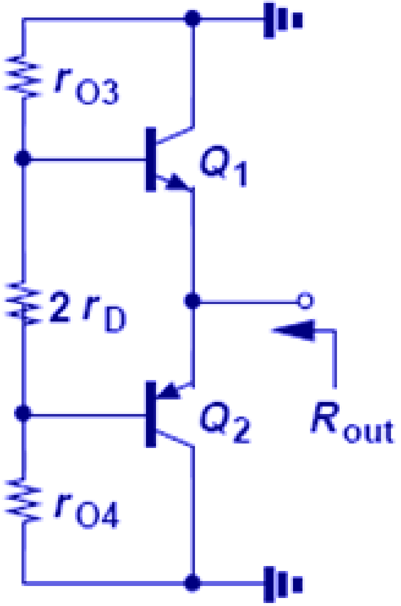


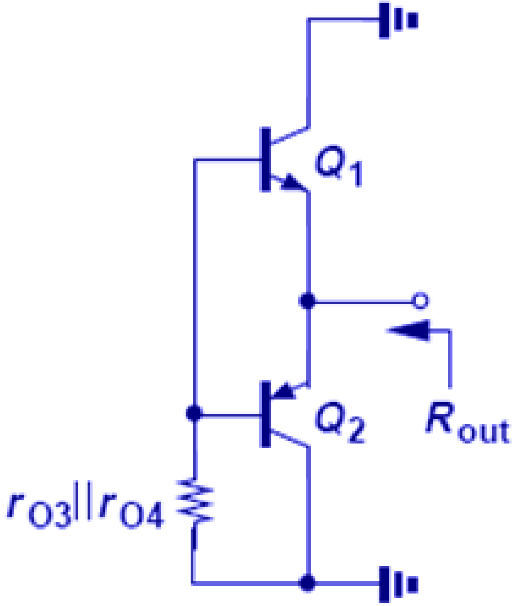
- **Assuming $2r_D$ is small and $(g_{m1}+g_{m2})R_L$ is much greater than 1,**

$$A_v = -g_{m4}\left(r_{\pi 1} \parallel r_{\pi 2}\right)\left(g_{m1}+g_{m2}\right)R_L$$

Example 13.9: Output Resistance Analysis





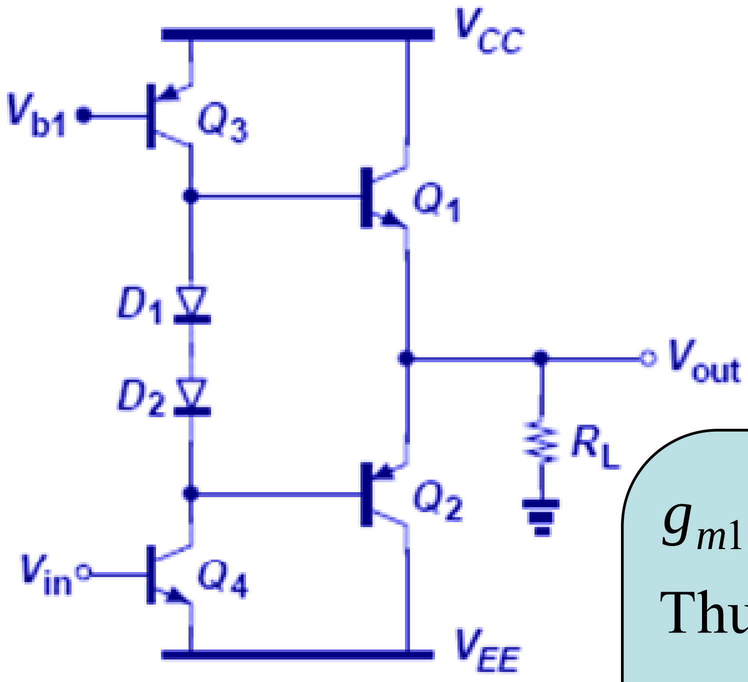


$$R_{out} \approx \frac{1}{g_{m1}+g_{m2}} + \frac{r_{O3} \| r_{O4}}{(g_{m1}+g_{m2})(r_{\pi 1} \| r_{\pi 2})}$$

- **If β is low, the second term of the output resistance will rise, which will be problematic when driving a small resistance.**

Example13.10: Biasing

- **Compute the required bias current.**



Predriver (CE stage): $A_V = 5$

Output Stage: $A_V = 0.8$ for $R_L = 8\ \Omega$

$\beta_{npn} = 2\beta_{pnp} = 100,\ I_{C1} \approx I_{C2}$

$$g_{m1} + g_{m2} = (2\ \Omega)^{-1} \Rightarrow g_{m1} \approx g_{m2} \approx (4\ \Omega)^{-1}$$

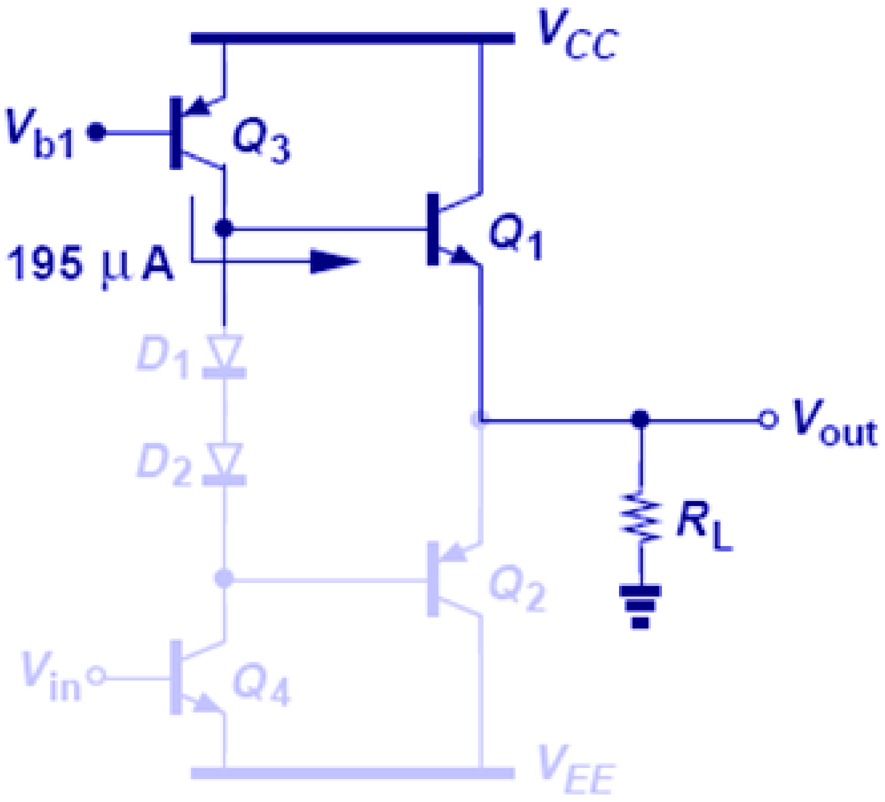
Thus, $I_{C1} \approx I_{C2} \approx 6.5$ mA

$$r_{\pi 1} \| r_{\pi 2} = 400\ \Omega \| 200\ \Omega = 133\ \Omega$$

$$g_{m4} \cdot (r_{\pi 1} \| r_{\pi 2}) \cdot \left[1 + (g_{m1} + g_{m2}) \cdot R_L\right] = 4$$

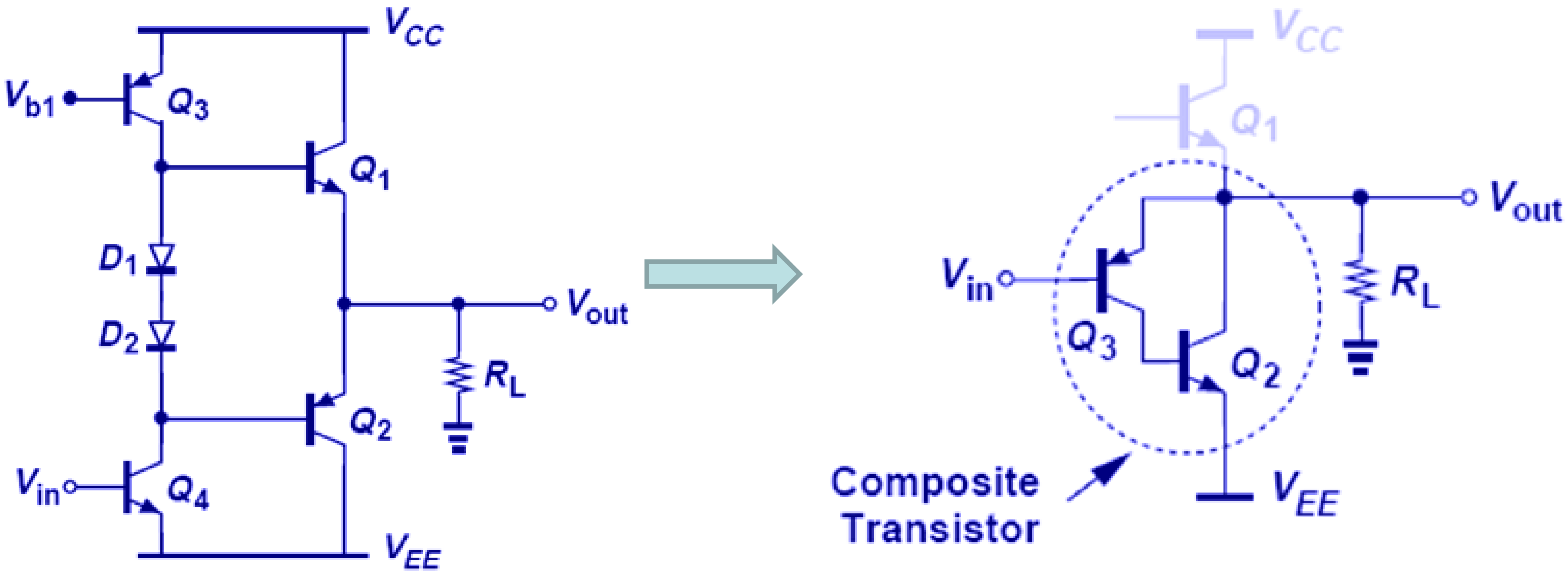
$$\Rightarrow g_{m4} = (133\ \Omega)^{-1} \Rightarrow I_{C3} \approx I_{C4} \approx 195\ \mu\text{A}$$

Problem of Base Current



- **195 µA of base current in Q_1 can only support 19.5 mA of collector current, insufficient for high current operation (500 mA for 4 V on 8 Ω).**

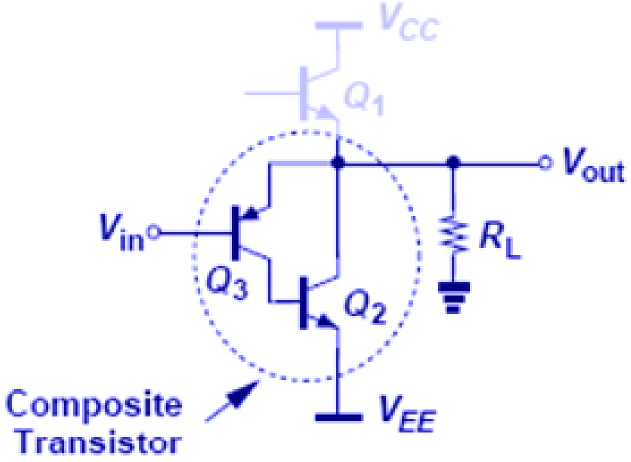
Modification of the PNP Emitter Follower

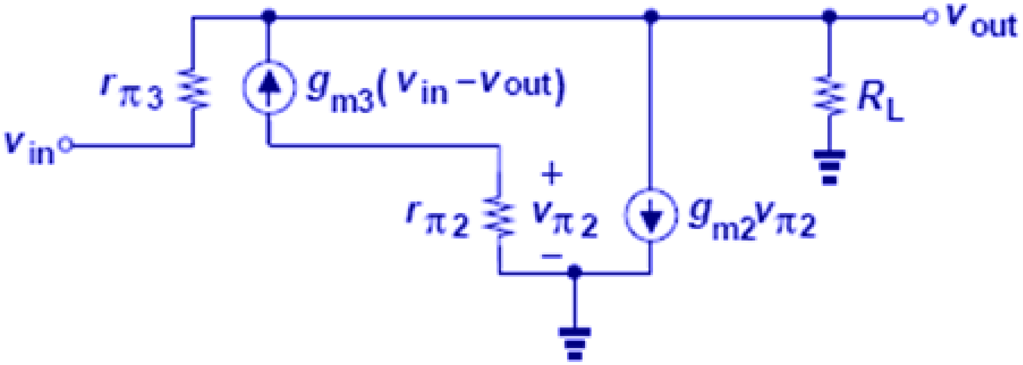


$$R_{out} \approx \frac{1}{(\beta_2+1)\,g_{m3}}$$

- **Instead of having a single PNP as the emitter-follower, it is now combined with an NPN (Q_2), providing a lower output resistance.**

Example 13.11: Input Resistance



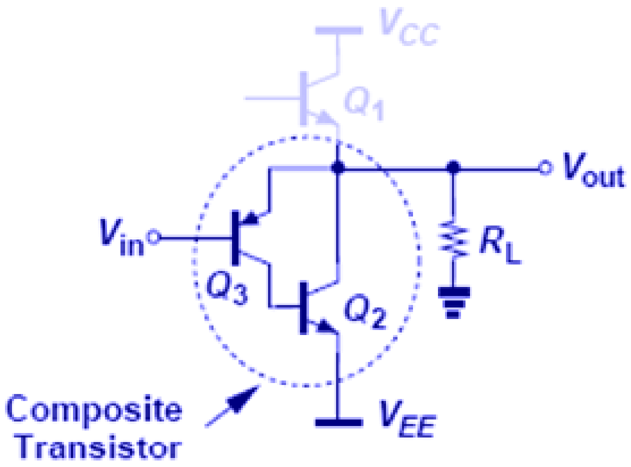


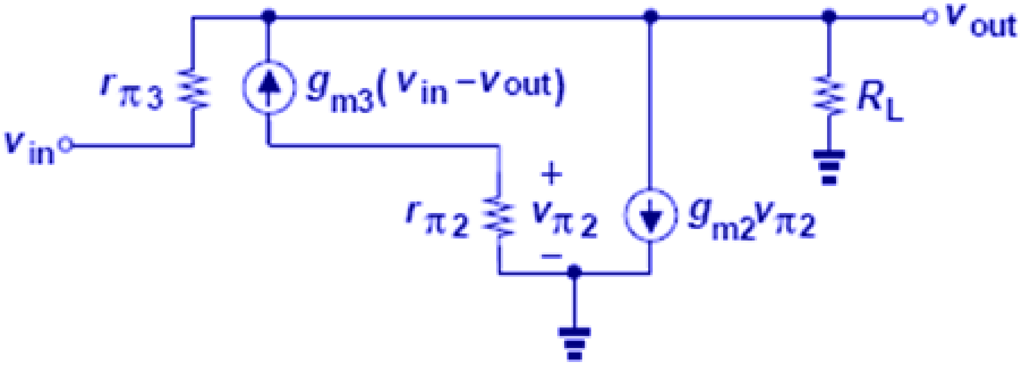
$$\frac{v_{out}}{v_{in}}=\frac{R_L}{R_L+\dfrac{1}{(\beta_2+1)g_{m3}+\dfrac{1}{r_{\pi 3}}}}$$

Comparing with the standard EF,

$$r_{out}=\frac{1}{(\beta_2+1)g_{m3}+\dfrac{1}{r_{\pi 3}}}\approx\frac{1}{(\beta_2+1)g_{m3}}$$

Example 13.11: Input Resistance

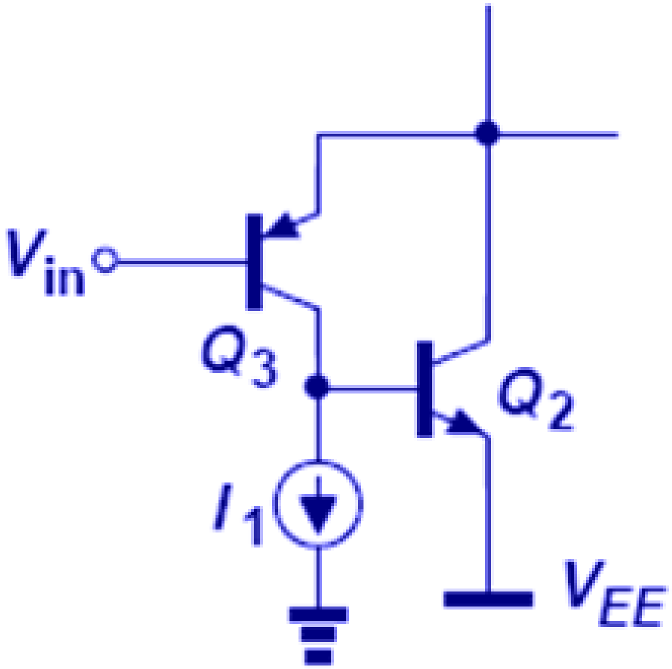




$$i_{in} = \frac{1}{r_{\pi 3}}\left(v_{in} - v_{in}\frac{R_L}{R_L + \dfrac{1}{(\beta_2+1)g_{m3}}}\right)$$

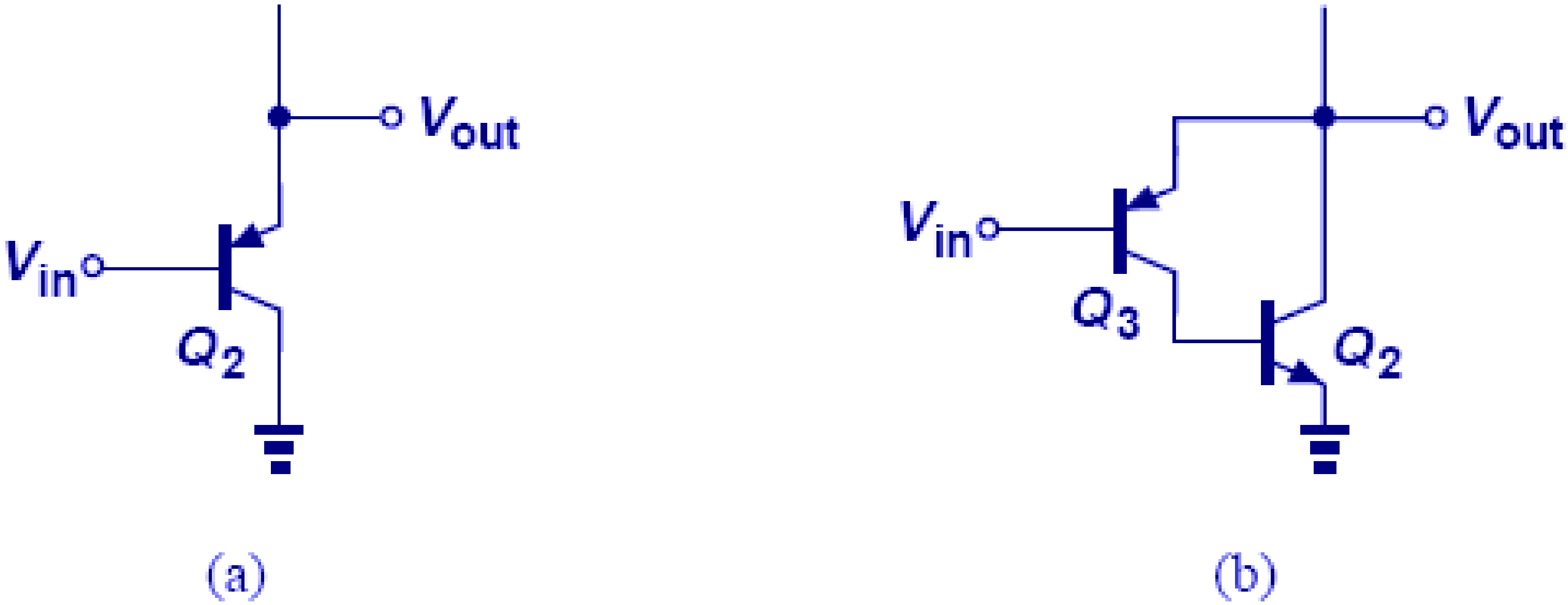
$$r_{in} = \beta_3(\beta_2+1)R_L + r_{\pi 3}$$

Additional Bias Current



- I_1 is added to the base of Q_2 to provide an additional bias current to Q_3 so the capacitance at the base of Q_2 can be charged/discharged quickly. Additional pole at the base of Q_2.

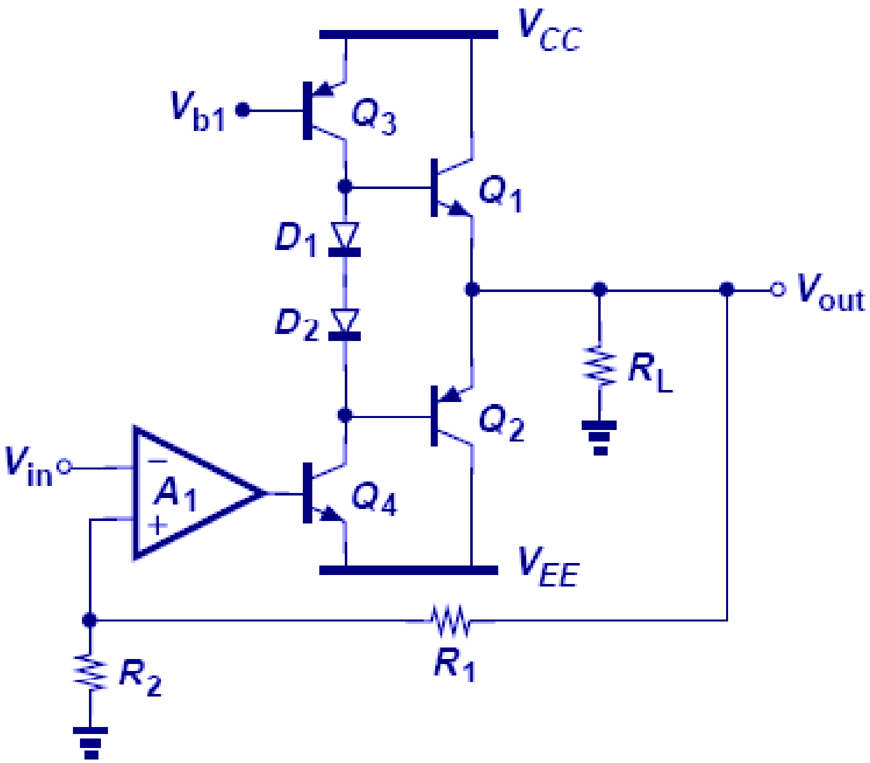
Example 13.12: Minimum V_{in}



$$Min\,V_{in} \approx 0$$
$$V_{out} \approx |V_{EB2}|$$

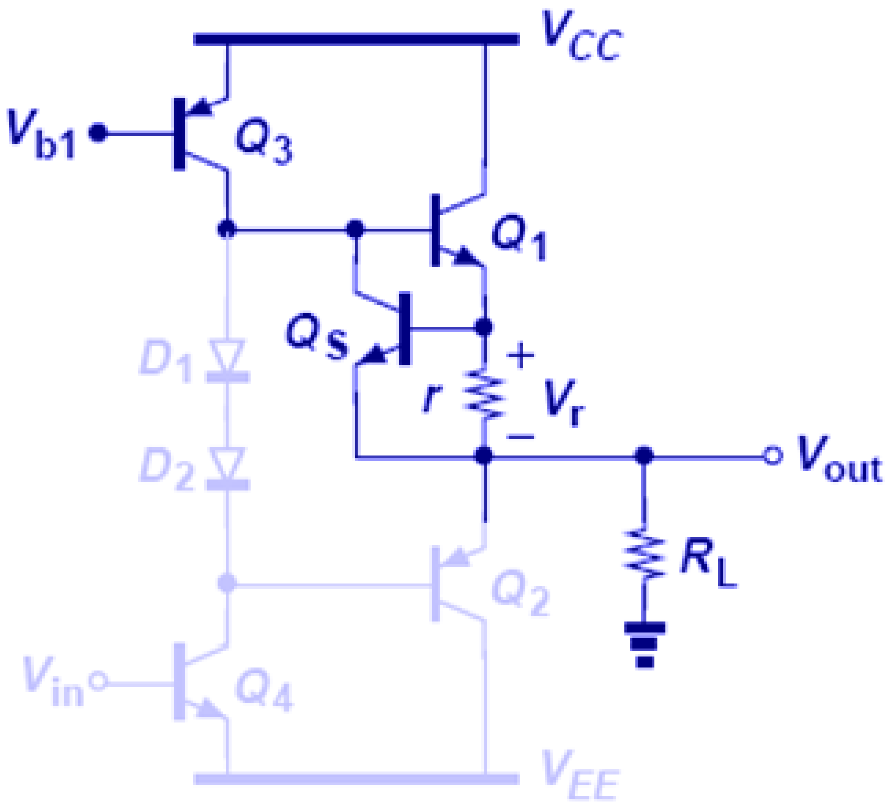
$$Min\,V_{in} \approx V_{BE2}$$
$$V_{out} \approx |V_{EB3}| + V_{BE2}$$

HiFi Design



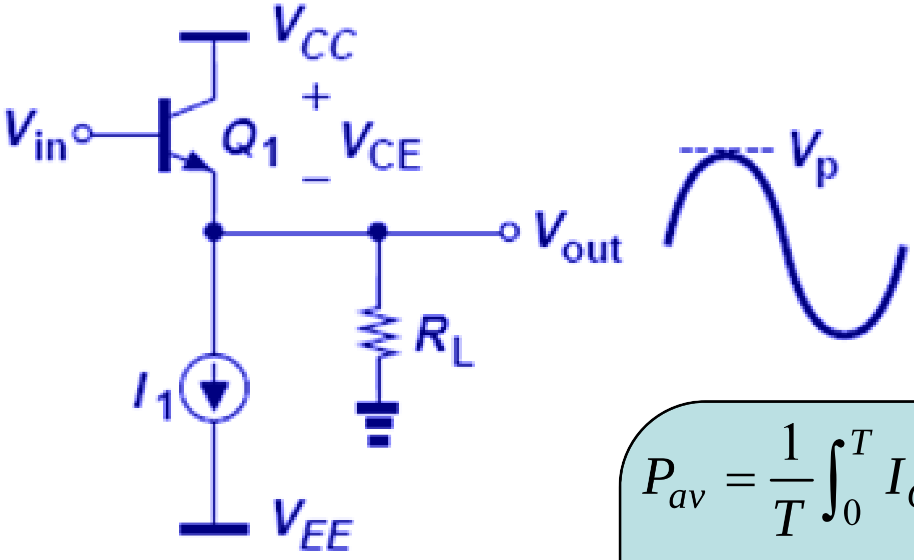
- As V_{out} becomes more positive, g_m rises and A_v comes closer to unity, resulting in nonlinearity.
- Using negative feedback, linearity is improved, providing higher fidelity.

Short-Circuit Protection



- Q_s and r are used to "steal" some base current away from Q_1 when the output is accidentally shorted to ground, preventing short-circuit damage.

Emitter Follower Power Rating



$$P_{av} = \frac{1}{T}\int_0^T I_C \cdot V_{CE}\, dt$$

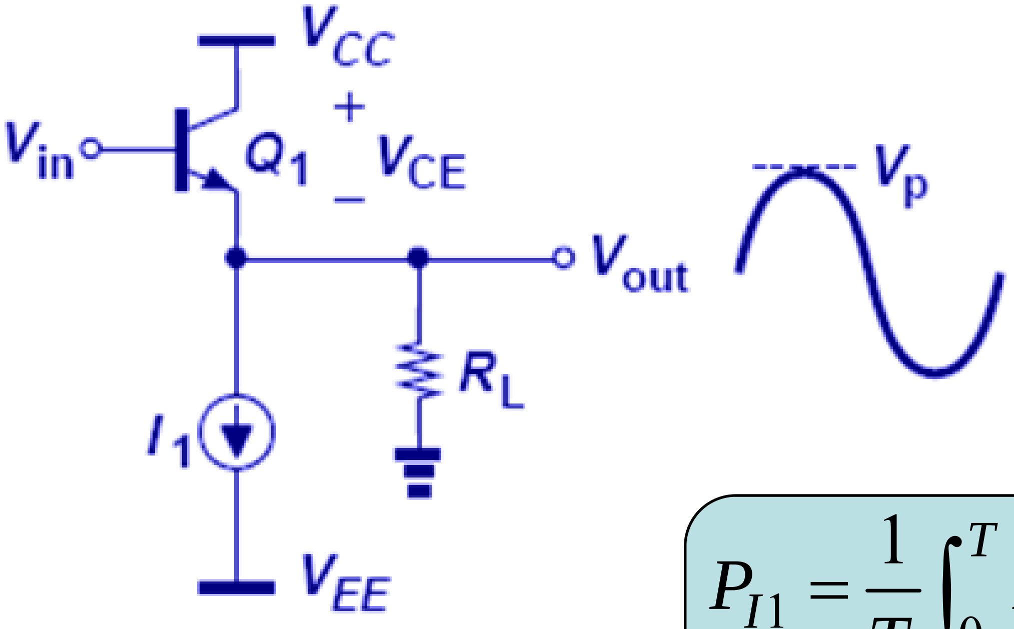
$$= \frac{1}{T}\int_0^T \left(I_1 + \frac{V_P \sin \omega t}{R_L}\right) \cdot \left(V_{CC} - V_P \sin \omega t\right) dt$$

$$= I_1 \cdot V_{CC} - \frac{V_P{}^2}{R_L} = I_1\left(V_{CC} - \frac{V_P}{2}\right) \text{ if } I_1 = \frac{V_P}{R_L}$$

- **Maximum power dissipated across Q_1 occurs in the *absence* of a signal.**

Example 13.13: Power Dissipation

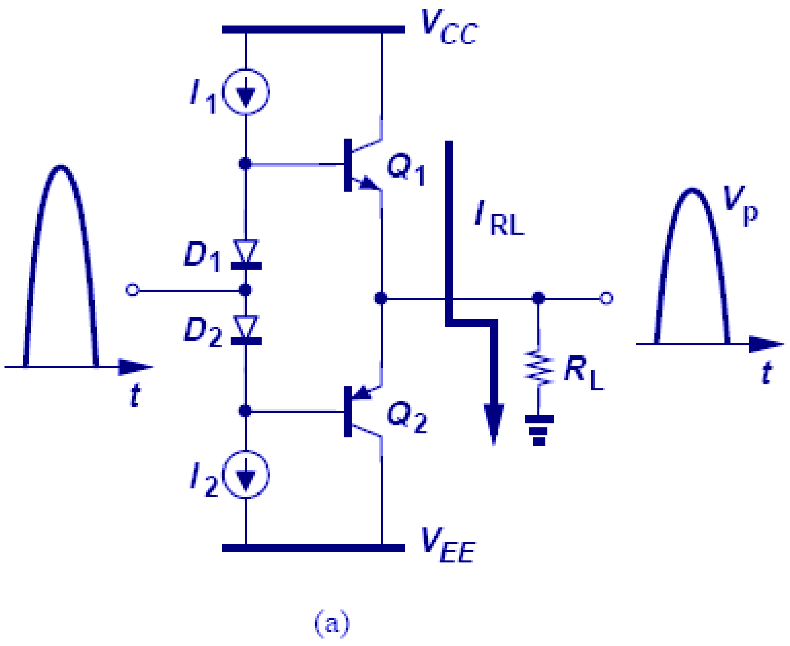
- **Avg Power Dissipated in the Current Source I_1**



$$P_{I1} = \frac{1}{T}\int_0^T I_1\left(V_p \sin\omega t - V_{EE}\right)dt$$

$$= -I_1 \cdot V_{EE}$$

Push-Pull Stage Power Rating



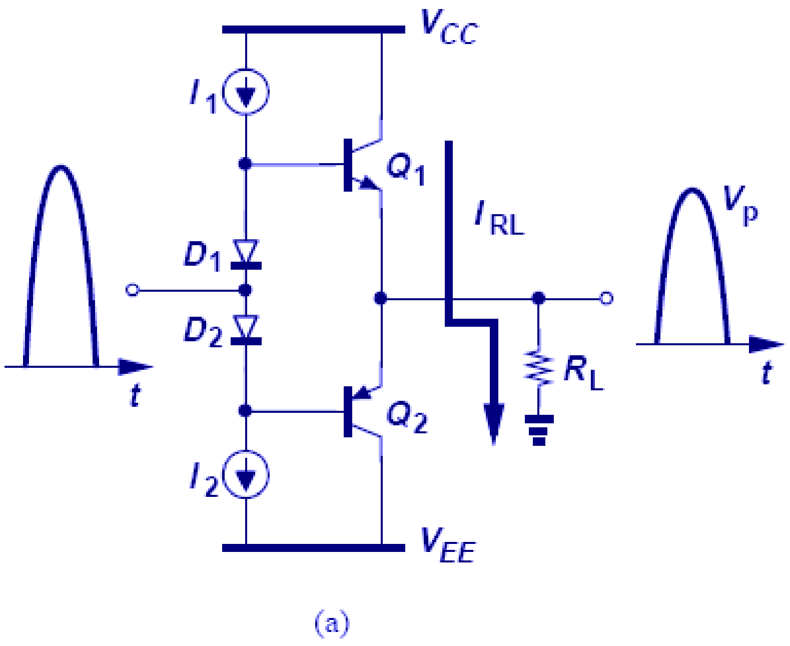
$$P_{av,NPN} = \frac{1}{T}\int_0^{T/2} I_C \cdot V_{CE}\,dt$$

$$= \frac{1}{T}\int_0^{T/2}\left(V_{CC} - V_P \sin\omega t\right)\cdot\frac{V_P\sin\omega t}{R_L}dt$$

$$= \frac{V_{CC}\cdot V_P}{\pi R_L} - \frac{V_P{}^2}{4R_L} = \frac{V_P}{R_L}\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$

- **No power for half of the period.**

Push-Pull Stage Power Rating



$$P_{av,NPN} = \frac{1}{T}\int_0^{T/2} I_C \cdot V_{CE}\,dt$$

$$= \frac{1}{T}\int_0^{T/2} \left(V_{CC} - V_P \sin\omega t\right)\cdot \frac{V_P \sin\omega t}{R_L}\,dt$$

$$= \frac{V_{CC}\cdot V_P}{\pi R_L} - \frac{{V_P}^2}{4R_L} = \frac{V_P}{R_L}\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$

- **No power for half of the period.**
- **Maximum power occurs between V_p=0 and $4V_{cc}/\pi$.**

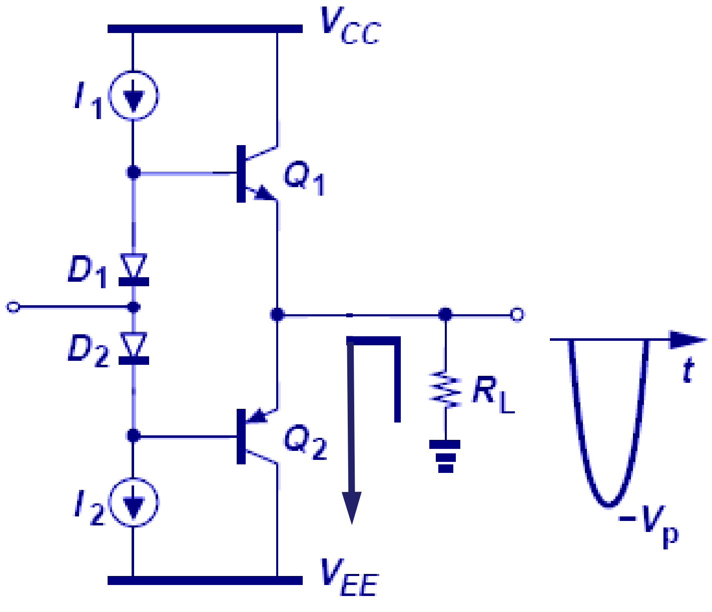
$$P_{av,\max} = \frac{{V_{CC}}^2 \cdot V_P}{\pi^2 R_L} \text{ when } V_P = 2\cdot\frac{V_{CC}}{\pi}$$

Push-Pull Stage Power Rating

$$P_{av,PNP} = \frac{1}{T}\int_{T/2}^{T} \left|I_C\right| \cdot \left|V_{CE}\right| dt$$

$$= \frac{1}{T}\int_{T/2}^{T} \left(V_P \sin \omega t - V_{EE}\right) \cdot \left(-\frac{V_P \sin \omega t}{R_L}\right) dt$$

$$= \frac{-V_{EE} \cdot V_P}{\pi R_L} - \frac{{V_P}^2}{4R_L} = \frac{V_P}{R_L}\left(\frac{-V_{EE}}{\pi} - \frac{V_P}{4}\right)$$

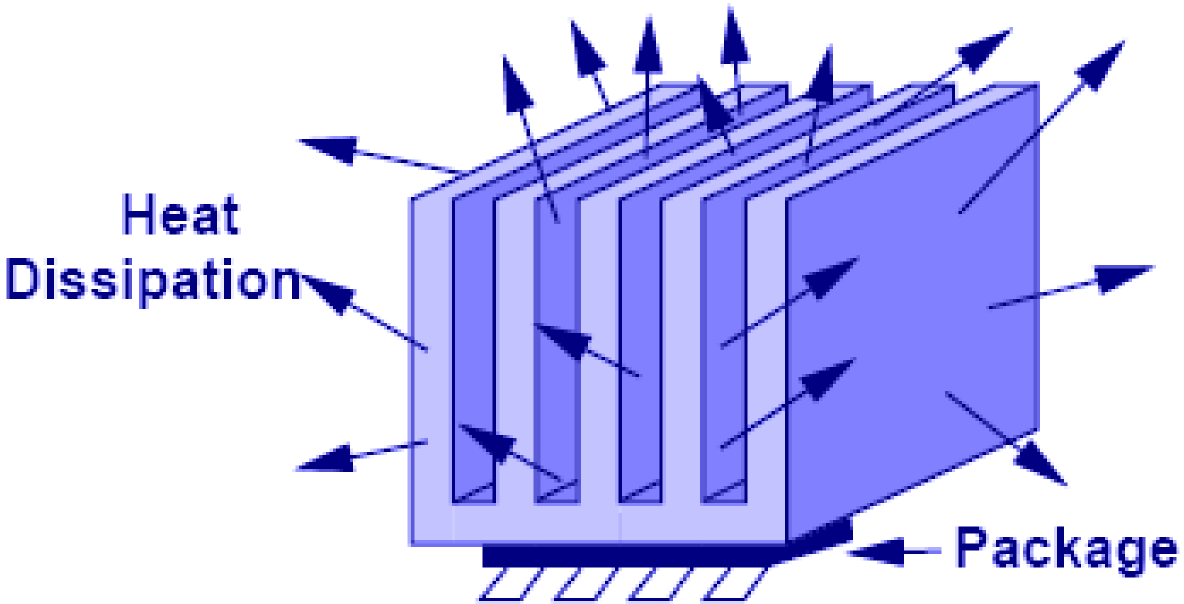


(b)

- **Maximum power occurs between V_p=0 and $4V_{CC}/\pi$.**

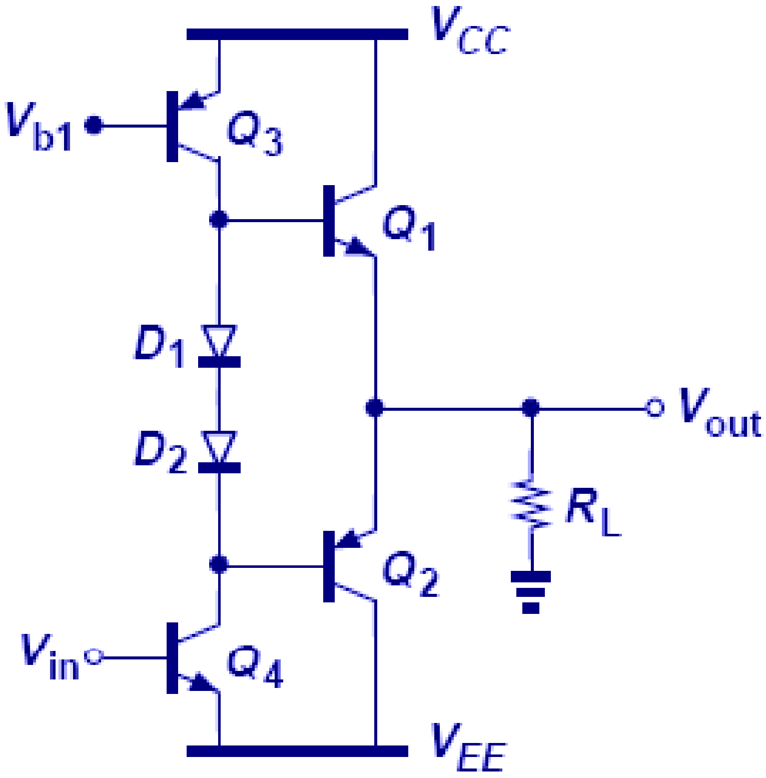
$$P_{av,\max} = \frac{{V_{CC}}^2 \cdot V_P}{\pi^2 R_L} \text{ when } V_P = 2 \cdot \frac{V_{CC}}{\pi}$$

Heat Sink



- **Heat sink, provides large surface area to dissipate heat from the chip.**

Thermal Runaway Mitigation



$$V_{D1}+V_{D2}=V_T\ln\frac{I_{D1}}{I_{S,D1}}+V_T\ln\frac{I_{D2}}{I_{S,D2}}$$

$$=V_T\ln\frac{I_{D1}I_{D2}}{I_{S,D1}I_{S,D2}}$$

$$V_{BE1}+V_{BE2}=V_T\ln\frac{I_{C1}}{I_{S,Q1}}+V_T\ln\frac{I_{C2}}{I_{S,Q2}}$$

$$=V_T\ln\frac{I_{C1}I_{C2}}{I_{S,Q1}I_{S,Q2}}$$

With the same V_T,

$$\frac{I_{D1}I_{D2}}{I_{S,D1}I_{S,D2}}=\frac{I_{C1}I_{C2}}{I_{S,Q1}I_{S,Q2}}$$

- **Using diode biasing prevents thermal runaway since the currents in Q_1 and Q_2 will track those of D_1 and D_2 as long as their I_s's track with temperature.**

Efficiency

- Efficiency is defined as the average power delivered to the load divided by the power drawn from the supply

$$\eta = \frac{\text{Power Delivered to Load}}{\text{Power Drawn From Supply Voltage}} = \frac{P_{out}}{P_{out} + P_{ckt}}$$

<u>Emitter Follower</u>

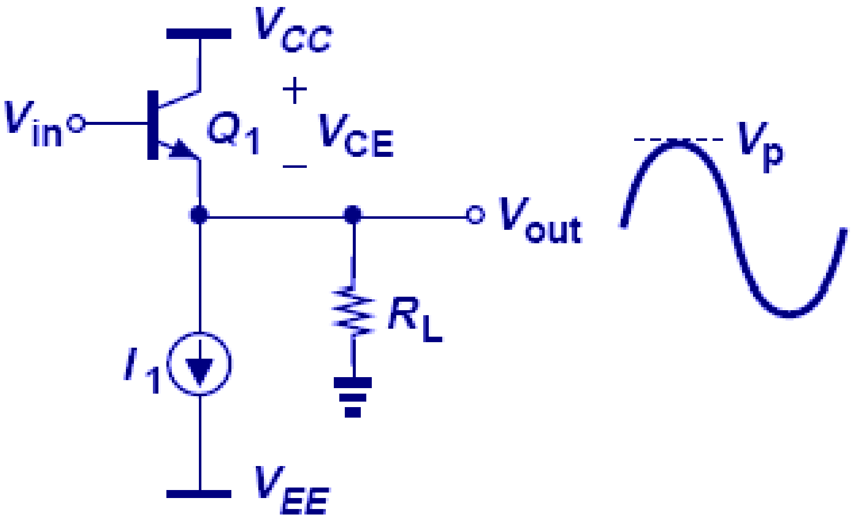
$$\eta_{EF} = \frac{V_P^2 / 2R_L}{V_P^2 / 2R_L + I_1 \left(V_{CC} - V_P / 2\right) - I_1 \cdot V_{EE}}$$

$$= \frac{V_P}{4V_{CC}} \text{ if } I_1 = \frac{V_P}{R_L} \text{ and } -V_{EE} = V_{CC}$$

- Maximum efficiency for EF is 25%.

Example 13.15: Efficiency of EF

- **EF designed for full swing operates with half swing.**



With $I_1 = \frac{V_P}{R_L} = \frac{V_{CC}}{R_L}$ and $-V_{EE} = V_{CC}$

$$\eta_{EF} = \frac{V_P^2/2R_L}{V_P^2/2R_L + I_1(V_{CC} - V_P/2) - I_1 \cdot V_{EE}}$$

$$= \frac{V_P^2/2R_L}{V_P^2/2R_L + \frac{V_{CC}}{R_L}(V_{CC} - V_P/2) + \frac{V_{CC}}{R_L} \cdot V_{CC}}$$

Thus,

$$\eta_{EF}\Big|_{V_P = V_{CC}/2} = \frac{1}{15}$$

Efficiency

Push-Pull Stage

$$\eta_{PP} = \frac{\dfrac{V_P^2}{2R_L}}{\dfrac{V_P^2}{2R_L} + \dfrac{2V_P}{R_L}\left(\dfrac{V_{CC}}{\pi} - \dfrac{V_P}{4}\right)}$$

$$= \frac{\pi}{4}\frac{V_P}{V_{CC}}$$

- **Maximum efficiency for PP is 78.5%.**

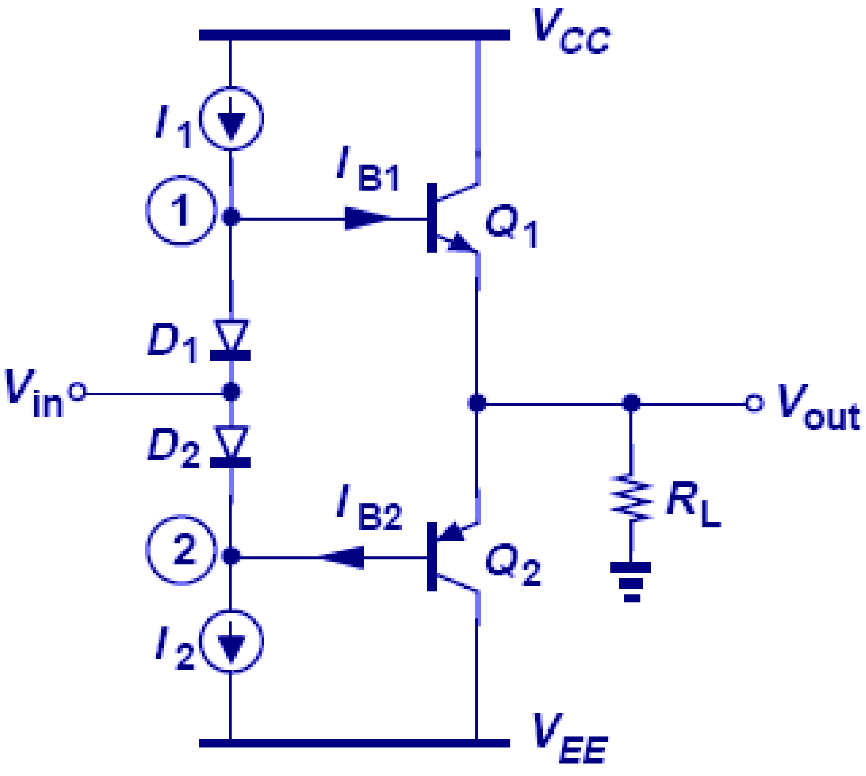
Example 13.16: Efficiency incl. Predriver

$$I_1 = \left(V_P / R_L\right) / \beta$$

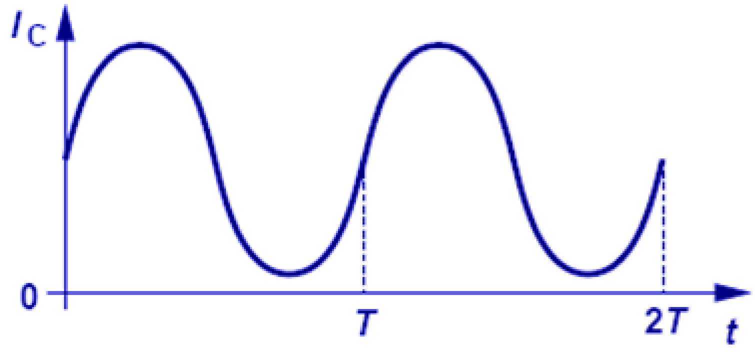
$$\eta = \frac{\dfrac{V_P^2}{2R_L}}{\dfrac{2V_P V_{CC}}{\pi R_L} + (V_{CC} - V_{EE})\dfrac{V_P}{\beta R_L}}$$

$$= \frac{1}{4}\frac{V_P}{V_{CC}/\pi + V_{CC}/\beta}$$

$$= \frac{1}{4}\frac{1}{\dfrac{1}{\pi} + \dfrac{1}{\beta}}\frac{V_P}{V_{CC}}$$

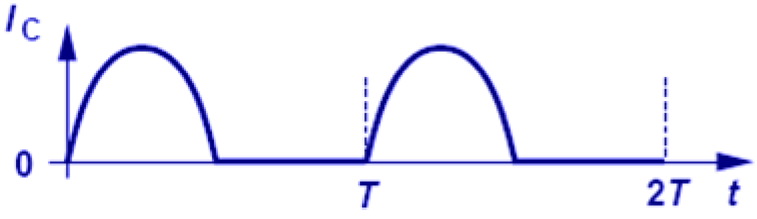


Power Amplifier Classes



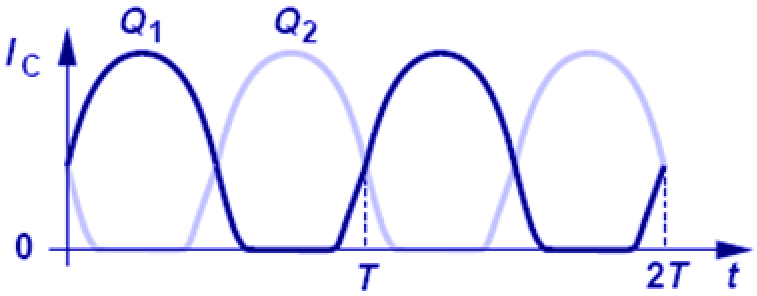
(a)

Class A: High linearity, low efficiency



(b)

Class B: High efficiency, low linearity



(c)

Class AB: Compromise between Class A and B