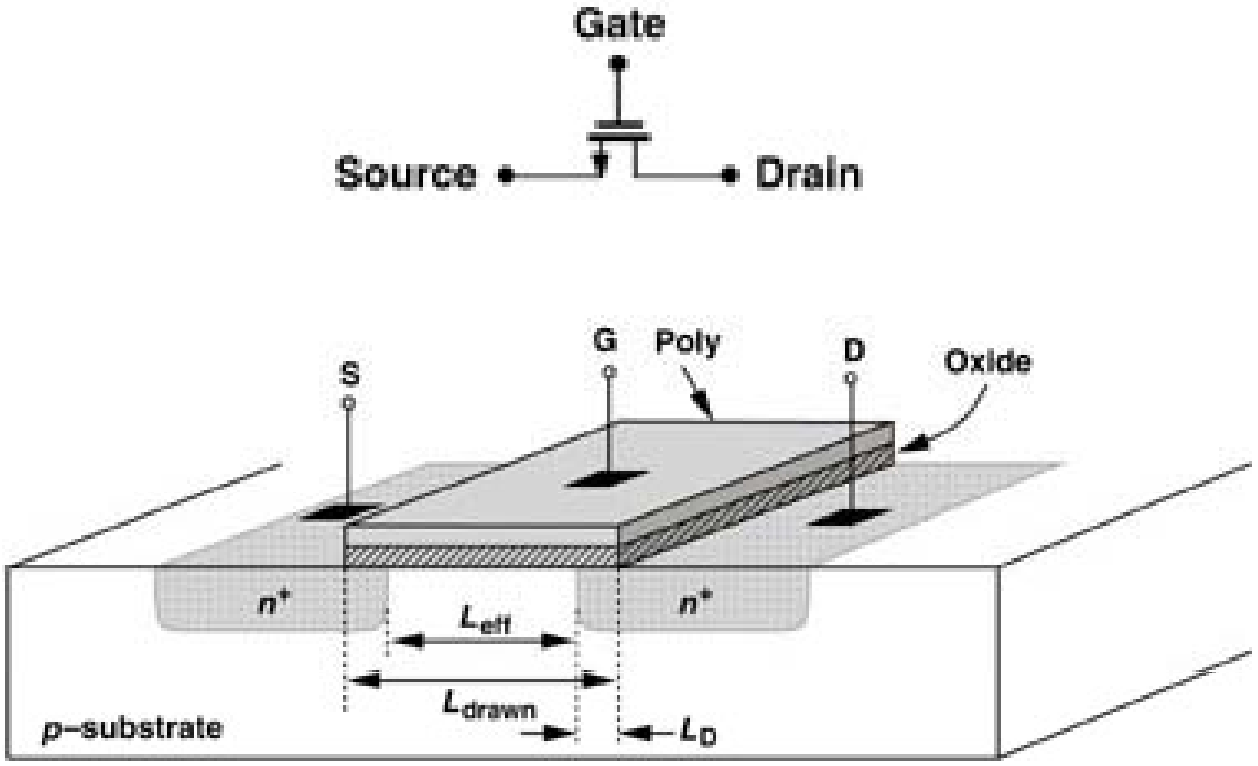
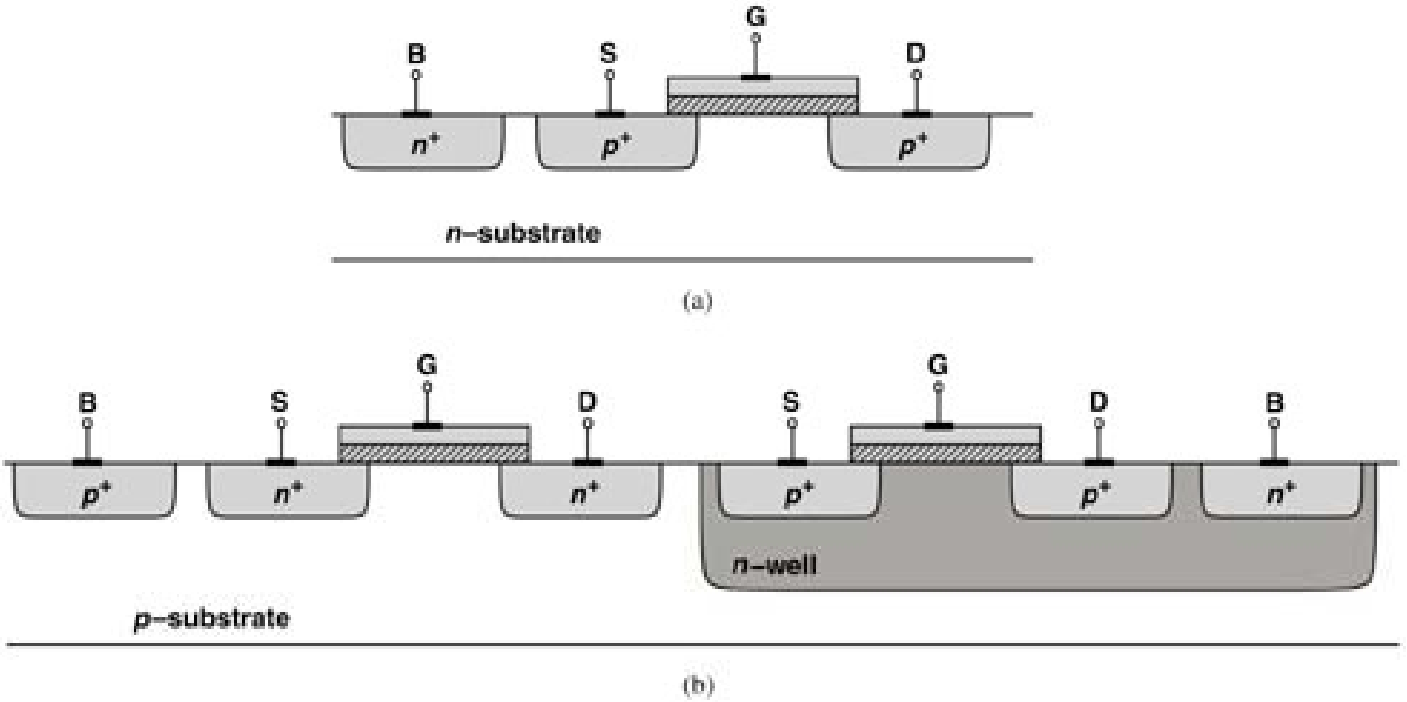
Chapter 2
Basic MOS Device Physics

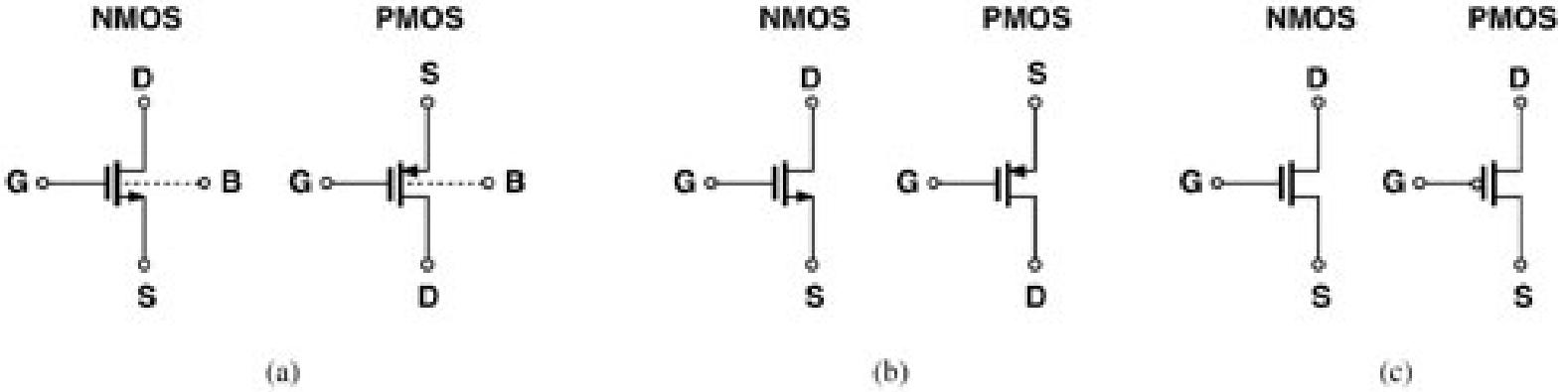
MOS Device Structure



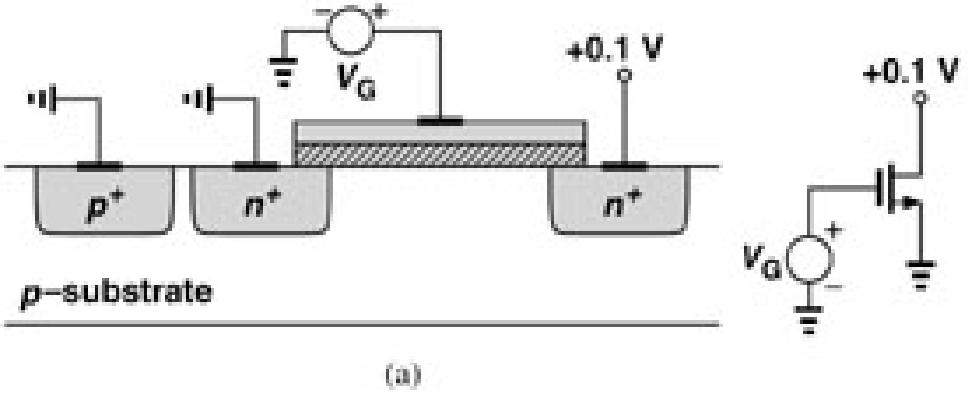
NMOS and PMOS with Well



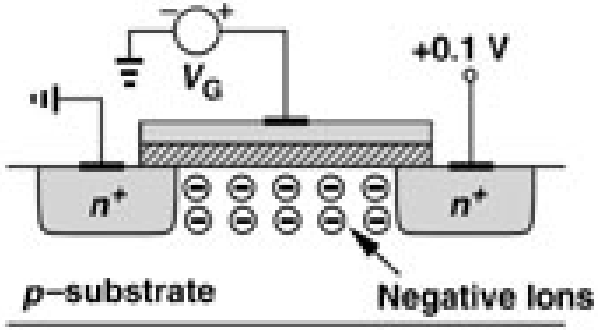
MOS Symbols



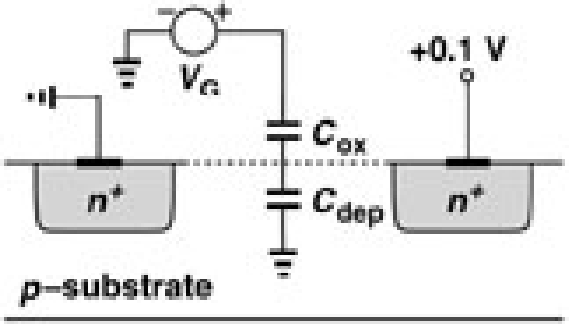
MOS Channel Formation



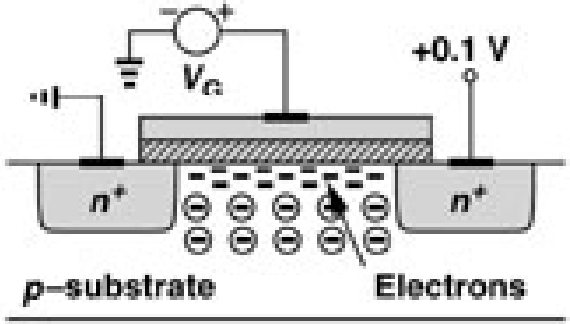
(a)



(b)

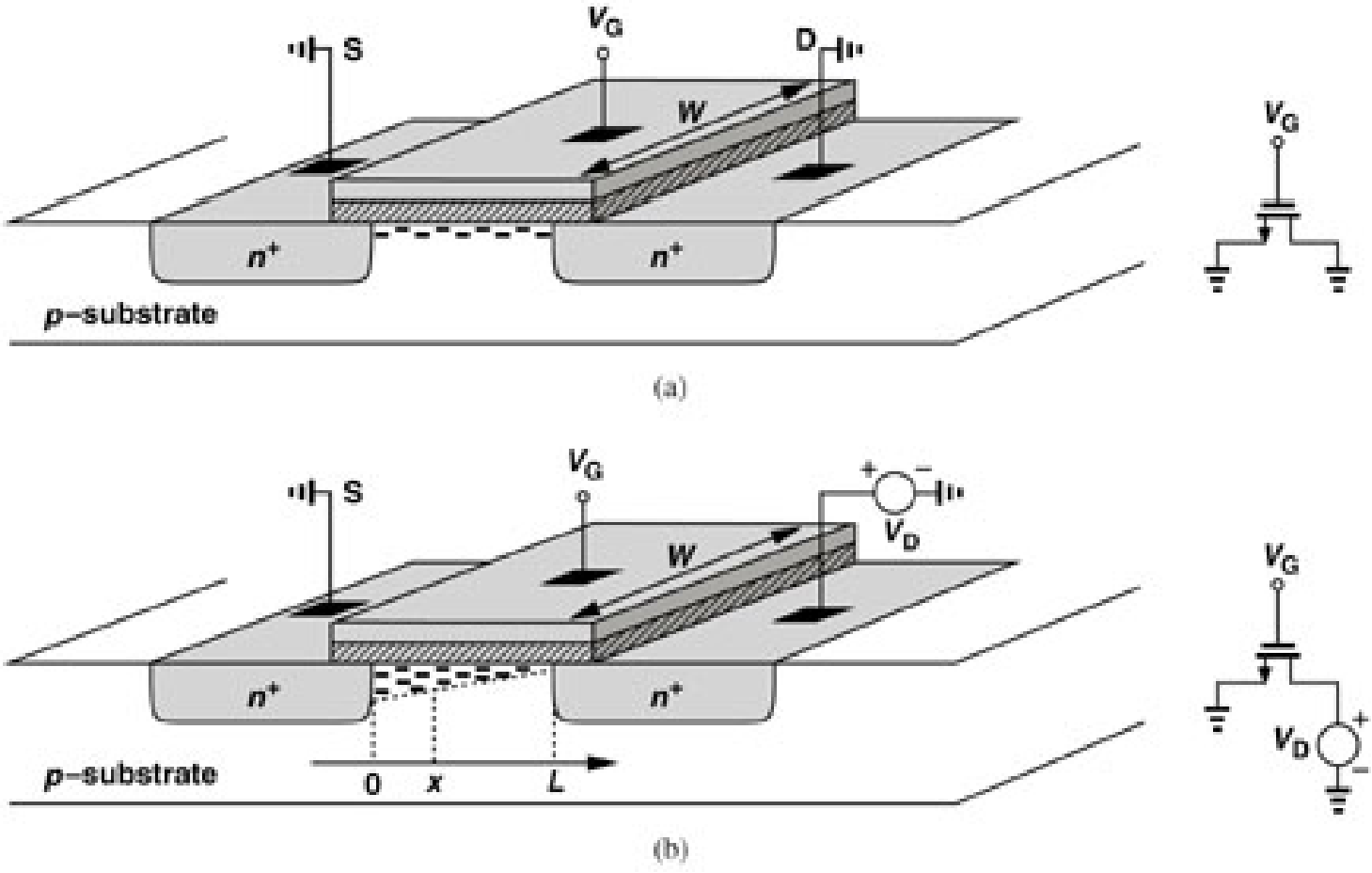


(c)

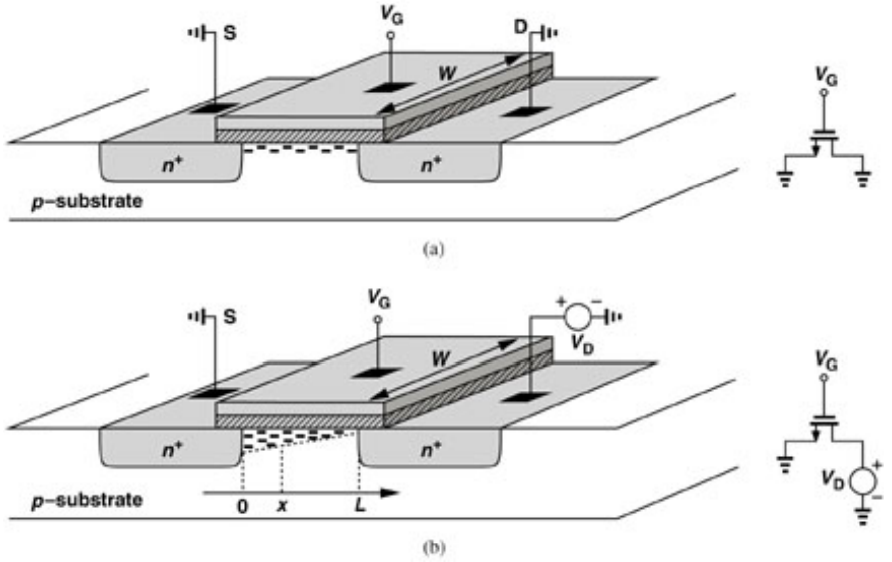


(d)

I/V Characteristics



I/V Characteristics



$$I = Q_d \cdot v$$

$$Q_d = WC_{ox}(V_{GS} - V_{TH})$$

$$Q_d(x) = WC_{ox}(V_{GS} - V(x) - V_{TH})$$

I/V Characteristics (cont.)

$$I_D = -WC_{ox}[V_{GS} - V(x) - V_{TH}]v$$

$$Given \;\; v = \mu E \;\; and \;\; E(x) = -\frac{dV(x)}{dx}$$

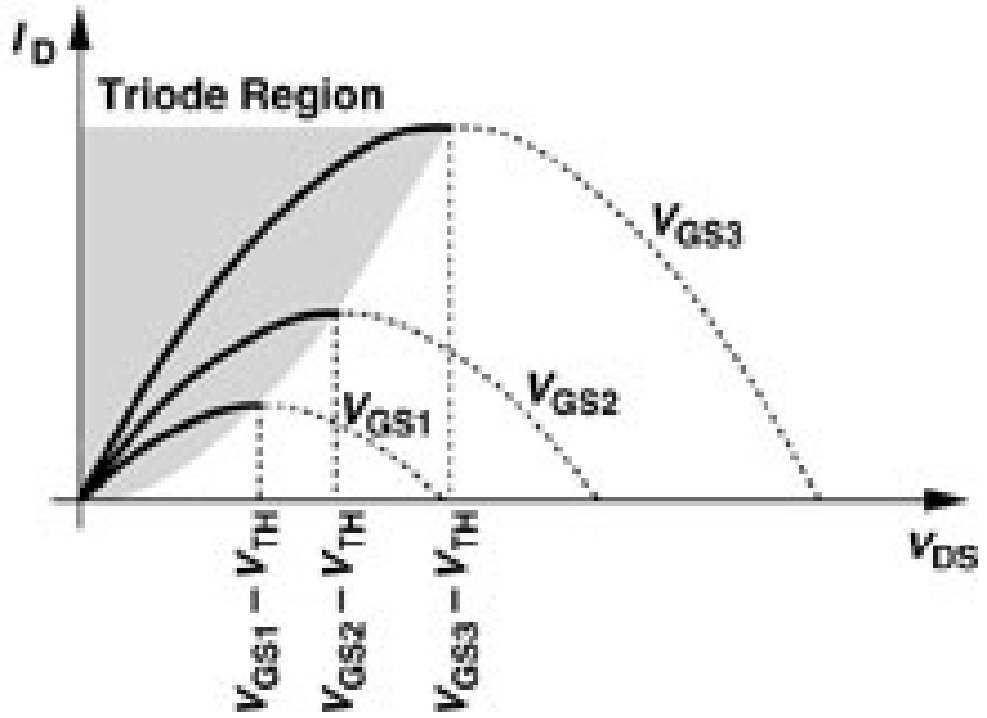
$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$$

$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{VDS} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]dV$$

$$I_D = \mu_n C_{ox}\frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{2}]$$

I/V Characteristics (cont.)

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

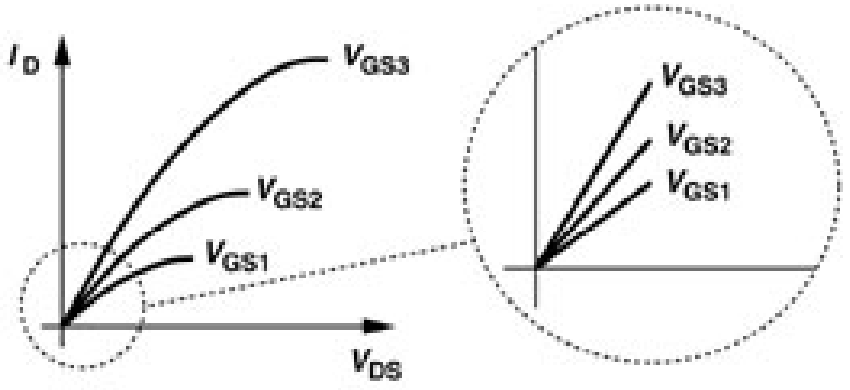


Operation in Triode Region

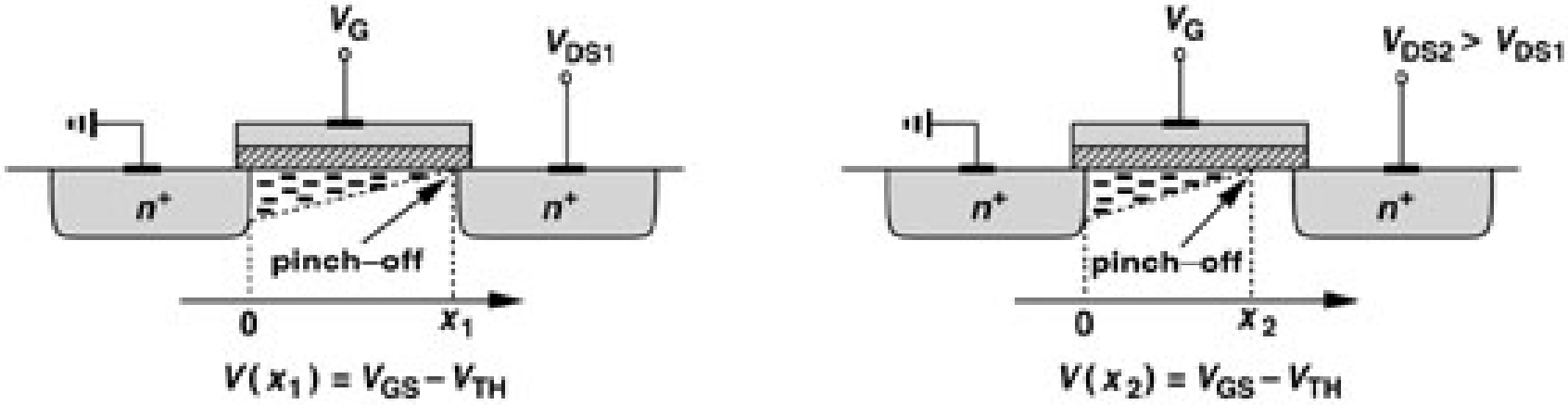
$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}, \quad V_{DS} << 2(V_{GS} - V_{TH})$$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$



Operation in Active (Saturation) Region

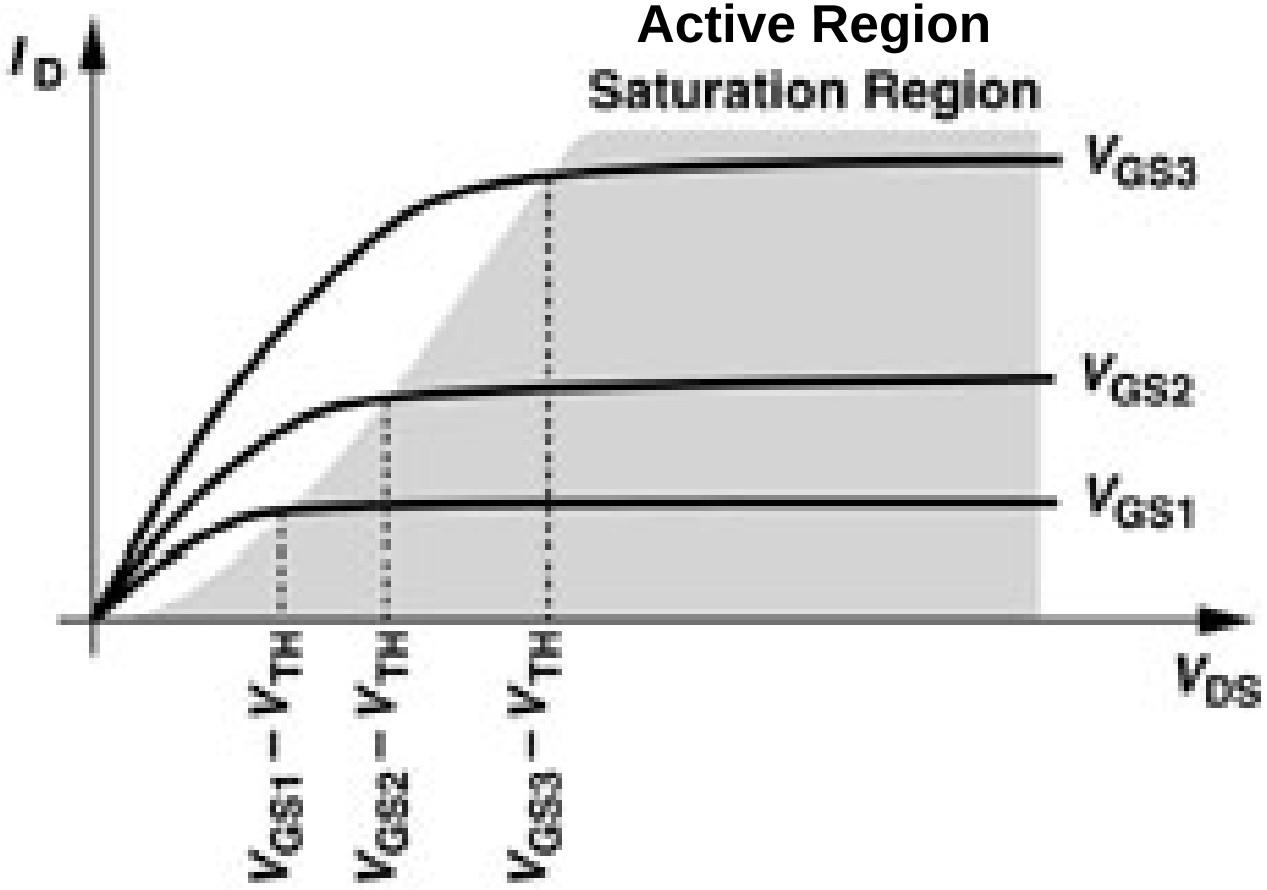


$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$V'_{DS} = V_{GS} - V_{TH} \qquad (Pinch - off)$$

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$$

Active Region (cont.)



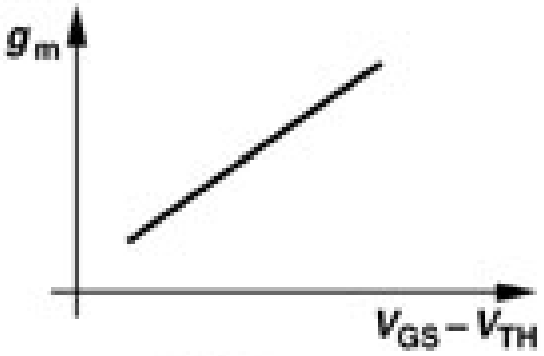
Transconductance, g_m

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS\ \ constant}$$

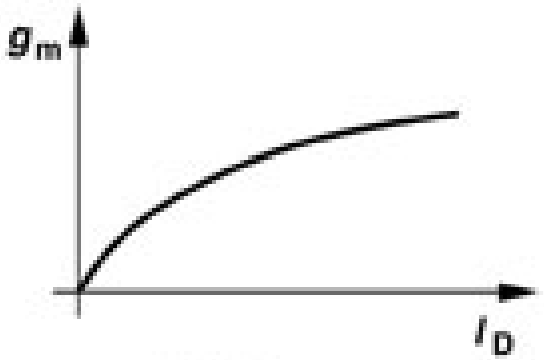
$$= \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D}$$

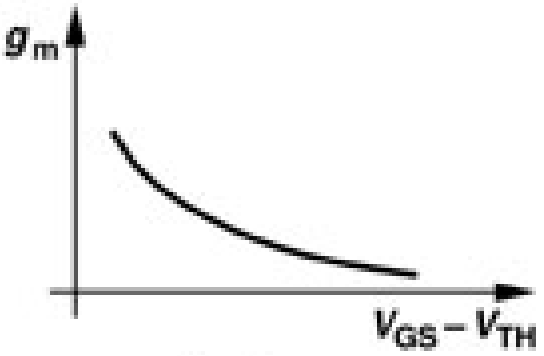
$$= \frac{2 I_D}{V_{GS} - V_{TH}}$$



W/L Constant

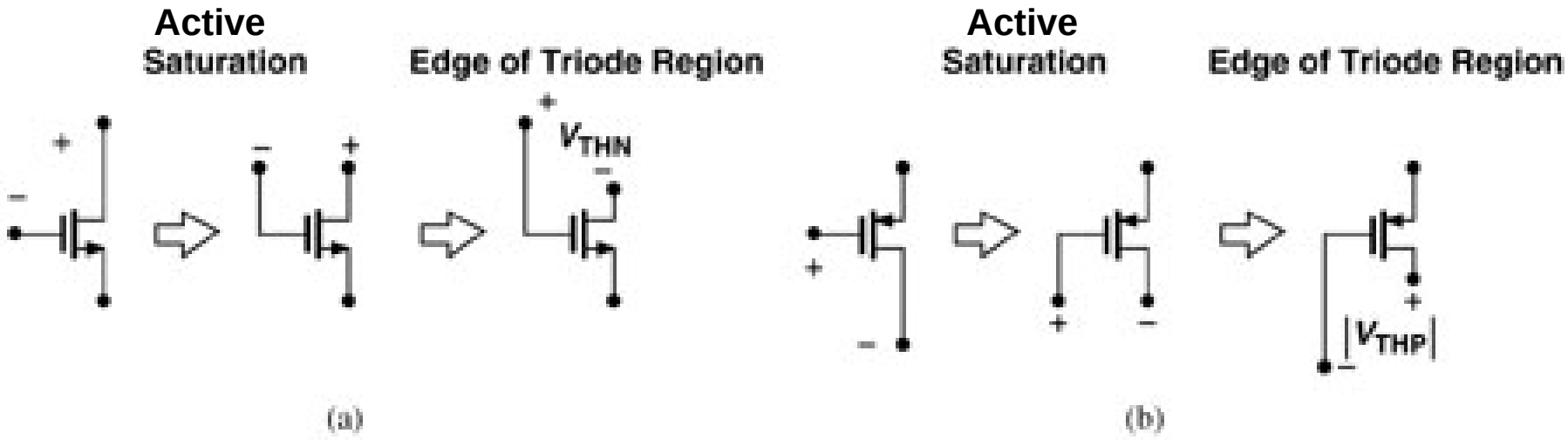


W/L Constant



I_D Constant

Triode and Active Region Transition



Threshold Voltage and Body Effect

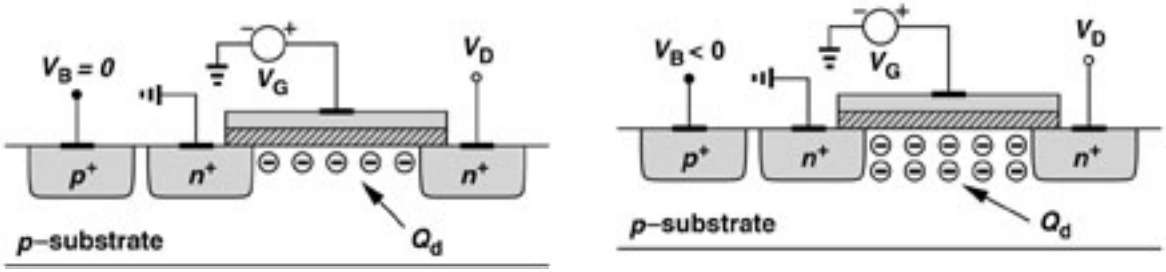
$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}} \quad , \quad where$$

$$\Phi_{MS} = \Phi_{gate} - \Phi_{silicon}$$

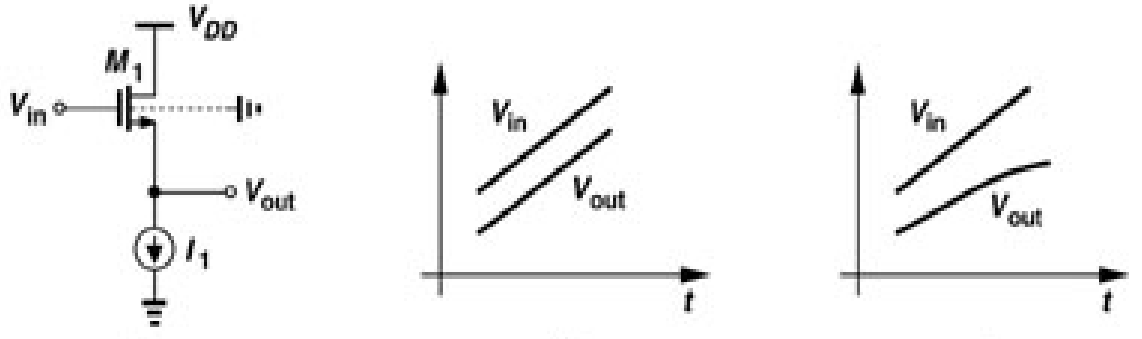
$$\Phi_F = \left(kT/q\right)\ln\left(N_{sub}/n_i\right)$$

$$Q_{dep} = \sqrt{4q\varepsilon_{si}\left|\Phi_F\right|N_{sub}}$$

Threshold Voltage and Body Effect (cont.)



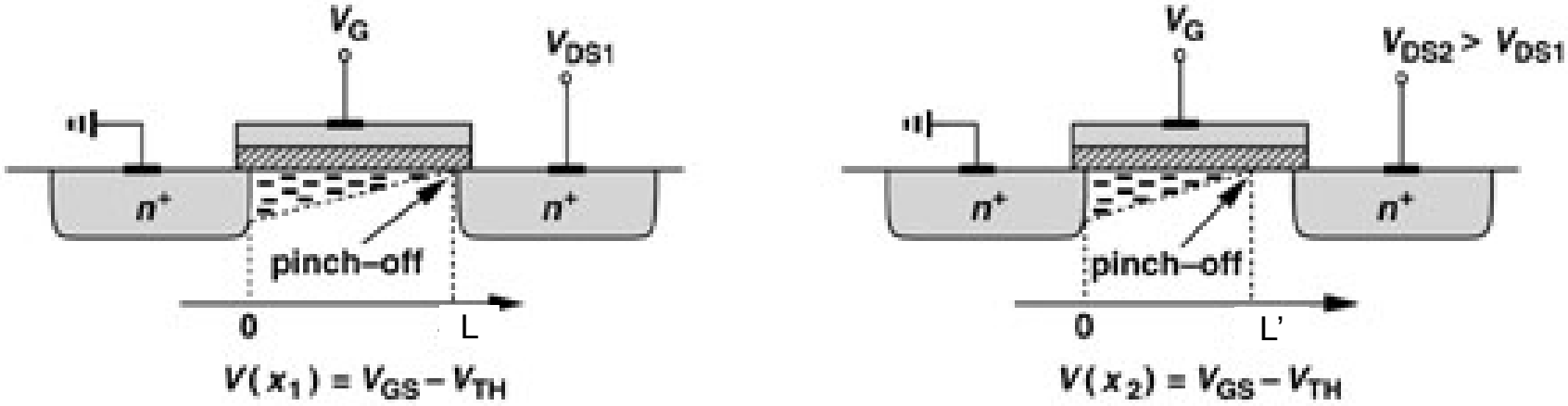
$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right), \quad \gamma = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C_{ox}}$$



No Body Effect

With Body Effect

Channel Length Modulation



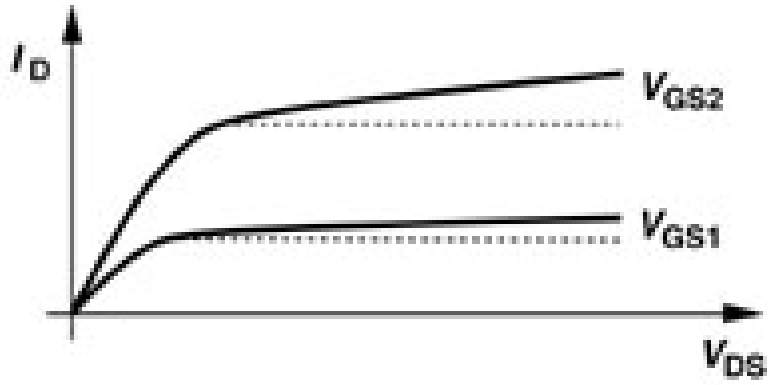
$$L' = L - \Delta L$$

$$1/L' = \frac{1}{L}(1 + \Delta L/L)$$

$$1/L' = \frac{1}{L}(1 + \lambda V_{DS}), \quad \lambda V_{DS} = \Delta L/L$$

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

Channel Length Modulation (cont.)



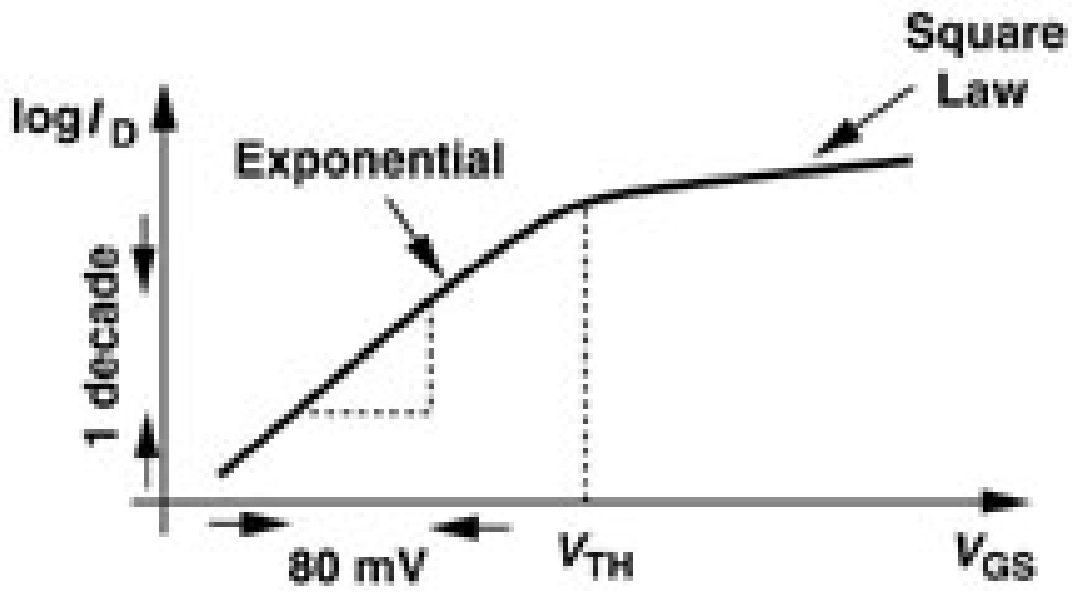
$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS})$$

$$g_m = \sqrt{\frac{2\mu_n C_{ox} W/L \, I_D}{(1 + \lambda V_{DS})}}$$

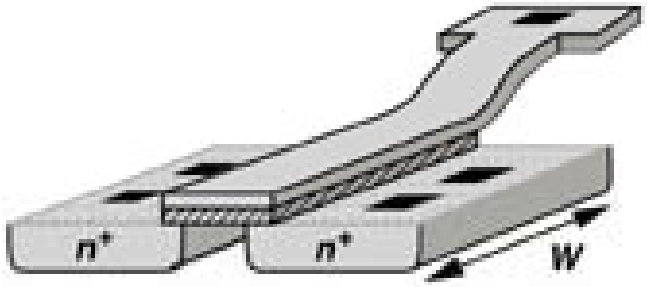
$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}, \quad (unchanged)$$

Subthreshold Conduction

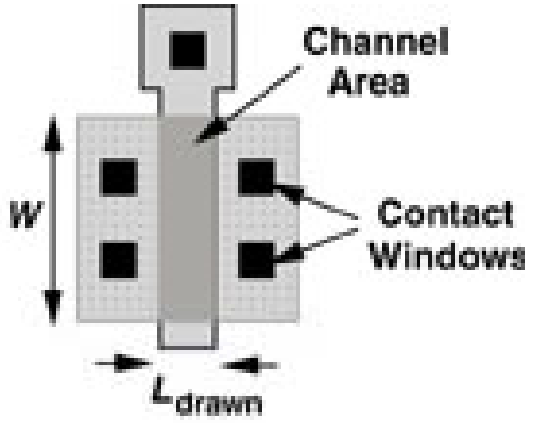
$$I_D = I_0 \exp\left(\frac{V_{GS}}{\zeta kT/q}\right)$$



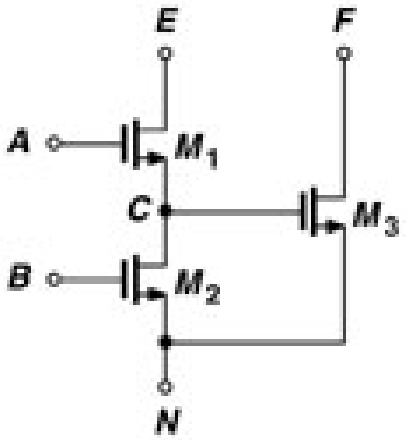
MOS Layout



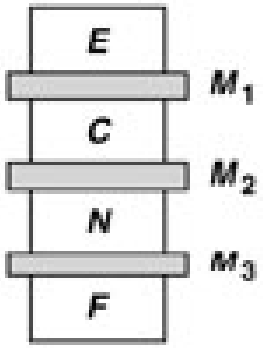
(a)



(b)



(a)



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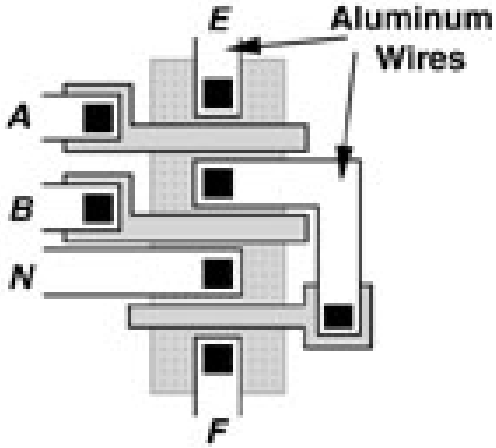
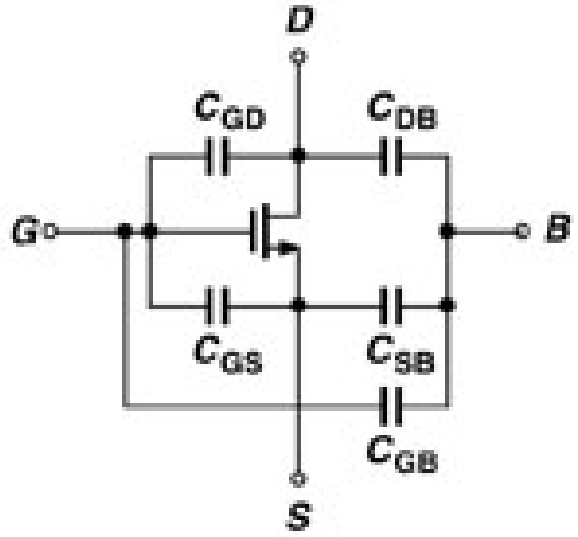
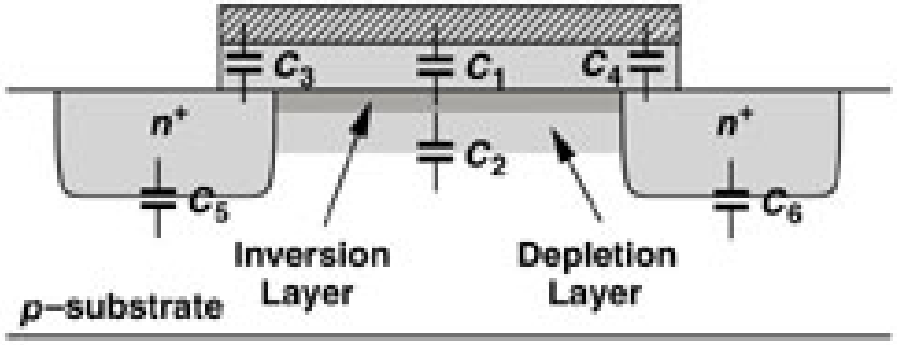


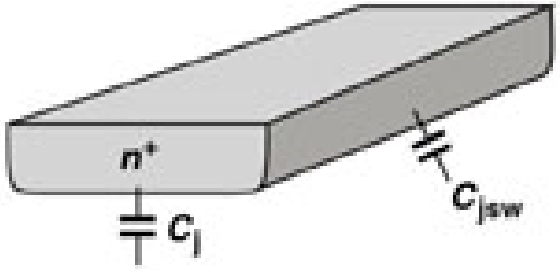
(c)

Device Capacitances



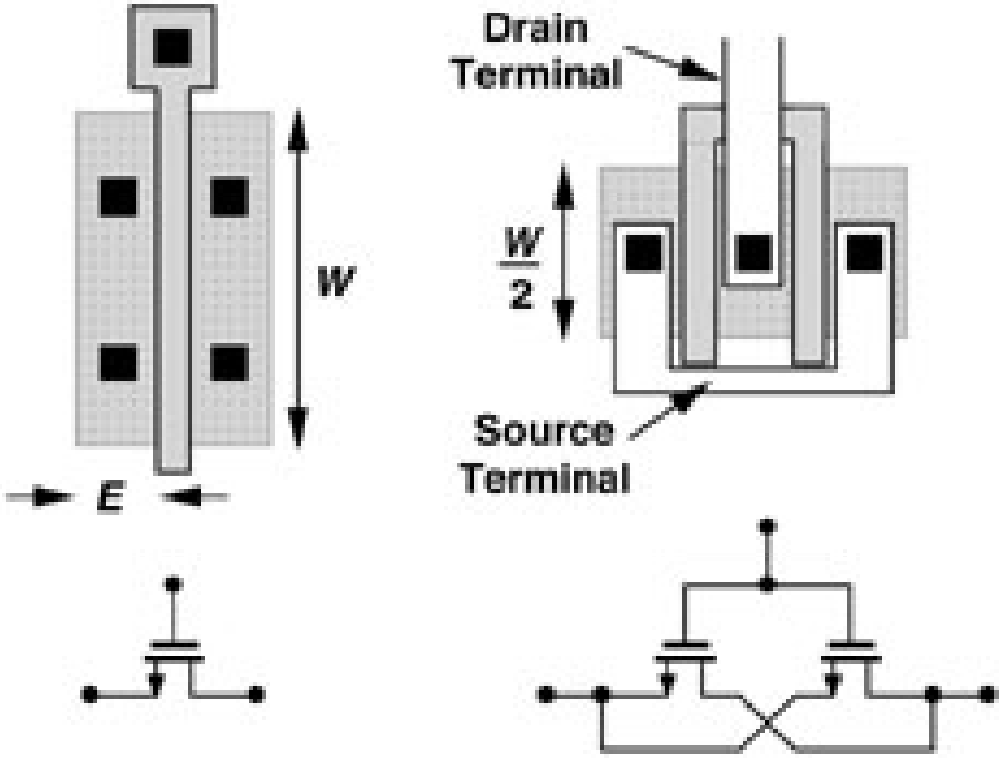


(a)

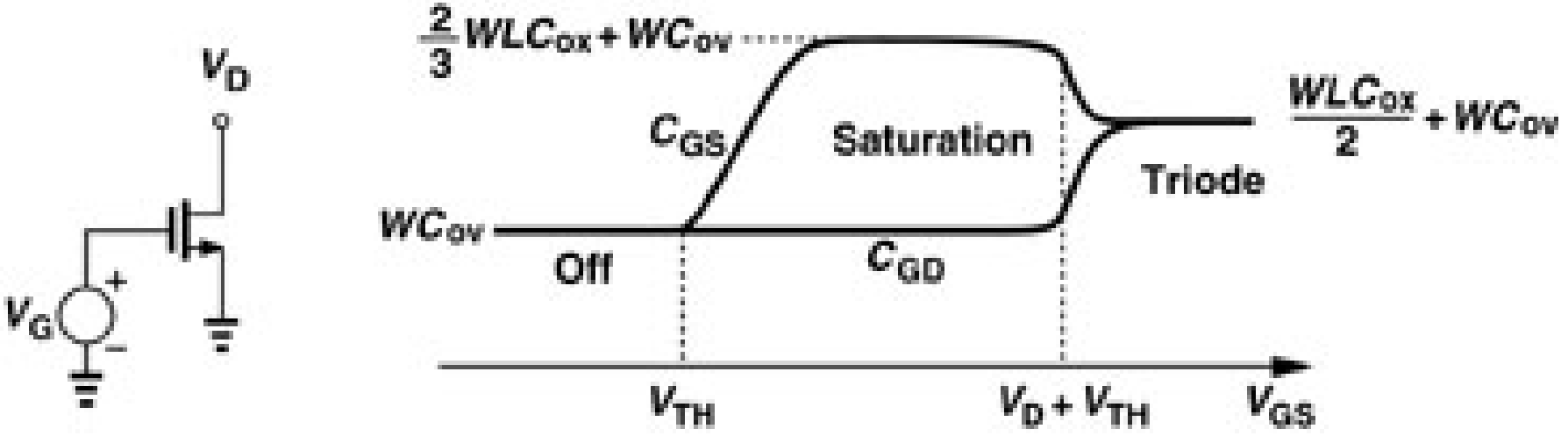


(b)

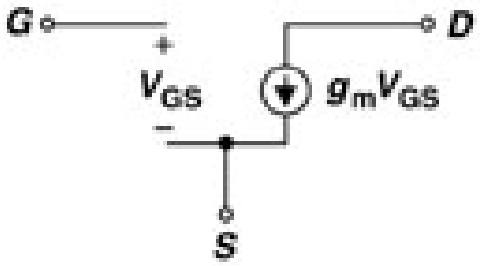
Layout for Low Capacitance

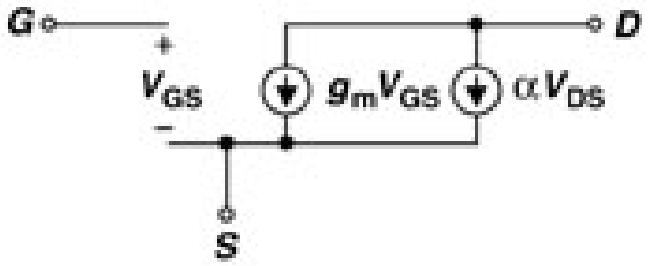


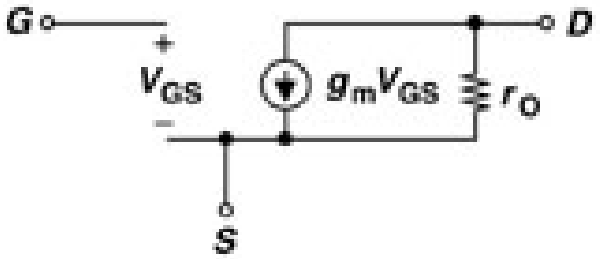
G-S and G-D Capacitance

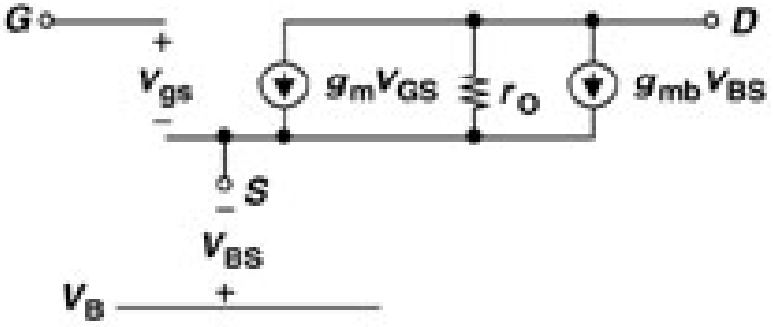


MOS Small Signal Models









$$r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \lambda} = \frac{1}{\lambda I_D}$$

Bulk Transconductance, g_{mb}

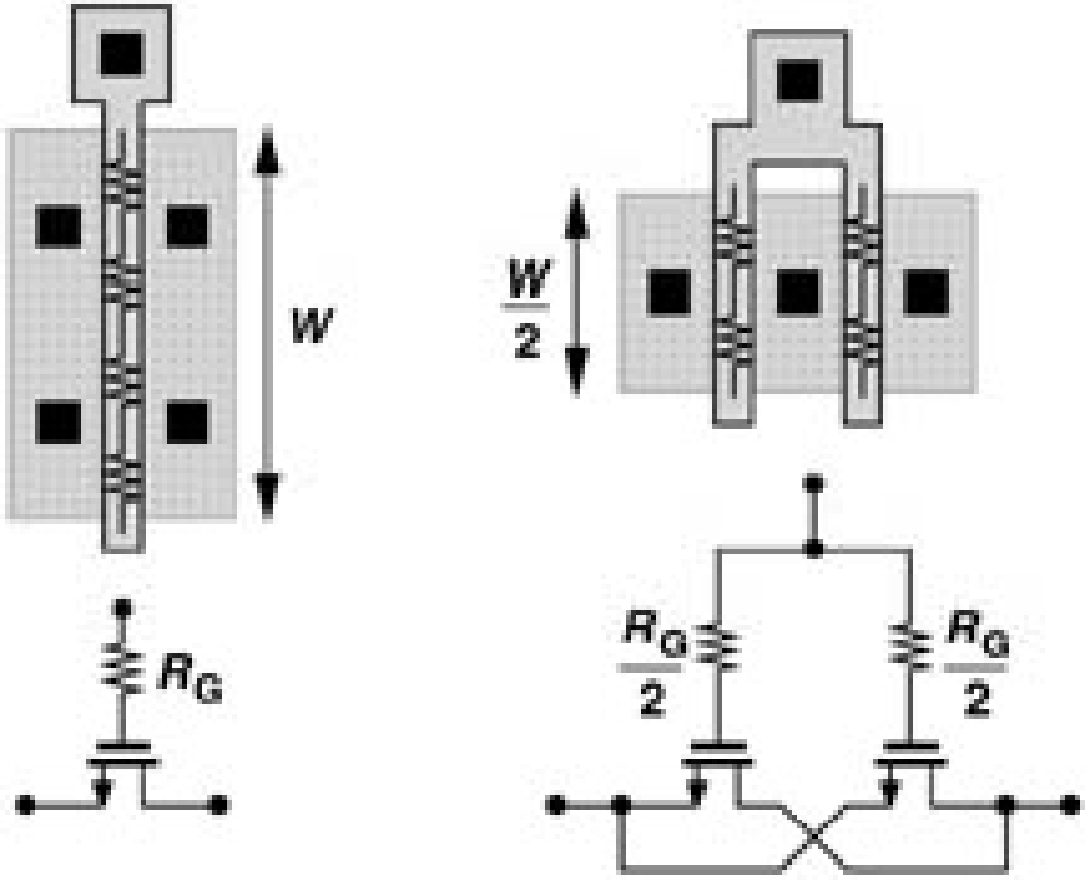
$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})\left(\frac{-\partial V_{TH}}{\partial V_{BS}}\right)$$

Also,

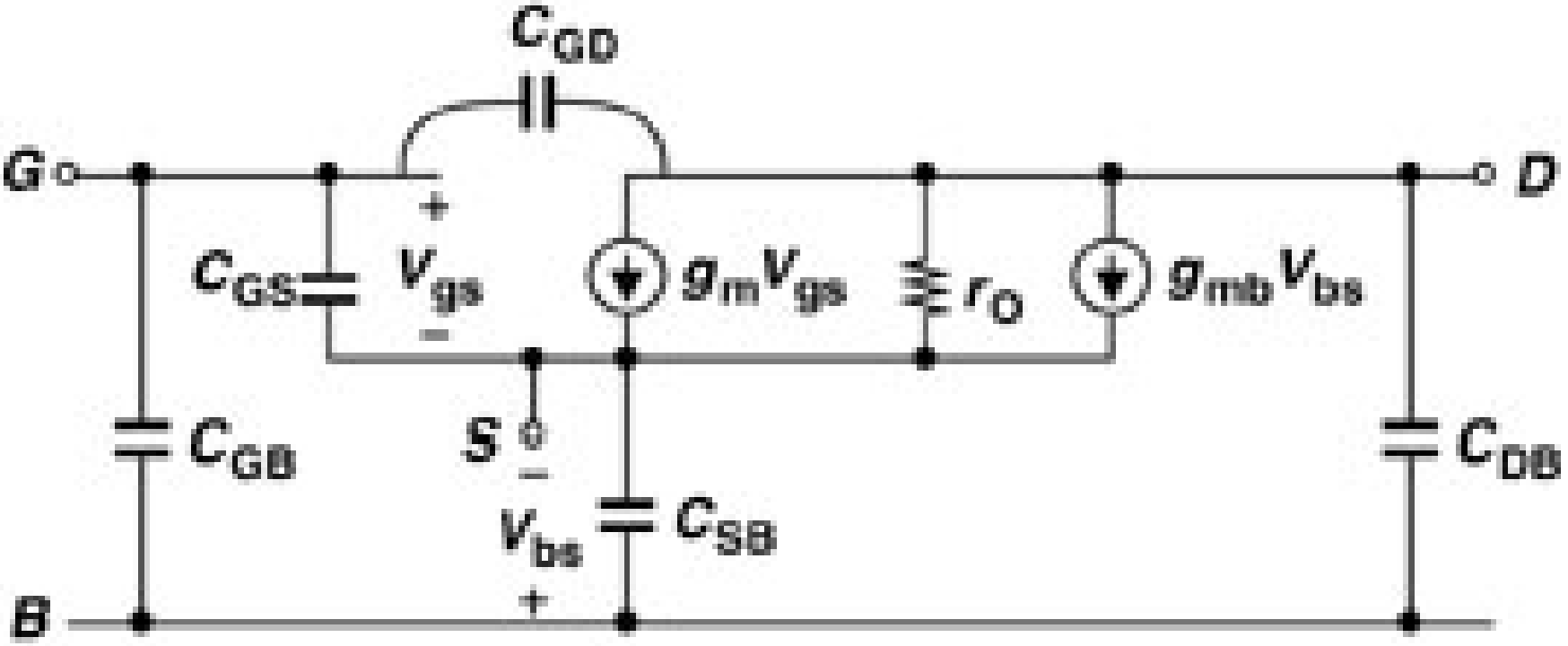
$$\frac{\partial V_{TH}}{\partial V_{BS}} = \frac{-\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-1/2}$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m$$

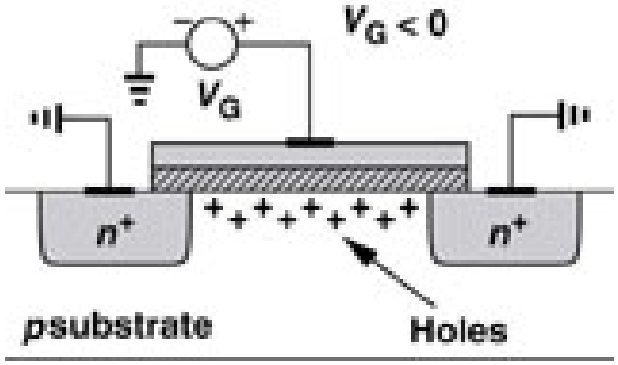
Gate Resistance

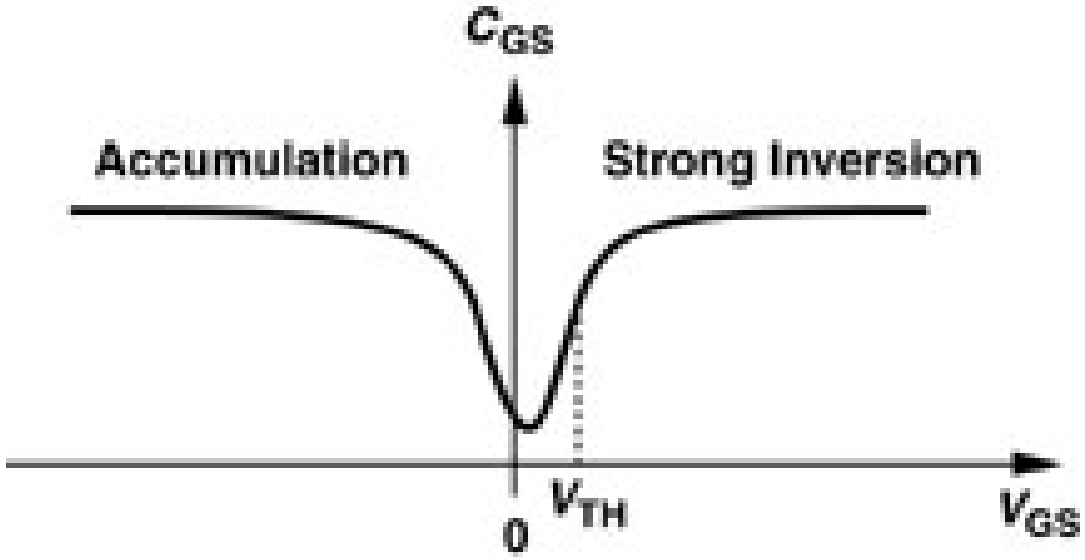


MOS Small Signal Model with Capacitance



C-V of NMOS


$V_G < 0$
V_G
n^+
n^+
psubstrate
Holes


C_{GS}
Accumulation
Strong Inversion
0
V_{TH}
V_{GS}