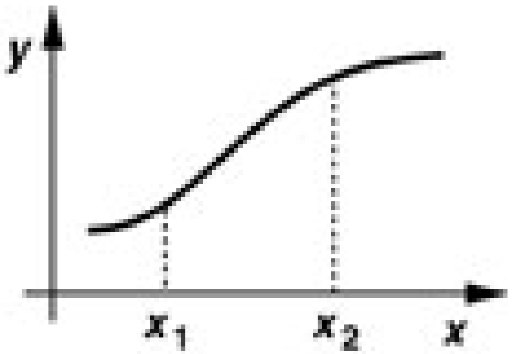
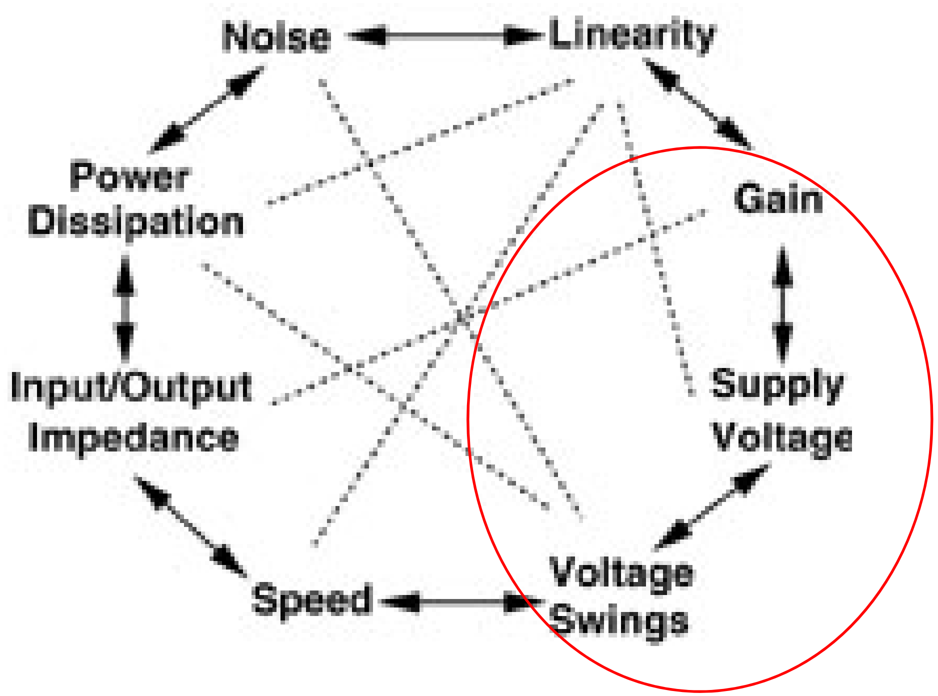
Chapter 3
Single-Stage Amplifiers

Analog Design



Non-linear system

Tradeoffs



Common-Source (CS) Amplifier With R_D Load

Design Method, Constraints and Tradeoffs-L5

Simple CS Amplifier

- <u>Given:</u> k_n', V_{TH}, λ
- <u>Need:</u> Specific voltage gain $A_v = -g_m R_D$

<u>Design Parameters:</u>

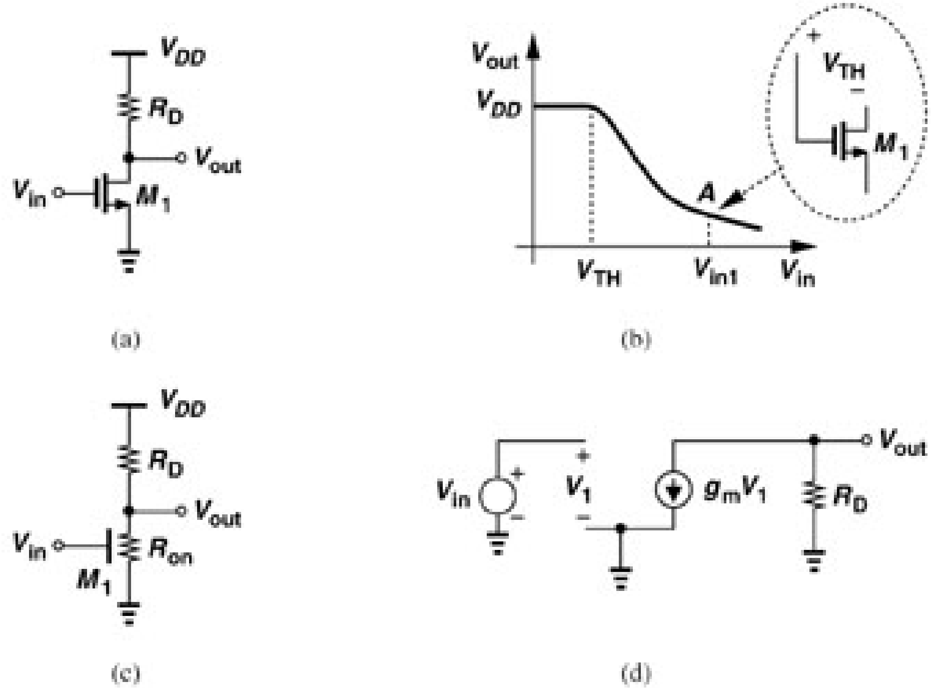
$V_{DD}, I_D, V_G, W/L, R_D$

<u>Constraints:</u>

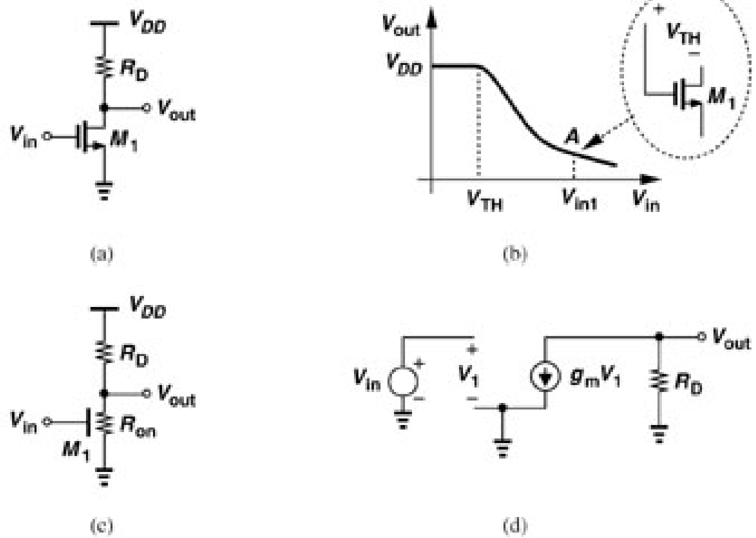
Saturation Mode

Current-Voltage relationship

Swing

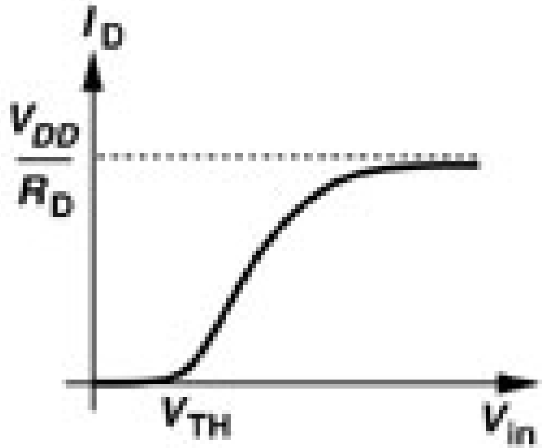


Common Source – Large Signal Analysis

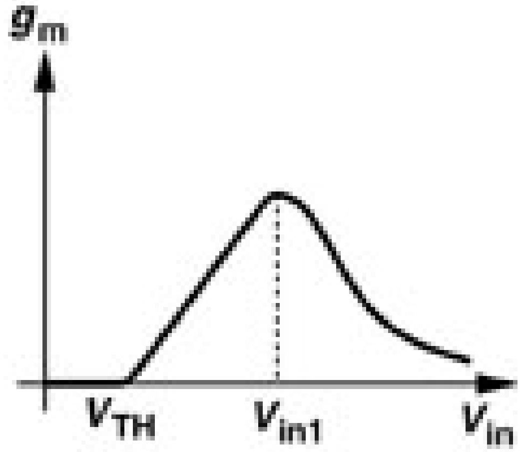


- If V_{in} is low (below threshold) transistor is OFF
- For V_{in} not-too-much-above threshold, transistor is in Saturation, and V_{out} decreases.
- For large enough input (V_{in}>V_{in1}) – Triode Mode.

Common Source (cont.)



(a)

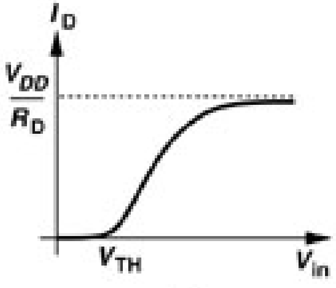


(b)

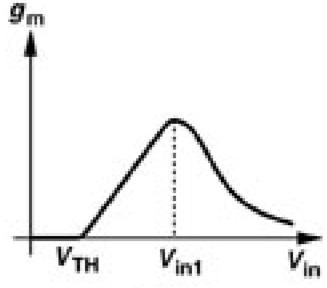
$$A_v = -g_m R_D$$

$$A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}}\,\frac{V_{RD}}{\sqrt{I_D}}$$

Design Tradeoffs



(a)

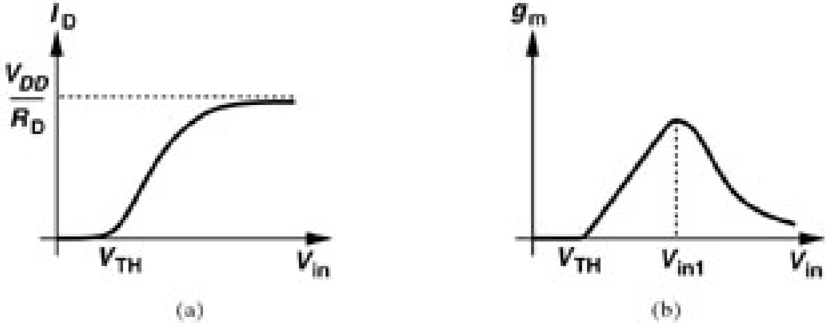


(b)

$$A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}}\frac{V_{RD}}{\sqrt{I_D}}$$

- Gain is determined by 3 factors: W/L, R_D DC voltage and I_D
- If current and R_D are kept constant, an increase of W/L increases the gain, but it also increases the gate capacitance – lower bandwidth

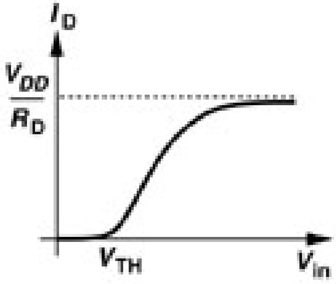
Design Tradeoffs



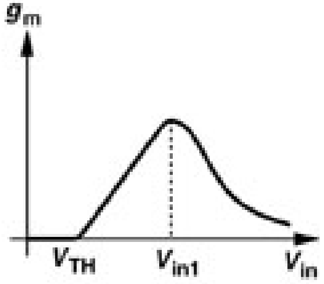
$$A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}}\,\frac{V_{RD}}{\sqrt{I_D}}$$

- If I_D and W/L are kept constant, and we increase R_D, then V_{DS} becomes smaller. Operating Point gets closer to the borderline of Triode Mode.
- It means – less “swing” (room for the amplified signal)

Design Tradeoffs



(a)

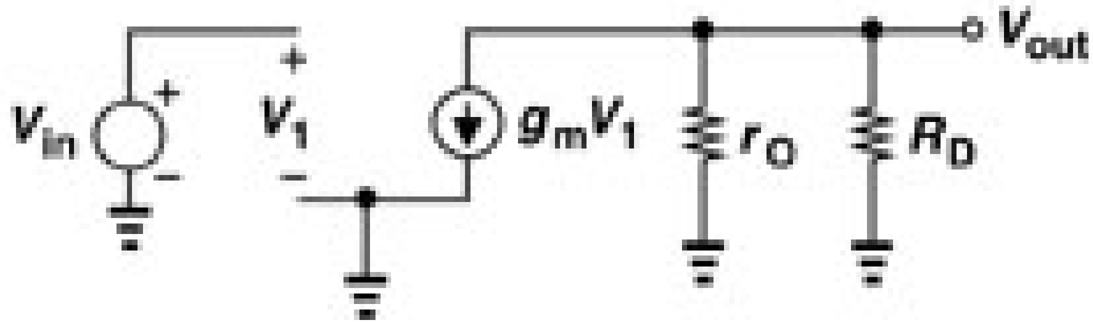


(b)

$$A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}}\frac{V_{RD}}{\sqrt{I_D}}$$

- If I_D decreases and W/L and V_{RD} are kept constant, then we must increase R_D
- Large R_D consumes too much space, increases the noise level and slows the amplifier down (time constant with input capacitance of next stage).

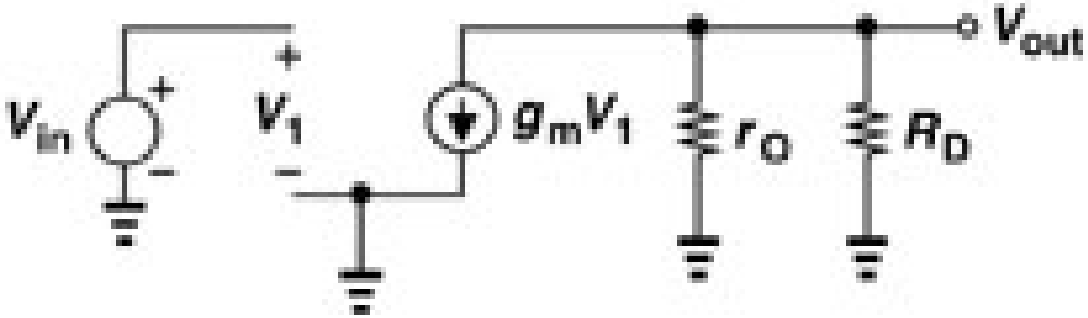
Common Source Tradeoffs

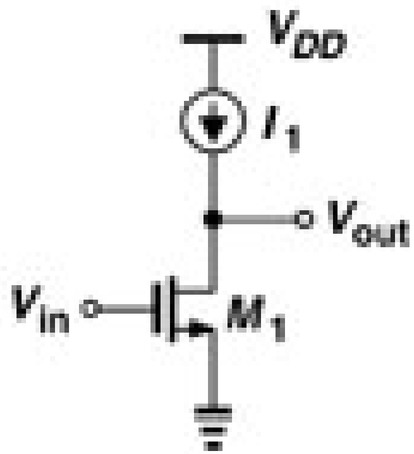


$$A_v = -g_m r_o \parallel R_D$$

- Larger R_D values increase the influence of channel-length modulation (r_o term begins to strongly affect the gain)

Common Source Maximum Gain



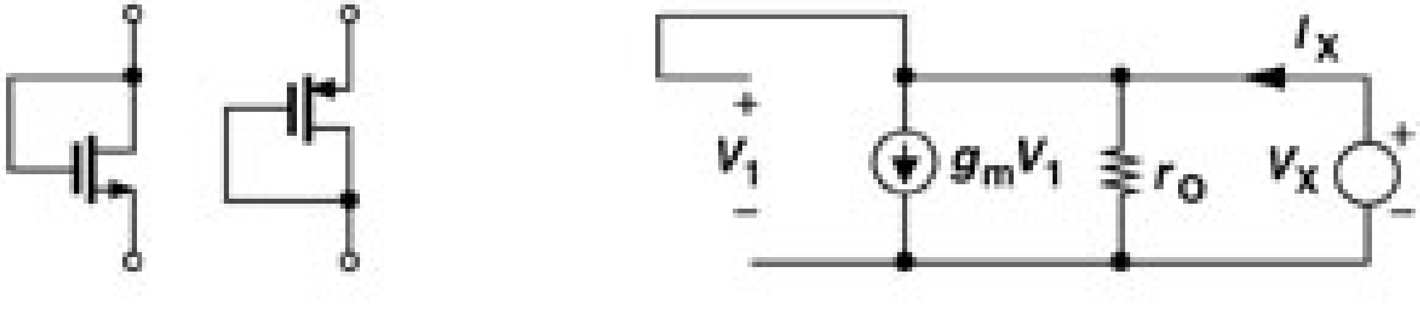


$$A_v = -g_m r_o \| R_D$$

$$A_v = -g_m r_o$$

"*intrinsic gain*"

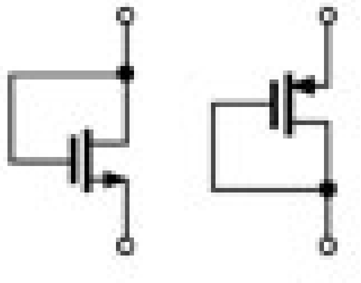
CS Amplifier with Diode-Connected Load-L6

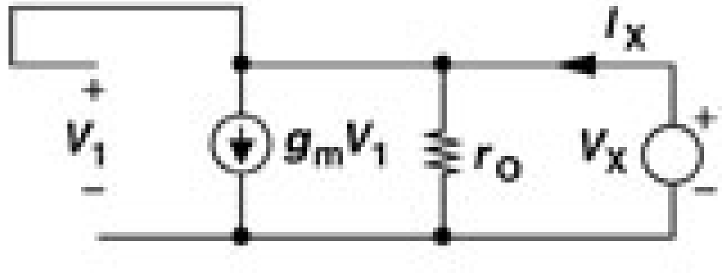


(a) (b)

- "Diode-Connected" MOSFET is only a name. In BJT if Base and Collector are short-circuited, then the BJT acts exactly as a diode.

CS Amplifier with Diode-Connected Load



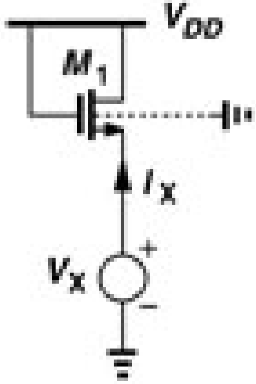


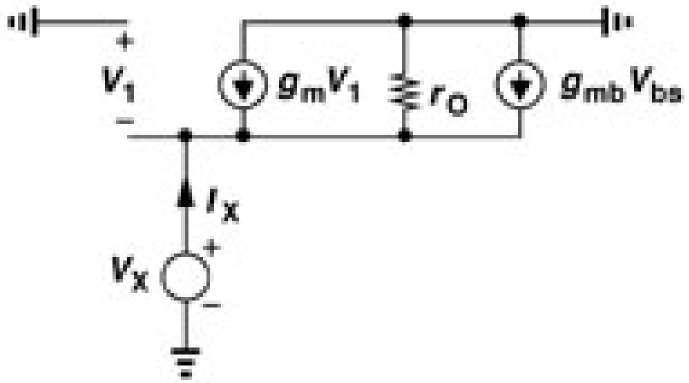
- We want to replace R_D with a MOSFET that will operate like a small-signal resistor.

$$V_1 = V_X \Rightarrow I_X = \frac{V_X}{r_o} + g_m V_X$$

$$\Rightarrow R_d = \frac{1}{g_m} \| r_o \approx \frac{1}{g_m}$$

Common Source with Diode-Connected NMOS Load (Body Effect included)

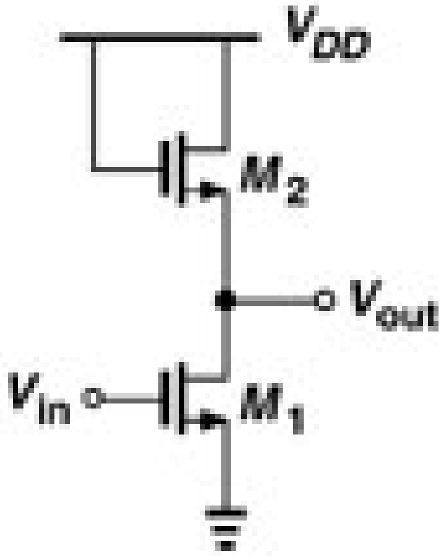




$$(g_m + g_{mb})V_x + \frac{V_x}{r_o} = I_x$$

$$\frac{V_x}{I_x} = \frac{1}{g_m + g_{mb}} \parallel r_o \approx \frac{1}{g_m + g_{mb}}$$

CS with Diode-Connected NMOS Load
Voltage Gain Calculation

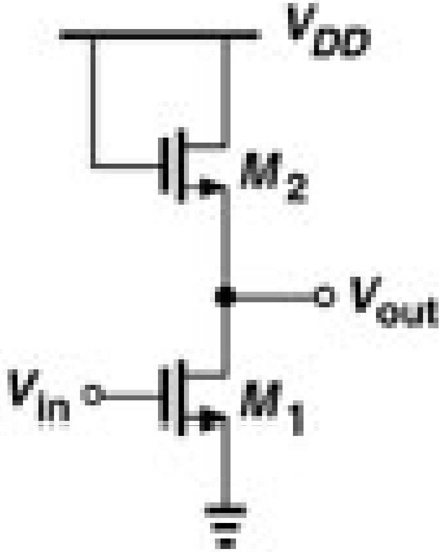


$$A_v = -g_{m1}\frac{1}{g_{m2}+g_{mb2}} = -\frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta}$$

$$A_v = -\sqrt{\frac{2\mu_n C_{OX}(W/L)_1 I_{D1}}{2\mu_n C_{OX}(W/L)_2 I_{D2}}}\frac{1}{1+\eta}$$

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta}$$

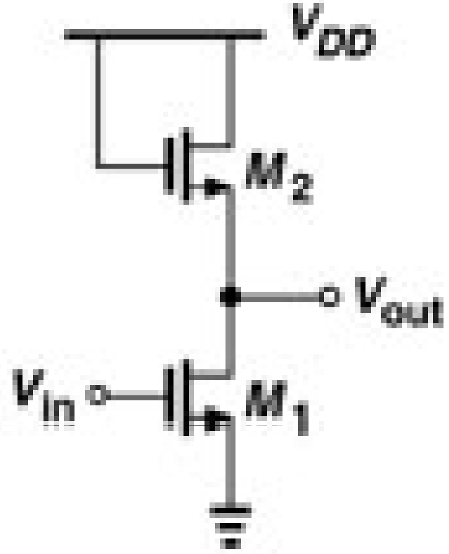
CS with Diode-Connected NMOS Load Voltage Gain Calculation



$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta}$$

- If variations of η with the output voltage are neglected, the gain is independent of the bias currents and voltages (as long as M_1 stays in Saturation)
- The point: Gain does not depend on V_{in} (as we so in the case of R_D load)

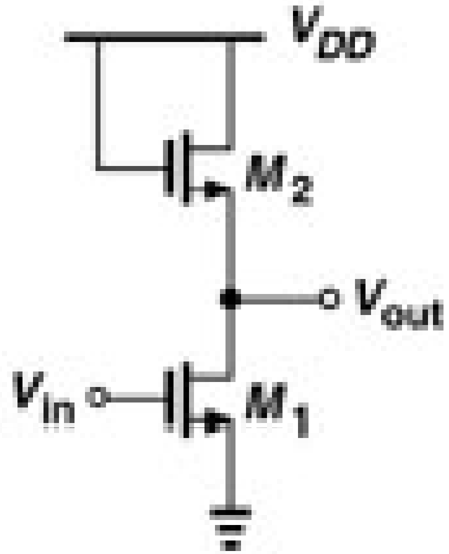
Amplifier is relatively linear (even for large signal analysis!)



$$0.5\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 = 0.5\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{out} - V_{TH2})^2$$

$$\sqrt{\left(\frac{W}{L}\right)_1} (V_{in} - V_{TH1}) = \sqrt{\left(\frac{W}{L}\right)_2} (V_{DD} - V_{out} - V_{TH2})$$

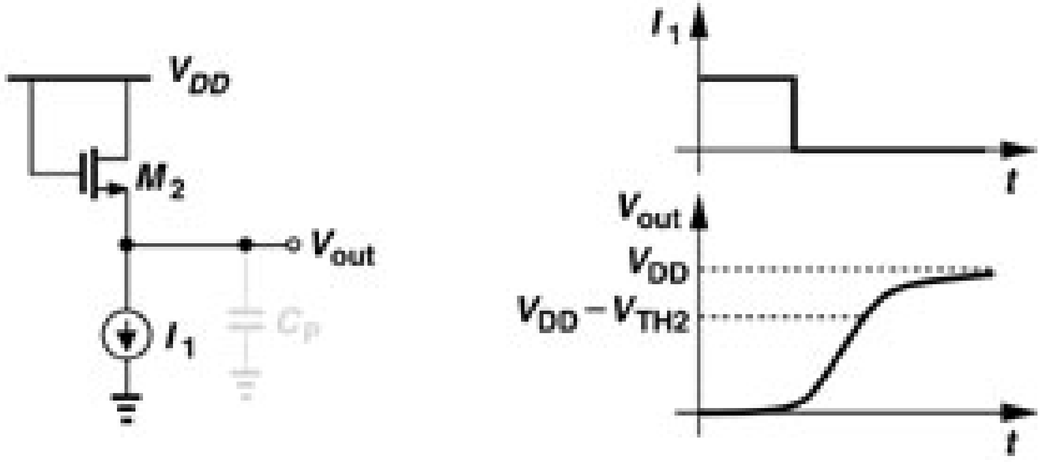
Assumptions made along the way:



$$\sqrt{\left(\frac{W}{L}\right)_1}(V_{in} - V_{TH1}) = \sqrt{\left(\frac{W}{L}\right)_2}(V_{DD} - V_{out} - V_{TH2})$$

- We neglected channel-length modulation effect
- We neglected V_{TH} voltage dependent variations
- We assumed that two transistors are matching in terms of C_{OX}.

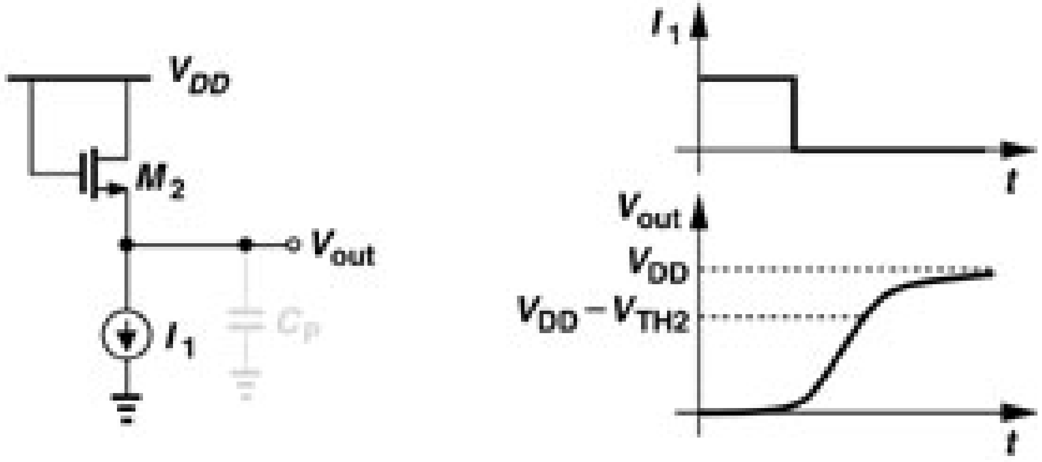
Comment about “cutting off”



(a) (b)

- If I_1 is made smaller and smaller, what happens to V_{out}?
- It should be equal to V_{DD} at the end of the current reduction process, or is it?

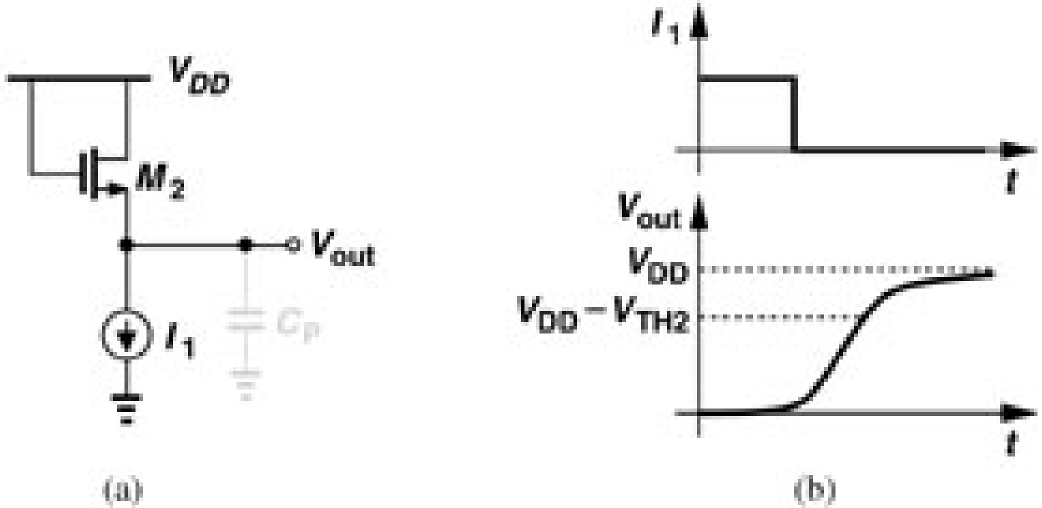
Comment about “cutting off” (cont’d)



(a) (b)

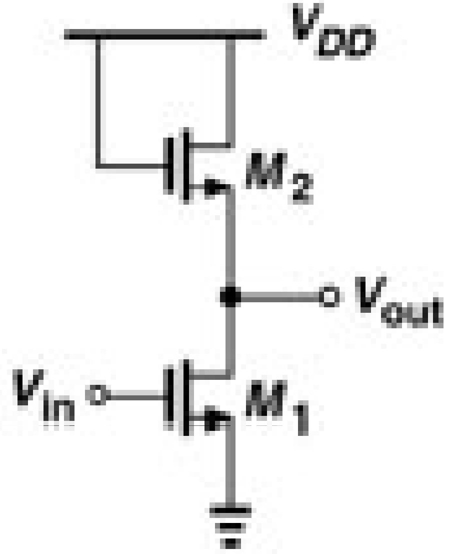
- If I_1 is made smaller and smaller, V_{GS} gets closer and closer to V_{TH}.
- Very near I_1=0, if we neglect sub-threshold conduction, we should have $V_{GS} \approx V_{TH2}$, and therefore $V_{out} \approx V_{DD}-V_{TH2}$!

Cutoff conflict resolved:

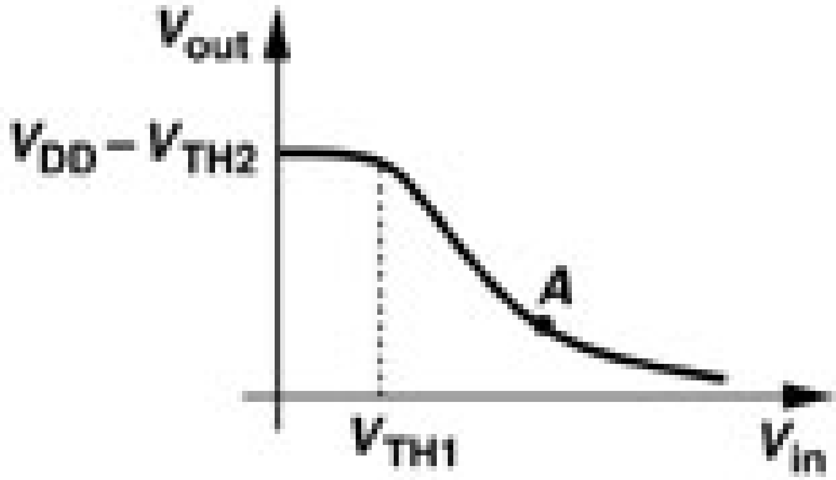


- In reality, sub-threshold conduction, at a very low current, eventually brings V_{out} to the value V_{DD}.
- Output node capacitance slows down this transition.
- In high-speed switching, sometimes indeed V_{out} doesn't make it to V_{DD}

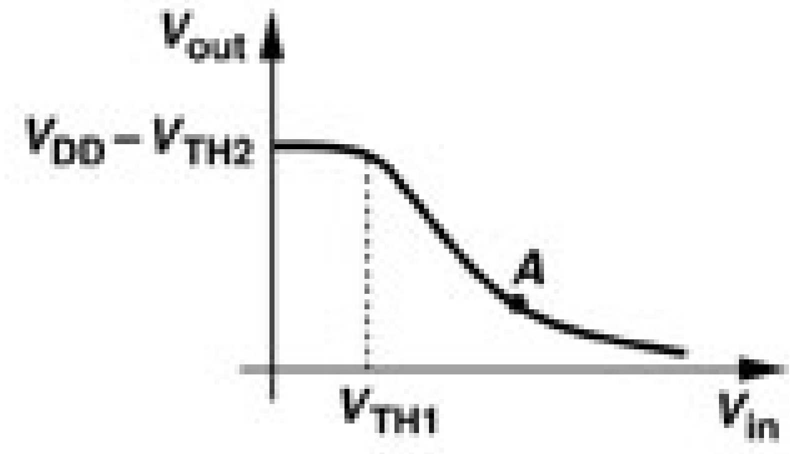
Back to large-signal behavior of the CS amplifier with diode-connected NMOS load:



$$\sqrt{\left(\frac{W}{L}\right)_1}(V_{in}-V_{TH1})=\sqrt{\left(\frac{W}{L}\right)_2}(V_{DD}-V_{out}-V_{TH2})$$

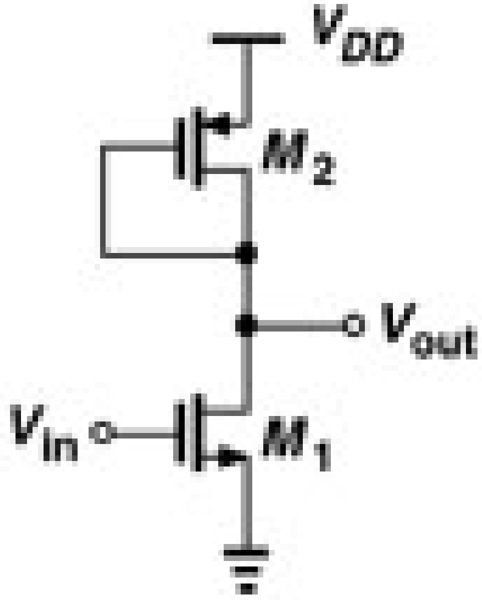


Large signal behavior of CS amplifier with diode-connected load



- When $V_{in}<V_{TH1}$ (but near), we have the above "imperfect cutoff" effect.
- Then we have a, more or less, linear region.
- When V_{in} exceeds $V_{out}+V_{TH1}$ amplifier enters the Triode mode, and becomes nonlinear.

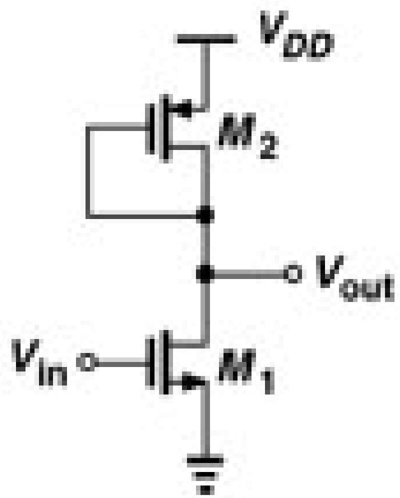
CS with Diode-Connected PMOS Load Voltage Gain



$$A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

No body effect!

Numerical Example



- Say that we want the voltage gain to be 10. Then:

$$A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} = -10$$

$$\Rightarrow \frac{\mu_n (W/L)_1}{\mu_p (W/L)_2} = 100$$

Example continued

$$\frac{\mu_n \, (W/L)_1}{\mu_p \, (W/L)_2} = 100$$

- Typically

$$\mu_n \approx 2\mu_p$$

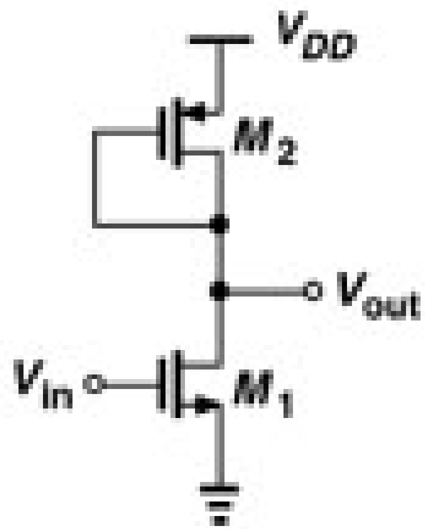
Example continued

$$\frac{(W/L)_1}{(W/L)_2} \approx 50$$

- Need a “strong” input device, and a “weak” load device.
- Large dimension ratios lead to either a larger input capacitance (if we make input device very wide $(W/L)_1 >> 1$) or to a larger output capacitance (if we make the load device very narrow $(W/L)_2 << 1$).
- Latter option (narrow load) is preferred from bandwidth considerations.

CS with Diode-Connected Load Swing Issues

$$ID1 = ID2, \quad \therefore$$



$$\mu_n\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 \approx \mu_p\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2$$

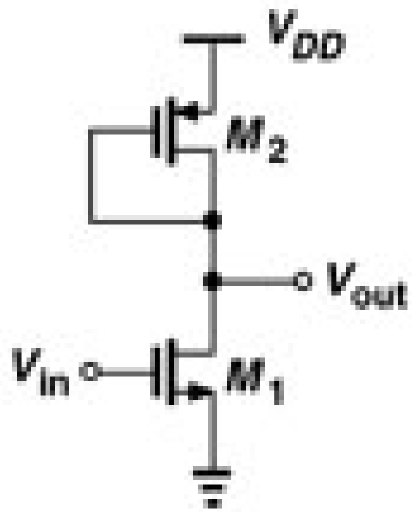
$$A_v = -\sqrt{\frac{\mu_n\,(W/L)_1}{\mu_p\,(W/L)_2}} \approx \frac{|V_{GS2} - V_{TH2}|}{(V_{GS1} - V_{TH1})}$$

This implies substantial voltage swing constraint. Why?

Numerical Example to illustrate the swing problems

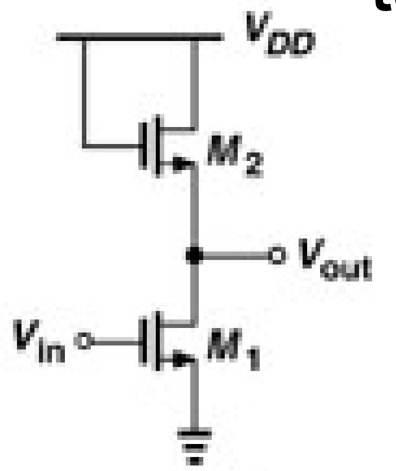
- Assume for instance V_{DD}=3V
- Let's assume that V_{GS1}-V_{TH1}=200mV (arbitrary selection, consistent with current selection)
- Assume also that $|V_{TH2}|$=0.7V (for PMOS load V_{TH2}=-0.7V)
- For a gain of 10, we now need $|V_{GS2}|$=2.7V (for PMOS load V_{GS2}<-2.7V)
- Therefore because V_{GD2}=0: V_{DS2}=V_{GS2}=-2.7V).
- Now V_{DS1}=V_{DD}-V_{SD2}<3-2.7=0.3V, and recall that V_{DS1}>V_{GS1}-V_{TH1}=0.2V. Not much room left for the amplified signal v_{ds1}.

DC Q-Point of the Amplifier

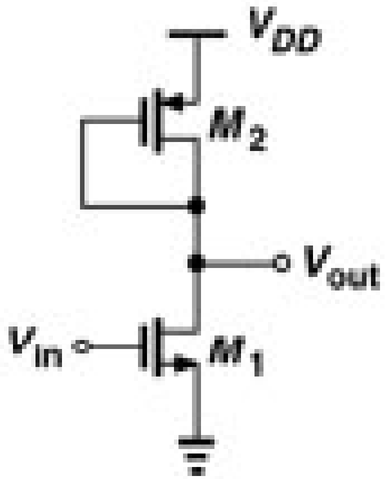


- V_{G1} determines the current and the voltage V_{GS2}
- If we neglect the effect of the transistors' λ, the error in predicting the Q-point solution may be large!

CS with Diode-Connected Load –How do we take into account λ?

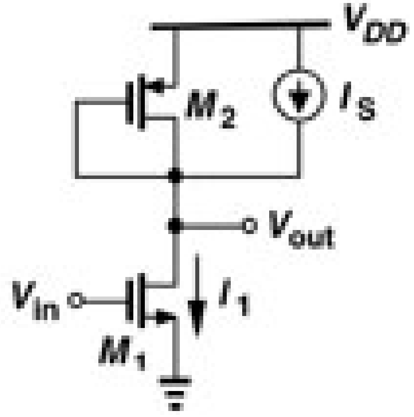


$$A_v = -g_{m1}\left(\frac{1}{g_{m2} + g_{mb2}} \parallel r_{o1} \parallel r_{o2}\right)$$



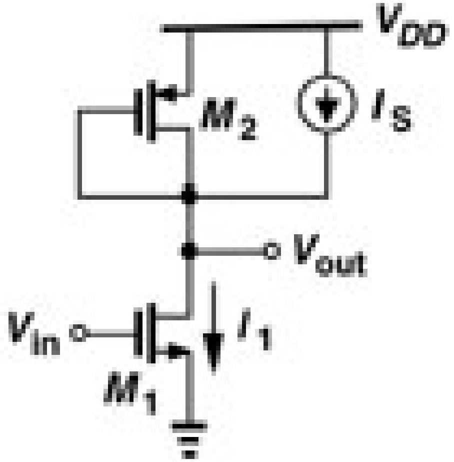
$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} \parallel r_{o1} \parallel r_{o2}\right)$$

Example as Introduction to Current Source Load



- M_1 is biased to be in Saturation and have a current of I_1.
- A current source of I_S=0.75I_1 is hooked up in parallel to the load – does this addition ease up the amplifier's swing problems?

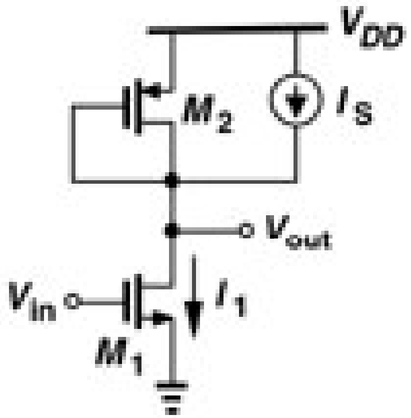
Example as Introduction to Current Source Load



- Now $I_{D2}=I_1/4$. Therefore (from the ratio of the two transconductances with different currents):

$$A_v \approx -\sqrt{\frac{4\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

Example: Swing Issues



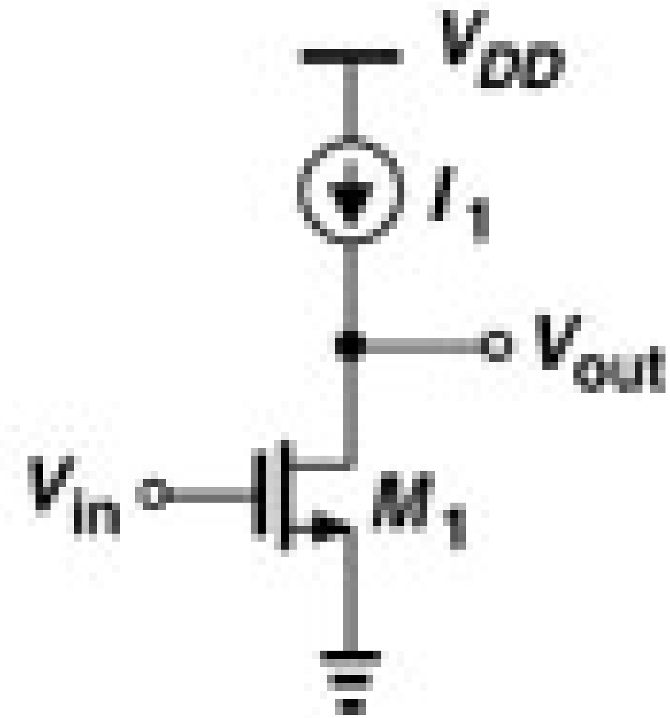
$$I_{D1} = 4I_{D2}, \quad \therefore$$

$$\mu_n\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 \approx 4\mu_p\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2$$

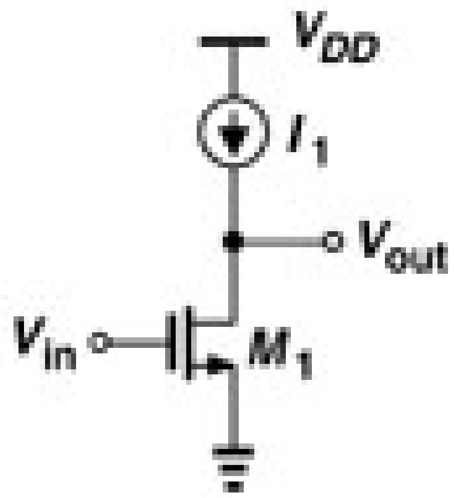
$$\frac{A_v}{4} \approx \frac{|V_{GS2} - V_{TH2}|}{(V_{GS1} - V_{TH1})}$$

It sure helps in terms of swing.

CS Amplifier with Current-Source Load-L7



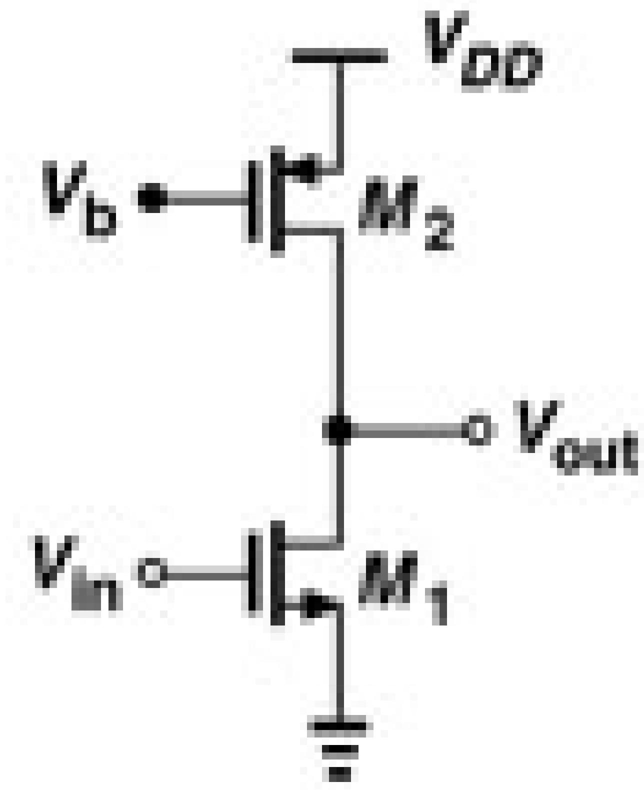
How can V_{in} change the current of M_1 if I_1 is constant?



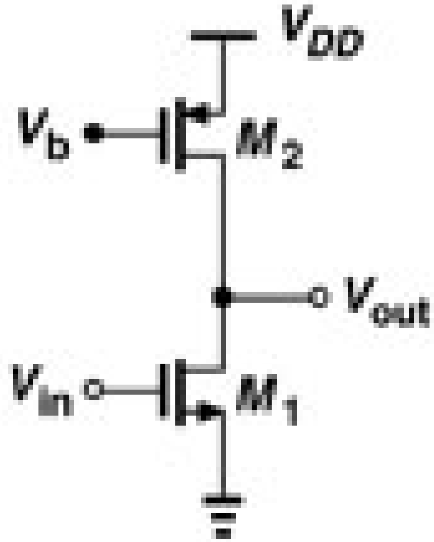
$$I_{D1} = 0.5\mu_n C_{OX}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 (1 + \lambda V_{out}) = I_1$$

- As V_{in} increases, V_{out} must decrease

Simple Implementation: Current Source obtained from M_2 in Saturation

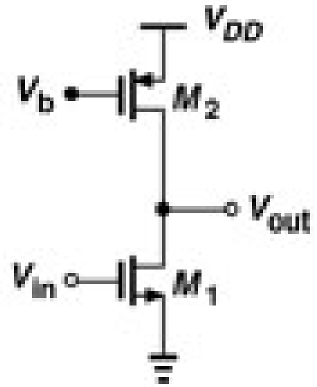


CS with Current Source Load



$$A_v = -g_m(r_{o1} \| r_{o2})$$

DC Conditions

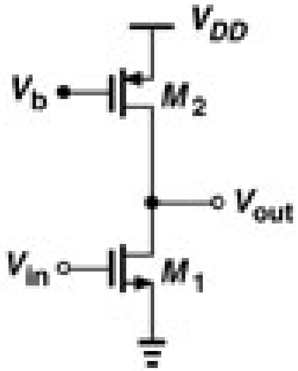


$$I_{D1} = 0.5\mu_n C_{OX}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2(1+\lambda_1 V_{out}) = I_{D2}$$

$$= 0.5\mu_p C_{OX}\left(\frac{W}{L}\right)_2 (V_b - V_{DD} - V_{TH2})^2(1+\lambda_2[V_{out} - V_{DD}])$$

- $\{(W/L)_1, V_{G1}\}$ and $\{(W/L)_2, V_b\}$ need to be more or less consistent, if we wish to avoid too much dependence on λ values.
- Need DC feedback to fix better the DC V_{out}

Swing Considerations

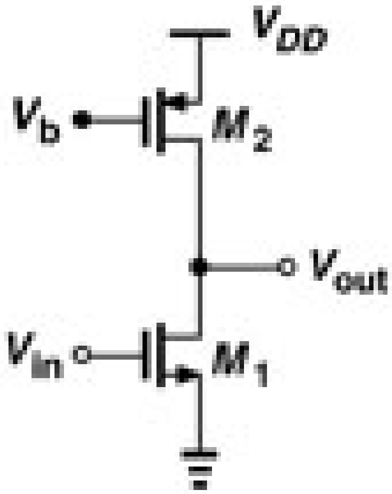


$$I_{D1} = 0.5\mu_n C_{OX}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 (1 + \lambda_1 V_{out}) = I_{D2}$$

$$= 0.5\mu_p C_{OX}\left(\frac{W}{L}\right)_2 (V_b - V_{DD} - V_{TH2})^2 (1 + \lambda_2 [V_{out} - V_{DD}])$$

- We can make $|V_{DS2}|>|V_{GS2}-V_{TH2}|$ small (say a few hundreds of mV), if we compensate by making W_2 wider.

How do we make the gain large?



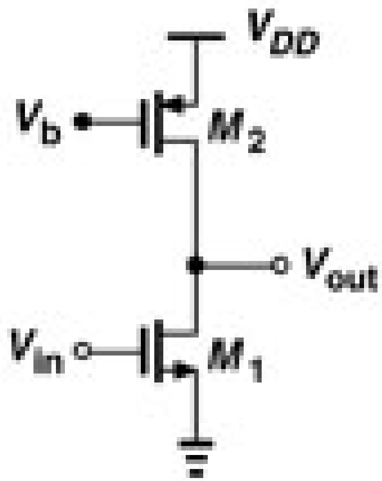
$$A_v = -g_m(r_{o1} \| r_{o2})$$

- Recall: λ is inversely proportional to the channel length L.
- To make λ values smaller (so that r_o be larger) need to increase L. In order to keep the same current, need to increase W by the same proportion as the L increase.

CS Amplifier with Current-Source Load Gains

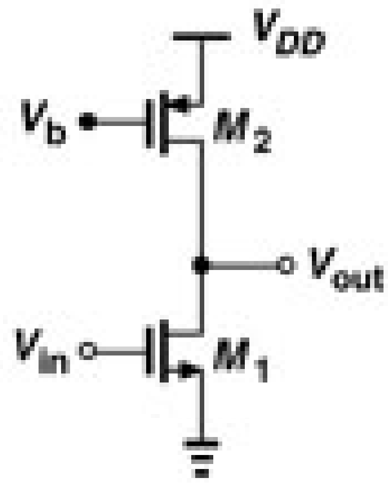
- Typical gains that such an amplifier can achieve are in the range of -10 to -100.
- To achieve similar gains with a R_D load would require much larger V_{DD} values.
- For low-gain and high-frequency applications, R_D load may be preferred because of its smaller parasitic capacitance (compared to a MOSFET load)

Numerical Example



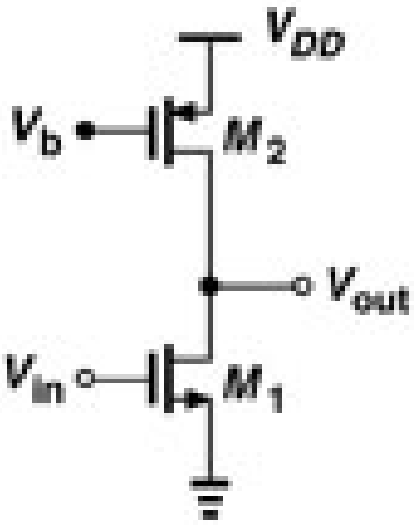
- Let W/L for both transistors be W/L = 100μm / 1.6μm
- Let $\mu_n C_{ox}$=90μA/V^2, $\mu_p C_{ox}$=30μA/V^2
- Bias current is I_D=100μA

Numerical Example (Cont'd)



- Let r_{o1}=8000L/I_D and r_{o2}=12000L/I_D where L is in µm and I_D is in mA.
- What is the gain of this stage?

Numerical Example (Cont'd)



$$g_{m1} = \sqrt{2\mu_n C_{OX}(W/L)_1 I_D} = 1.06 mA/V$$

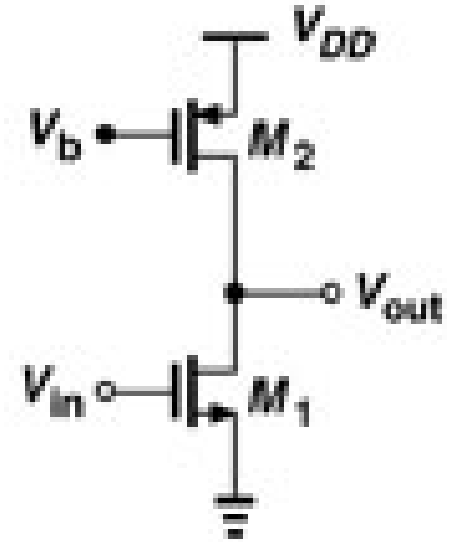
$$r_{o1} = 8000 \cdot 1.6/0.1 = 128 K\Omega$$

$$r_{o2} = 12000 \cdot 1.6/0.1 = 192 K\Omega$$

$$A_V = -g_{m1}(r_{o1} \| r_{o2}) = -81.4$$

How does L influence the gain?

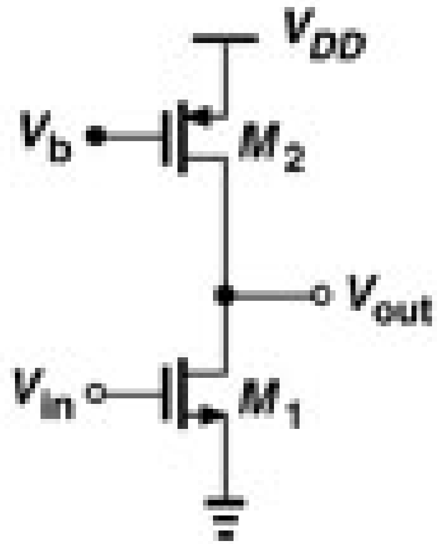
$$A_v = -g_m r_{o1} \parallel r_{o2}$$



Assuming r_{o2} large,

$$A_v \approx -g_m r_{o1} = -\sqrt{2\mu_n C_{ox} I_D \left(\frac{W}{L}\right)_1} \frac{1}{\lambda I_D}$$

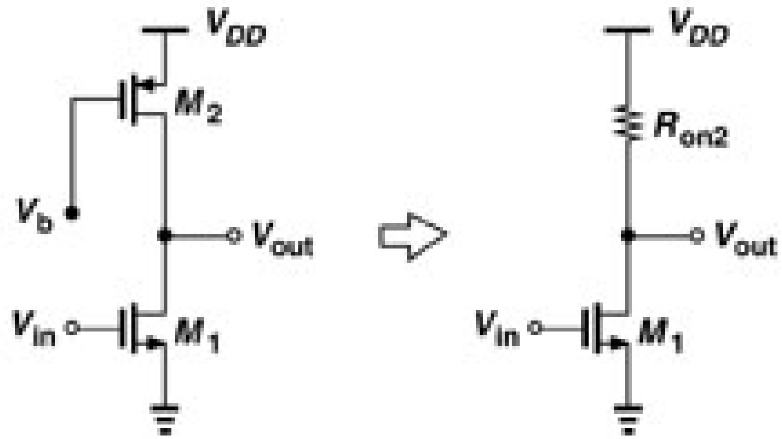
How does L influence the gain?



$$A_v \approx -g_m r_{o1} = -\sqrt{2\mu_n C_{ox} I_D \left(\frac{W}{L}\right)_1} \frac{1}{\lambda_1 I_D}$$

- As L_1 increases the gain increases, because λ_1 depends on L_1 more strongly than g_{m1} does!
- As I_D increases the gain decreases.
- Increasing L_2 while keeping W_2 constant increases r_{o2} and the gain, but $|V_{DS2}|$ necessary to keep M_2 in Saturation increases.

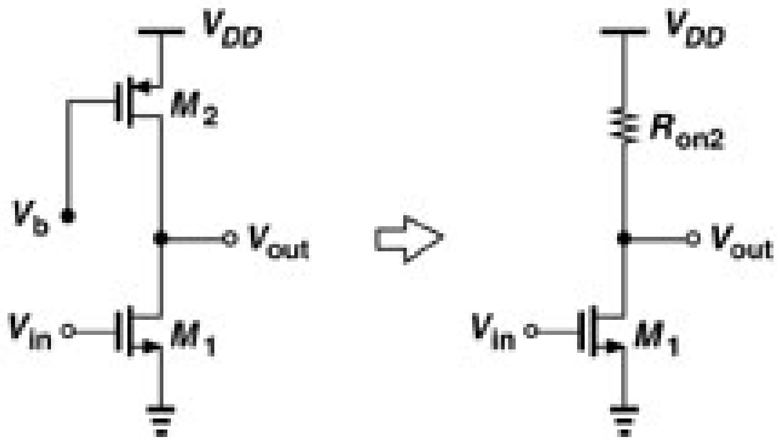
CS with Triode Region Load



$$A_v = -g_{m1} R_{ON2}$$

$$R_{ON2} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_{DD} - V_b + V_{TH2})}$$

How should V_b be chosen?



- M_2 must conduct: $V_b - V_{DD} \le V_{TH2}$, or $V_b \le V_{DD} + V_{TH2}$
- M_2 must be in Triode Mode: $V_{out} - V_{DD} \le V_b - V_{DD} - V_{TH2}$, or $V_b \ge V_{out} + V_{TH2}$
- M_2 must be "deep inside" Triode Mode: $2(V_b - V_{DD} - V_{TH2}) >> V_{out} - V_{DD}$, or: $V_b >> V_{DD}/2 + V_{TH2} + V_{out}/2$
- Also V_b and $(W/L)_2$ determine the desired value of R_{on2}

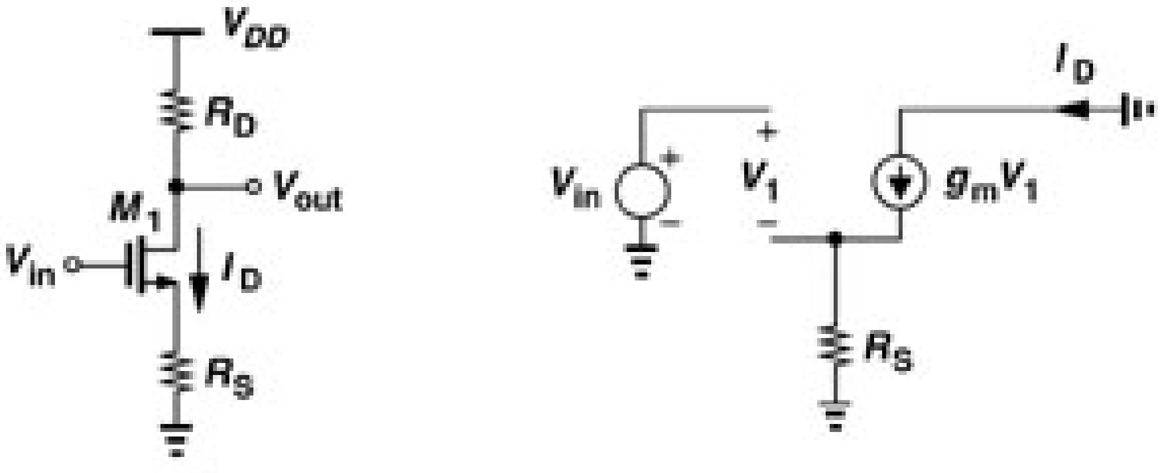
It’s not easy at all to determine (and implement) a working value for V_b

CS Amplifiers with Triode Region load is rarely used

CS Amplifier with Source Degeneration-L9

The effects of adding a resistor R_S between Source and ground.

CS Amplifier with Source Degeneration



(a) (b)

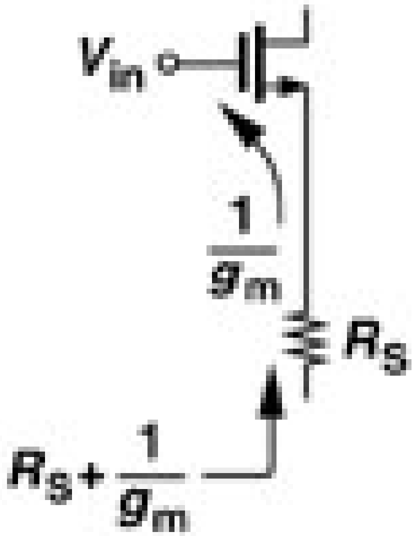
$$G_m \approx \frac{g_m}{1 + g_m R_S}$$

$$A_v = -G_m R_D$$

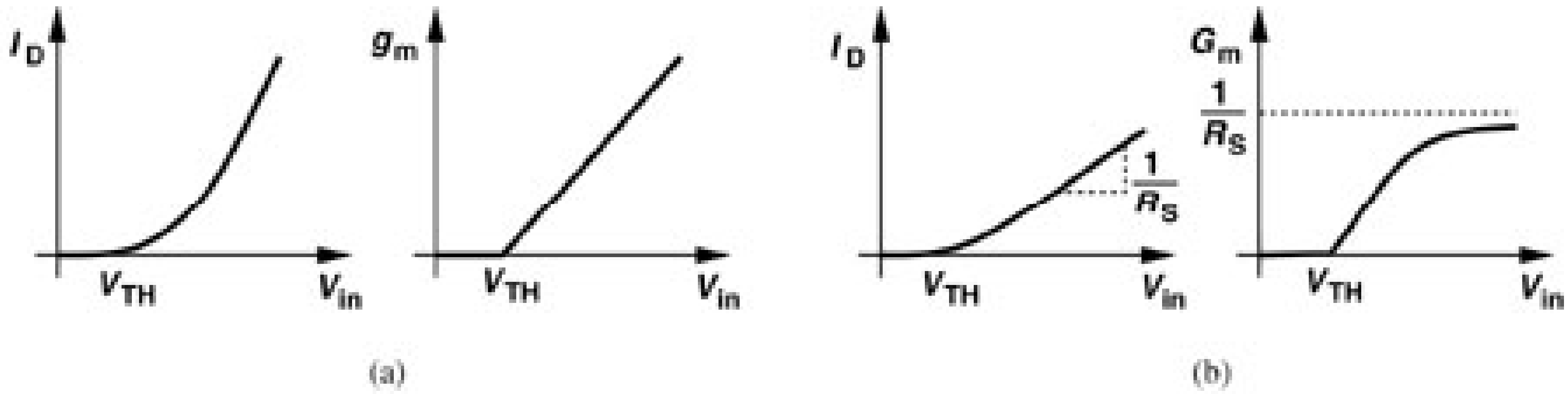
$$A_v \approx \frac{-g_m R_D}{1 + g_m R_S}$$

Summary of key formulas,
Neglecting
Channel-Length Modulation and
Body Effect

Linearizing effect of R_S:

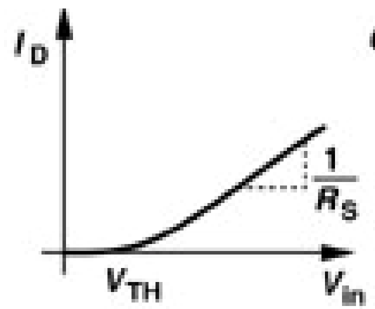


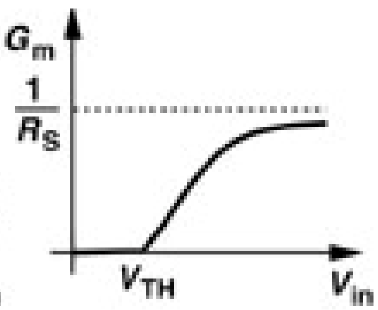
$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = -\frac{R_D}{1/g_m + R_S}$$



Linearizing effect of R_S:

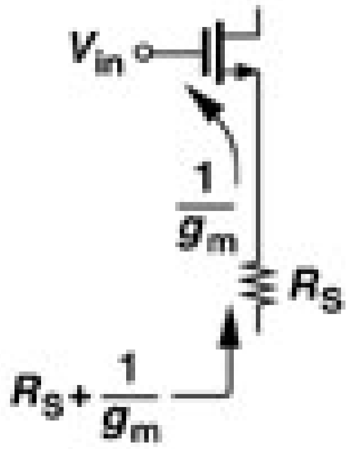
$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = -\frac{R_D}{1/g_m + R_S}$$





- For low current levels $1/g_m >> R_S$ and therefore $G_m \approx g_m$.
- For very large V_{in}, if transistor is still in Saturation, G_m approaches $1/R_S$.

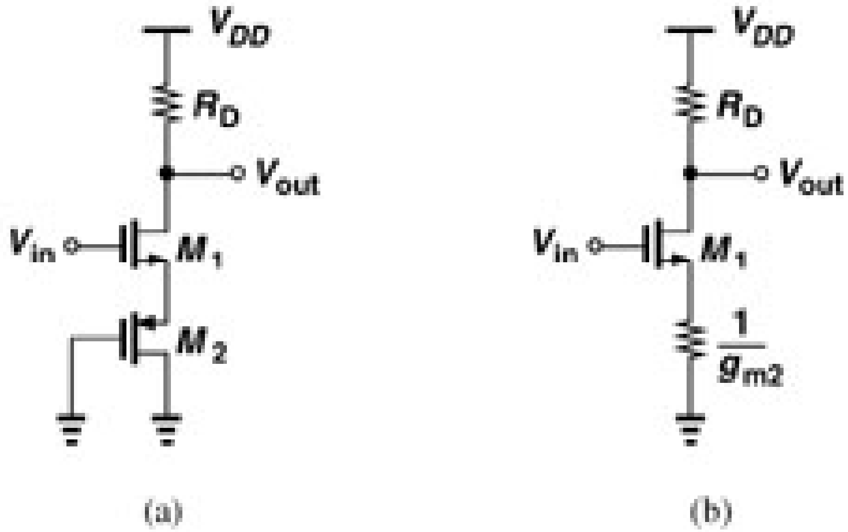
Estimating Gain by Inspection



$$A_v = \frac{-g_m R_D}{1+g_m R_S} = -\frac{R_D}{1/g_m + R_S}$$

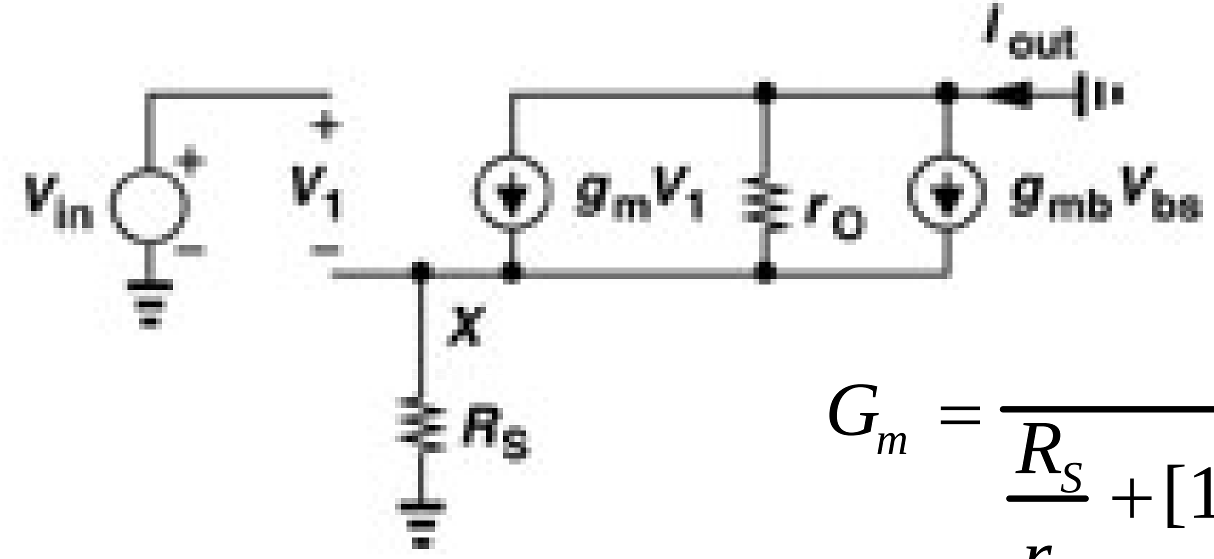
- Denominator: Resistance seen the Source path, “looking up” from ground towards Source.
- Numerator: Resistance seen at Drain.

Example to demonstrate method:



- Note that M_2 is "diode-connected", thus acting like a resistor $1/g_{m2}$
- $A_V = -R_D/(1/g_{m1}+1/g_{m2})$

CS Amplifier with Source Degeneration Key Formulas with λ and Body-Effect Included

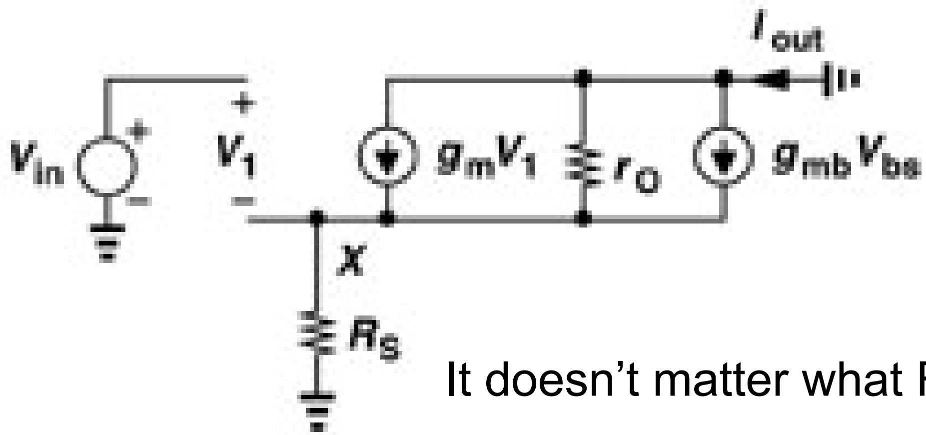


$$G_m = \frac{g_m}{\frac{R_S}{r_o} + [1 + (g_m + g_{mb})R_S]}$$

$$R_{OUT} = [1 + (g_m + g_{mb})r_o]R_S + r_o$$

$$A_v = -G_m(R_D \parallel R_{OUT})$$

Derivation is similar to that of the simplified case – generalized transconductance



It doesn't matter what R_D is because we treat I_D as "input"

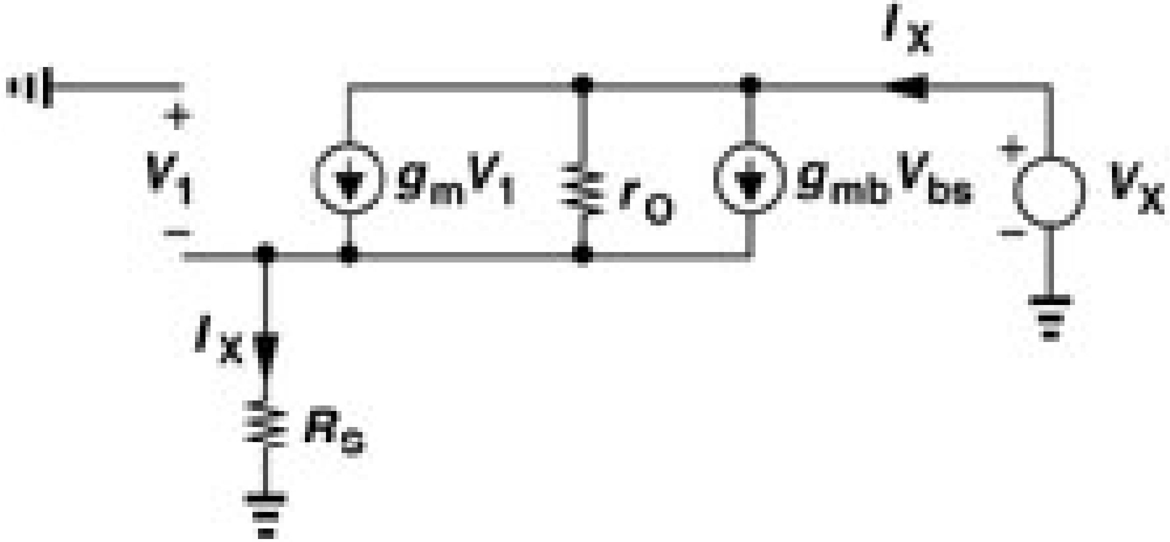
$$I_D = g_m V_1 + g_{mb} V_{bs} + I_{ro}$$

$$= g_m V_1 - g_{mb} V_X - \frac{I_D R_S}{r_o}$$

$$= g_m (V_{in} - I_D R_S) + g_{mb}(-I_D R_S) - \frac{I_D R_S}{r_o}$$

$$\Rightarrow G_m = \frac{I_D}{V_{in}} = \frac{g_m r_o}{R_S + [1 + (g_m + g_{mb}) R_S] r_o}$$

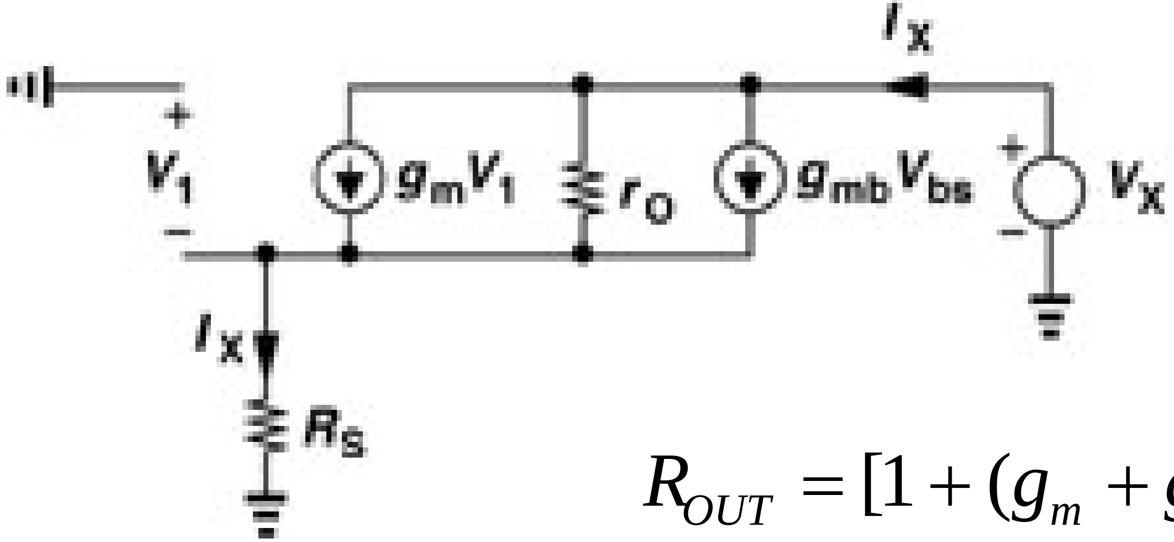
R_S effect on CS Output Resistance



$$I_X = g_m V_1 + g_{mb} V_{bs} + I_{ro}$$
$$= g_m(-I_X R_S) - g_{mb} I_X R_S + I_{ro}$$

$$V_X = r_o(I_X + (g_m + g_{mb}) R_S I_X) + I_X R_S$$

CS Output Resistance

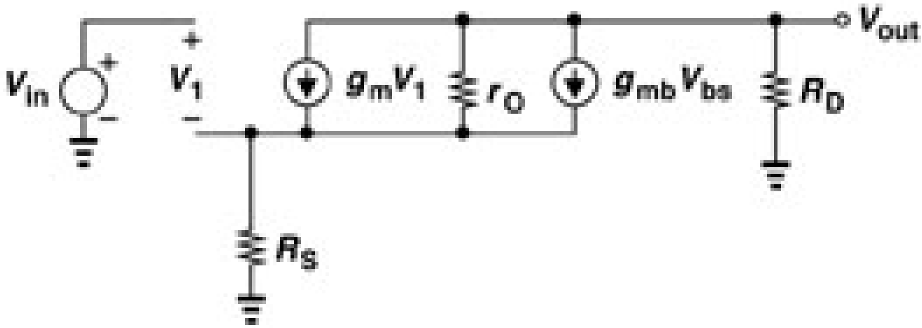


$$R_{OUT} = [1 + (g_m + g_{mb})r_o]R_S + r_o$$

$$R_{OUT} = r_o' \approx r_o[1 + (g_m + g_{mb})R_S]$$

R_S causes a significant increase in the output resistance of the amplifier

CS Amplifier with Source Degeneration Gain Formula with λ and Body-Effect Included



$$G_m = \frac{g_m}{\dfrac{R_S}{r_o} + [1 + (g_m + g_{mb})R_S]}$$

$$R_{OUT} = [1 + (g_m + g_{mb})r_o]R_S + r_o$$

$$A_v = -G_m(R_D \,||\, R_{OUT})$$

Source Follower

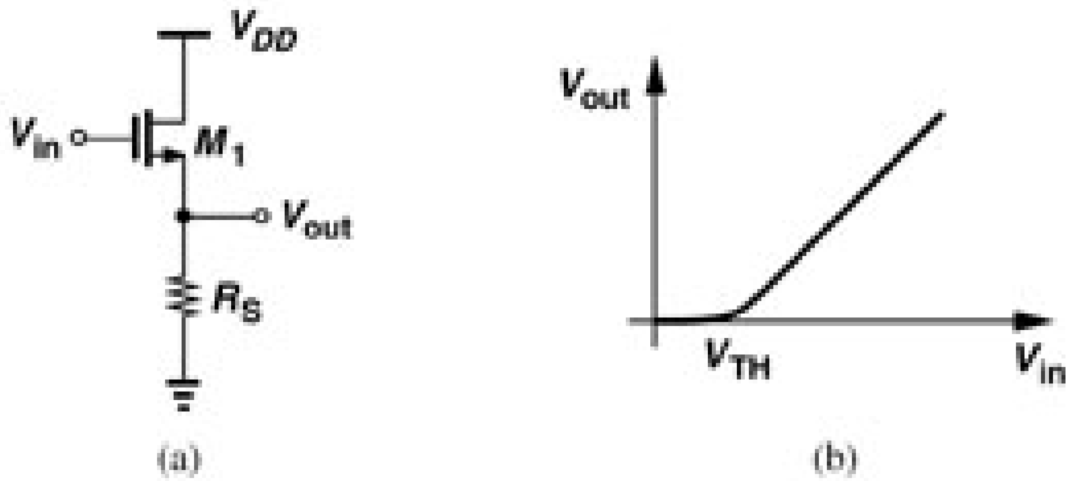
Main use: Voltage Buffer

- To achieve a high voltage gain with limited supply voltage, in a CS amplifier, the load impedance must be as large as possible.
- If such a stage is to drive a low impedance load, then a “buffer” must be placed after the amplifier so as to drive the load with negligible loss of the signal level.
- The source follower (also called the “common-drain” stage) can operate as a voltage buffer.

Buffering Action

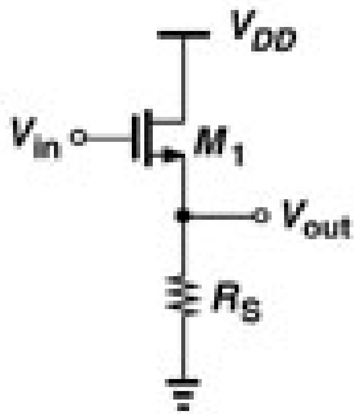
- Input resistance of source follower is large.
- CS amplifier, connected to a Source Follower, will see as a load R_{in} of the Source Follower.
- R_{in} of the Source Follower is unaffected by R_L of the Source Follower. Variations in R_L has no effect on R_{in} of the MOSFET.

Source Follower with R_S resistance

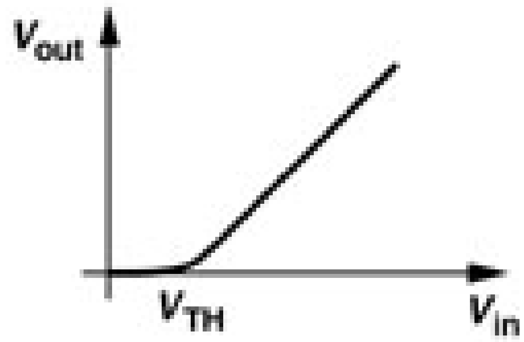


- Source Follower: Input signal comes into the Gate; Output signal comes out of the Source.
- Load connected between Source and ground.

Source Follower with R_S resistance: Large Signal Behavior



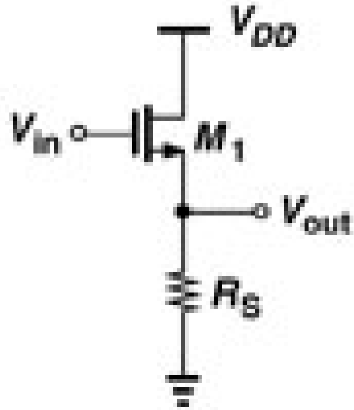
(a)



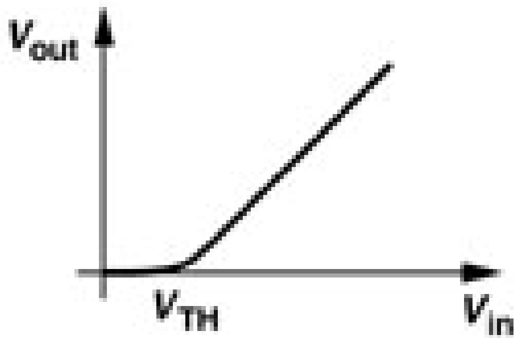
(b)

- If V_{in}<V_{TH} M_1 is off.
- As V_{in} exceed V_{TH} M_1 is in Saturation.
- M_1 goes into Triode Mode only when V_{in} exceeds V_{DD}.

Why V_{out} follows V_{in}?



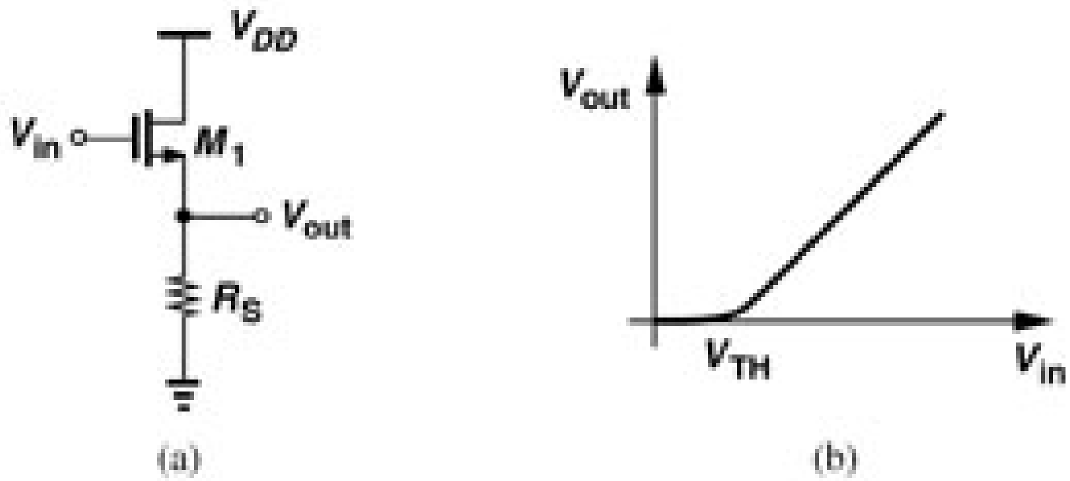
(a)



(b)

- Source followers exhibit a Body Effect: As I_D increases, $V_S=I_DR_S$ increases. As V_{SB} increases, V_{TH} increases.

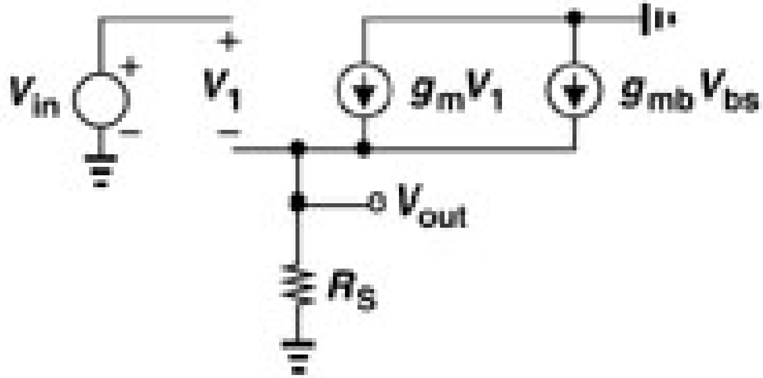
Why V_{out} follows V_{in}? (Cont'd)



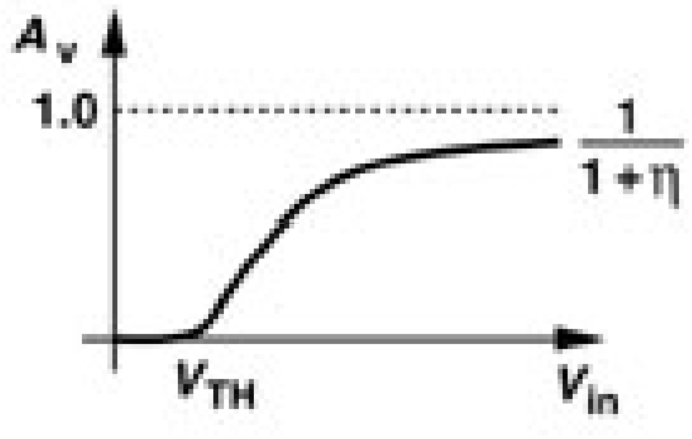
- If V_{in} slightly increases, I_D slightly increases and therefore V_{out} slightly increases.
- As I_D increases V_{TH} increases due to Body Effect.
- FACT: V_{GS} increases but not at the same rate that V_{in} increases.

Source Follower Gain

Source Follower Gain

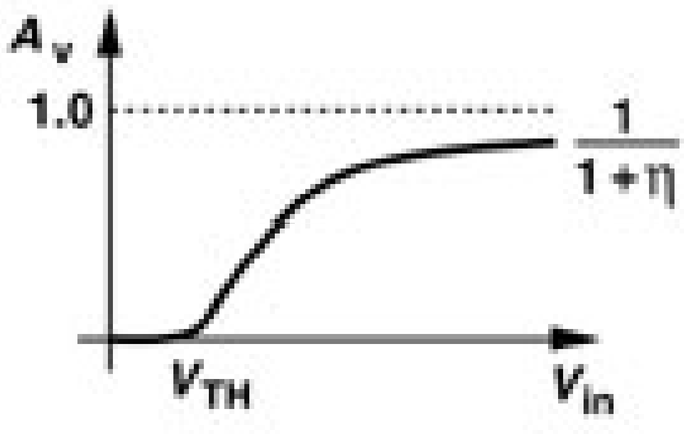


Gain Dependence on V_G



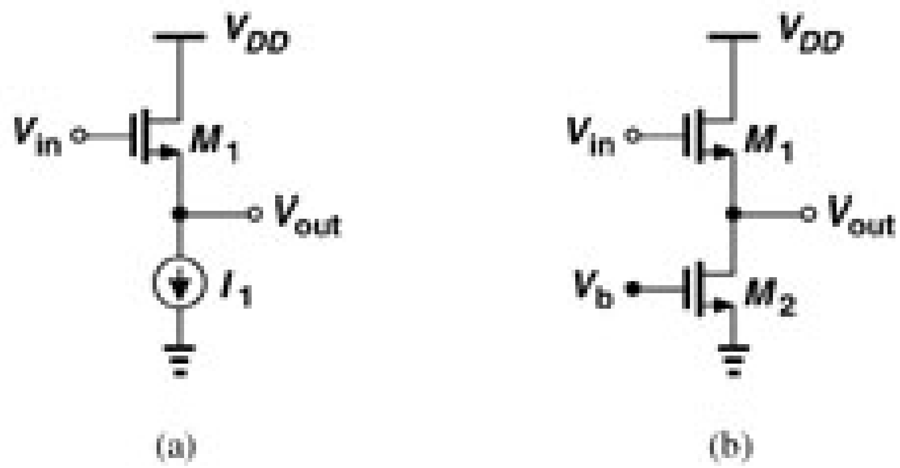
- When V_G is slightly above V_{TH}, g_m is very small, and therefore A_V is small.
- When g_m becomes large enough (i.e. $g_m R_S >> 1$), then A_V approaches $1/(1+\eta)$.

Gain Dependence on V_G (cont'd)



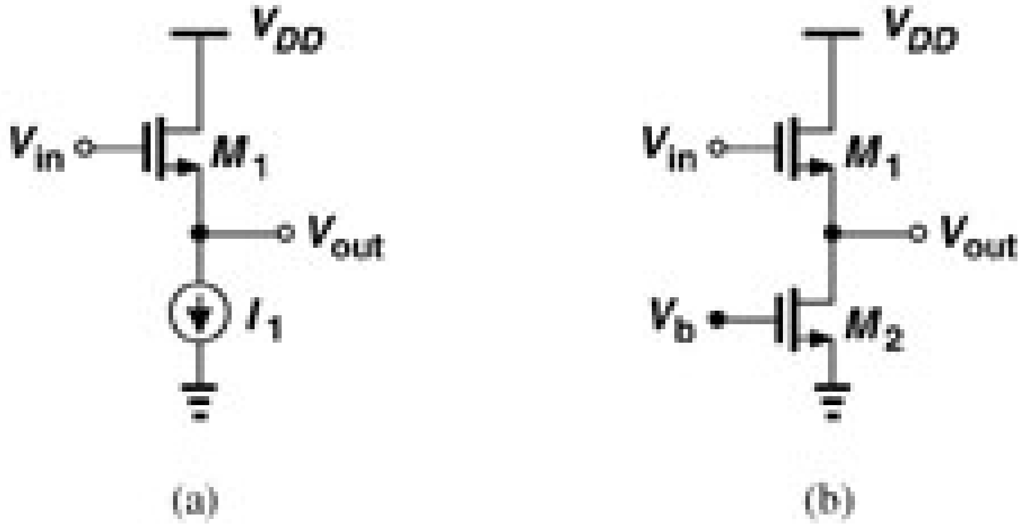
- Recall $\eta = \gamma/(2(2\Phi_F + V_{SB})^{1/2}) = \gamma/(2(2\Phi_F + V_{out})^{1/2})$
- As V_G increases, and V_{out} increases, η decreases, and the gain may approach 1.
- In most practical circuits η remains >0.2.

Source Follower with Current Source Load



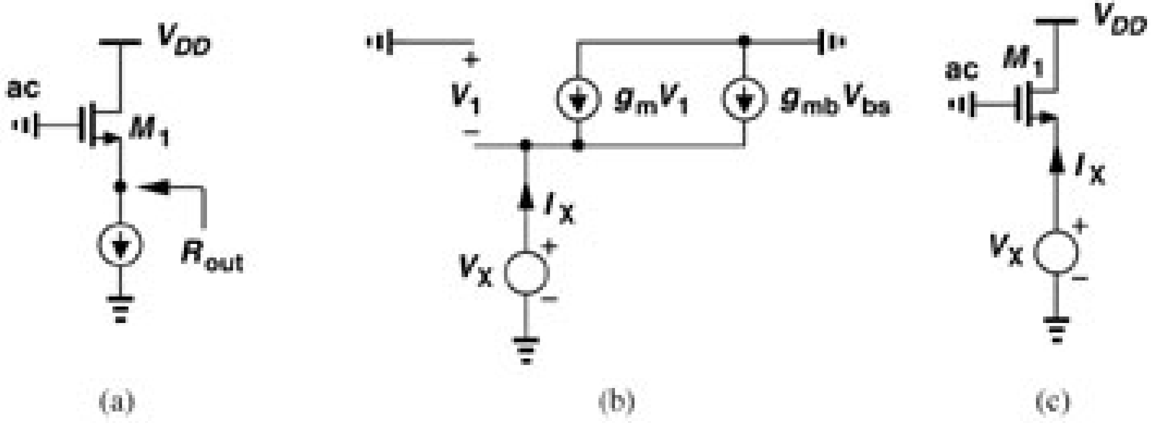
- Left: Conceptual diagram
- Right: Actual implementation, using a NMOS operating in Saturation Mode.

Example



- Let $(W/L)_1=20/0.5$, $I_1=200\mu A$, $V_{THO}=0.6V$, $2\Phi_F=0.7V$, $\mu_n C_{OX}=50\mu A/V^2$, $\gamma=0.4V^{1/2}$
- Let $V_{in}=1.2V$, what is V_{out}?

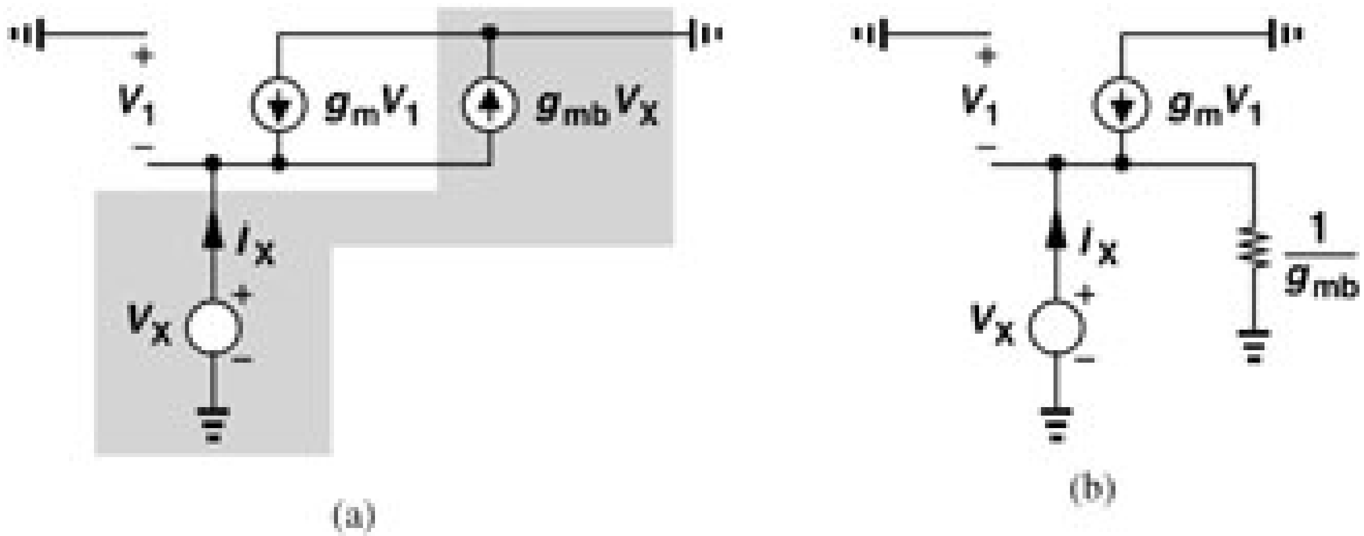
Output Resistance of the Ideal Source Follower with Current Source Load



$$V_1 = -V_X \Rightarrow I_X - g_m V_X - g_{mb} V_X = 0$$

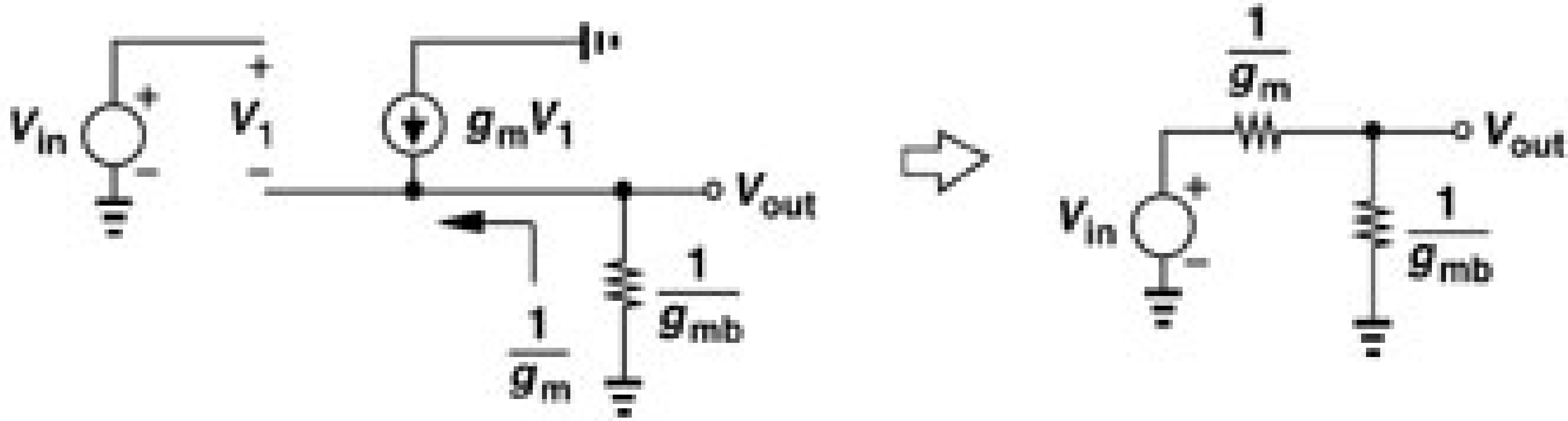
$$\boxed{R_{out} = \frac{1}{g_m + g_{mb}}}$$

Output Resistance of the Ideal Source Follower with Current Source Load becomes smaller with the help of the Body Effect!



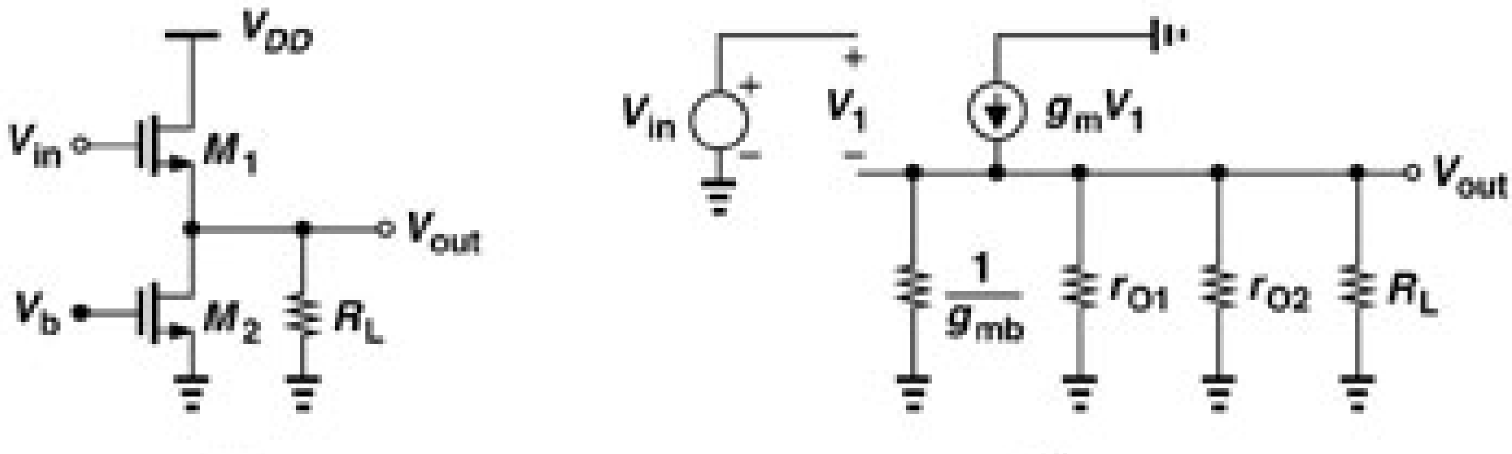
- Only in a Source Follower the current source $g_{mb}V_{bs}$ is equivalent to a resistor $1/g_{mb}$ in parallel to the output.

Gain of Source Follower with Ideal Current Source Load



$$A_V = \frac{g_m}{g_m + g_{mb}}$$

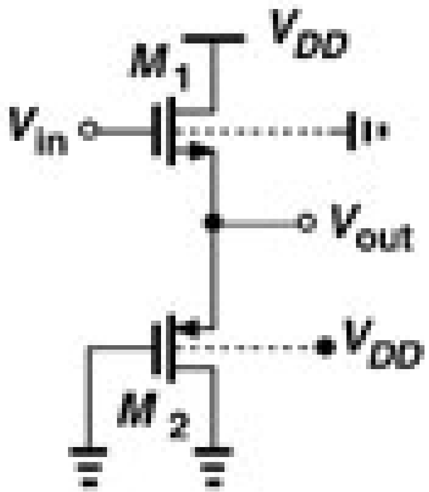
Gain Formula: NMOS Source Follower with NMOS Current Source and R_L Loads



(a) (b)

$$A_v = \frac{\frac{1}{g_{mb1}} \| r_{o1} \| r_{o2} \| R_L}{(\frac{1}{g_{mb1}} \| r_{o1} \| r_{o2} \| R_L) + \frac{1}{g_{m1}}}$$

Gain Formula: NMOS Source Follower with PMOS Current Source Load

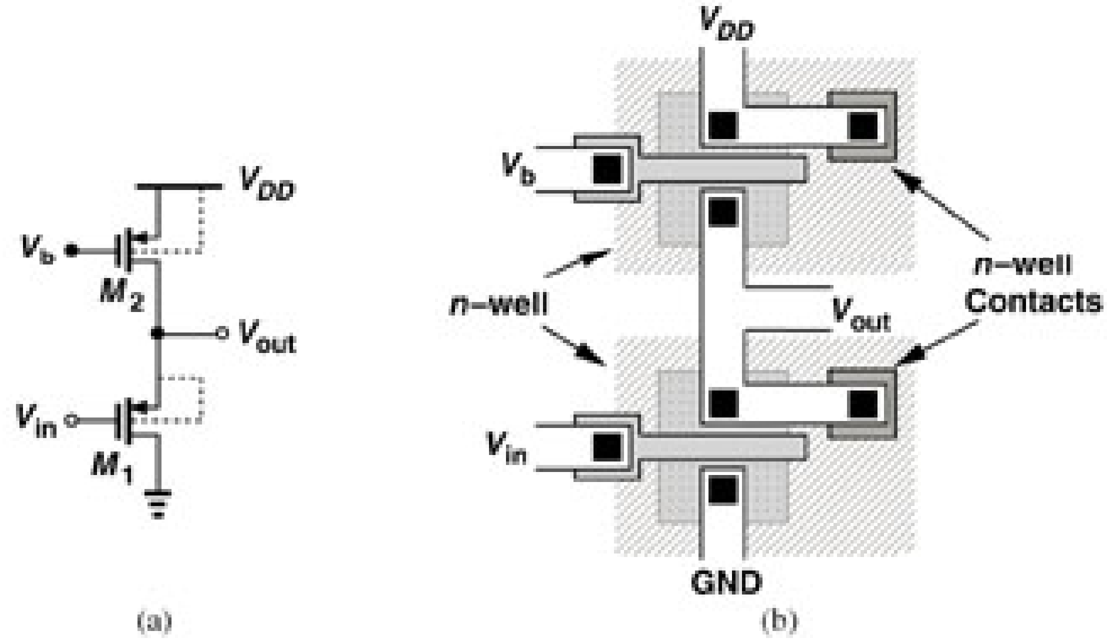


$$A_v = \frac{\frac{1}{g_{mb1}} \| r_{o1} \| r_{o2} \| \frac{1}{g_{m2} + g_{mb2}}}{\left(\frac{1}{g_{mb1}} \| r_{o1} \| r_{o2} \| \frac{1}{g_{m2} + g_{mb2}}\right) + \frac{1}{g_{m1}}}$$

Sources of Nonlinearities in NMOS Source Followers

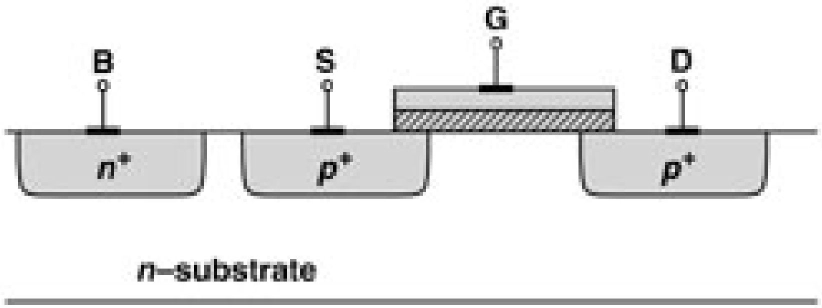
- Body Effect in the driving NMOS transistor causes V_{TH} to vary with V_{in}
- Are we allowed to connect substrate to source in the driving NMOS? (to eliminate the body effect). Answer: No! All NMOS transistors in the entire circuit share the same substrate, so it has to be grounded!
- r_o resistors vary with V_{DS}. Problem becomes more and more aggravated as L becomes smaller and smaller

PMOS Source Follower

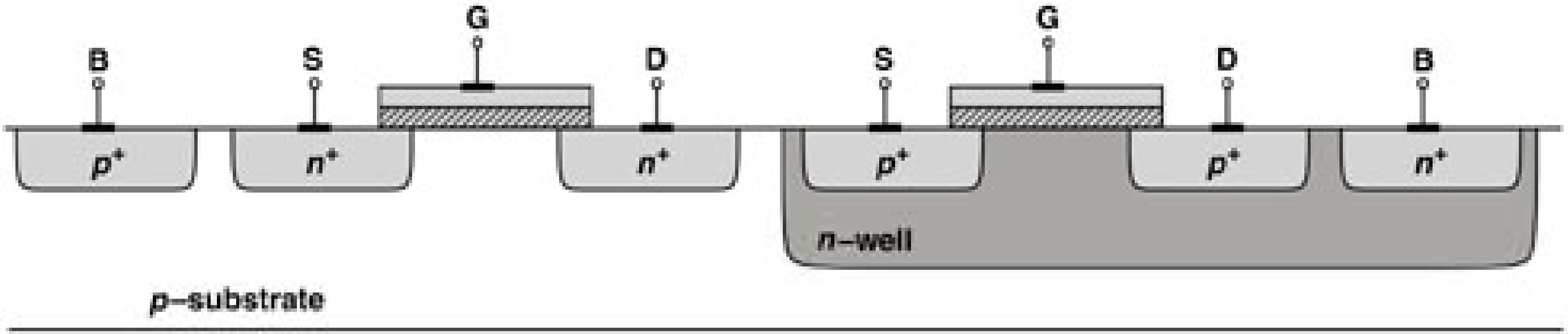


- Key idea: PMOS transistors have each a separate substrate. Each can be powered differently

CMOS fabrication process: All NMOS share the same substrate, each PMOS has a separate substrate

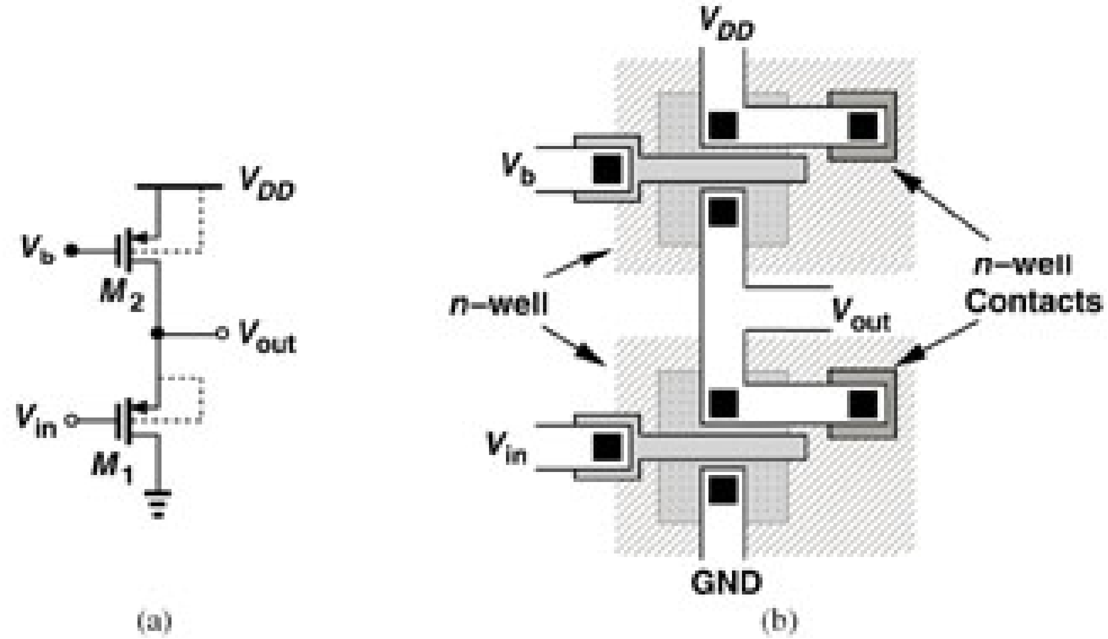


(a)



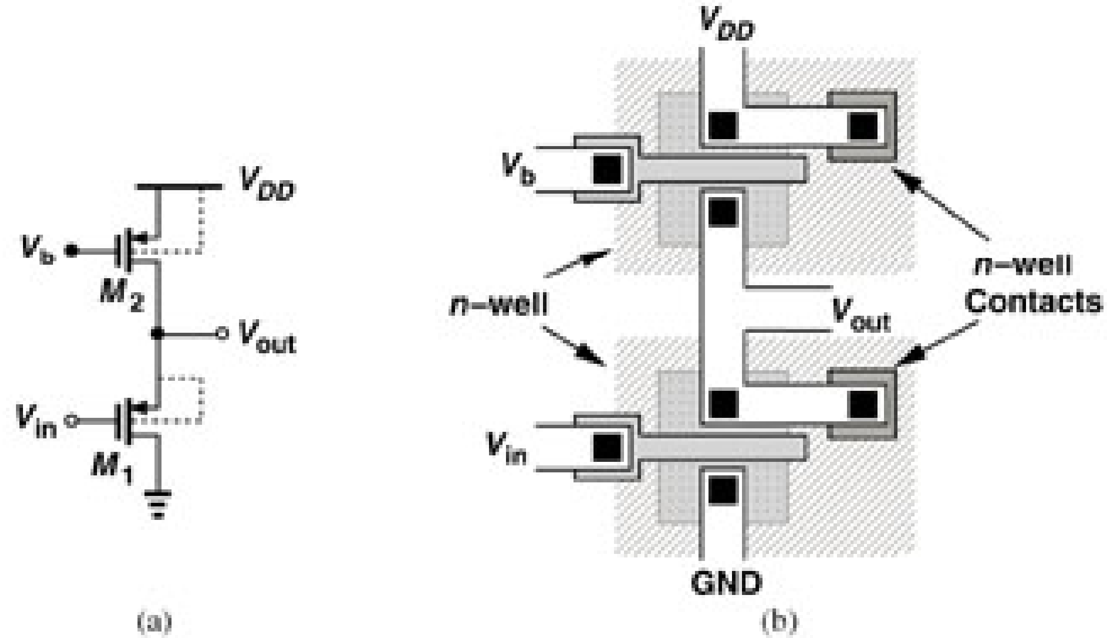
(b)

PMOS Source Follower Advantage



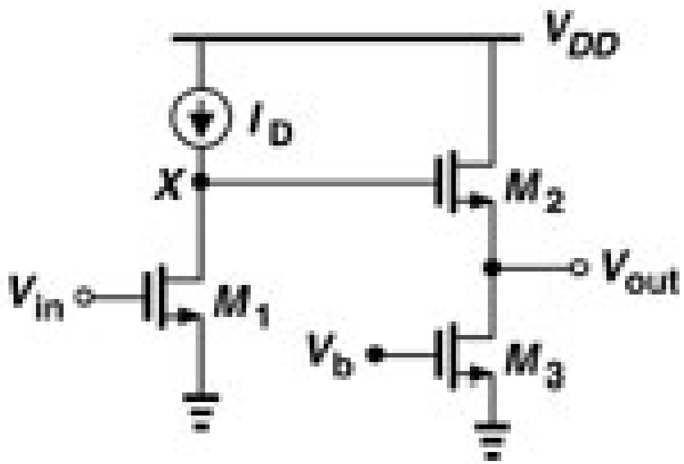
- Body Effects eliminated – device is more linear than NMOS Source Follower

PMOS Source Follower Drawbacks



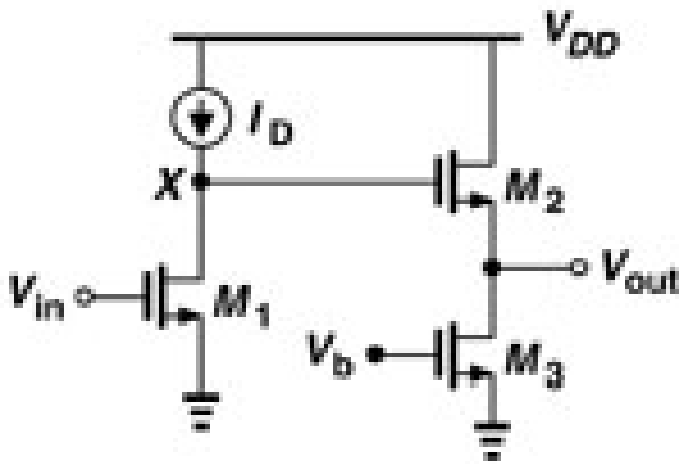
- PMOS carriers mobility is smaller than that of NMOS.
- As a result of mobility differences: PMOS source followers have larger output resistance, than NMOS followers.

CS Amplifier directly driving a Source Follower: DC levels considerations



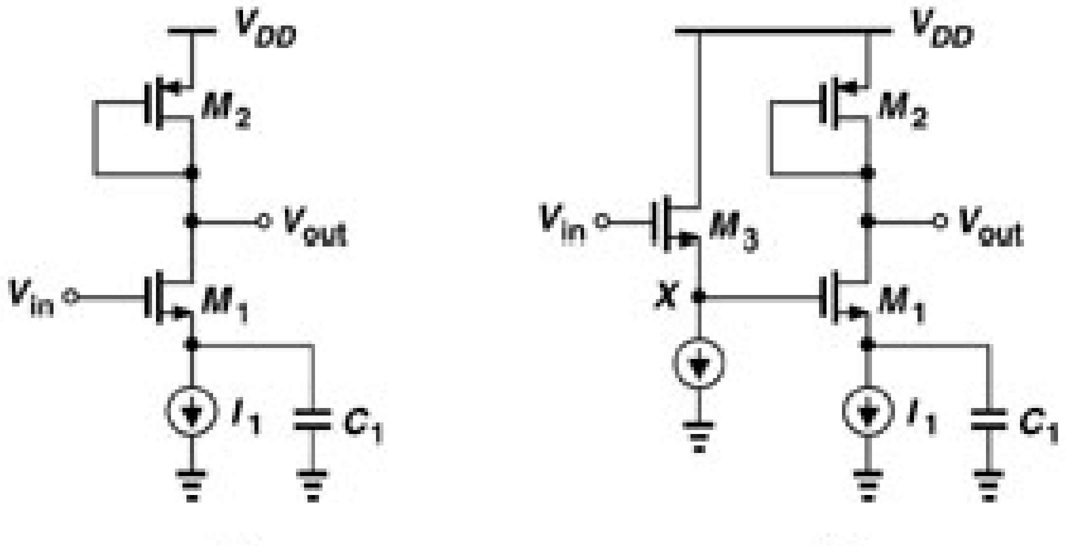
- CS Amplifier alone: $V_X \geq V_{GS1} - V_{TH1}$ to assure that M_1 is in Saturation.
- With Source Follower: $V_X \geq V_{GS2} + (V_{GS3} - V_{TH3})$ to assure that M_3 is in Saturation.

CS Amplifier directly driving a Source Follower: DC levels considerations



- If V_{GS1}-V_{TH1} ≈ V_{GS3}-V_{TH3} then $V_{X,\text{with Source Follower}}$ must be bigger than $V_{X,\text{ without Source Follower}}$ by about V_{GS2}.
- Swing of CS reduces by V_{GS2}.

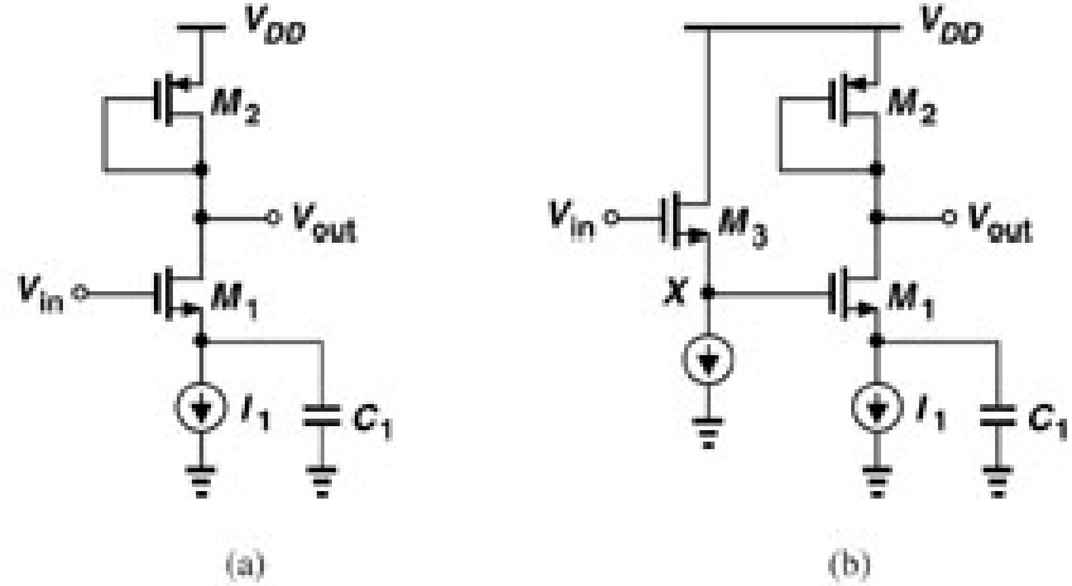
Source Followers as Level Shifters



(a) (b)

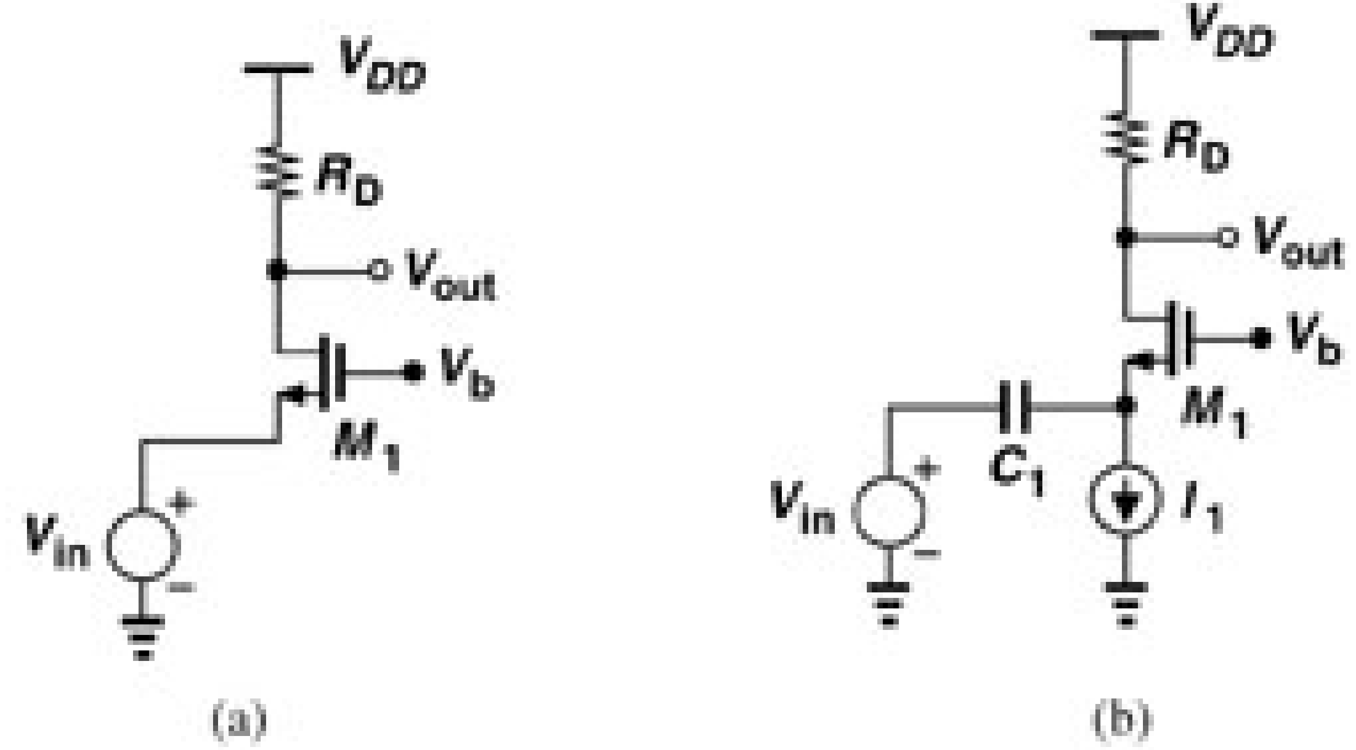
- Example (a): DC level of V_{in} cannot exceed V_{DD}-$|V_{GS2}|$+V_{TH1}
- Example (b): If V_{in} has a DC level of around V_{DD}, we put first a Source Follower.

Source Followers as Level Shifters

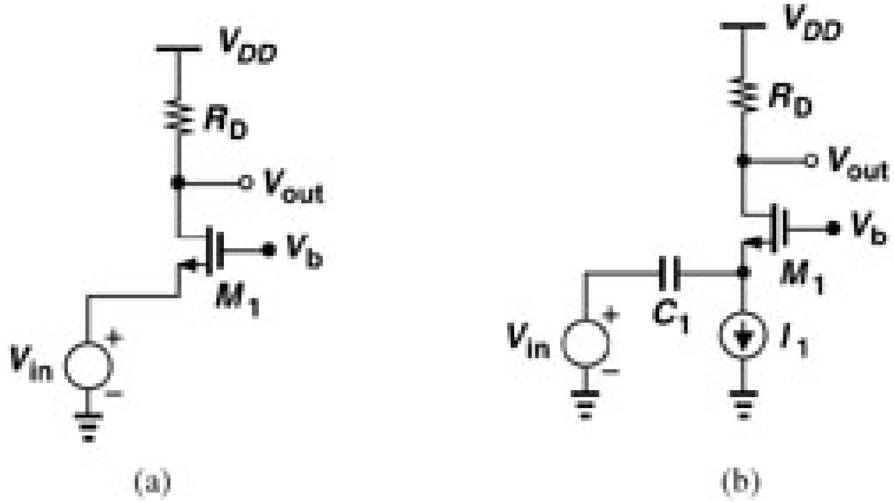


- If $V_{in} \approx V_{DD}$, then for M_1 to be in Saturation, we need: $V_{DD} - V_{GS3} - V_{TH1} \leq V_{DD} - |V_{GS2}|$

Common-Gate Amplifier-L12

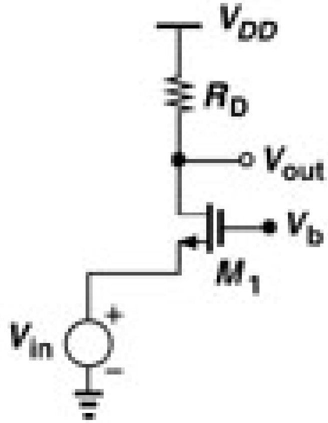


CG Amplifier: Input-Output Structure

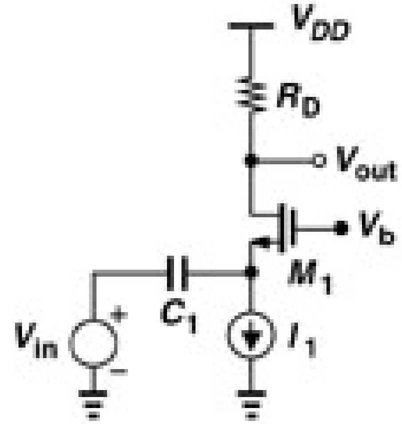


- Input signal goes into Source
- Output signal comes out of Drain.
- It is called Common-Gate because in the small signal model Gate is grounded.

CG Amplifier: Two types of input signal interface



(a)



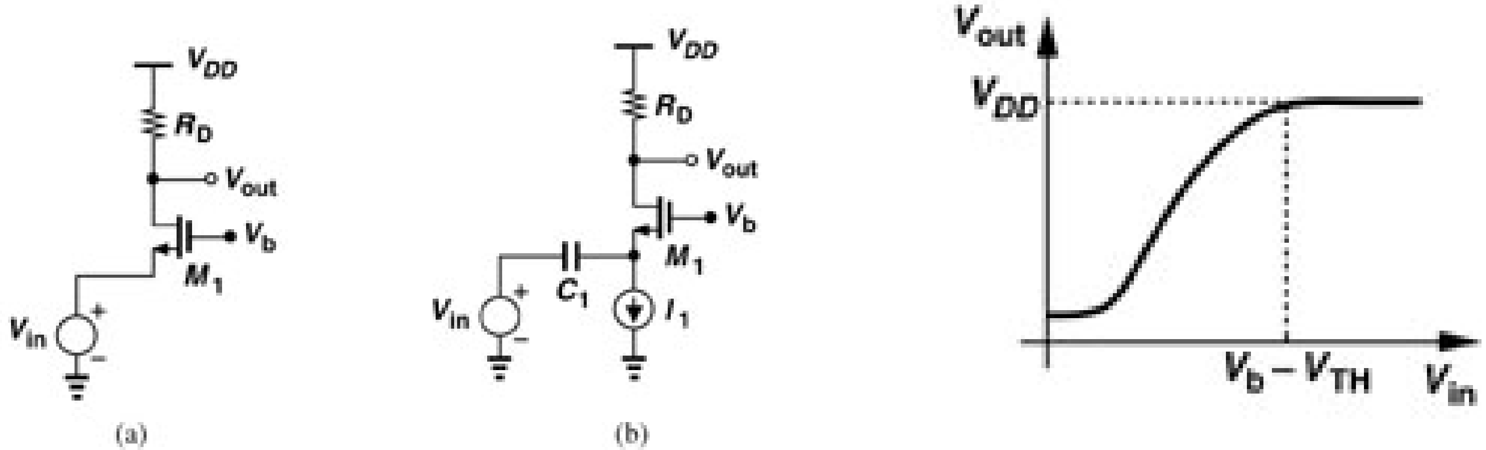
(b)

- (a): Direct coupling: DC bias current of M_1 flows through the input signal source.
- (b): Coupling (large) capacitor: Bias current is independent of the input signal source.

CG Amplifier's Properties

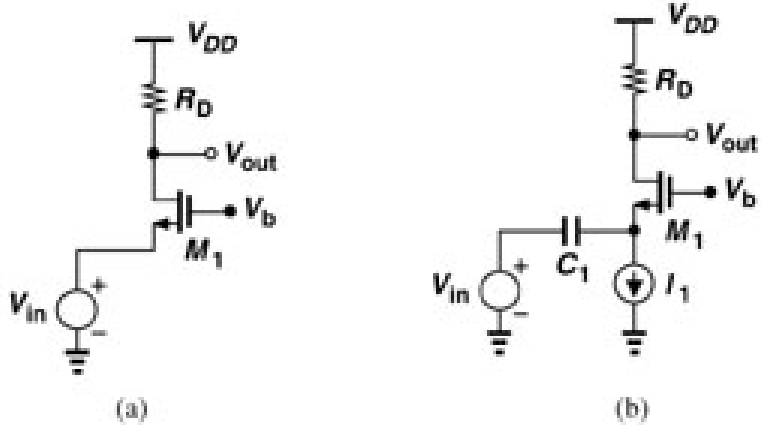
- Voltage gain comparable to that of a CS amplifier.
- Current gain of 1 – amplifier is used as current buffer.
- Small input resistance
- Large output resistance
- Bandwidth much larger than that of a CS amplifier.

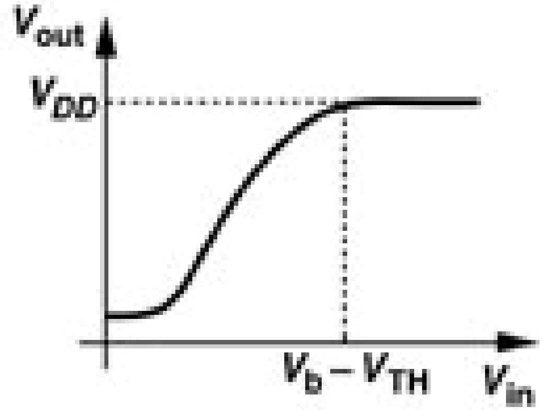
CG Amplifier with R_D load – Large Signal Analysis



- In (a), if DC part of $V_{in} \geq V_b - V_{TH}$ transistor is in Cutoff.
- If M_1 in Saturation, and V_{in} decreasing, then V_{out} decreasing too.

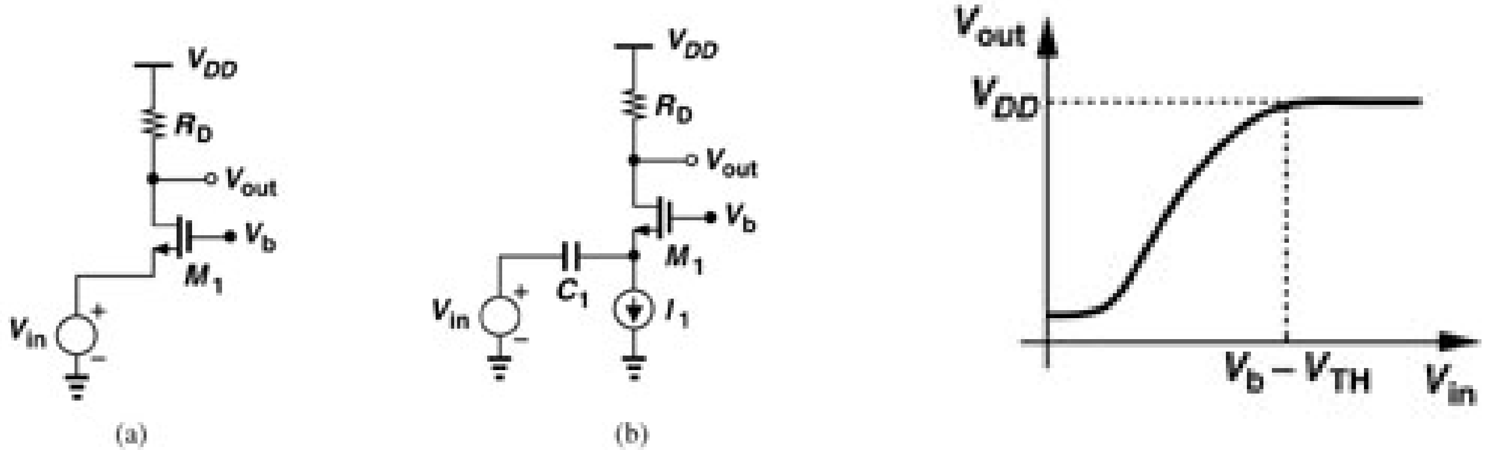
CG Amplifier with R_D load – Large Signal Analysis





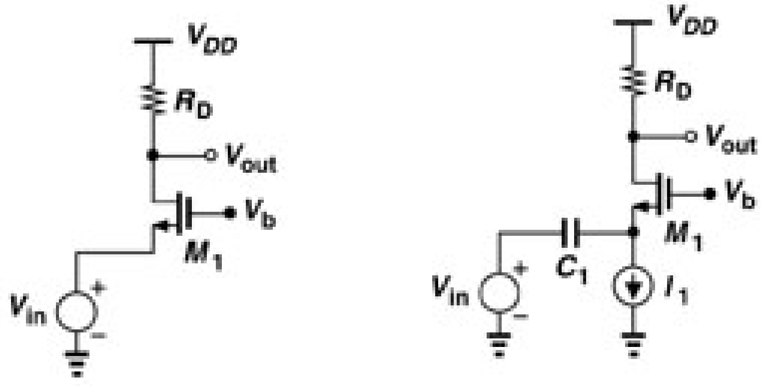
- Saturation:
- $V_{out}=V_{DD}-0.5\mu_n C_{OX}(W/L)(V_b-V_{in}-V_{TH})^2 R_D$
- Small-Signal Voltage Gain derivation:
- $dV_{out}/dV_{in}= -\mu_n C_{OX}(W/L)(V_b-V_{in}-V_{TH})(-1-dV_{TH}/dV_{in})R_D$
- Note: $dV_{TH}/dV_{in}=dV_{TH}/dV_{SB}=\eta$

CG Amplifier with R_D load – Small-Signal Voltage Gain

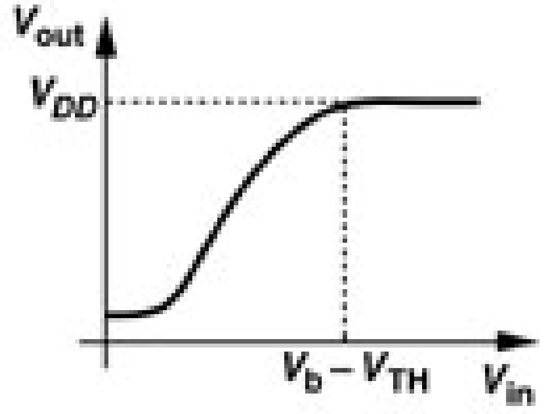


- $dV_{out}/dV_{in} = \mu_n C_{OX}(W/L)(V_b - V_{in} - V_{TH})(1+\eta)R_D$
- $A_V = dV_{out}/dV_{in} = g_m(1+\eta)R_D$
- Same order of magnitude as CS gain, however it is positive.
- Can you derive it from the small-signal model?

CG Amplifier with R_D load – Small-Signal Input Resistance

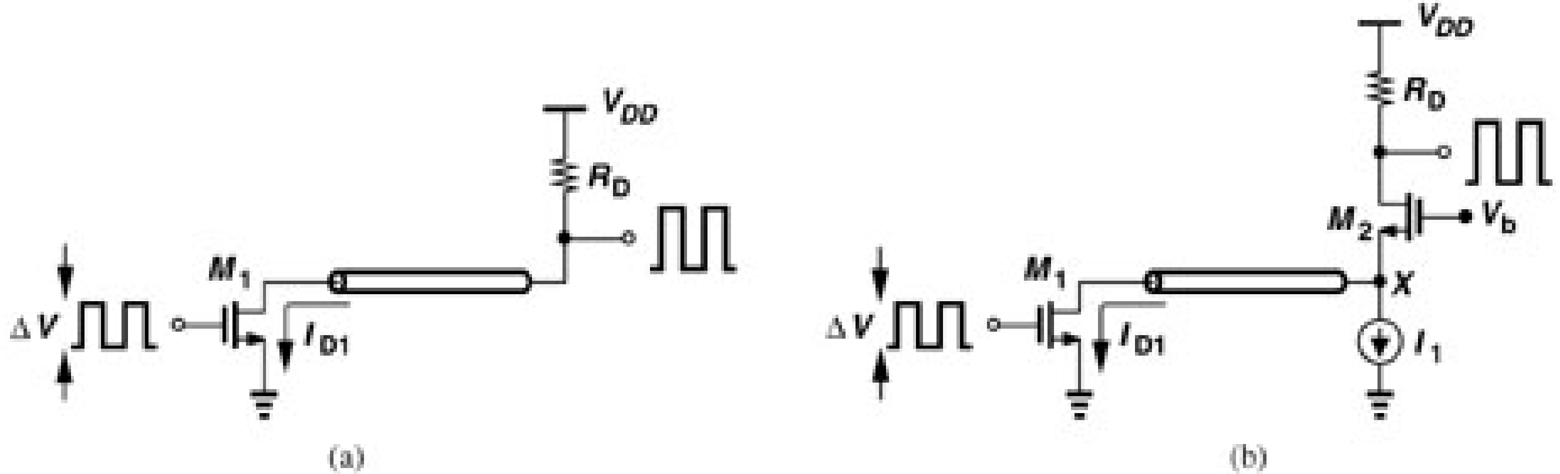


(a) (b)



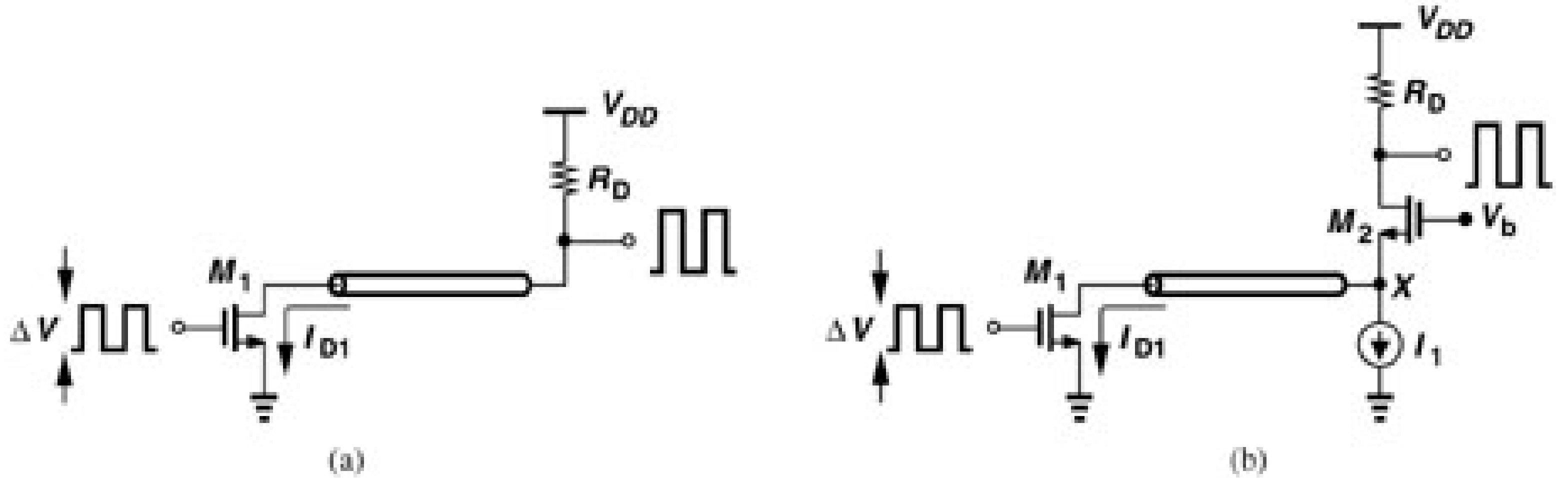
- If λ=0 then
- $R_{in}=1/(g_m+g_{mb})=1/[g_m(1+\eta)]$
- Body effect makes gain larger and R_{in} smaller – this is good! However – it adds nonlinearity.

Low R_{in} of CG Amplifiers is useful if signal comes from a transmission line



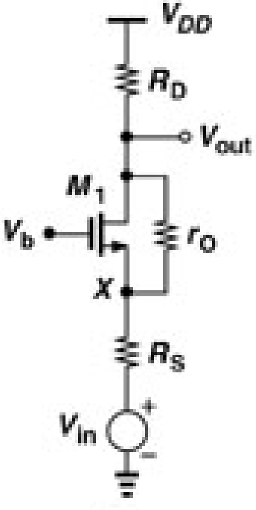
- Assume: 50Ω transmission line
- If λ=γ=0, then theoretically both circuits have the same voltage gain $A_V \approx -g_m R_D$.
- In (a): If $R_D \neq 50\Omega$ there will be reflections (see simulations)

Low R_{in} of CG Amplifiers is useful if signal comes from a transmission line

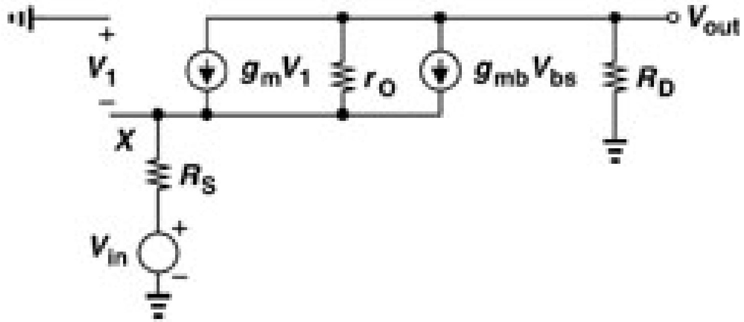


- In (b): R_{in} of M_2 is set to 50Ω to prevent reflections.
- R_D can be much larger to determine the deired gain.

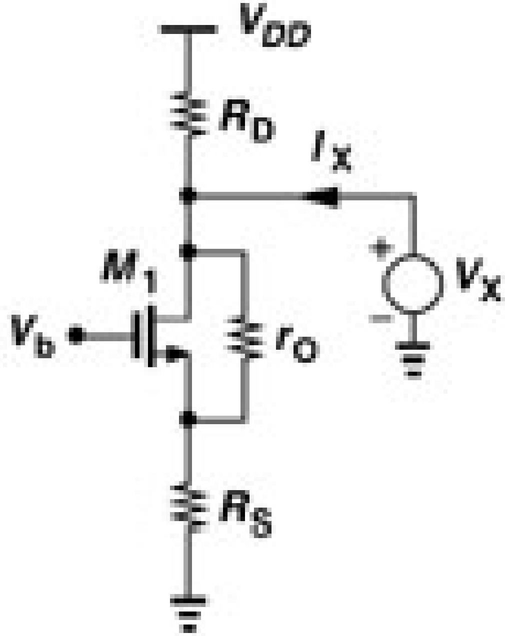
Common Gate Amplifier – Output Resistance



(a)

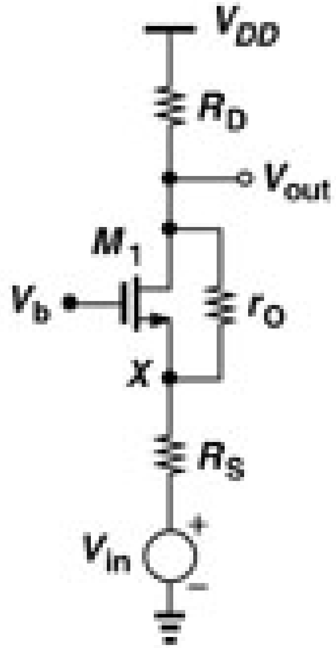


(b)

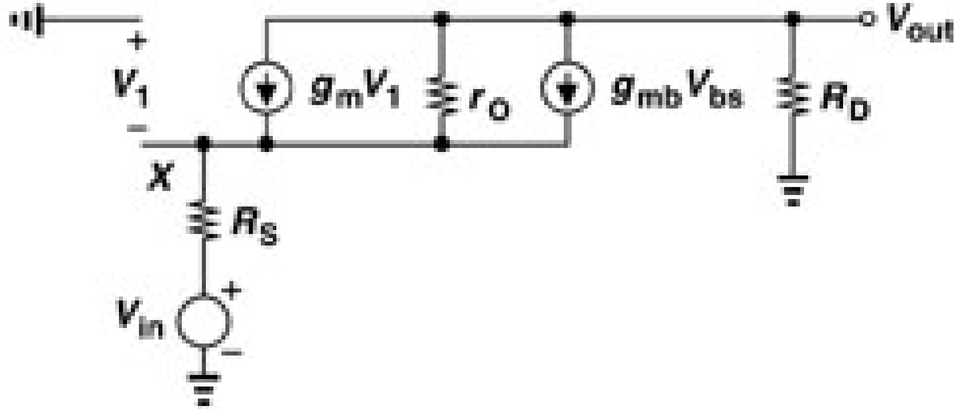


$$R_{out} = \{[1 + (g_m + g_{mb})r_o]R_S + r_o\} \parallel R_D$$

Common Gate Voltage Gain, taking into account r_o and V_{in} source resistance



(a)



(b)

$$A_v = \frac{(g_m + g_{mb})r_o + 1}{r_o + (g_m + g_{mb})r_o R_S + R_S + R_D} R_D$$

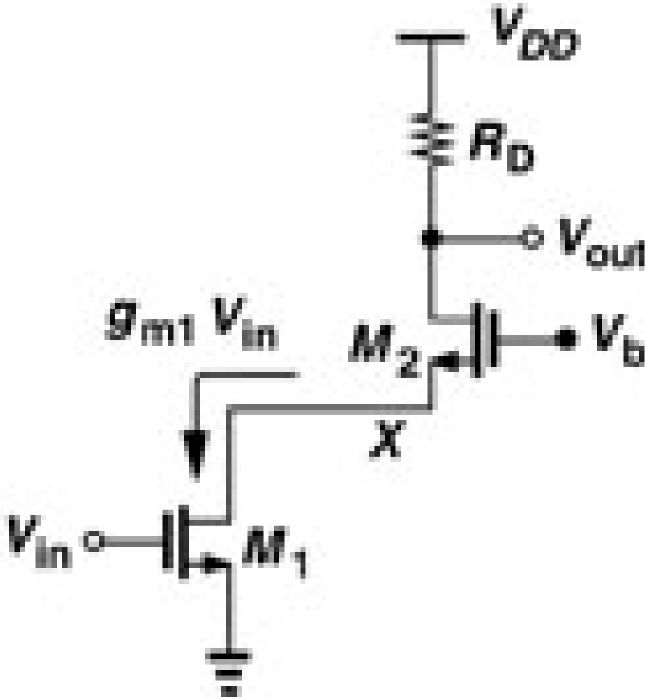
Common Gate Gain and R_{in} taking r_o into account, and assuming ideal signal source

$$A_v = \frac{(g_m + g_{mb})r_o + 1}{r_o + (g_m + g_{mb})r_o R_S + R_S + R_D} R_D$$

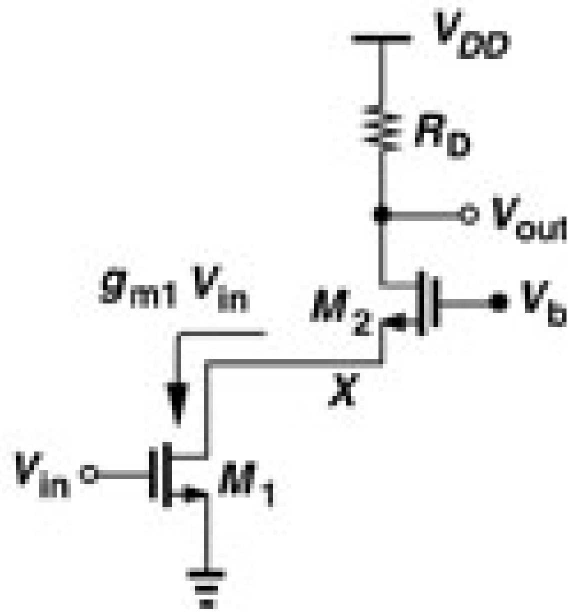
$$A_v \approx (g_m + g_{mb})(r_o \parallel R_D), \quad R_S = 0$$

$$R_{in} = r_o \parallel \frac{1}{g_m} \parallel \frac{1}{g_{mb}}$$

Cascode Amplifier-L13,L14

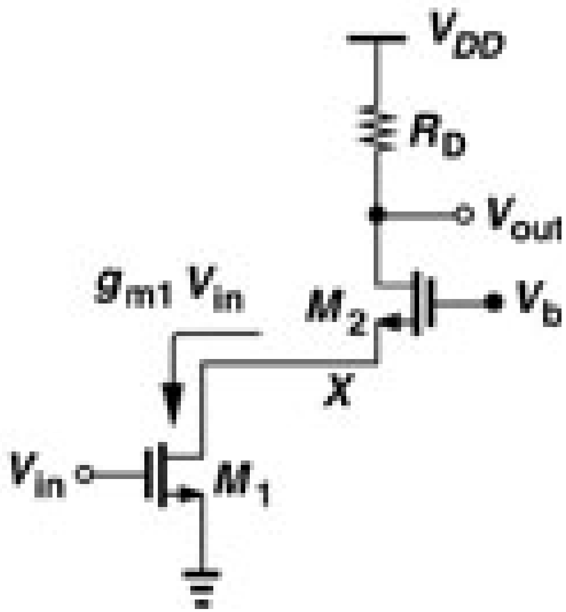


Cascode Amplifier



- M_1 generates small-signal drain current proportional to V_{in}.
- M_2 routes the current to the load R_D

Cascode Amplifier

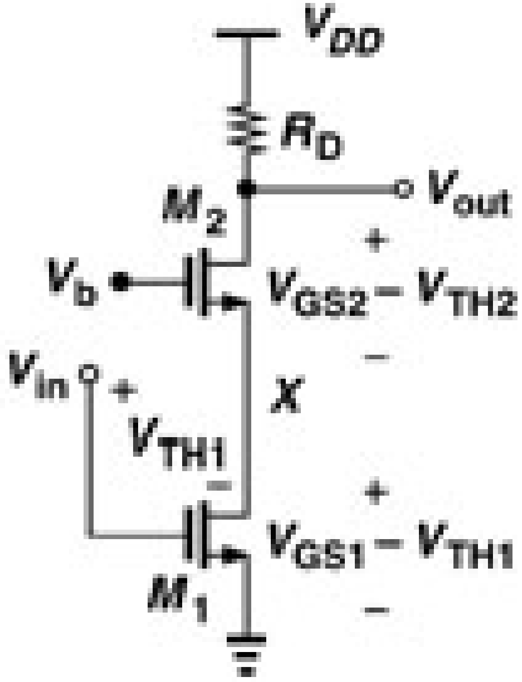


- M_1 is the input device (CS amplifier with small load resistance)
- M_2 is the Cascode device

Properties of Cascode Amplifiers

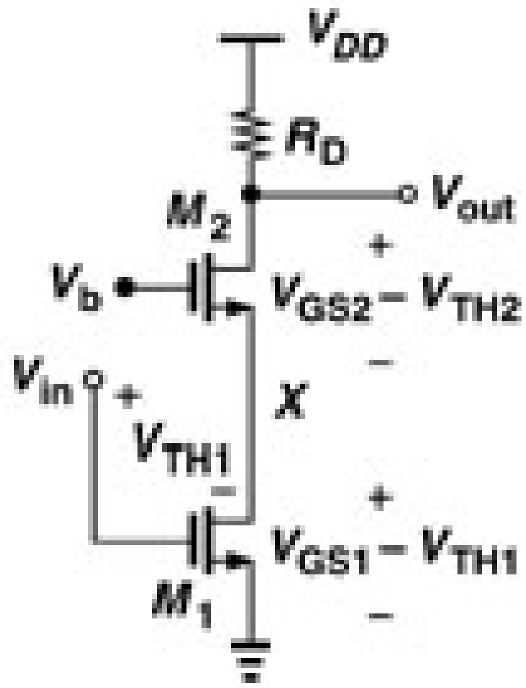
- Same voltage gain and input resistance as a CS amplifier.
- Output resistance much larger than that of CS or CG amplifiers.
- Bandwidth much larger than that of a CS amplifier.

Cascode amplifier – Bias Conditions: How big should V_b be?



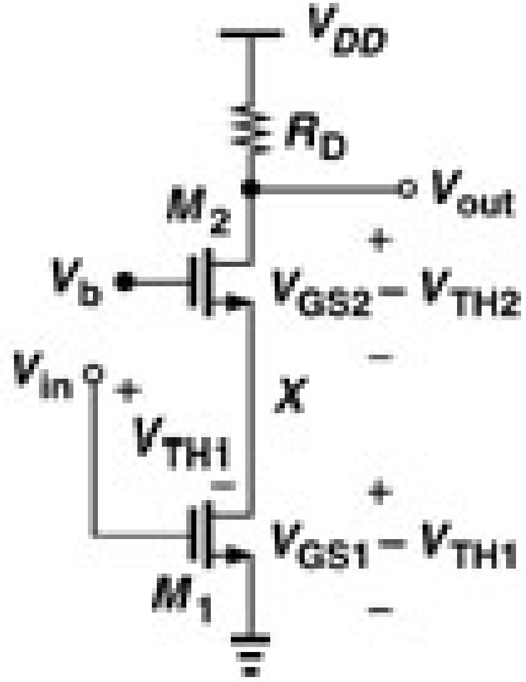
- M_1 in Saturation: $V_X \geq V_{in} - V_{TH1}$. That is:
- $V_b - V_{GS2} \geq V_{in} - V_{TH1}$

Cascode amplifier – Bias Conditions: How big should V_{out} be?



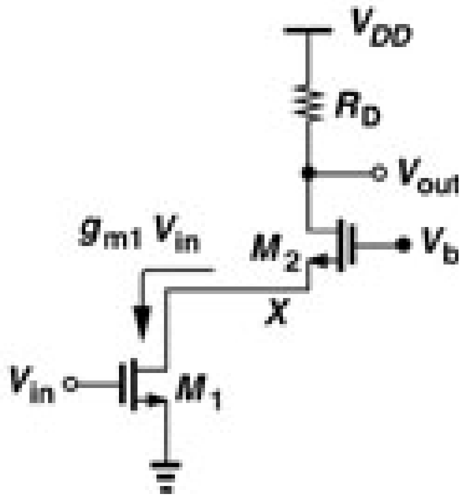
- M_2 in Saturation: $V_{out} \geq V_b - V_{TH2}$. That is:
- $V_{out} \geq V_{in} - V_{TH1} + V_{GS2} - V_{TH2}$ if V_b places M_1 at edge of Triode Mode. This is the minimum V_{out}

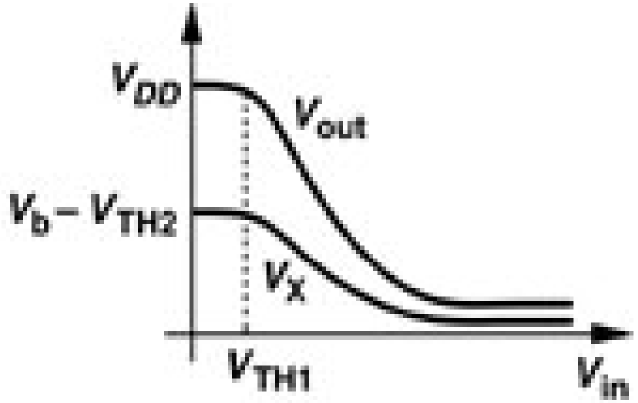
Cascode amplifier – Reduced Swing



- Tradeoff: For all the nice properties of Cascode, the “stacking” of M_2 on top of M_1 reduces the swing.

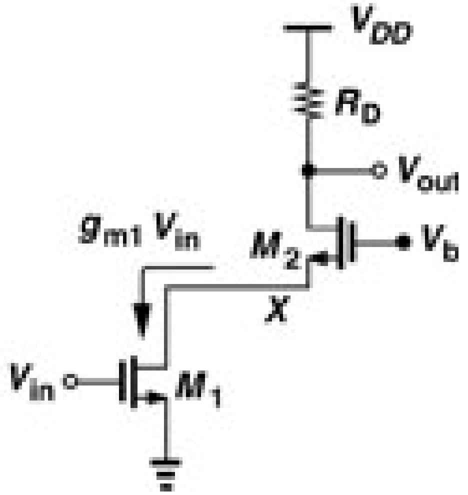
Cascode Large Signal Analysis - Cutoff

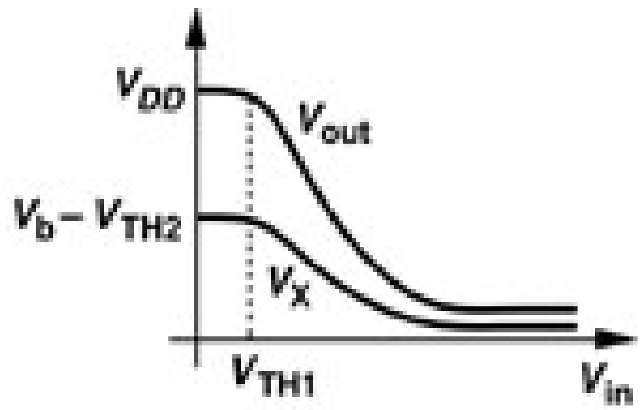




- If $V_{in} \leq V_{TH1}$ both transistors are off.
- $V_{out} = V_{DD}$
- If no sub-threshold conduction, then $V_X \approx V_b - V_{TH2}$! (as explained for CS with diode-connected load)

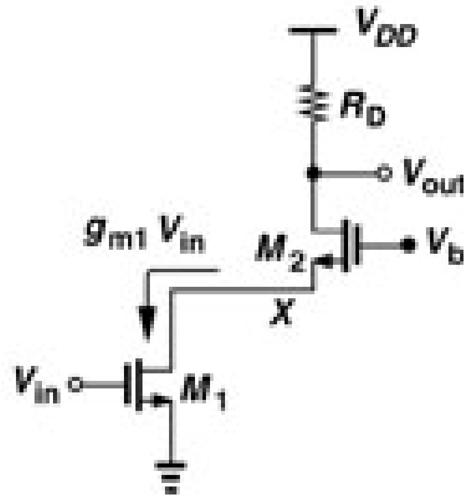
Cascode Large Signal Analysis – Saturation Mode

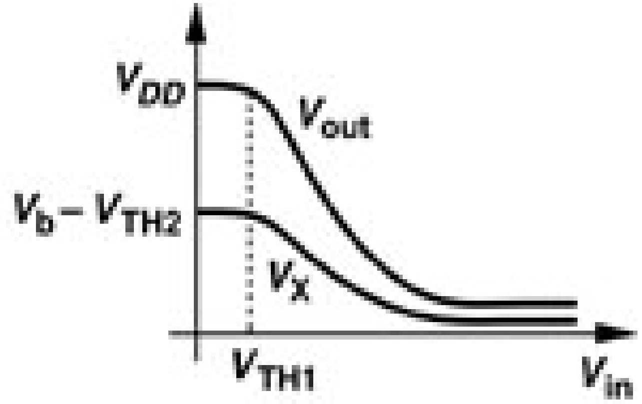




- As $V_{in} \geq V_{TH1}$ a current develops. V_{out} must drop.
- As I_D increases, V_{GS2} increases, causing V_X to fall.
- As we keep increasing V_{in} which transistor enters Triode Mode first?

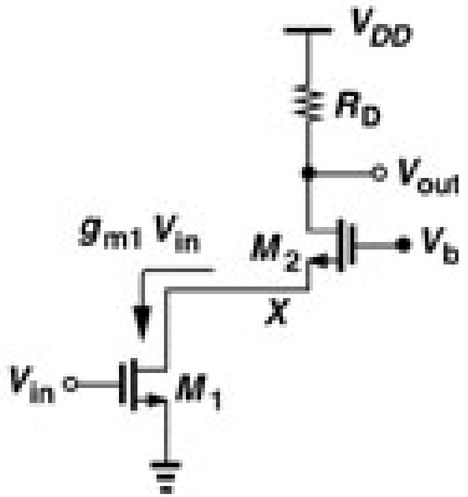
Cascode Large Signal Analysis – Edge of Triode Mode

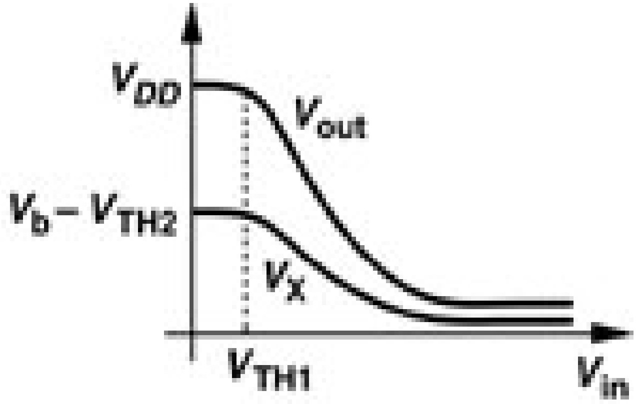




- As we keep increasing V_{in} which transistor enters Triode Mode first?
- Either one may, depending on the parameters and R_D,V_b

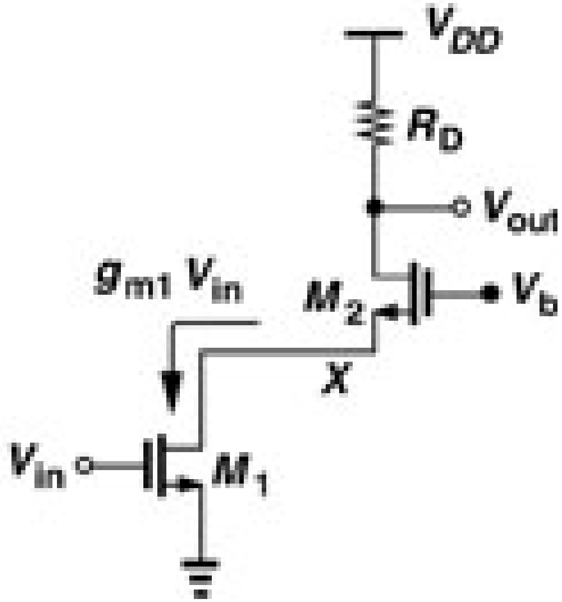
Cascode Large Signal Analysis – Edge of Triode Mode





- If V_X falls below $V_{in} – V_{TH1}$ then M_1 goes into Triode Mode.
- If V_{out} drops below $V_b – V_{TH2}$ then M_2 goes into Triode Mode.
- For instance, if V_b is low, M_1 enters Triode First.

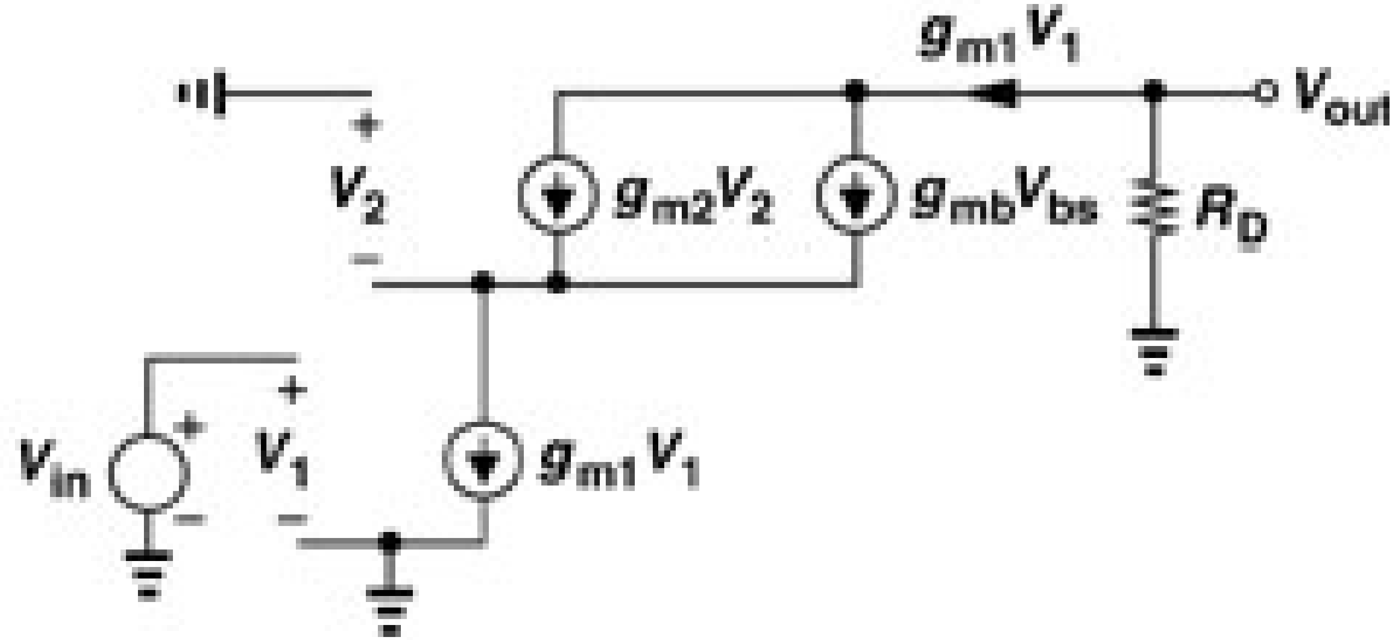
Cascode Volatge Gain Formula if we neglect λ effects



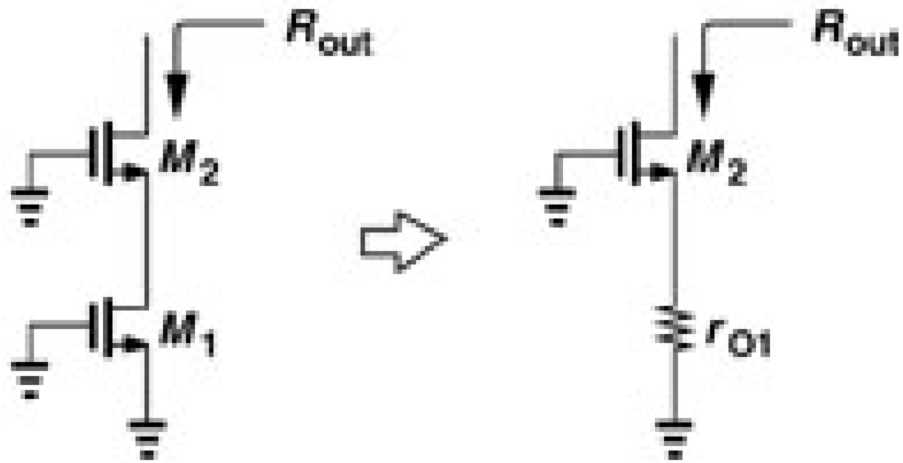
$$A_V \approx -g_{m1} R_D$$

Gain independent of g_{m2} and body effect of M_2 !

Small-Signal Equivalent Circuit of Cacode Stage

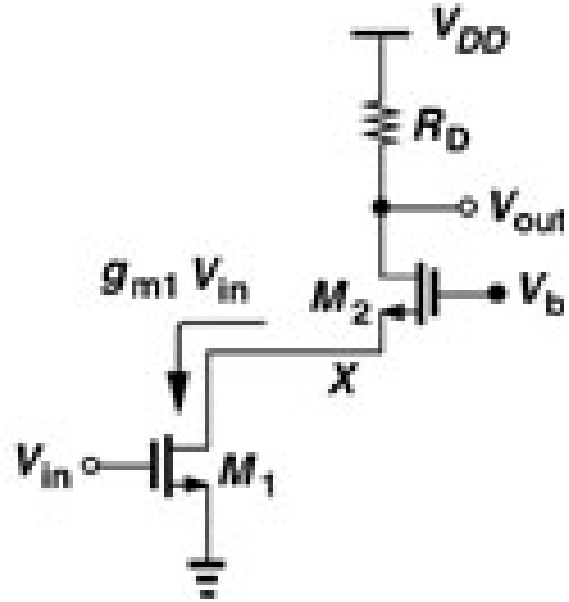


Cascode's Output Resistance



$$R_{out} = [1 + (g_{m2} + g_{mb2}) r_{o2}] r_{o1} + r_{o2}$$
$$\approx r_{o1} r_{o2} (g_{m2} + g_{mb2})$$

Cascode Gain taking into account r_o resistors

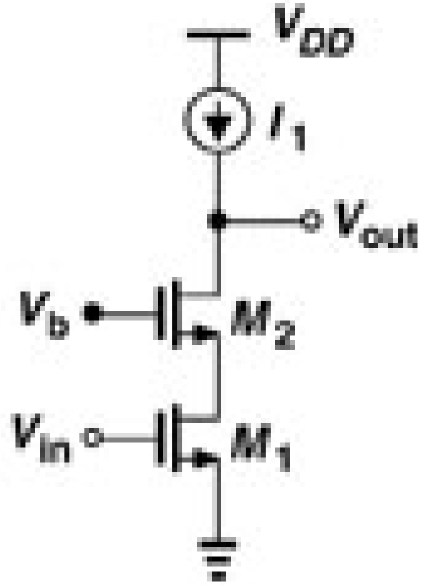


Recall the generalized gain formula $A_V = G_m R_{out}$ discussed in the context of CS amplifier with R_S

$$R_{out} = \{[1 + (g_{m2} + g_{mb2}) r_{o2}] r_{o1} + r_{o2}\} \| R_D$$
$$\approx [r_{o1} r_{o2} (g_{m2} + g_{mb2})] \| R_D$$

$$A_V \approx -g_{m1} \{[r_{o1} r_{o2} (g_{m2} + g_{mb2})] \| R_D]\}$$

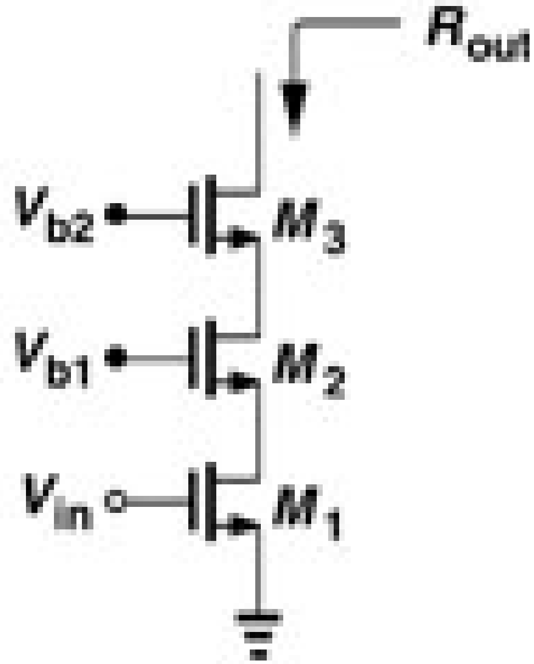
Cascode Gain Example



$$R_{out} = [1 + (g_{m2} + g_{mb2}) r_{o2}] r_{o1} + r_{o2}$$
$$\approx r_{o1} r_{o2} (g_{m2} + g_{mb2})$$

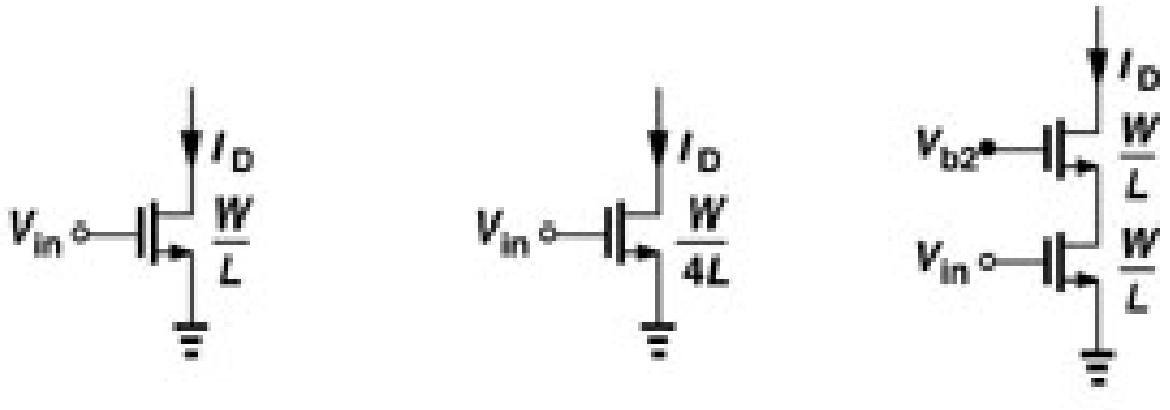
$$A_V \approx -g_{m1} r_{o1} r_{o2} (g_{m2} + g_{mb2})$$

Cascoding extended



Can achieve phenomenal R_{out} values, at the expense of a much reduced swing

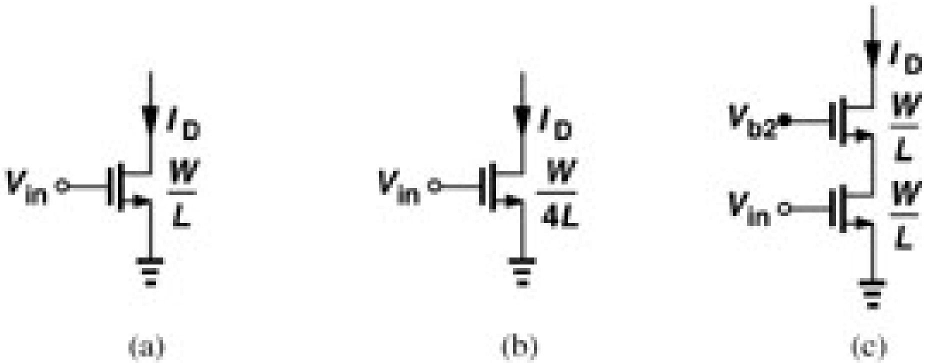
CS and Cascode Size vs. Swing Comparison



(a) (b) (c)

- What happens to a CS amplifier if we quadruple L without changing W and I_D ?
- The "overdrive" V_{GS}-V_{TH} doubles, and as a result, swing will be similar to that of Cascode (c).

CS and Cascode Size vs. Output Resistance Comparison



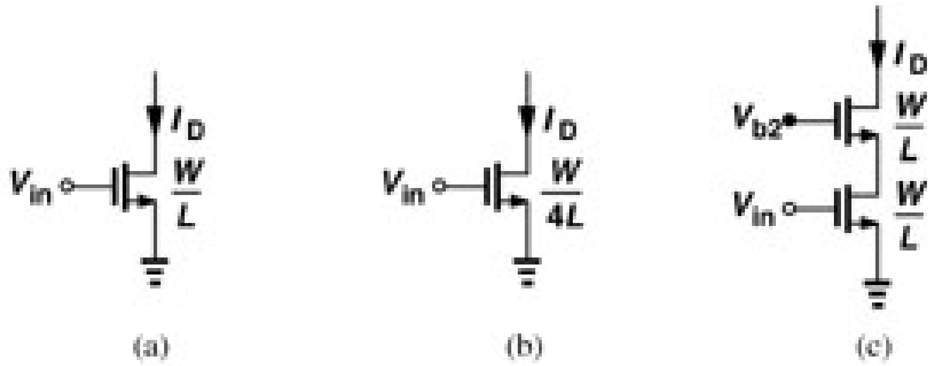
$$g_m r_o = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D} \frac{1}{\lambda I_D}$$

Recall that λ is proportional to 1/L. Quadrupling of L only doubles the value of $g_m r_o$.

Output resistance of (b) is four times bigger than that of (a).

Output resistance of (c) is approximately $(g_m r_o)^2$, much bigger than (b).

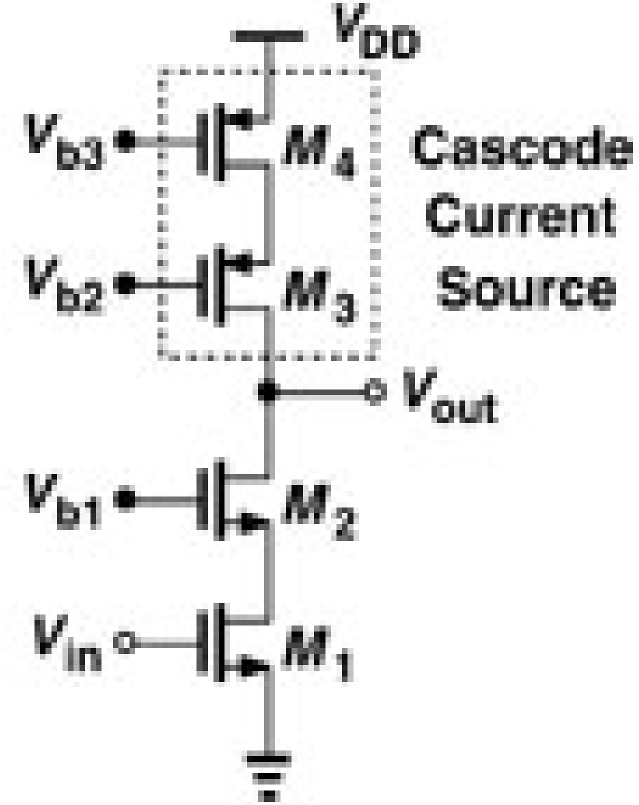
CS and Cascode Noise Comparison

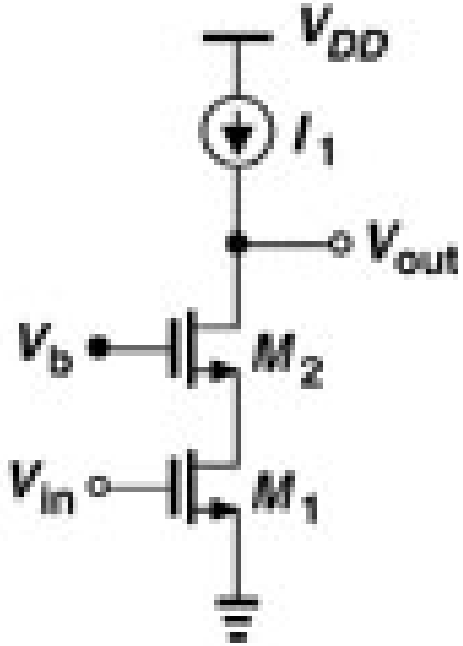


$$g_m = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D}$$

g_m in (b) is half of that of (c). As a result the CS amplifier with quadrupled L is noisier than the Cascode amplifier (We'll learn about device noise later on).

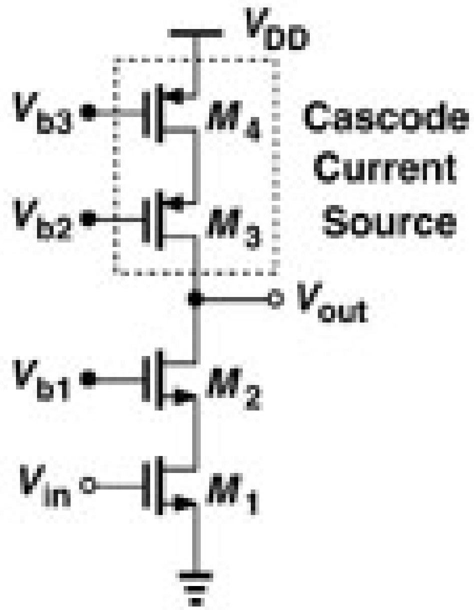
PMOS Cascode as Current Source Load for an NMOS Cascode amplifier





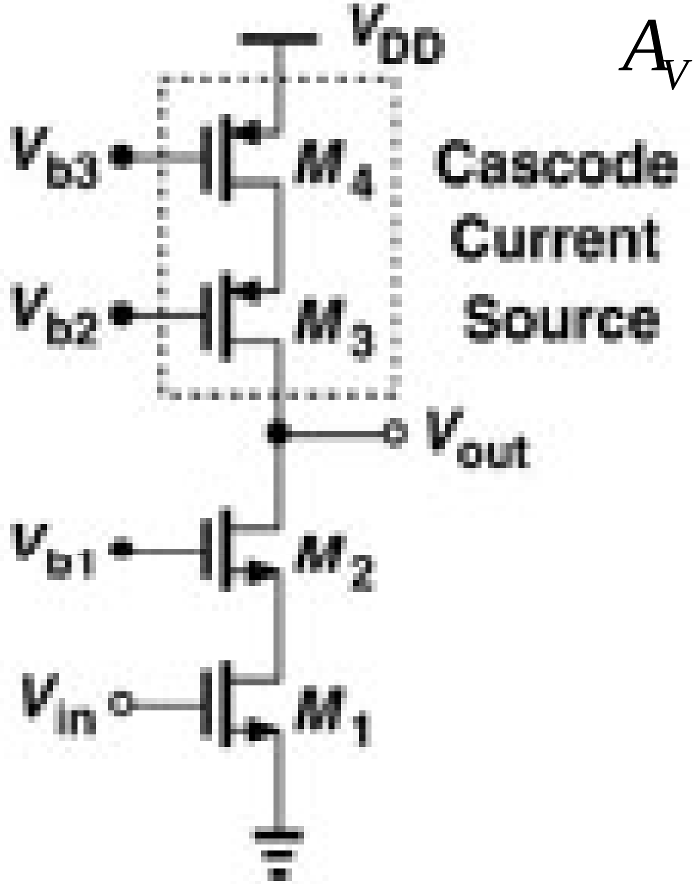
$$R_{out,current\_source} = [1 + (g_{m3} + g_{mb3})r_{o3}]r_{o4} + r_{o3}$$

PMOS Cascode as Current Source Load for an NMOS Cascode amplifier - Swing



If all gates' DC voltages are properly chosen, the maximum output swing equals $V_{DD} – (V_{GS1}-V_{TH1}) – (V_{GS2}-V_{TH2}) – |V_{GS3}-V_{TH3}| -|V_{GS4} – V_{TH4}|$

PMOS Cascode as Current Source Load for an NMOS Cascode amplifier – Gain



$$A_V \approx g_{m1}[(r_{o1}r_{o2}g_{m2}) \| (r_{o3}r_{o4}g_{m3})]$$

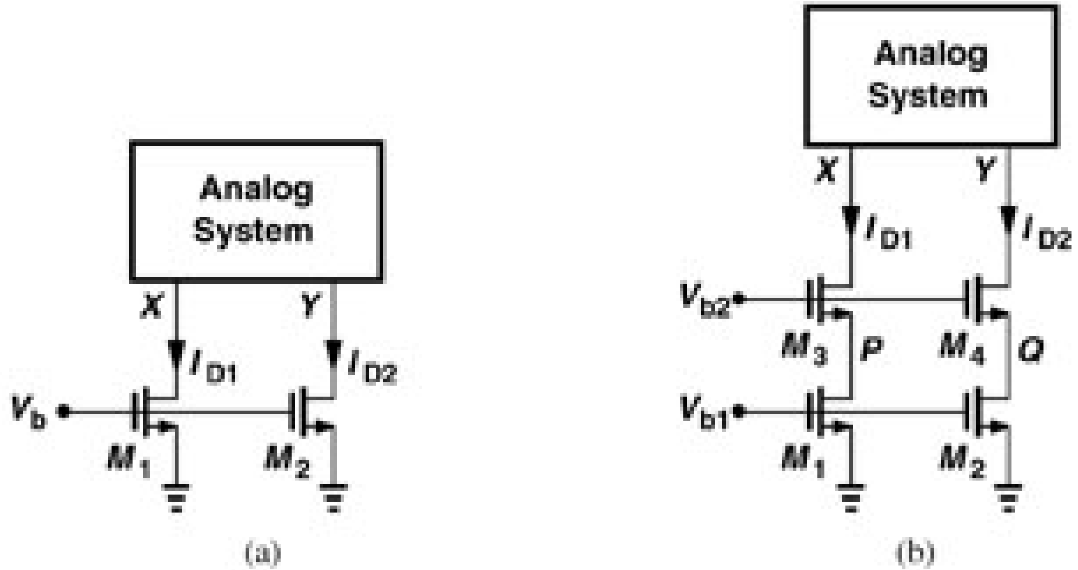
Explanation:

$A_V = G_m R_{out}$

$$G_m \approx g_{m1}$$

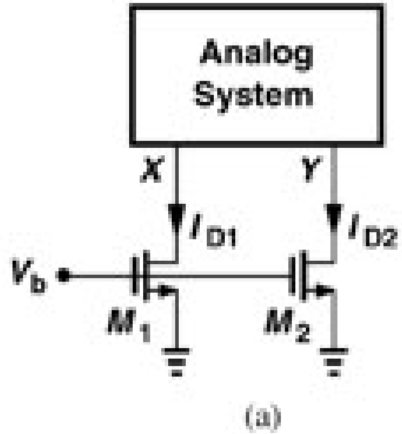
$$R_{out} = \{[1+(g_{m2}+g_{mb2})r_{o2}]r_{o1}+r_{o1}\} \| \{[1+(g_{m3}+g_{mb3})r_{o3}]r_{o4}+r_{o3}\}$$

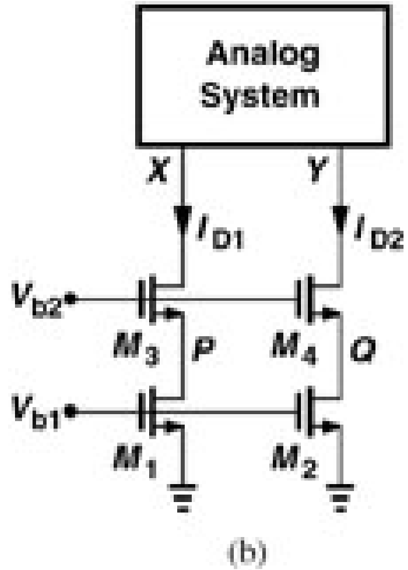
Current Mirror Current Sources



- Assume that I_{D1} is the reference current, and I_{D2} is the desired current source.
- If $\lambda \neq 0$ and if $V_X \neq V_Y$ then there may be a significant error between the two currents.

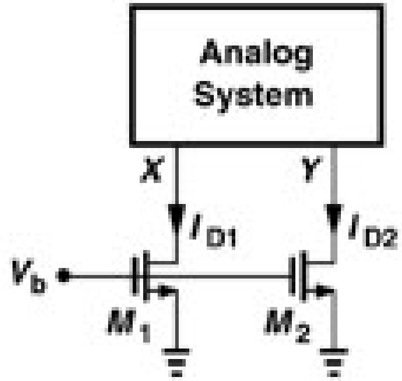
Current Mirror Current Sources



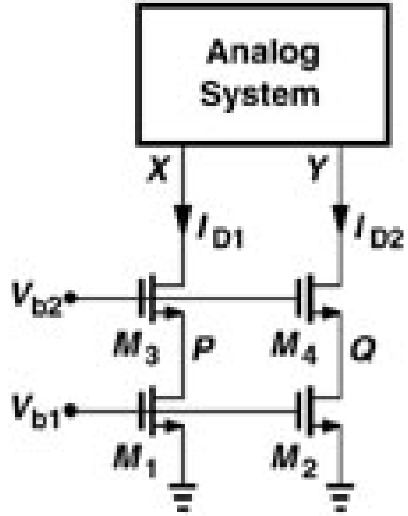


- Error in (a): (assuming that both transistors have the same W/L ratio)
- $I_{D1}-I_{D2} = 0.5k_n'(W/L)(V_b-V_{TH})^2\lambda(V_X-V_Y)$

Current Mirror Current Sources



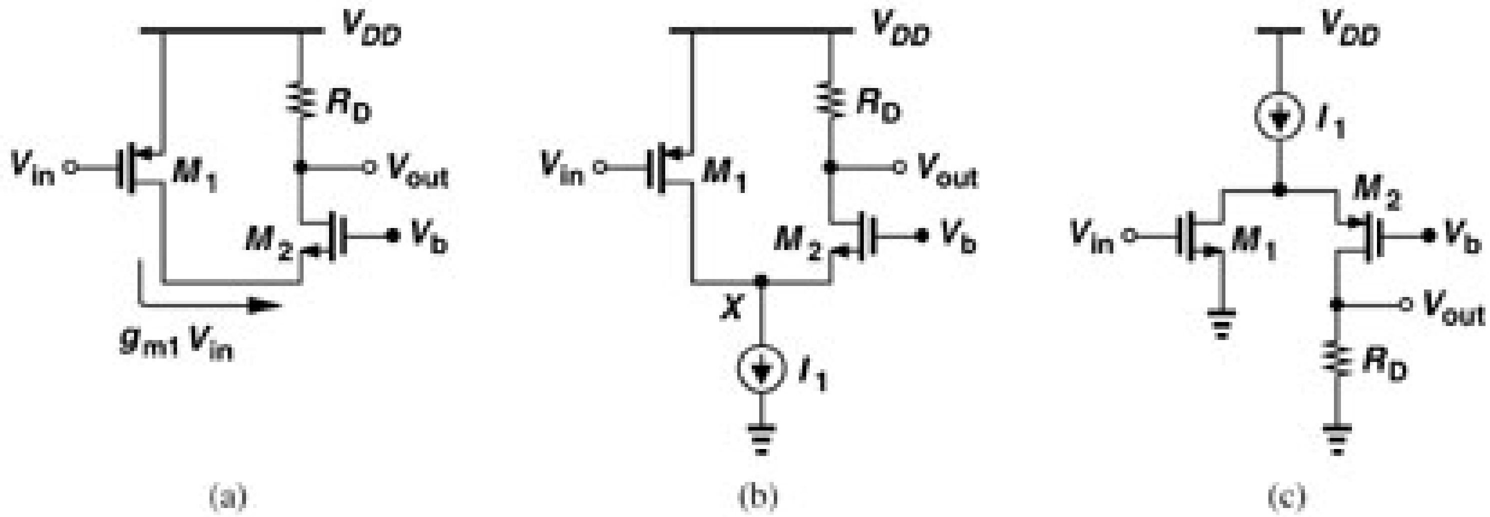
(a)



(b)

- In (b) it can be shown that $I_{D1}-I_{D2} \approx 0.5k_n'(W/L)(V_b-V_{TH})^2\lambda(V_X-V_Y)/[(g_{m3}+g_{mb3})r_{o3}]$
- Cascoding significantly reduces the mismatch between the two mirrored currents

Folded Cascode



- Folded Cascode: NMOS CS feeding into PMOS CG, or vice versa.
- Biasing by a DC current source is necessary.