Lecture 4

Microfabrication – Wafer-Level Processes (II)

- Wafer-Level Processes
  - Oxidation of Silicon
    - Deal-Grove Model
    - Dry and Wet Oxidation
    - Thickness of Silicon Oxides
  - Local Oxidation
  - Doping
    - Ion Implantation
    - Drive-In Diffusion

Oxidation of Silicon

- High quality of oxide can be thermally grown its surface.
- A molecule of oxygen reacts directly with the silicon, forming silicon dioxide.
- This is accomplished in tube furnaces, operated at temperatures from about 850 ^{o}C to 1150 ^{o}C.
- In dry oxidation, pure oxygen is used as the oxidant, flowed through the oxidation furnace with a background flow of nitrogen as a diluent.
- The oxidation rate depends on the arrival of oxygen at the silicon-oxide interface.
- The oxygen must diffuse through the oxide to reach this interface, so as the oxide gets thicker, this arrival rate decreases.
- As a result, a bare silicon wafer grows oxide quickly, but an already oxidized wafer, subjected to the same conditions, adds relatively little additional oxide.

Deal-Grove Model

- **Deal-Grove model of oxidation kinetics**

  x_i is the initial oxide thickness present on the wafer when the oxidation begins, the final oxide thickness x_f is given by

$$x_f = 0.5 A_{DG}\left[\sqrt{1+\frac{4B_{DG}}{A_{DG}^2}(t+\tau_{DG})}-1\right],$$

$$\tau_{DG} = \frac{x_i^2}{B_{DG}} + \frac{x_i}{(B_{DG}/A_{DG})}$$

- At short times, linear rate model

$$x_f = \frac{B_{DG}}{A_{DG}}(t+\tau_{DG})$$

- At long times, parabolic model.

$$x_f = \sqrt{B_{DG}t}$$

Dry Oxidation

Table Deal-Grove rate constants for the dry oxidation of silicon. The value of τ_{DG} is the recommended value when starting with a bare wafer.

Temperature (^oC)	A_{DG} (μm)	B_{DG} $(\mu m^2/hr)$	B_{DG}/A_{DG} $(\mu m/hr)$	τ_{DG} (hr)
920	0.235	0.0049	0.0208	1.4
1,000	0.165	0.0117	0.071	0.37
1,100	0.090	0.027	0.30	0.067

- The value of τ_{DG} is what should be used for a bare wafer and corresponds to an initial oxide thickness of about 27 nm.
- The Deal-Grove model is accurate only for oxides thicker than about 30 nm.
- Most oxides used in MEMS devices meet this criterion.
- Dry oxidation is typically used when the highest-quality oxides are required. Ex) thin gate oxides of MOS transistors (10 nm thick).

Wet Oxidation

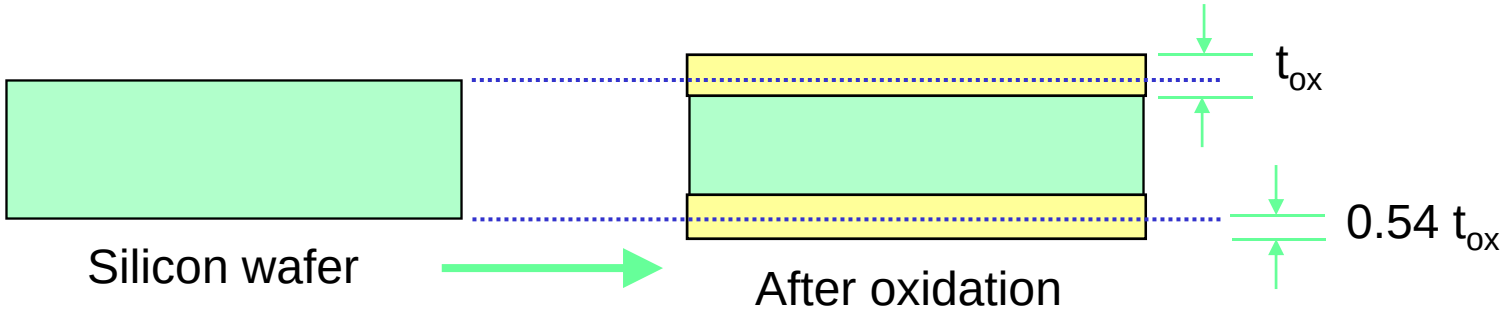
Table Deal-Grove rate constants for the wet oxidation of silicon. The value of τ_{DG} is the recommended value when starting with a bare wafer.

Temperature (^oC)	A_{DG} (μm)	B_{DG} $(\mu m^2/hr)$	B_{DG}/A_{DG} $(\mu m/hr)$	τ_{DG} (hr)
920	0.05	0.203	0.406	0
1,000	0.226	0.287	1.27	0
1,100	0.11	0.510	4.64	0

- The diffusion rate of oxygen through oxide can be significantly enhanced if there is water vapor present.
- Water breaks a silicon-oxygen-silicon bond, forming two OH groups.
- This broken-bond structure is relatively more mobile than molecular oxygen; the oxidation rate is faster.
- The water vapor can be provided by oxidizing hydrogen to steam in the furnace.
- Wet oxidation is used to make thicker oxides, from several hundred nm up to about 1.5 microns.

Thickness of Silicon Oxides

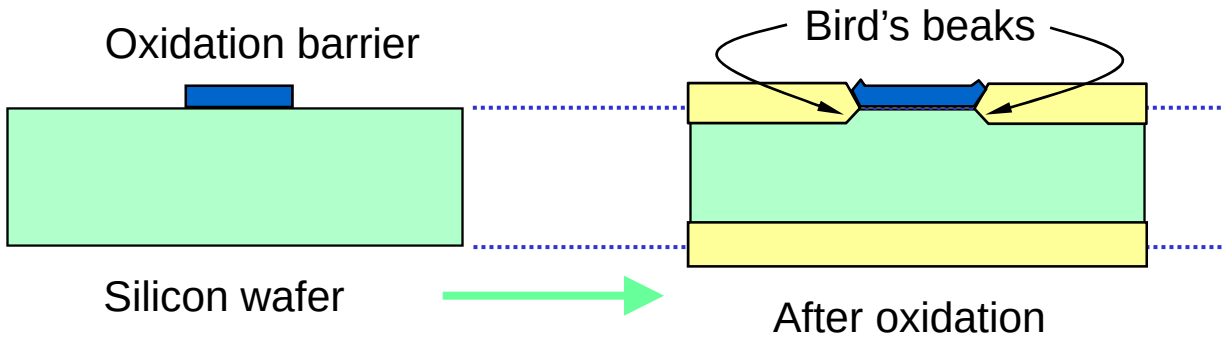
- Because the density of silicon atoms in silicon dioxide is lower than in crystalline silicon, the conversion of silicon to silicon dioxide makes the overall wafer thickness increase.
- About 54 % of the total oxide thickness appears as added thickness.
- The remaining 46 % is conversion of substrate material to oxide.



Thermal oxidation consumes some of the wafer thickness. Only 54% of the final oxide thickness appears as a net increase in wafer thickness. The remaining 46% appears as a conversion of silicon to oxide within the original wafer.

Local Oxidation

- When a portion of silicon wafer is covered with an oxygen diffusion barrier, such as an silicon nitride, oxidation cannot occur.
- Protected regions of a wafer remain at their heights, while unprotected regions are converted to oxide.
- During the oxidation process, stresses are generated that slightly lift the protective nitride at its edges, creating a tapered oxide called a *bird's beak*.



Illustrating selective oxidation of silicon with a silicon nitride thin film serving as an oxidation barrier. In practice, a very thin strain-relief oxide, of order 5 nm thick, is placed beneath the nitride to relieve strains generated during the oxidation process. This oxide is not shown in the diagram.

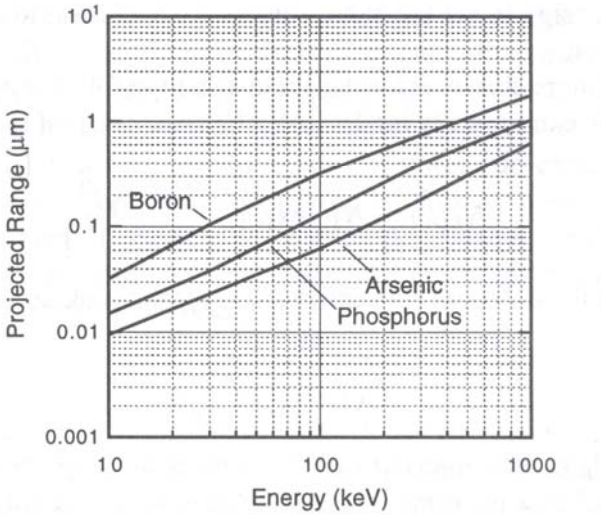
Doping

- Doping is the process whereby minute quantities of impurities are added to semiconductor crystals at substitutional sites, thereby modifying the electrical characteristics of the material.
- Silicon: IV group.
- Dopants: III group(boron), Mobile charge carriers: holes, P-type.
- Dopants: V group(phosphorous, arsenic, antimony), Mobile charge carriers: conduction electron, N-type.
- Dopants: Both. Net dopant concentration in a region that determines its conductivity type.
- Counter doping: An initially p-type region can be converted to an n-type region by adding more n-type dopant than the amount of p-type dopant originally present.
- **Deposition and Drive-in**
- **Deposition:** the delivery of the correct amount of dopant atom to region near the wafer surface, usually by ion-implantation.
- **Drive-in:** the redistribution of the dopant atoms by diffusion.

Ion Implantation

- A process in which a particle accelerator shoots a beam of dopant atoms directly into the wafer.
- The beam is scanned across the wafer surface as the wafer is rotated so as to achieve uniform deposition.
- By monitoring the ion current, the total ion dose Q_I, in atoms/cm^2, can be controlled.

- It introduces a very thin sheet of a known number of dopant atoms at a particular depth into the substrate.
- The depth of this sheet(projected range) depends on the ion energy, the ion species, and the material into which the implantation is performed.

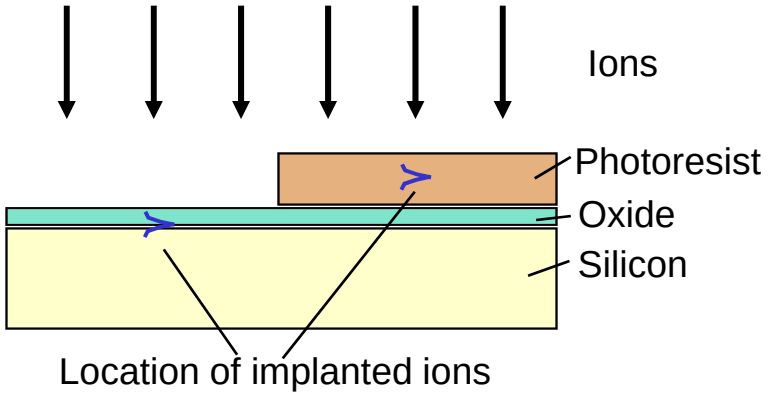


Projected ranges of ions implanted into silicon

Projected Range

- The fact that ion implantation has a finite range means that surface layers can be used to mask regions of the wafer, preventing the dopant ion from reaching the wafer.
- Implant mask: photoresist, silicon dioxide, silicon nitride.
- As a first approximation, one can use the silicon range data for silicon dioxide and other inorganic materials.

- For the heavier ions (phosphorous and arsenic), the projected range in oxide is about 20% less than in silicon.
- The projected range in photoresist is about 2-3 times greater than in silicon, its thickness needs to be about 3 times the projected range in silicon.



Illustrating the use of a photoresist mask to keep the implant from reaching the silicon in selected regions

Dopant Concentration

- Ion profile described by a Gaussian of the form:

$$N_I(x) = N_{I,p} \exp\left[-\frac{(x - R_p)^2}{2(\Delta R_p)^2}\right]$$

where $N_I(x)$ is dopant concentration, N_p is the peak dopant concentration is given by

$$N_{I,p} = \frac{Q_I}{\sqrt{2\pi}\Delta R_p}$$

and where R_p is the projected range.

- ΔR_p is the projected range standard deviation, and is a measure of the statistical spread of implanted ions (the width of the implanted sheet).
- Following ion implantation, an anneal at about 900 ^{o}C is required to assist the implanted atoms to reach their required substitutional positions in the crystalline lattice and to reduce lattice defects (atoms out of place) caused by the ion bombardment.

Thin Protective Layer

- Direct ion bombardment into a surface can knock surface atoms loose (a process called sputtering).
- It is normal to do ion implantation through a thin protective layer, such as a few tens of nm of silicon dioxide.
- This oxide also tends to scatter the ions slightly as they pass through, providing a range of impact angles into the silicon.
- This reduces an effect called ***channeling***, which is the deep penetration of an atom that is moving exactly along a high symmetry direction and happens to strike the crystal between atoms.
- The presence of the oxide layer affects the penetration depth into the substrate, and must be taken into account by using SUPREM.
- The final dopant distribution can be modified by the diffusion that takes place during any high-temperature process step that occurs after the implant.

Drive-In Diffusion

- Ion implantation provides a certain dose of dopants in a layer near the silicon surface.
- To redistribute these dopants (as well as to remove any residual defects produced by the implantation process), high-temperature anneals in a suitable atmosphere are used.
- Usually, one chooses to do such drive-in anneals beneath a protective oxide layer to prevent dopant evaporation.
- Diffusion: A flux of dopants form regions of high concentration toward regions of lower concentration.
- The flux proportional to the concentration gradient of the dopant.
- The proportionality constant: diffusion constant.

Temperature Dependence of Diffusion

- Diffusion constants for the various dopant atoms are thermally activated, having the typical form,

$$D = D_0 e^{-E_A/\kappa_B T}$$

where κ_B is Boltzmann's constant (1.38 x 10^{-23} J/K), *T* is temperature in Kelvins, D_o is a constant and E_A is the activation energy, typically in the range of 0.5 to 1.5 eV, depending on the diffusion mechanism.

Parameters governing the temperature dependence of diffusion in silicon

Ion	D_o (cm^2/sec)	E_A (eV)
Boron	0.72	3.46
Phosphorus	3.85	3.66

- At 1100 ^oC, the dopant diffusivities for boron and phosphorous are both about 1.4 x 10^{-13} cm^2/sec.

Effect of Drive-In

- Drive-in diffusions require high temperatures, typically in the 1000 ^{o}C to 1150 ^{o}C range.
- The net effect of drive-in diffusion is to take the original dose produced during the deposition step and spread it out into a Gaussian profile with a width proportional to $\sqrt{Dt}$, where *D* is the diffusion constant for the species at the anneal temperature, and *t* is the drive-in time.
- For example, if an ion implant step is used to introduce a narrow layer of dopant atoms very near the surface with total dose Q_I atoms per square cm, the dopant profile as a function of time during a drive-in anneal takes the form

$$N(x,t) = \frac{Q_I}{\sqrt{\pi Dt}} \exp\left[-\frac{x^2}{4Dt}\right]$$

Dopant Profile

- If a complete process sequence involves several high-temperature steps, each one enables some diffusive motion of dopants.
- Thus, the accumulated *Dt* product for a complete process sequence is a rough measure of how much overall dopant motion to expect.
- When building MOS transistors, too much dopant motion can destroy device performance.
- Therefore, process sequences in which transistors are being fabricated have strict limits on the total *Dt* product.

pn Junction

- When a p-dopant is diffused into an n-type substrate, or vice versa, a pn junction is created.
- What is physically important is the junction depth, the distance beneath the silicon surface at which the concentration of introduced dopant of one type equals the background concentration of the wafer.
- If the background concentration of the wafer is N_D, then the resulting junction depth x_j is

$$N(x,t) = \frac{Q_I}{\sqrt{\pi Dt}} \exp\left[-\frac{x^2}{4Dt}\right] \quad \Rightarrow \quad x_j = \sqrt{(4Dt)\ln\left(\frac{Q}{N_D\sqrt{\pi Dt}}\right)}$$

- There are many second-order effects that affect diffusion profiles.
- Boron can dissolve slowly into overlaying oxide, slightly depleting the surface concentration.
- Diffusion rates are also affected by the presence of point defect and, to some degree, by other dopants and by whether or not oxidation is taking place during the drive-in.