Lecture 17

Process Integration – A Bulk- and Surface-Micromachined Examples

- A Bulk-Micromachined Diaphragm Pressure Sensor
  - Starting Material
  - Oxide and Alignment Target
  - Visibility of Alignment Target
  - Piezoresistors
  - Diaphragm
  - Undercut
  - Vias
  - Test, Mount and Package
- A Surface-Micromachined Suspended Filament

Starting Material

- The starting material is selected to be a lightly-doped p-type wafer with a 10 micron epitaxial layer that is moderately-doped n-type.
- One could specify a wafer thickness of 500 +/- 5micron.
- Following cleaning, a thermal oxide of thickness 0.17 micron.
- This choice of thickness is dictated by our goal of creating stress balance in the dielectric layers.
- As-deposited LPCVD silicon nitride has about 1 GPa of tensile stress whereas thermal oxide grown at temperature above 950^{o}C has a compressive stress of about 300 mega-Pascal.

	Step	Description
	Starting material	100 mm (100) p-type silicon, 1 x 10^{15} cm^{-3} boron, with 10 micron n-type epi-layers, 5 x 10^{16} cm^{-3} phosphorous
1	Clean	Standard RCA cleans with HF dip.
2	Oxide	Grow 0.17 micron

Oxide and Alignment Target

- To achieve stress balance, thickness of the oxide times its stress should equal the thickness of the nitride times stress.
- We plan to use 50 nm of nitride as an etch mask for the KOH etch, which thus suggests we should use 0.17 micron, for the oxide thickness, provided it is grown above 950^{o}C.
- Mask 1 contains alignment marks needed to locate the otherwise invisible implanted piezoresistors with respect to the rest of the device features.
- In order to align a mask to a wafer, there must be a visible feature already present on the wafer, called an *alignment target.*
- Alignment targets are typically produced during an etch step.

Target on lower layer Alignment feature on mask Perfect registration of mask to target

Visibility of Alignment Target

- It is also important to keep track of the visibility of the alignment targets in multi-mask processes, because some intermediate steps might obscure the visibility of targets in lower layers.
- In the example here, separate alignment targets for each mask layer will be etched into the thermal oxide using Mask 1.
- There are no visibility problems.
- The most critical alignment, the positioning of the backside etch relative to the piezoresistor locations, comes early in the process with only 50 nm of nitride as an added layer.
- The only deposited layer that potentially obscures visibility is the aluminum.
- In this case, the topography of the alignment target initially etched into the oxide should provide a corresponding topographic feature on the aluminum surface to permit alignment of the metal mask.

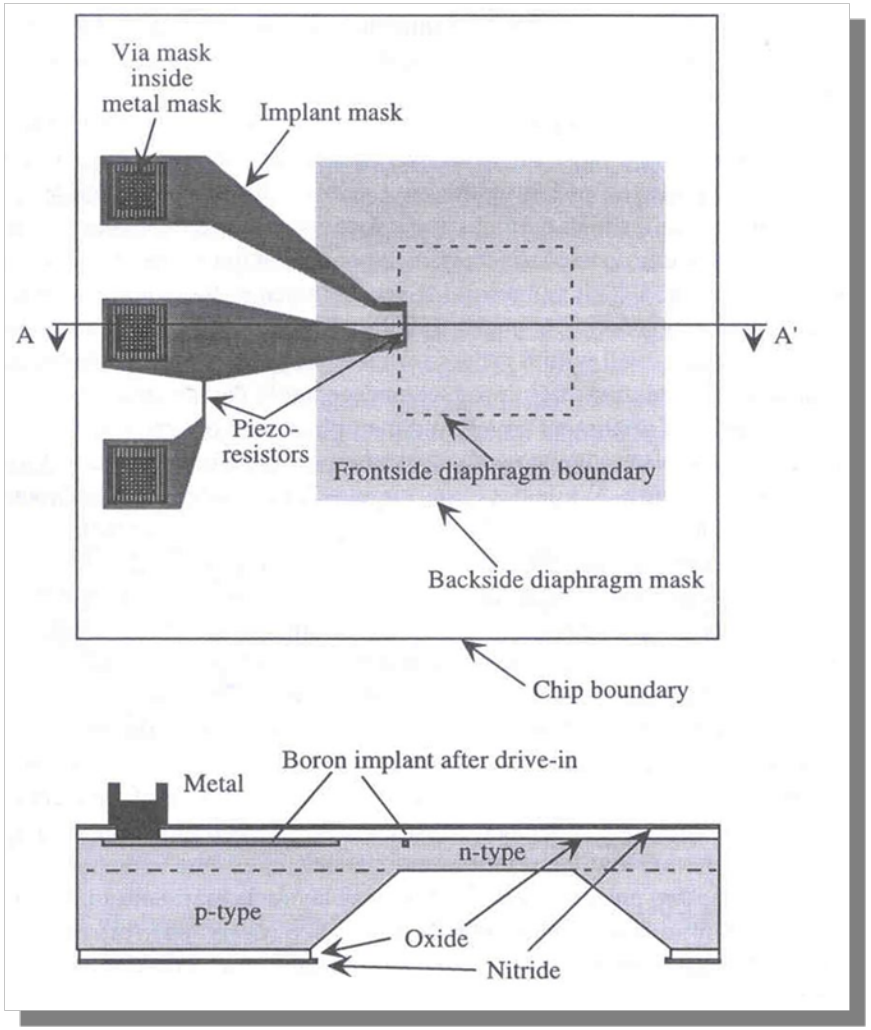
Alignment Feature Size

- To get precise registration of one mask level to another, it is desirable that the alignment targets be small, with overlaps between mask feature and target close to the resolution of the patterning process.
- But if the alignment feature size is much smaller that typical device features, as often happens in MEMS devices, special care is need to set etch recipes so that the alignment features are faithfully patterned.
- This can result in over- or under-etching of device features.
- Once the alignment targets have been patterned into the oxide and the photoresist has been stripped, the lithography for implanting of the piezoresistors can be done.

	Step	Description
3	Photolithography	Mask 1 (alignment)
4	Etch	Etch alignment masks into SiO_2
5	Strip	Strip Photoresist

Piezoresistors

- The ion energy, dose and drive-in conditions needed to meet the specification in Table.
- The mask for the piezoresistors is shown in Figure with the remaining three masks.



Figure

Above: an overlay of the dour device masks for the pressure sensor example.

Below: a not-to-scale cross-section through A-A'

(continued)

Piezoresistors

- Note that one of the piezoresistors is located near what will become the edge of the diaphragm, and one is located over unetched substrate.
- The wide regions on the implant mask are to provide low-resistance interconnect between the three bond pads on the left and the two piezoresistors.
- This mask layout is for illustration only, and has not been optimized for chip area.

	Step	Description
6	Photolithography	Mask 2 (piezoresistors)
7	Implant	Ion implantation of boron to achieve 1 x 10^{19} cm^{-3} at surface after drive-in
8	Strip	Strip photoresist
9	Clean	RCA clean, no HF dip
10	Drive-in	Drive in diffusion to achieve 0.2 micron junction depth.
11	Clean	RCA clean, no HF dip

Diaphragm

- After implant of the piezoresistors, LPCVD nitride is deposited.
- The backside lithography is then done to open the etch window for the KOH etch.
- The nitride is removed, then the oxide.
- Wet etching of the oxide will slightly undercut the nitride mask, and because the masking oxide does etch slowly in KOH, further undercutting the nitride, the final diaphragm boundary will be slightly larger than that which would result from the mask dimension.

	Step	Description
12	Nitride	Deposit 50 nm LPCVD silicon nitride
13	Backside Photolithography	Mask 3 (diaphragm)
14	Etch	Remove nitride and oxide from back of wafer
15	KOH Etch	Etch back side with KOH using electrochemical etch stop

Undercut

- Determination of the correct backside mask feature size must include three:
  (1) the size of the final diaphragm

  (2) the extra area required for the sloped sidewalls by the KOH etch,

  (3) correction for mask undercut during etching.
- The undercut is shown greatly exaggerated in the cross-section in Figure.
- If the backside etch mask is not accurately aligned with the <110> crystalline directions, the diaphragm size will increase.

Vias

- Once the diaphragm is etched, the rest of the process is just like the diode example.
- Vias are etched and metal is evaporated and patterned.

	Step	Description
16	Photolithography	Mask 4 (vias)
17	Etch	Plasma etch nitride and oxide from vias
18	Strip	Strip photoresist
19	Clean	Pre-metal clean (RCA without HF dip)
20	Metal	Evaporate 1 micron aluminum
21	Photolithography	Mask 5 (aluminum)
22	Etch aluminum	PAN etch(phosphorus-acetic-nitric acids)

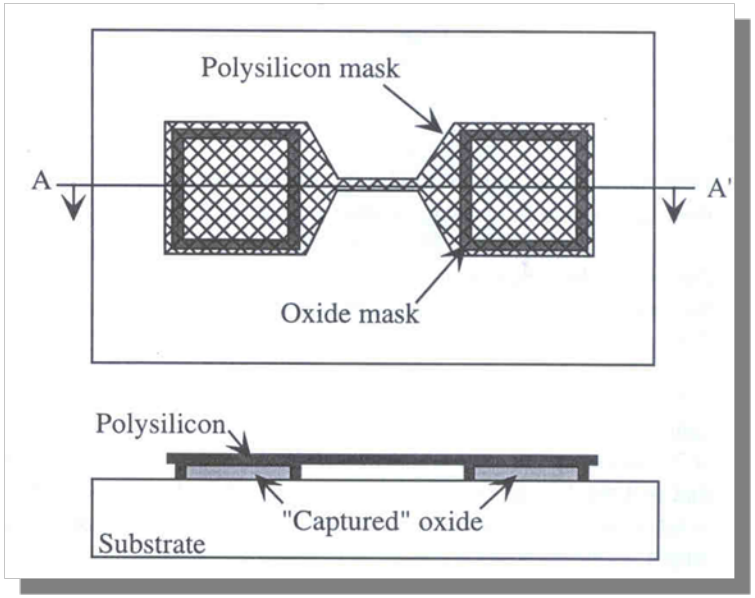
Test, Mount and Package

- Then, prior to die separation, each piezoresistor circuit is tested electrically, and chips with bad circuits are marked.
- Following die separation with a die saw, individual good devices are placed into their packages and wire-bonded.
- Final test and calibration can then take place.

	Step	Description
23	Strip	Strip photoresist
24	Sinter	Anneal contacts at 425 ^{o}C, 30 mim
25	Test	Test for piezoresistor value at wafer level
26	Die separation	Separate devices with die saw
27	Mount	Mount in package (failed die not used)
28	Wire bond	Form wire bonds to package
29	Seal	Close and seal package
30	Test	Final test and calibration

A Surface-Micromachined Suspended Filament

- A silicon substrate is used in this process, as silicon is not attacked by the release etch.
- A 2 micron oxide is deposited by CVD.
- This oxide is patterned with oxide mask, creating two square trenches.
- The width of these trenches is designed to be about twice the thickness of the polysilicon so that when polysilicon is deposited, they fill completely.



Masks and not-to-scale cross-section through A-A' for the suspended filament process. The mask polarities assume negative resist for the oxide mask and positive resist for the polysilicon mask.

(continued)

A Surface-Micromachined Suspended Filament

- There follows 2 micron deposition of polysilicon which is then patterned with the polysilicon mask.
- The final step is the release etch, immersion in buffered HF to remove all the oxide except that which is surrounded by the polysilicon-filled trench.
- The filament is thus suspended above the substrate by the thickness of the sacrificial oxide, but is strongly supported by the blocks of “captured” oxide within the polysilicon trench.
- The captured oxide also provides supported pedestals onto which bond-pad metal could be deposited.