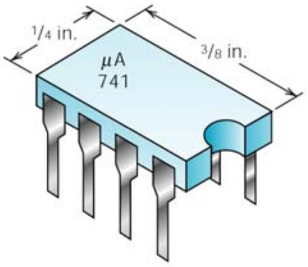
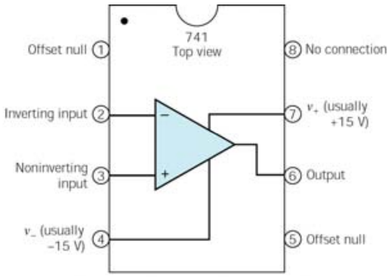
Operational Amplifier



(a) A μA741 integrated circuit has eight connecting pins



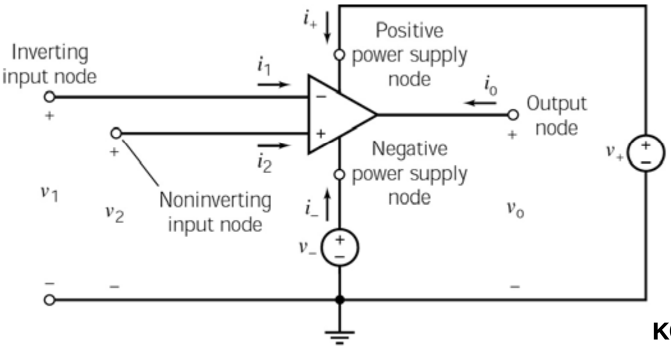
(b) The correspondence between the circled pin numbers of the integrated circuit and the nodes of the operational amplifier.

주요한 단자

1. inverting input
2. noninverting input
3. output
4. positive power supply (v^+)
5. negative power supply (v^-)

- NC : no connection
- Balance(offset null) : compensate for a degradation

Symbol and Circuits



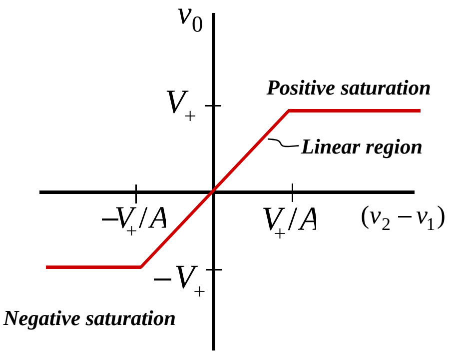
KCL

$$i_1 + i_2 + i_o + i_+ + i_- = 0$$

An op amp, including power supplies v^+ and v^-.

Common node : reference
- All voltages rise from the reference node.
- All currents come into the amplifier.

Ideal Operational Amplifier



- **Op amp**가 선형이기 위해서는 다음의 조건을 만족해야 한다.

$$|v_o| \le v_{sat}$$

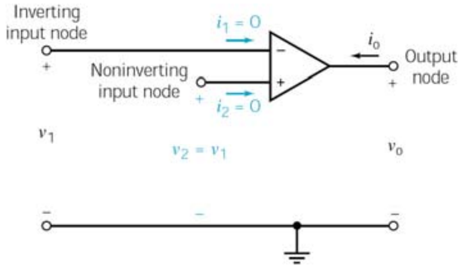
$$|i_o| \le i_{sat}$$

$$\left|\frac{dv_o(t)}{dt}\right| \le SR \quad (SR,\ slew\ rate)$$

$$-For\ \mu A741,$$

$$v_{sat} = 14\ \text{V}, \quad i_{sat} = 2\ \text{mA}, \quad SR = 500{,}000\ \text{V/s}$$

Ideal Operational Amplifier



The ideal operational amplifier

Table. Operating Condition for an Ideal Operational Amplifier

Variable	Ideal Condition	
Inverting node input current	$i_1 = 0$	⇦ $R_i \to \infty$
Noninverting node input current	$i_2 = 0$	
Voltage difference between inverting node voltage v_1 and noninverting node voltage v_2	$v_2 - v_1 = 0$	⇦ $A \to \infty$

− Ideal operational amplifier

Op amp input current는 영이다.

$$i_1 = 0, \quad i_2 = 0$$

Input node voltage는 같다.

$$v_2 = v_1$$

* Virtual short condition.

Ideal Operational Amplifier

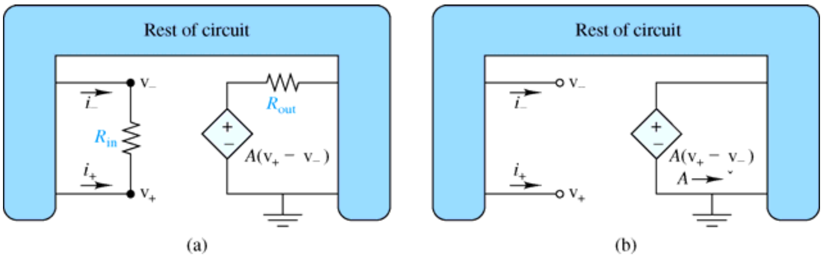


Figure 4.4 (a) Op amp model. (b) Idealized model.

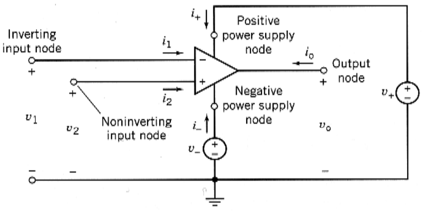
-Ideal OP Amp

(1) Infinite gain, (2) infinite input resistance, (3) zero output resistance

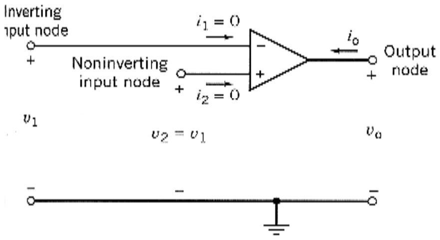
$$\boxed{R_i \to \infty, \quad R_o \to 0, \quad A \to \infty}$$

– 실제 소자 거동(e.g. saturation)을 정확히 묘사하지 못하나, 해석을 단순화.

Op amp 회로의 간략화



An op amp, including power supplies v^+ and v^-.



The ideal operational amplifier

KCL

$i_2 + i_1 + i_o + i_+ + i_- = 0$

여기서 i_2 , i_1은 매우 작으므로

$i_2 = i_1 \approx 0$

따라서, $i_o = -(i_+ + i_-)$

입력전류는 영이지만 출력전류는 상당히 흐른다.

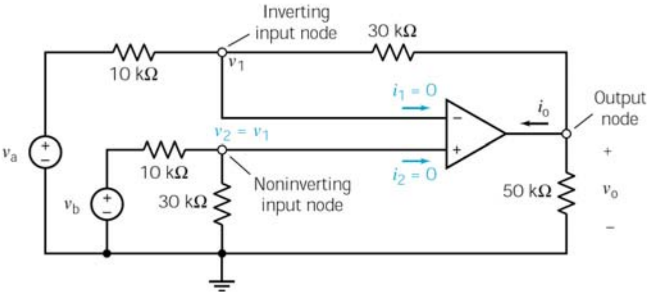
Op amp 회로는 선형 구간에서 그림과 같이 간략화 할 수 있다.

여기서 $|v_0| < V_+$ 이고

$i_2 + i_1 + i_o = 0$ 은 성립하지 않는다.

왜냐하면 이 회로는 간략화한 회로이기 때문이다.

Nodal Analysis of Op Amp Circuits



Op amp : virtual short condition

$$v_2 = v_1, \quad i_1 = i_2 = 0$$

Input 단자에서 KCL 적용.

Node 1

$$\frac{v_1 - v_a}{10k\Omega} + \frac{v_1 - v_o}{30k\Omega} + 0 = 0 \qquad (1)$$

Node 2 $$\frac{v_1 - v_b}{10k\Omega} + \frac{v_1 - 0}{30k\Omega} + 0 = 0 \qquad (2)$$

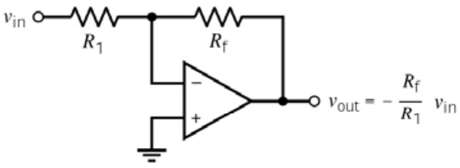
v_1 , v_o가 미지수

$$\frac{4}{3}v_1 - v_a - \frac{v_o}{3} = 0 \qquad (1')$$

$$\frac{4}{3}v_1 - v_b = 0 \qquad (2')$$

따라서, $v_o = -3(v_b - b_a)$

Inverting Amplifier



(a) Inverting amplifier

$v_2 = 0$ 이고 $v_2 = v_1$ 이므로 $v_1 = 0, i_1 = 0$

KCL에서 $i_{R1} + i_{Rf} = 0$.

$$\frac{0 - v_{in}}{R_1} + \frac{0 - v_0}{R_f} = 0$$

$$v_0 = -\frac{R_f}{R_1} v_{in} \qquad \left(\frac{R_f}{R_1} : scaling \;\; factor\right)$$

$|v_0| < V_+$ 이어야 하므로

$$\left|\frac{R_f}{R_1} v_{in}\right| < V_+ \rightarrow |v_{in}| < \frac{V_+}{R_f / R_1}$$

R_f가 없는 open loop인 경우

$v_o = -Av_1$이 되고 $i_1 \approx 0$ 이므로

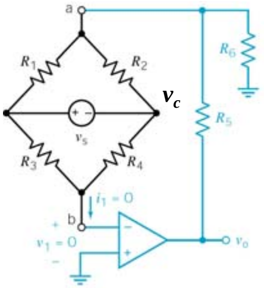
$v_1 \approx v_{in}$가 된다.

따라서, $v_o = -Av_{in}$이고

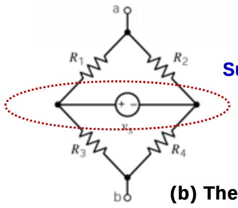
$|v_s| < V_+ / A$ 이어야 하므로

v_{in}는 매우 작아야 **Op amp**가 선형 동작한다.

Bridge Amplifier Circuits (I)



(a) A bridge amplifier, including the bridge circuit



Supernode

(b) The bridge circuit

Virtual short condition

$v_2 = v_1 = v_b = 0,\quad i_1 = 0$

v_c, $v_c + v_s$로 **Node voltage** 정의

Node b 의 KCL

$$\frac{0-(v_c+v_s)}{R_3} + \frac{0-v_c}{R_4} = 0 \qquad (1)$$

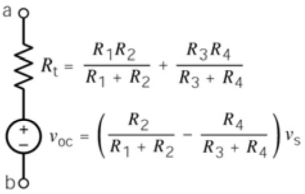
Node a 의 KCL

$$\frac{v_a-(v_c+v_s)}{R_1} + \frac{v_a-v_c}{R_2} + \frac{v_a-v_o}{R_5} + \frac{v_a}{R_6} = 0 \qquad (2)$$

Supernode c, d 의 KCL

$$\frac{v_c-v_a}{R_2} + \frac{v_c-0}{R_4} + \frac{v_c+v_s-v_a}{R_1} + \frac{v_c+v_s-0}{R_3} = 0 \qquad (3)$$

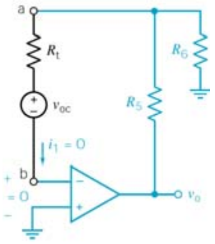
Bridge Amplifier Circuits (II)



$$R_t = \frac{R_1R_2}{R_1+R_2} + \frac{R_3R_4}{R_3+R_4}$$

$$v_{OC} = \left(\frac{R_2}{R_1+R_2} - \frac{R_4}{R_3+R_4}\right)v_s$$

(c) Its Thévenin equivalent circuit



v_c, v_a, v_o가 미지수.

$$v_c\left(\frac{1}{R_3}+\frac{1}{R_4}\right) = -\frac{v_s}{R_3} \qquad (1')$$

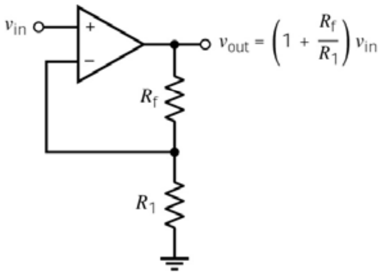
$$\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_5}+\frac{1}{R_6}\right)v_a - \left(\frac{1}{R_1}+\frac{1}{R_2}\right)v_c - \frac{1}{R_5}v_0 = \frac{v_s}{R_1} \qquad (2')$$

$$-\left(\frac{1}{R_1}+\frac{1}{R_2}\right)v_a + \left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+\frac{1}{R_4}\right)v_c = -\left(\frac{1}{R_1}+\frac{1}{R_3}\right)v_s \qquad (3')$$

v_a, v_c를 소거하면 v_o를 구할 수 있다.

(d) The bridge amplifier, including the Thévenin equivalent of the bridge

Noninverting Amplifier



(*b*) Noninverting amplifier

$i_2 \approx 0$ 이므로 R_g 에서의 전압강하 = 0.

따라서, $v_2 \approx v_{in}$이고 $v_1 \approx v_2$이므로

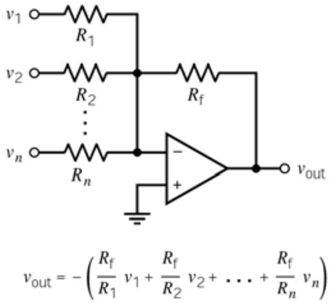
$v_1 = v_{in}$

KCL에서 $$\frac{v_{in} - 0}{R_1} + \frac{v_{in} - v_o}{R_f} = 0$$

$$\frac{v_o}{R_f} = \left(\frac{1}{R_1} + \frac{1}{R_f}\right) v_{in}$$

$$v_o = \left(\frac{R_f}{R_1} + 1\right) v_{in}$$

Summing Amplifier



(*d*) Summing amplifier

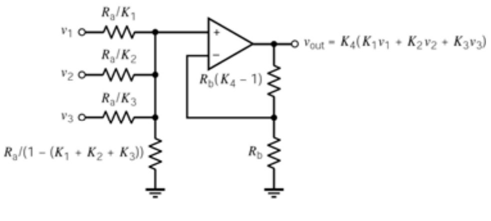
$v_p = v_n = 0$ 이고 **KCL**을 적용.

$$\frac{v_n - v_o}{R_f} + \frac{v_n - v_1}{R_1} + \frac{v_n - v_2}{R_2} + \frac{v_n - v_3}{R_3} = 0$$

$$v_o = \left(-\frac{R_f}{R_1}\right) v_1 + \left(-\frac{R_f}{R_2}\right) v_2 + \left(-\frac{R_f}{R_3}\right) v_3$$

따라서, v_o는 **scale**된 **n**개의 입력 전압의 합이고 부호는 역전되어 있다.

Noninverting Summing Amplifier



(e) Noninverting summing amplifier

$v_p = v_n$ 이고 **KCL을 적용.**

$$\frac{v_n - 0}{R_b} + \frac{v_n - v_0}{(K_4-1)R_b} = 0 \Rightarrow$$

$$\frac{K_4 v_n}{(K_4-1)R_b} = \frac{v_0}{(K_4-1)R_b} \Rightarrow v_n = \frac{v_0}{K_4}$$

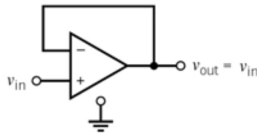
$$\frac{v_n - v_1}{R_a/K_1} + \frac{v_n - v_2}{R_a/K_2} + \frac{v_n - v_3}{R_a/K_3} + \frac{v_n - 0}{R_a/(1-(K_1+K_2+K_3))} = 0 \Rightarrow$$

$$\frac{K_1 v_n}{R_a} + \frac{K_2 v_n}{R_a} + \frac{K_3 v_n}{R_a} + \frac{(1-(K_1+K_2+K_3))v_n}{R_a} = \frac{K_1v_1 + K_2v_2 + K_3v_3}{R_a}$$

$$v_n = K_1v_1 + K_2v_2 + K_3v_3$$

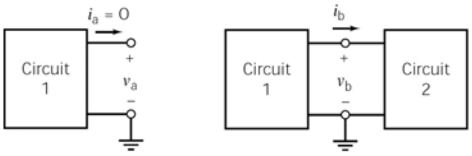
따라서, $v_o = K_4(K_1v_1 + K_2v_2 + K_3v_3)$

Voltage Follower and Loading Effect



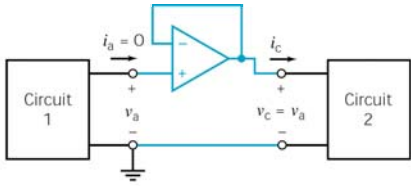
Voltage follower
(buffer amplifier)

$v_- = v_{in} = v_{out}$



(a) Circuit#1 before

(b) After Circuit#2 is connected

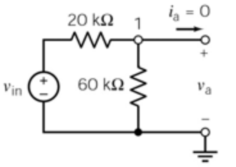


(c) Preventing loading using a voltage follower

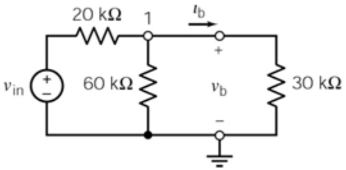
Circuit #1의 출력은 Circuit #2를 연결하는 순간 변하고 만다. 이를 Loading effect라고 한다.

그림**(b)**와 같은 전압은 바뀌게 된다**. Op amp**의 **voltage follower**를 이용하면 출력전압을 그대로 유지할 수 있다**.**

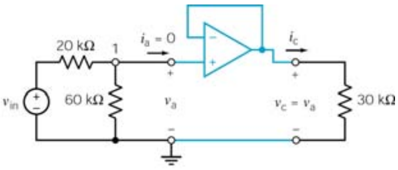
Voltage Follower (Buffer or Isolation Amplifier)



(a) A voltage divider before a 30 kΩ resistor is added



(b) A voltage divider after a 30-kΩ resistor is added



(c) A voltage follower is added to prevent loading

그림 (a)의 경우 $v_a = \frac{60}{20+60} v_{in} = \frac{3}{4} v_{in}$

그림 (b)의 경우.

30 kΩ 의 저항을 연결했으므로

$$v_b = \frac{60//30}{20+60//30} = \frac{1}{2} v_{in}$$

그림 (c)와 같이**voltage follower**를 삽입.

Node a의 KCL

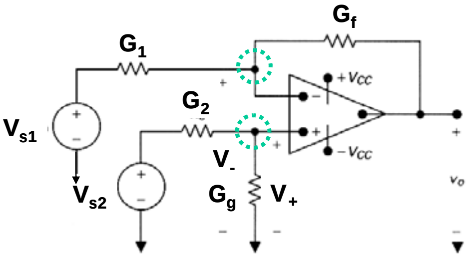
$$\frac{v_a - v_{in}}{20k\Omega} + \frac{v_a - 0}{60k\Omega} = 0 \quad \Rightarrow \left(\frac{1}{20k\Omega} + \frac{1}{60k\Omega}\right) v_a = \frac{v_{in}}{20k\Omega}$$

$$v_a = 3/4\, v_{in}$$

$v_{out} = v_a$ 이므로 $v_{out} = 3/4\, v_{in}$

$i_c = \tfrac{3}{4} v_{in} / 30k\Omega = v_{in} / 40k\Omega$

Difference Amplifier



$i_+ = 0$ 이므로 $G_2(v_+ - v_{s2}) + G_g v_+ = 0$

$i_- = 0$ 이므로 $G_1(v_+ - v_{s1}) + G_f(v_+ - v_o) = 0$

두 식에서

$$v_o = -\frac{G_1}{G_f} v_{s1} + \left(1 + \frac{G_1}{G_f}\right)\left(\frac{G_2}{G_2 + G_g}\right) v_{s2}$$

만약 $G_1 = G_f$ 이고 $G_2 = G_g$ 이면 $v_o = v_{s2} - v_{s1}$

만약 $G_1 = kG_f$ 이고 $G_2 = kG_g$ 이면 $v_o = k(v_{s2} - v_{s1})$

Saturation & the Active Mode

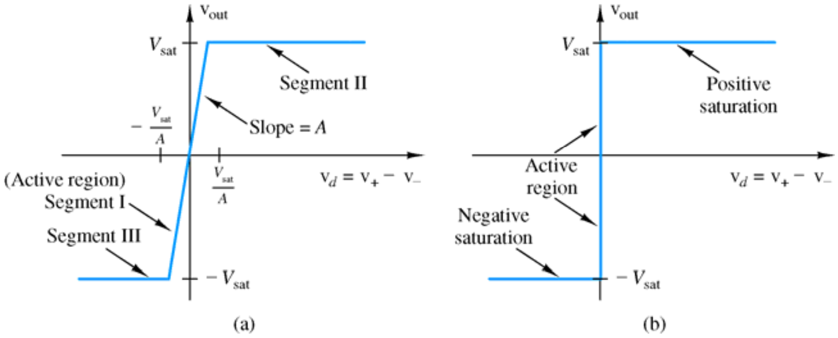


Figure 4.17 Piecewise linear (three-segment) curve for op amp, specifying the active and the positive and negative saturation regions of operation. (a) Finite gain *A*. (b) (Ideal) infinite gain *A*.

$$v_d = v_+ - v_- \neq 0$$

(1) Finite gain : typically 10^4 to 10^6.

(2) Saturation : Output voltage cannot exceed the saturation voltage

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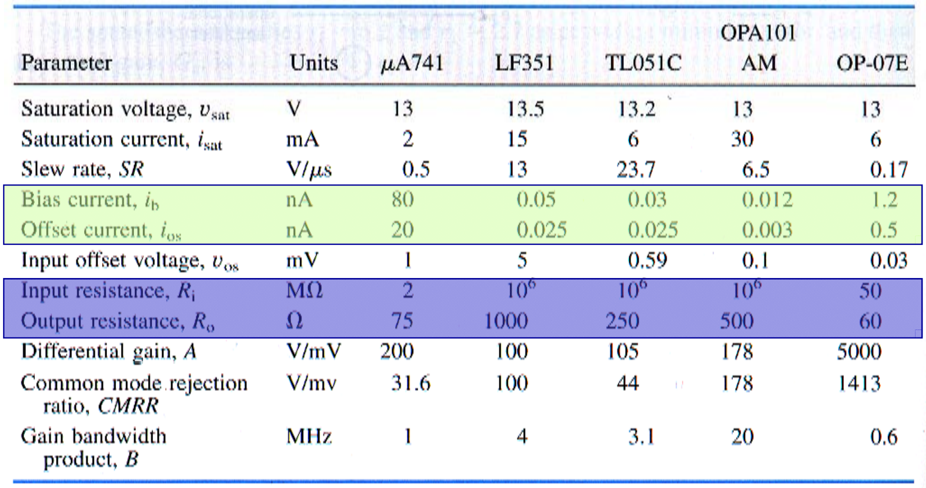
Typical Op-Amp



Parameter	Units	μA741	LF351	TL051C	OPA101 AM	OP-07E
Saturation voltage, v_{sat}	V	13	13.5	13.2	13	13
Saturation current, i_{sat}	mA	2	15	6	30	6
Slew rate, *SR*	V/μs	0.5	13	23.7	6.5	0.17
Bias current, i_b	nA	80	0.05	0.03	0.012	1.2
Offset current, i_{os}	nA	20	0.025	0.025	0.003	0.5
Input offset voltage, v_{os}	mV	1	5	0.59	0.1	0.03
Input resistance, R_i	MΩ	2	10^6	10^6	10^6	50
Output resistance, R_o	Ω	75	1000	250	500	60
Differential gain, *A*	V/mV	200	100	105	178	5000
Common mode rejection ratio, *CMRR*	V/mv	31.6	100	44	178	1413
Gain bandwidth product, *B*	MHz	1	4	3.1	20	0.6

Equivalent Circuit of a 741 Op Amp

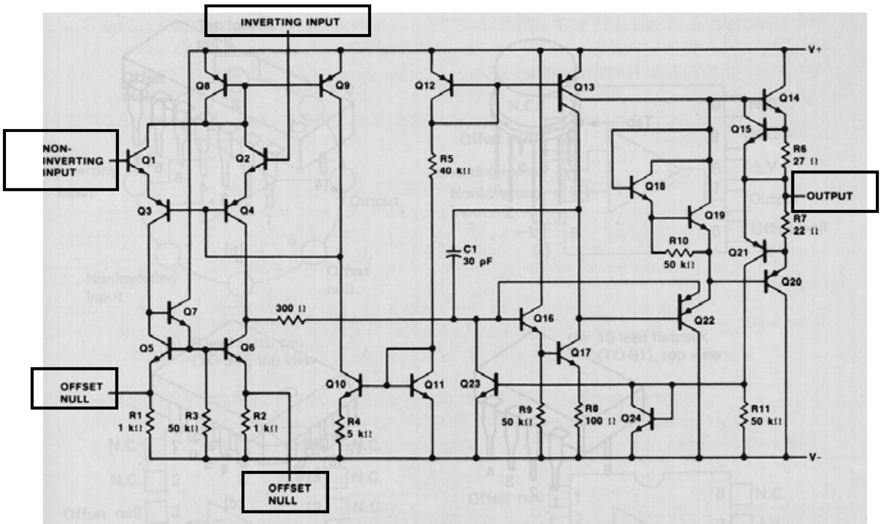
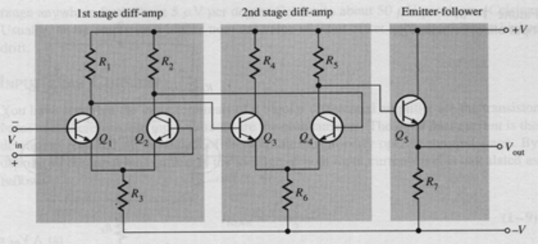
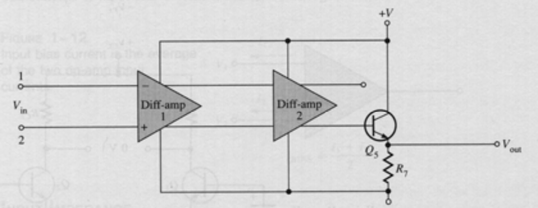


FIGURE 1-2 Equivalent circuit of a 741 op amp. (Courtesy of Fairchild Semiconductor, a Division of Fairchild Camera and Instrument Corporation.)

Simplified Internal Circuitry of a Basic Op Amp



(a) Circuit



(b) Block diagram

FIGURE 1–10
Simplified internal circuitry of a basic op-amp.

Practical Op-Amp

Ideal op amp.

$i_1 = 0,\ i_2 = 0,\ v_1 - v_2 = 0$

Practical op amp.

- **nonzero bias currents** $(i_{b1},\ i_{b2})$
- **nonzero input offset voltage** $(v_{os}$
- **finite input resistance** (R_i)
- **nonzero output resistance** (R_o)
- **finite voltage gain** (A)

$i_1 = i_{b1},\ i_2 = i_{b2},\ v_1 - v_2 = v_{os}$

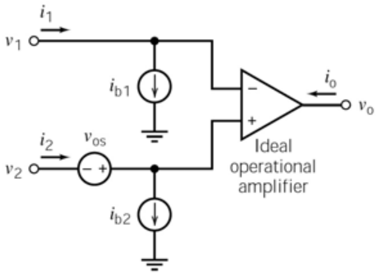
$i_{os} = i_{b1} - i_{b2}$

For μA 741,

$|i_{b1}| \le 500\ \text{nA},\quad |i_{b2}| \le 500\ \text{nA}$

$|i_{b1} - i_{b2}| \le 200\ \text{nA}$

$|v_{os}| \le 5\ \text{mV}$



(b) The offsets model of an operational amplifier

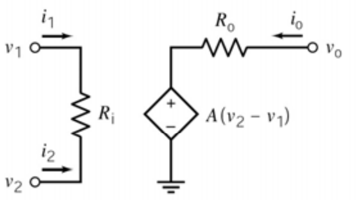
Practical Op-Amp

Ideal op amp.

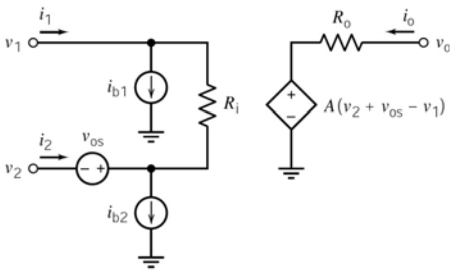
$i_1 = 0,\ i_2 = 0,\ v_1 - v_2 = 0$

Practical op amp.

- **nonzero bias currents** $(i_{b1},\ i_{b2})$
- **nonzero input offset voltage** (v_{os})
- **finite input resistance** (R_i)
- **nonzero output resistance** (R_o)
- **finite voltage gain** (A)

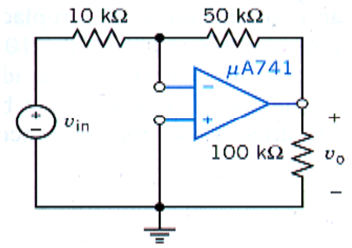


(c) The finite gain model of and operational amplifier

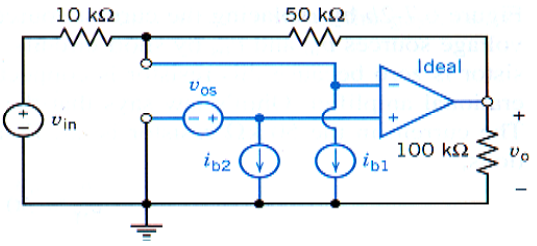


(d) The offsets and finite gain model of an operational amplifier

Realistic Model - Inverting Amp(I)



(a) An inverting amplifier

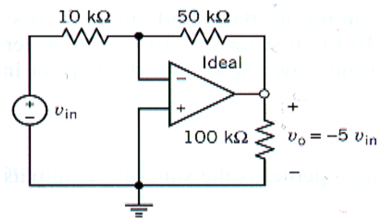


(b) An equivalent circuit that accounts for the input offset voltage and bias currents of the operational amplifier

- **Op amp는 μA 741임.**

- 실제 **Op amp**는 **bias current source** 두 개와 **offset voltage source** 한 개가 **ideal Op amp**에 더해져 있는 것으로 간주 **(**그림 **(b)).**

Realistic Model - Inverting Amp (II)



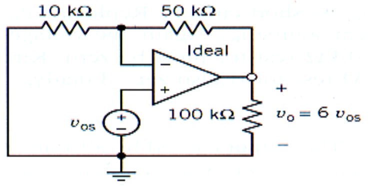
(c) Analysis using superposition

- 그림 **(c)**는 **ideal Op amp.**

$$\frac{0-v_{in}}{10\ \text{k}\Omega}+\frac{0-v_o}{50\ \text{k}\Omega}=0$$

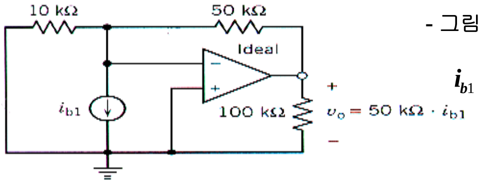
$$v_o=-5v_{in}$$

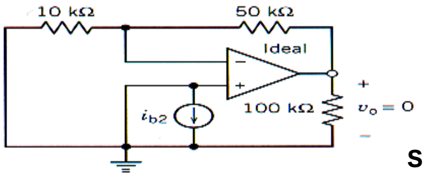
- 그림 **(d) : Offset voltage source**



$$\frac{v_{os}-0}{10\ \text{k}\Omega}+\frac{v_{os}-v_o}{50\ \text{k}\Omega}=0 \quad \Rightarrow \quad v_o=6v_{os}$$

Realistic Model - Inverting Amp (III)





- 그림 (e) : Bias current source, i_{b1}

$$i_{b1} + \frac{0-0}{10\,\mathrm{k\Omega}} + \frac{0-v_o}{50\,\mathrm{k\Omega}} = 0 \quad \Rightarrow \quad v_o = 50\,\mathrm{k\Omega}\cdot i_{b1}$$

- 그림 (f) : Bias current source, i_{b2}

  $i_n = 0$, $v_p = v_n = 0$ 이므로
  10 kΩ 에 흐르는 전류=0 이고
  50 kΩ 에 흐르는 전류=0. $v_0 = 0$

Superposition에 의해서

$$v_o = -5v_{in} + \underbrace{6v_{os} + 50k\Omega\cdot i_{b1}}_{\text{output offset voltage}}$$

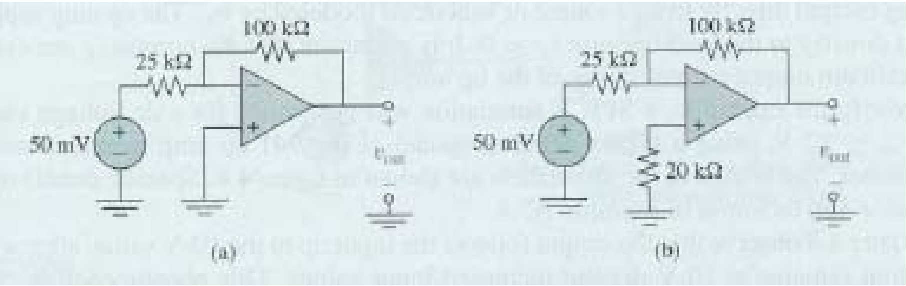
Output offset voltage for μA 741

= $\underbrace{6\times5}_{\text{최대}}$ mV + 50 $\underbrace{\mathrm{k\Omega}\cdot 500}_{\text{최대}}$ nA = 55 mV

$5v_{in}$> 500 mV인 영역에서 offset voltage를 무시.

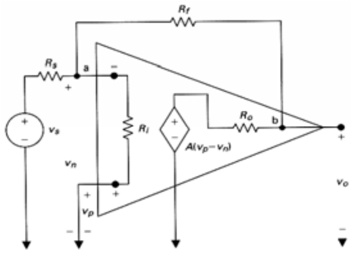
Offset Voltage - Inverting Amp

20 kΩ 의 역할



(a) Bias current 에 의해 offset 전압이 발생.
(b) Offset current에 의해 offset 전압이 발생.
(c) 대개 offset current는 bias current 의 ¼ 정도.

Real Inverting Op-Amp Circuit



$$node\ a:\ \frac{v_n - 0}{R_i} + \frac{v_n - v_s}{R_s} + \frac{v_n - v_o}{R_f} = 0$$

$$node\ b:\ \frac{v_o - v_n}{R_f} + \frac{v_o - A(0 - v_n)}{R_o} = 0$$

$$\frac{1}{R_i} = G_i,\ \frac{1}{R_s} = G_s,\ \frac{1}{R_f} = G_f,\ \frac{1}{R_o} = G_o$$ 라 하면

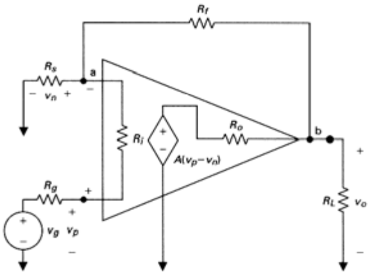
$$(G_i + G_s + G_f)v_n - G_f v_o = G_s v_s$$

$$(AG_o - G_f)v_n + (G_f + G_o)v_o = 0$$

$$v_0 = \frac{D_2}{D} = \frac{-G_s(AG_o - G_f)v_s}{(G_i + G_s + G_f)(G_f + G_o) + G_f(AG_o - G_f)}$$

Ideal op amp의 경우, $A \to \infty$, $G_i \to 0$, $G_o \to \infty$ 이므로 이를 대입하면 앞의 예와 같다. 출력 단에 부하저항 R_L을 연결하면 v_o가 바뀌며 이 값도 **KCL**에 의해서 구할 수 있다.

Real Noninverting Op-Amp Circuit



$$node\ a: G_s v_n + \frac{v_n - v_g}{R_i + R_g} + G_f(v_n - v_o) = 0$$

$$node\ b: G_f(v_o - v_n) + G_o(v_o - A(v_p - v_n)) + G_L v_o = 0$$

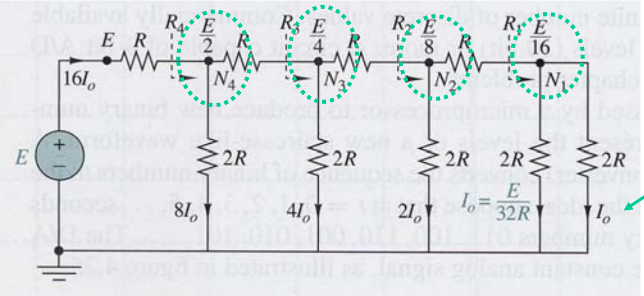
또한 R_i 와 R_g 에 흐르는 전류가 같으므로

$$\frac{v_n - v_g}{R_i + R_g} = \frac{v_p - v_g}{R_g}$$

여기서, v_p, v_n, v_o가 미지수이고 식이 세 개이므로 v_o를 구할 수 있다.

Applications - D/A Converter Building-Weighted Summing Circuit (I)

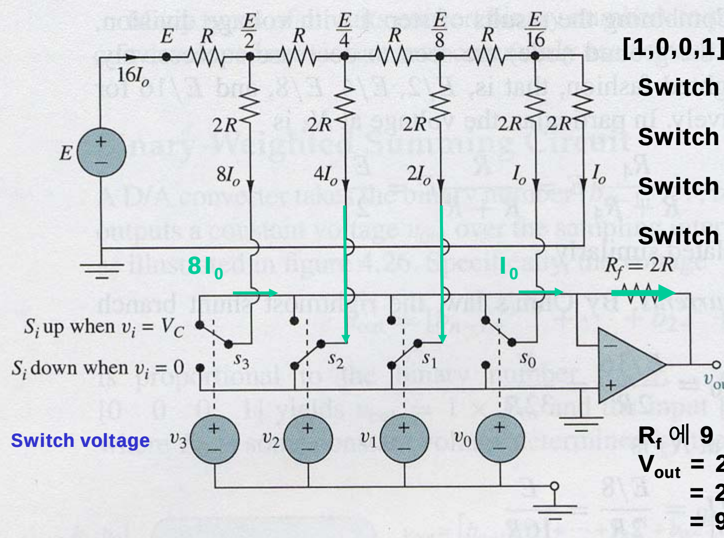
$$[b_{n-1},....,b_0] \longrightarrow \boxed{\text{D/A converter}} \longrightarrow v_{out}=[b_{n-1}2^{n-1}+..+b_1 2^1+b_0]E_0$$



$$I_0=\frac{E}{32R}$$

Node 1 voltage : E/16
Node 2 voltage : E/8
Node 3 voltage : E/4
Node 4 voltage : E/2

Applications - D/A Converter Building-Weighted Summing Circuit (II)



[1,0,0,1]=[b_3,b_2,b_1,b_0]

Switch 0 : up

Switch 1 : down

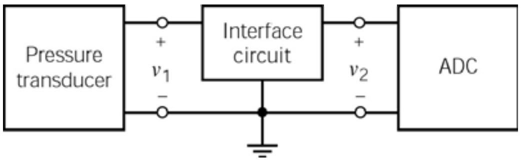
Switch 2 : down

Switch 3 : up

R_f 에 9 I_0가 흐르므로
V_{out} = 2R x 9 I_0
= 2R X 9 E/32R
= 9 E/16

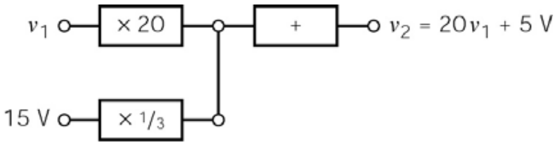
Transducer Interface Circuit (I)

- **Pressure sensor** 의 출력을 **PC**에 입력을 하려면 **ADC (analog-digital converter)**를 이용해야 한다**.**
- **ADC** 는 **0 ~ 10 V** 의 입력을 필요로 하는데 **pressure sensor**의 출력은 **– 250 mV ~ 250 mV** 이다**.**
- 이것을 증폭시켜야 한다**.**

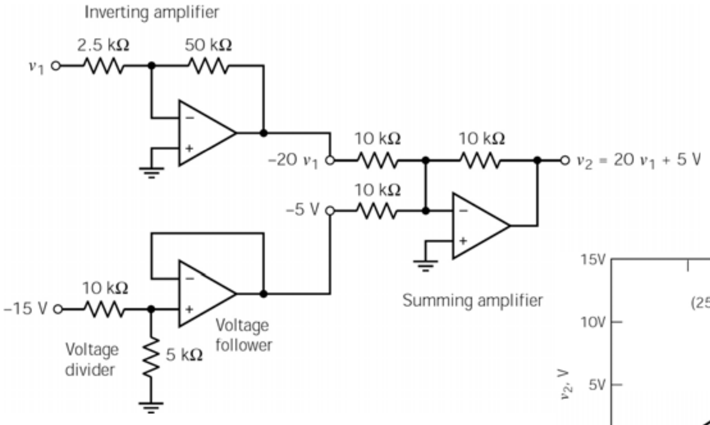


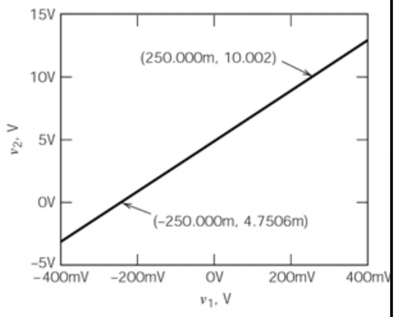
$$-250\ \text{mV} \le v_1 \le 250\ \text{mV}$$
$$0\ \text{V} \le v_2 \le 10\ \text{V}$$

$$v_2 = a \cdot v_1 + b \;\Rightarrow\; v_2 = 20 v_1 + 5 \quad \text{V}$$



Transducer Interface Circuit (II)





- **Inverting amplifier, voltage follower, summing amplifier**를 이용하여 회로를 완성한다**.**