Lecture 11:

RIE of Silicon
- Poly-silicon and Bulk-silicon-

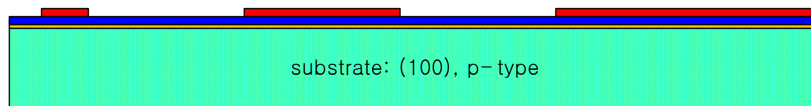
Dong-il "Dan" Cho

School of Electrical Engineering and Computer Science, Seoul National University
Nano/Micro Systems & Controls Laboratory

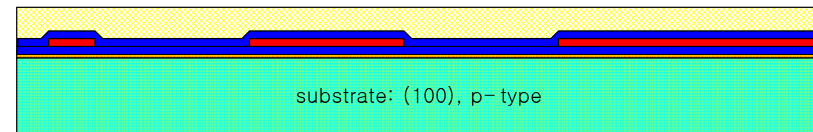
Email: dicho@snu.ac.kr
URL: http://nml.snu.ac.kr

RIE in Thin Film Etching (1)

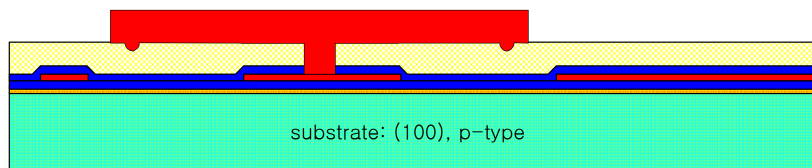
- Thin poly silicon etch in surface micromachining
  - Usually, photo resist is used for etch mask material



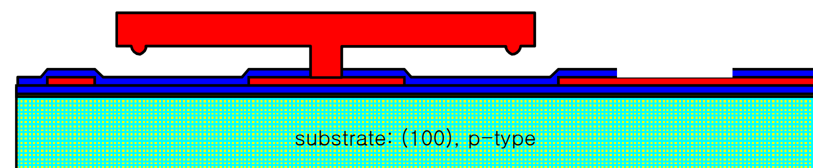
(a) Oxide/nitride deposition, **polysilicon deposition & patterning (RIE is performed)**



(b) Nitride deposition, sacrificial oxide deposition



(c) Anchor patterning, **polysilicon deposition & patterning (RIE is performed)**



(d) Sacrificial wet etch in HF

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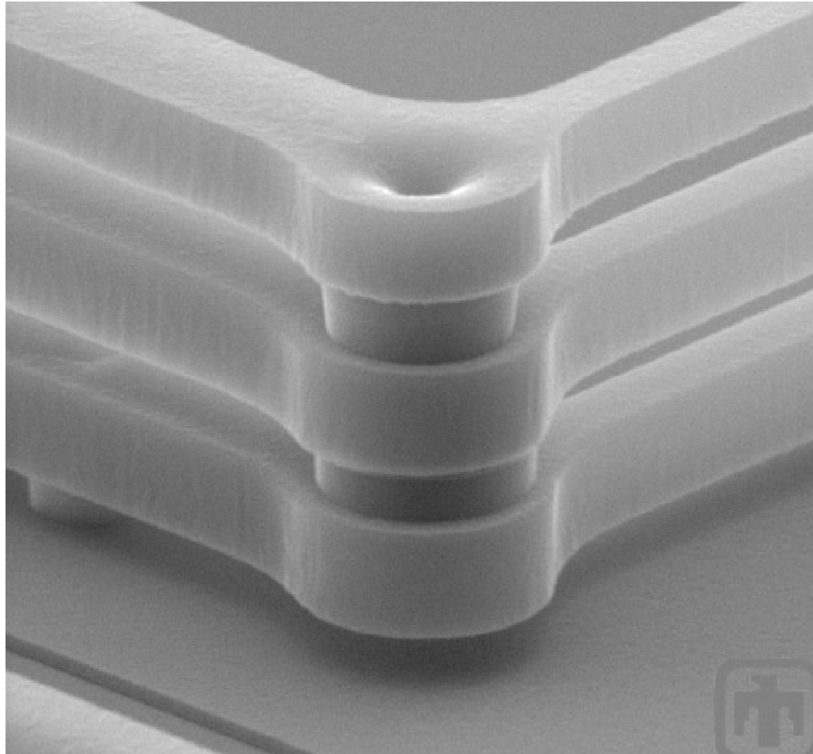
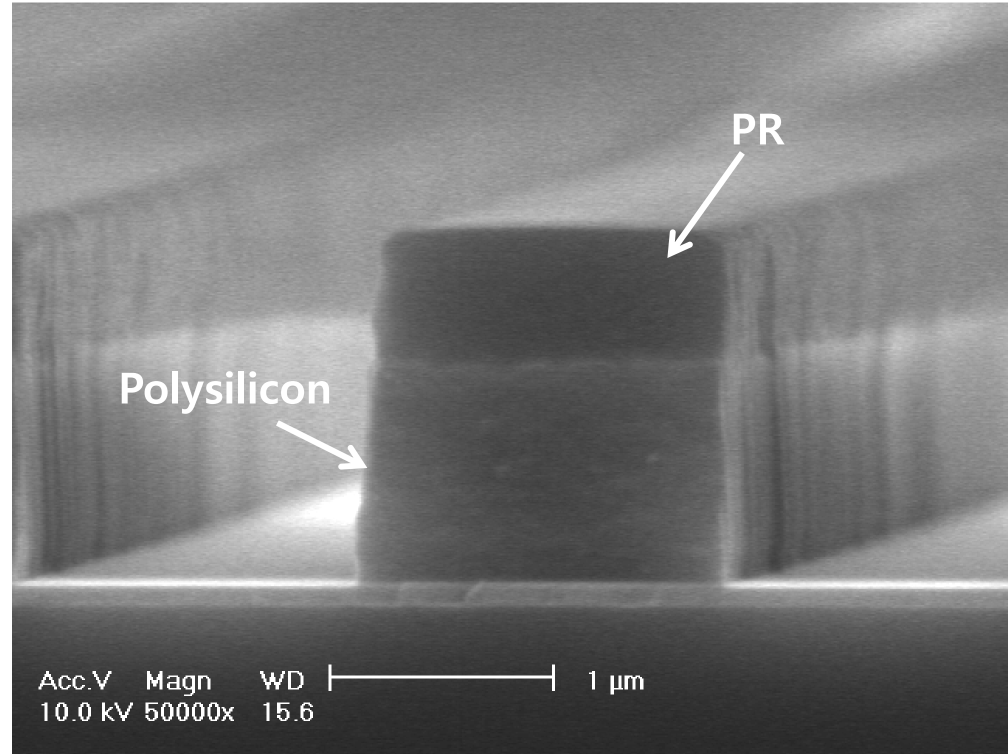
RIE in Thin Film Etching (2)



Detailed view of the multi-level polysilicon that are a critical part of a microengine



Detailed view of polysilicon beam with PR mask after RIE

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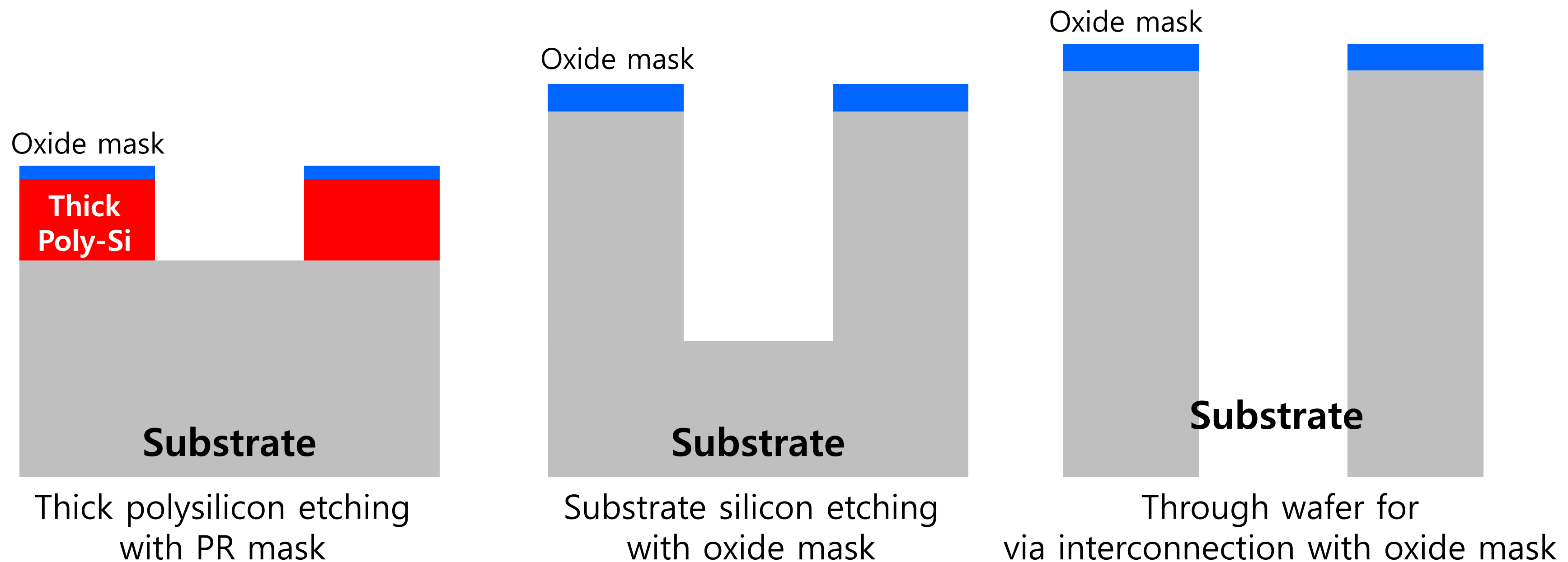
RIE in Bulk Etching (1)

- Thick polysilicon, epipoly silicon, and bulk silicon etch
  - Selectively remove significant amounts of silicon from a substrate
  - Maximum etch thickness is several hundred micro meters.
  - Usually, oxide hard mask and photo resist are used for etch mask material

    (When etch thickness is less then 10 μm, photo resist is used)



Thick polysilicon etching with PR mask | Substrate silicon etching with oxide mask | Through wafer for via interconnection with oxide mask

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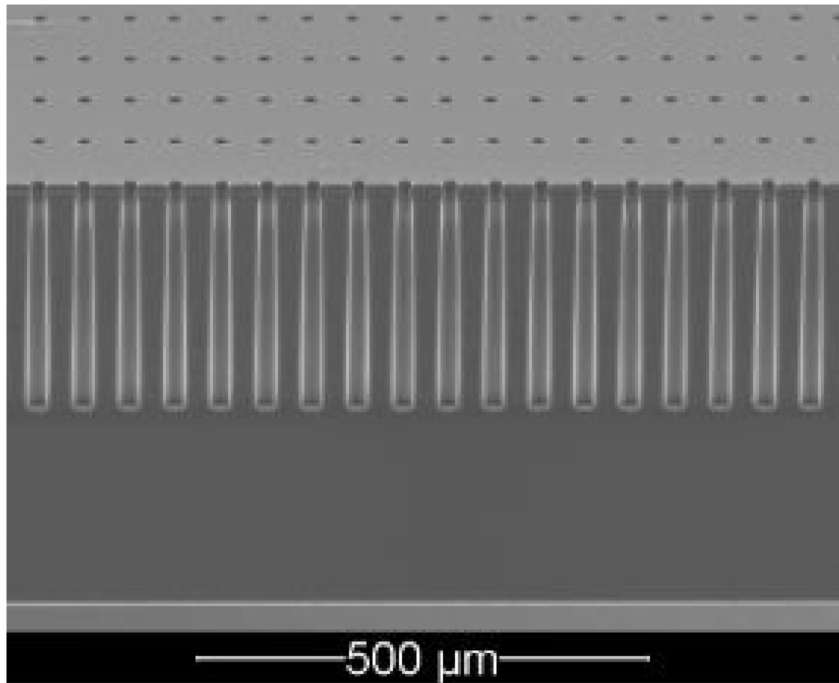
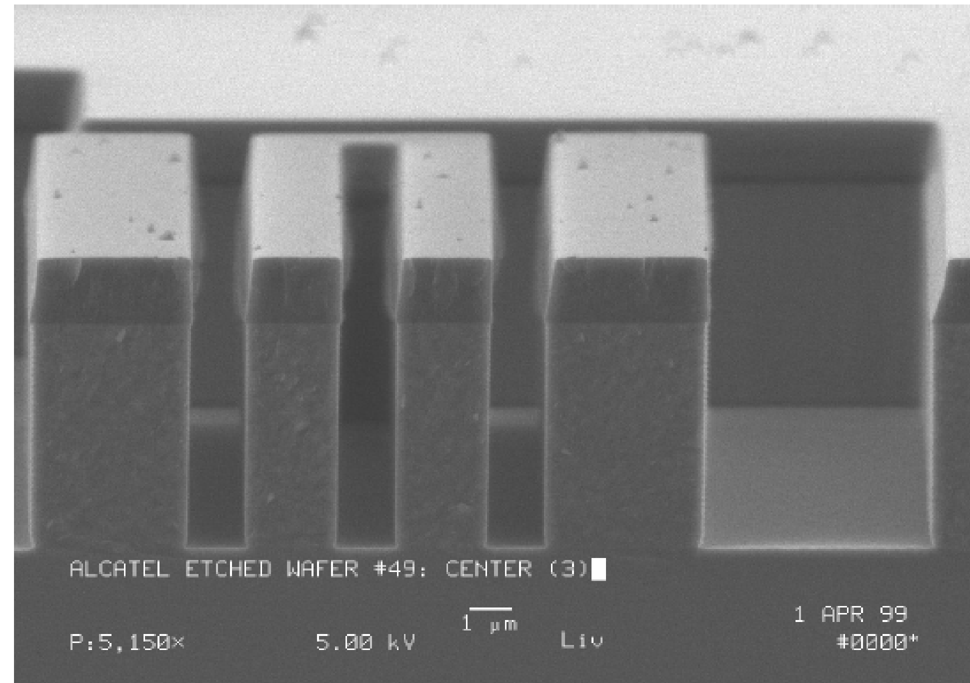
RIE in Bulk Etching(2)



DRIE for through wafer holes
(400 μm deep 50x50 μm^2 holes)



6 μm beam poly etch (before resist strip).

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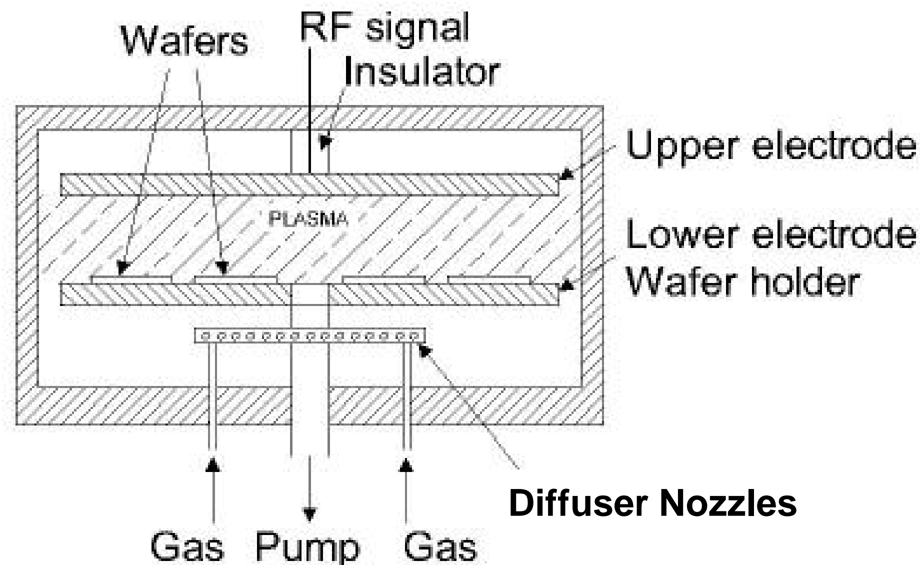
RIE Principles (1)

- RIE: **R**eactive **I**on **E**tching
- Process in which chemical etching is accompanied by ionic bombardment
- Combination of physical and chemical etching
- Faster and simpler etching in a few cases
- Anisotropic etching



Typical parallel-plate reactive ion etching system

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RIE Principles (2)

- Basic steps in a plasma etching process

Plasma

1 Generation of Etchant Species

Gas Flow

2 Diffusion to Surface

Ion Bombardm ent

6 Diffusion into con vection flow

Sheath layer

Boundary layer

3 Adsorption

Byproducts

5 Desorption

4 Reaction

Film

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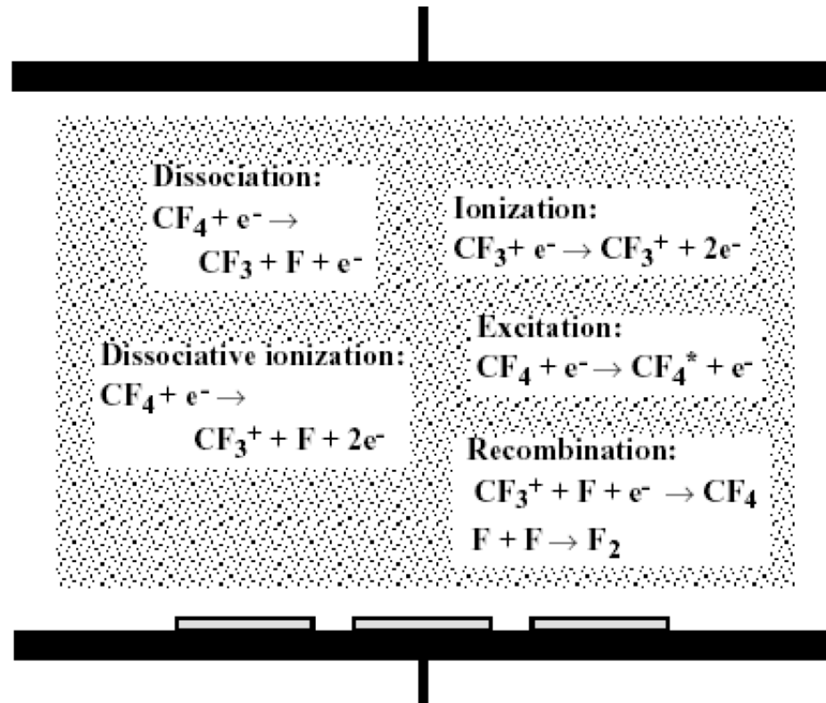
RIE Principles (3)

- Typical reactions and species present in a plasma used for plasma etching
- Typically there are about 10^{15} cm^{-3} neutral species (1 to 10% of which may be free radicals) and 10^{8}- 10^{12} cm^{-3} ions and electrons.



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RIE Principles (4)

	Plasma Etching		Reactive Etching		Physical Etching	
	Barrel Reactor	Planar Reactor	Ion	Ion Beam	Sputtering	Ion Beam Milling
Substrate Location	Surrounded by plasma	On grounded electrode in Plasma	On powered electrode in plasma	In beam, remote from plasma	On powered electrode in plasma	In beam, remote from plasma
Pressure (torr)	$10^{-1} \sim 1$	$10^{-1} \sim 1$	$10^{-2} \sim 10^{-1}$	$10^{-4} \sim 10^{-3}$	$10^{-5} \sim 10^{-3}$	10^{-4}
Ion energy(eV)	0	1 ~ 100	100 ~ 1000	100 ~ 1000	100 ~ 1000	100 ~ 1000
Active Species	Atoms. Radicals	Atoms, radicals, reactive ions	Radicals, reactive ions	Reactive ions	Ar^+ ions	Ar^+ ions
Products	Volatile	Volatile	Volatile	Volatile	Nonvolatile	Nonvolatile
Mechanism	Chemical	Chemical/ Chemical-Physical	Chemical/ Physical	Chemical/ Physical	Physical	Physical
Etch Profile	Isotropic	Isotropic/ Anisotropic	Isotropic/ Anisotropic	Anisotropic	Anisotropic	Anisotropic
Selectivity	30 : 1 – 10 : 1	10 : 1 – 5 : 1	30 : 1 – 5 : 1	10 : 1 – 3 : 1	1 : 1	1 : 1
Resist Compatibility	Excellent	Excellent	Good	Good	Poor	Poor
Device Damage	Little	Little	Some possible	Some possible	Very possible	Very possible
Etch Rate (um/min)	0.1 ~ 0.5	0.1 ~ 0.5	0.05 ~ 0.1	0.05 ~ 0.1	0.02 ~ 0.05	0.02 ~ 0.05
Resolution (um/min)	3	2	1 ~ 2	1 ~ 2	0.5 ~ 1	0.5 ~ 1

Ref: J. D. Lee, "Silicon Integrated Circuit microfabrication technology," 2nd edition

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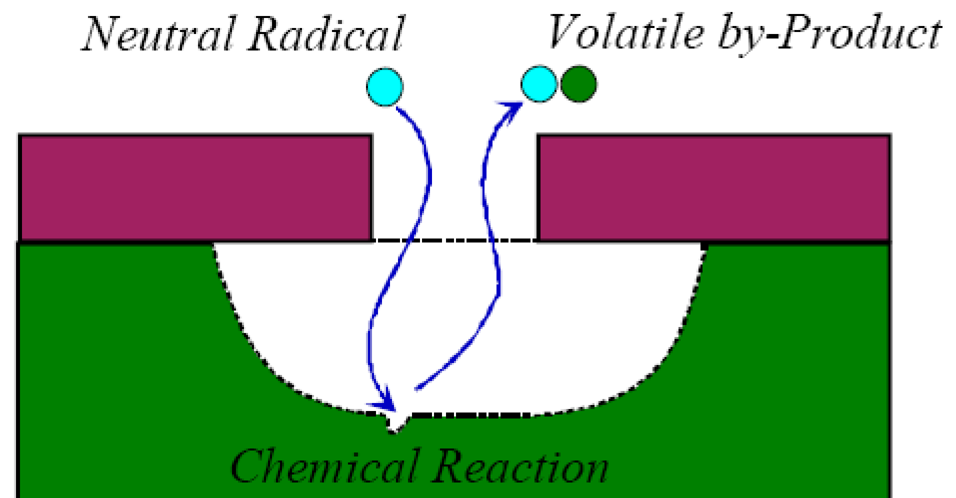
Basic Method of RIE (1)

- Chemical
  - Thermalized neutral radicals chemically combine with substrate material forming volatile products
  - Isotropic
  - Pure Chemical Reaction
  - High Pressure
  - Batch Wafer Type
  - Less Electrical Damage



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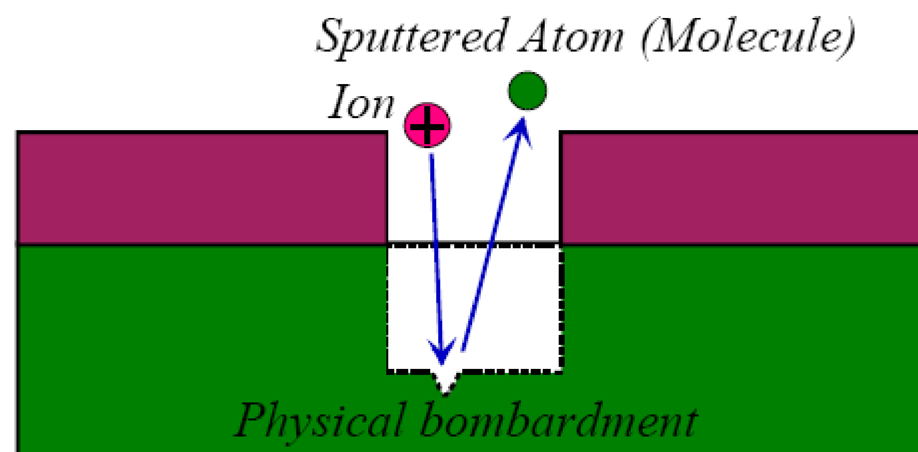
Basic Method of RIE (2)

- Sputtering
  - The ion energy mechanically ejects substrate material
  - Anisotropic
  - By Purely Physical Process
  - High Directionality
  - Low Pressure: long mean free path
  - Single Wafer Type
  - Low Etch rate



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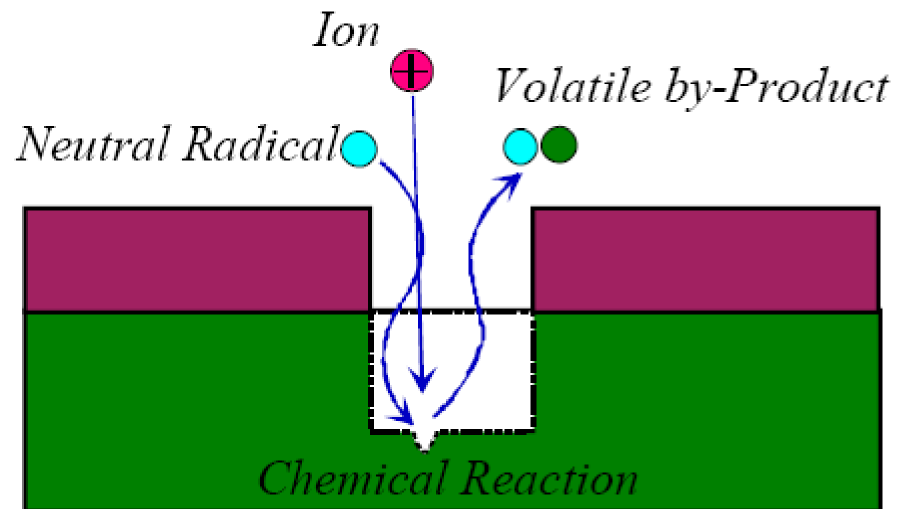
Basic Method of RIE (3)

- Energetic Ion Enhanced
  - Ion bombardment enhances or promotes the reaction between an active species and the substrate material
  - Damage Enhanced Chemical Reactivity
  - Chemical Sputtering
  - Chemically Enhanced
  - Physical Sputtering
  - Ion Reaction



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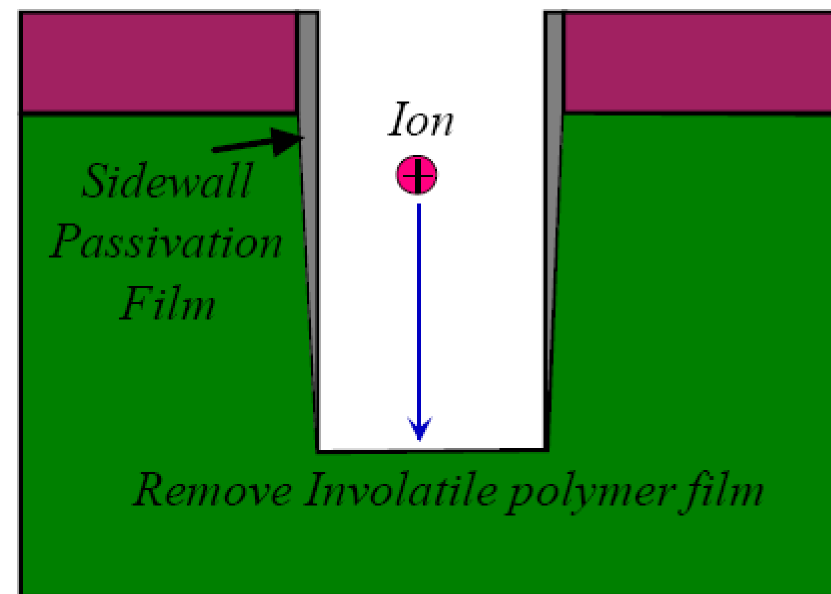
Basic Method of RIE (4)

- Protective Ion Enhanced
  - An inhibitor film coats the surface forming a protective barrier which excludes the neutral etchant
  - Sidewall passivation
  - Stopping lateral attack by neutral radical
  - Ion directionality
  - Involatile polymer film
  - Additive film former
    (N_2 , HBr, BCl_3, CH_3F)



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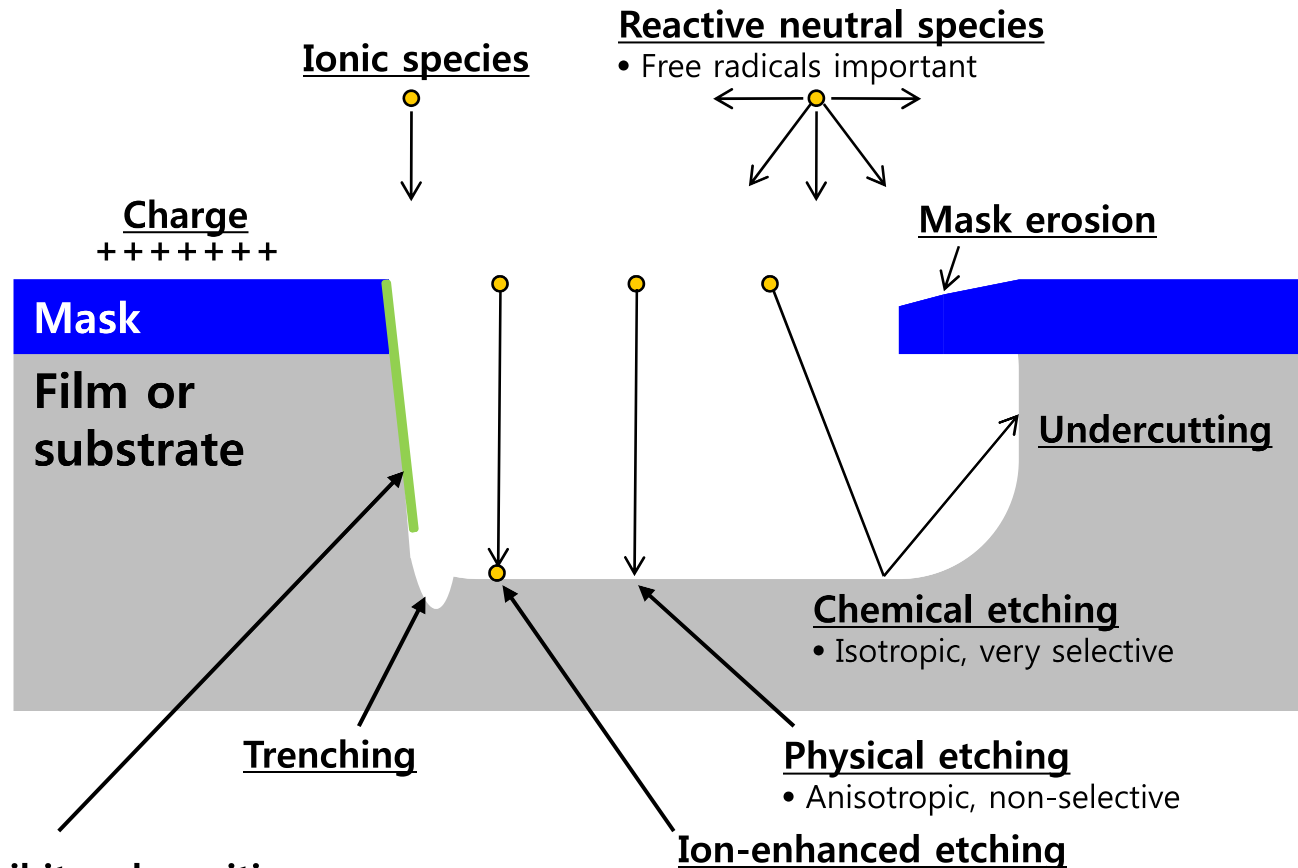
Summary of RIE Mechanisms and Systems



Ion-enhanced etching
- Needs both ions and reactive neutrals
- May be due to enhanced etch reaction or removal of etch by product or inhibitor
- Anisotropic, selective

Sidewall-inhibitor deposition
- Sources: etch byproducts, mask erosion, inlet gases
- Removed on horizontal surfaces by ion bombardment
- A possible mechanism in ion enhanced etching

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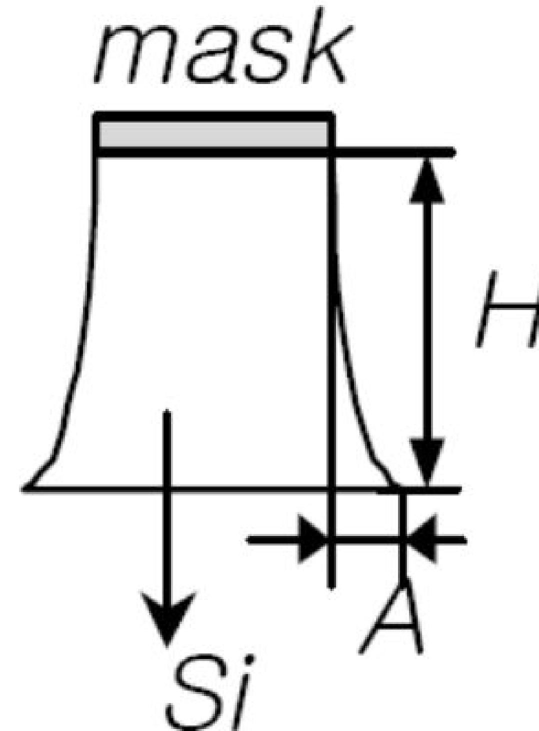
Characterization of RIE Performance

- Etch performance valuation
  - Etch rate
  - Anisotropy (define as 1-A/H)
  - Selectivity to mask material
  - Micro-loading effect (RIE lag)
  - Macro-loading effect
    (dark field or bright field)
  - Etch uniformity
  - Surface quality



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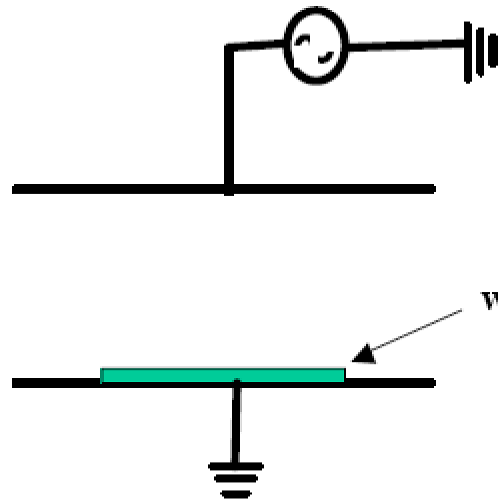
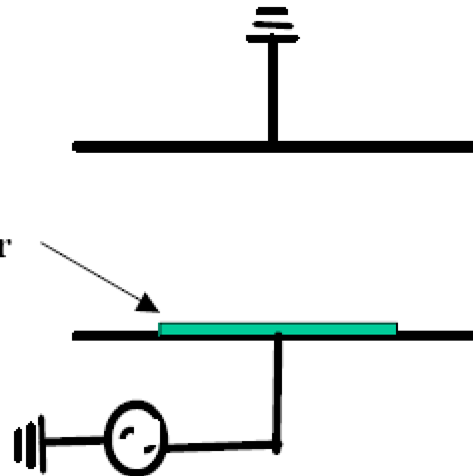
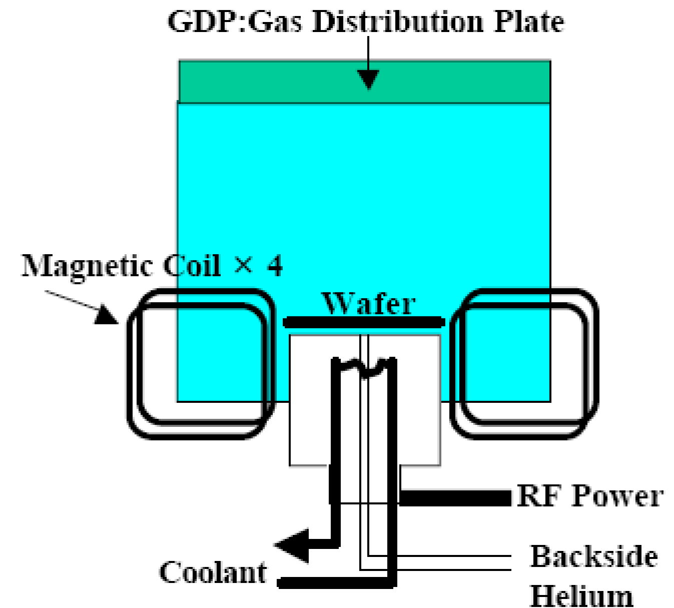
Plasma Etch & RIE & MERIE







Plasma Etch
- Plasma Sheath Potential: low
- Ion Bombardment: weak
- Chemical Reaction: dominant
- Etch Selectivity: high
  → Isotropic Etching

Conventional RIE
- Plasma Sheath Potential : high
- Strong Ion Bombardment plus Chemical Reaction
  → high etch rate
  → Anisotropic Etching

MERIE
(Magnetically Enhanced RIE)
- Magnetic Field Parallel to Cathode
- Secondary Electron confined near Cathode
  → increasing ionization
  → higher etch rate

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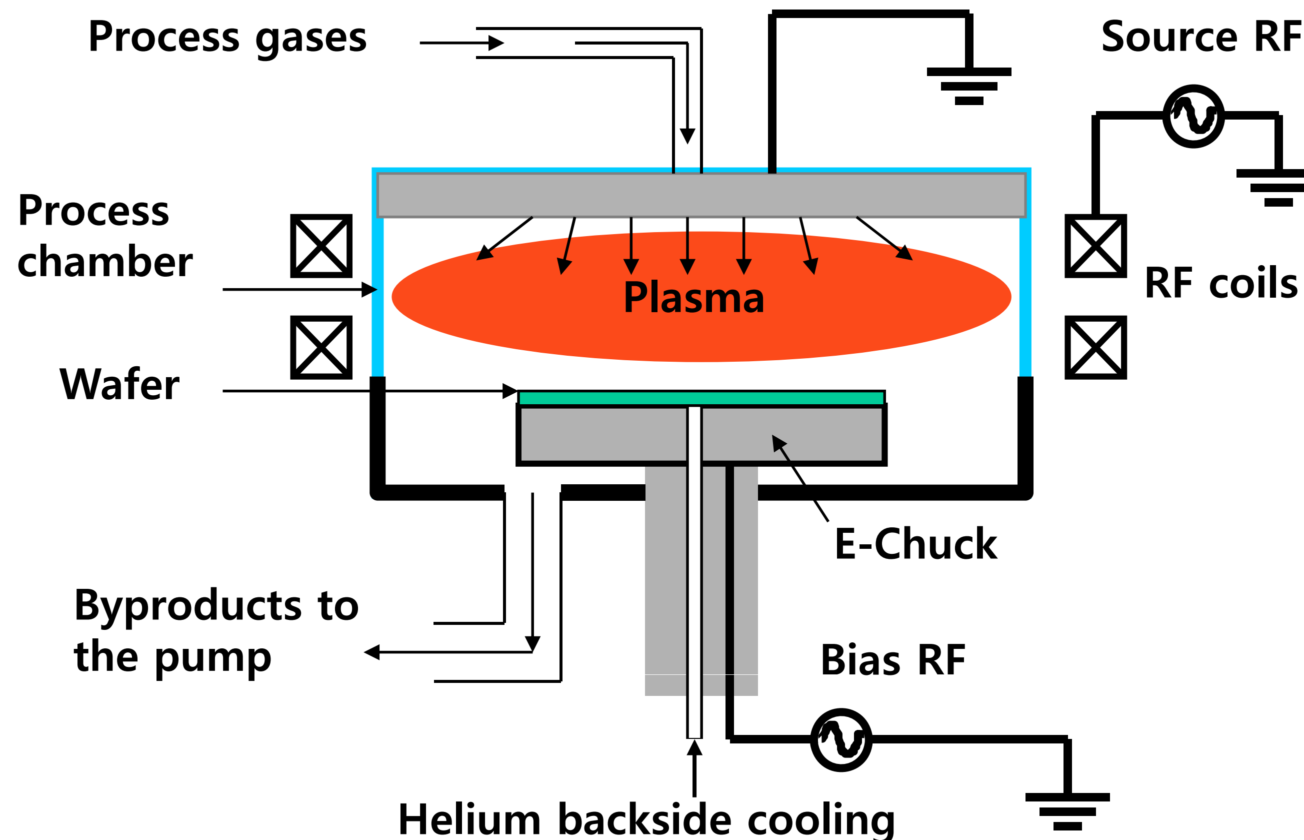
Schematic of ICP(Inductively Coupled Plasma)



- Low pressure(< 5 mTorr) and low temperature(-50°C ~+50°C) etching
- Independent power control and high density plasma (~ 10^{12})
- Improved Plasma Uniformity

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Mask Materials for RIE

- Etch mask
  - PR (Photo Resist), Hard mask (SiO_2, Al) is used
  - Selectivity
    = etch rate of etching material / etch rate of mask
  - Usually, standard PR (for CMOS) is not adequate for O_2 plasma etch → hard mask required

  - Selectivity of silicon:AZ1512
    - Cl based etch (physical etch): <2
    - F based etch (chemical etch): < 10
      (if O_2 gas is inserted the chamber the selectivity would be lower than 10)

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Reaction in RIE Process (1)

- Reactants
  - Cl-based (Cl_2, BCl_3)
    - Sputtering or ion-enhanced etch mechanism
    - High anisotropy
    - Low selectivity
  - F-based(SF_6)
    - Chemical etch mechanism
    - High selectivity
    - High etch rate
    - Isotropic etching
  - Br-based (HBr, Br_2)
    - Good anisotropy
    - Sidewall passivation: SiBrx ($x<4$)
    - Good selectivity to oxide

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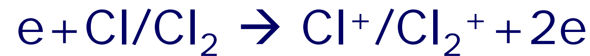
Reaction in RIE Process (2)

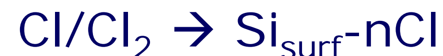
- An example of RIE mechanisms (Cl based)

Ion and electron formation

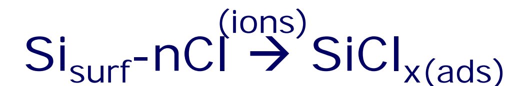


Etchant formation

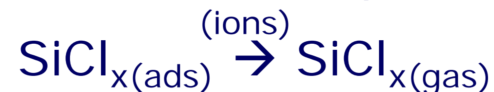
Adsorption of etchant on the substrate



Reaction on surface



Product desorption



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Reaction in RIE Process (3)

- An example of RIE mechanisms (F based Si etch)

F

F Si
SiFx
Si

Si

F
F F
F Si F
Si Si

a

b

F F
Si

F F F
Si Si

F F
F F Si F
Si Si

(I)

F
F F
Si F
Si

F F
F Si F
Si

(II)

F
F F
F Si F
Si

SiF4
F
Si

(III)

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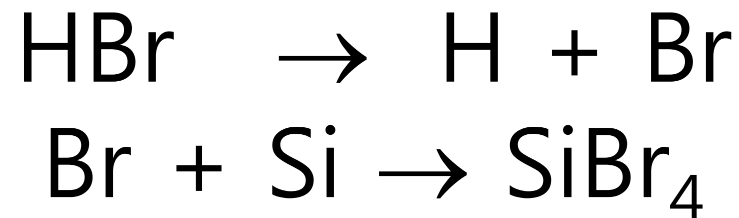
Reaction in RIE Process (4)

- An example of RIE mechanisms (Br based Si etch)



  - Small amount O_2 for sidewall passivation
  - A little NF_3 for preventing black silicon
  - Endpoint by time

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CCP: BCl_3 Recipe and Example (1)

- System: Drytek DRIE-284
- Process parameter

		Step 1	Step 2	Step 3
Power		200 W	300 W	475 W
Pressure		20 mTorr	20 mTorr	40 mTorr
Time		1 min	1 min	10 min
Gas	Cl_2	0 sccm	2 sccm	50 sccm
	BCl_3	14 sccm	14 sccm	5 sccm
	N_2	7 sccm	7 sccm	0 sccm

- Etch rate: 850 nm/min
- Selectivity: 8.5:1 for oxide hard mask

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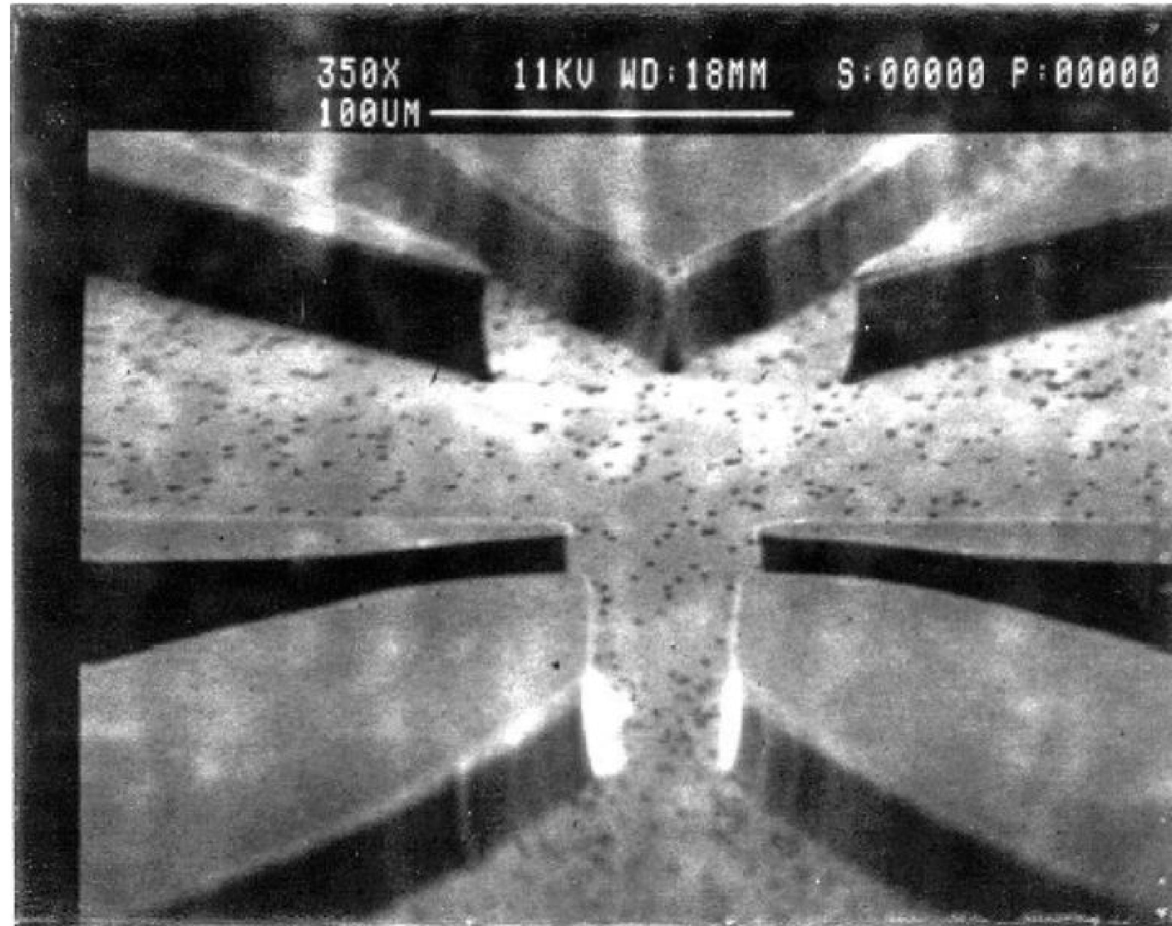
CCP: BCl_3 Recipe and Example (2)

- Fabrication example (proportional amplifier)



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CCP: SF_6 Recipe and Example (1)

- System: Drytek DRIE-284
- Process parameter

Power	150 W
Pressure	150 mTorr
SF_6	30 sccm
O_2	10 sccm

- Etch rate: 4.2 um/min
- Selectivity: 14.2:1 for oxide hard mask

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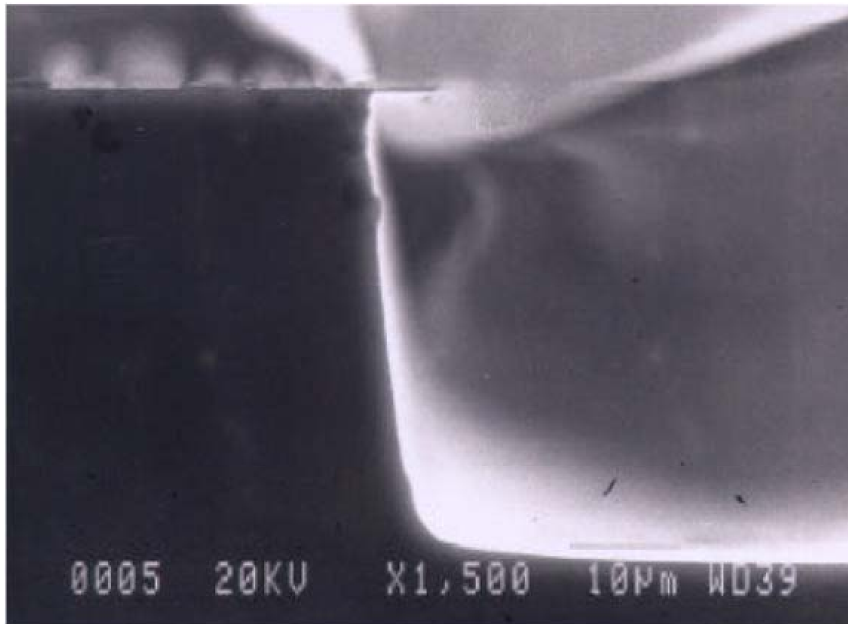
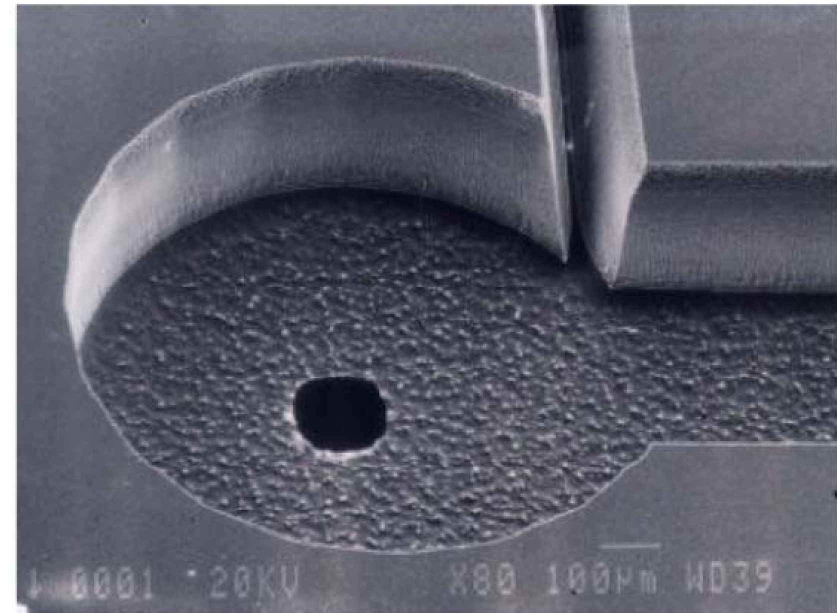
CCP: SF_6 Recipe and Example (2)

- Fabrication example (vortex amplifier)





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CCP: Poly-Si Etch Test (1)

- System: Drytek DRIE-284

- Process parameter

Power	300 W
Pressure	75~250 mTorr
Cl_2	58 sccm
He_2	100 sccm

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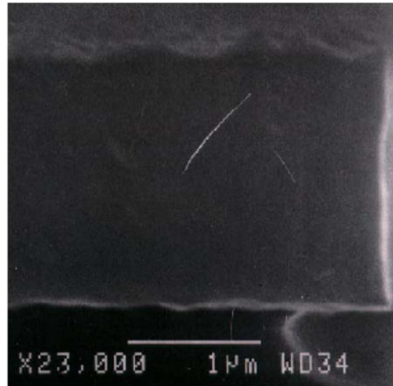
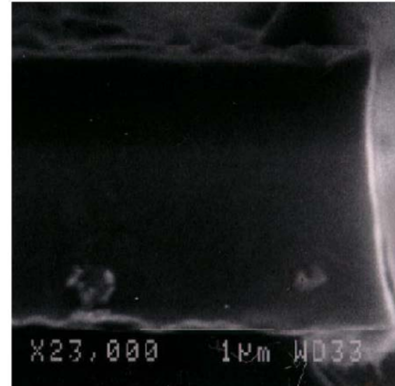
CCP: Poly-Si Etch Test (2)

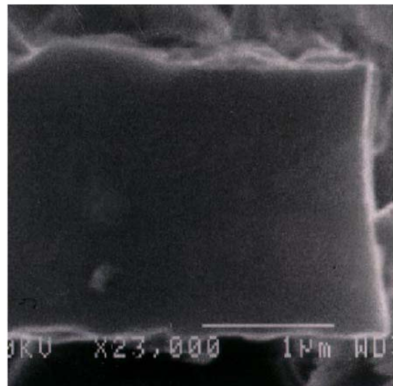
- Test results



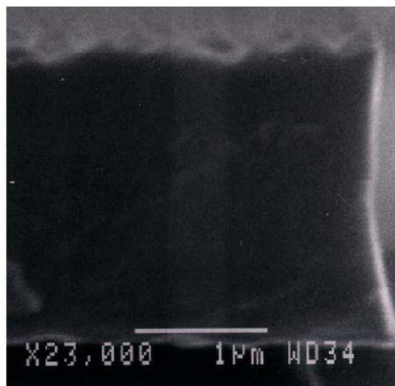
100 mTorr



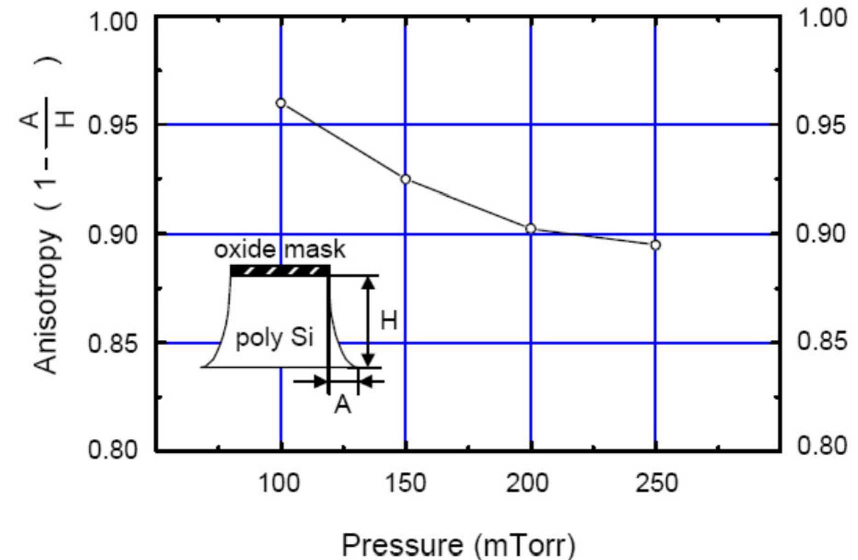
150 mTorr



200 mTorr



250 mTorr



Etch anisotropy as a function of pressure

Ref: S. Lee, et. al., *IOP JMM*, vol. 8, pp. 330-337, 1998.

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ICP: Poly-Si Etch Recipe of ISRC (1)

- System: STS ICP poly Etcher
- Process parameter (Br based etch)

		Step 1 (native oxide etch)	Step 2 (poly-Si etch)
Power	Coil	600 W	900 W
	Platen	100 W	50 W
Pressure		2 mTorr	2 mTorr
Time		15 sec	60 sec
Temperature		20 ^{O}C	20 ^{O}C
Gas	Cl_2	20 sccm	0 sccm
	HBr	0 sccm	20 sccm
	O_2	0 sccm	1 sccm

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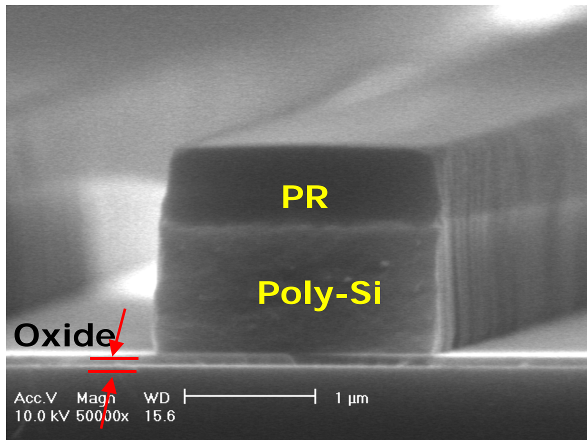
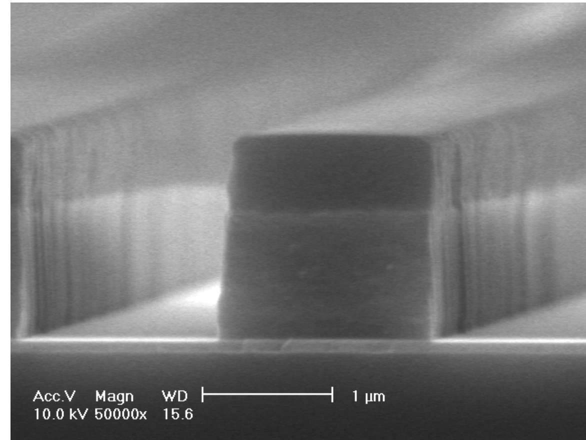
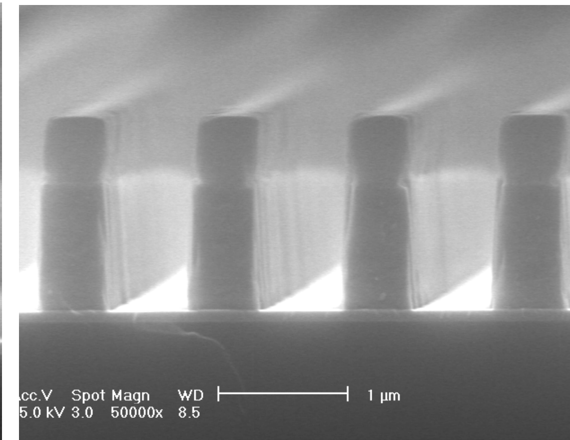
ICP: Poly-Si Etch Recipe of ISRC (2)



Line width: 2 um



Line width: 1.5 um



Line width: 0.55 um

- Etch rate of poly-Si: 0.3 um/min
- Selectivity to PR: 3:1
- Selectivity to oxide: 100:1
- Etch profile: 88 $^{\circ}$ to 90 $^{\circ}$

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ICP RIE System in ISRC (1)

- STS ICP poly Etcher (in CMOS area)
  - Plasma source type: ICP (inductively coupled plasma)
  - Main feed gas :HBr, Cl_2, Ar, SF_6, O_2, He_4
  - Main power: 13.56 MHz – 1000 W
  - Bias power: 13.56 MHz - 30/300 W

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ICP RIE System in ISRC (2)

- STS ICP poly etcher for MEMS
  - Plasma source type: ICP (inductively coupled plasma)
  - Pump
    - Dry pump : Edwards iH80 800 ℓ/m
    - Turbo pump Leybold MAG 1500 CT 1000 ℓ/sec
  - RF generator
    - ENI ACG-10B 1000 W, 13.56 MHz
    - ENI ACG-3B 300 W, 13.56 MHz
  - Gas
    - HBr – 50 sccm
    - Cl2 – 20 sccm
    - O2 – 20 sccm
    - Ar – 50 sccm

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Various Gas for Poly-Si Etching

Gas	Reactor Type	Pressure (torr)	Etch Rate (μm/min)	Etch Selectivity	Comments
CCl_4/Argon	Planar	.4	.02(Undoped)	Poly Si : SiO_2 15:1	-
SiF_4(50%)/ Argon(50%)	Planar	.2	.4(Undoped)	Poly Si : SiO_2 25:1	-
CF_4/O_2	Barrel	.2	.05 ~ .1(Undoped)	Poly Si : Si_3N_4 : SiO_2 25 : 2.5: 1	-
CF_4/O_2(4%)	Planar	.4	.057(Phos doped)	Poly Si : SiO_2 10:1	-
C_2ClF_3	Planar	.225	.05(Phos doped)	Poly Si : SiO_2 3.5 :1	-
CF_4(92%)/O_2(8%)	Planar	.35	.115(Phos doped) .105(Phos doped)	Poly Si : SiO_2 10:1 Poly Si : SiO_2 9:1	Isotropic
C_2F_4(50%)/ CF_3Cl(50%)	Planar	.4	.159(Phos doped) .098(Undoped)	Poly Si : SiO_2 8:1 Poly Si : SiO_2 5:1	Isotropic
C_2F_4(81%)/ CF_3Cl(19%)	Planar	.4	.082(Phos doped) .070(Undoped)	Poly Si : SiO_2 5:1 Poly Si : SiO_2 4:1	Anisotropic
C_2F_4(92%)/ Cl_2(8%)	Planar	.35	.057(Phos doped) .050(Undoped)	Poly Si : SiO_2 6:1 Poly Si : SiO_2 5:1	Anisotropic
CF_3Cl	Planar	.35	.08(Phos doped) .03(Undoped)	Poly Si : SiO_2 13:1 Poly Si : SiO_2 6:1	Intermediate between Isotropic and Anisotropic

Ref: J. D. Lee, "Silicon Integrated Circuit microfabrication technology," 2nd edition

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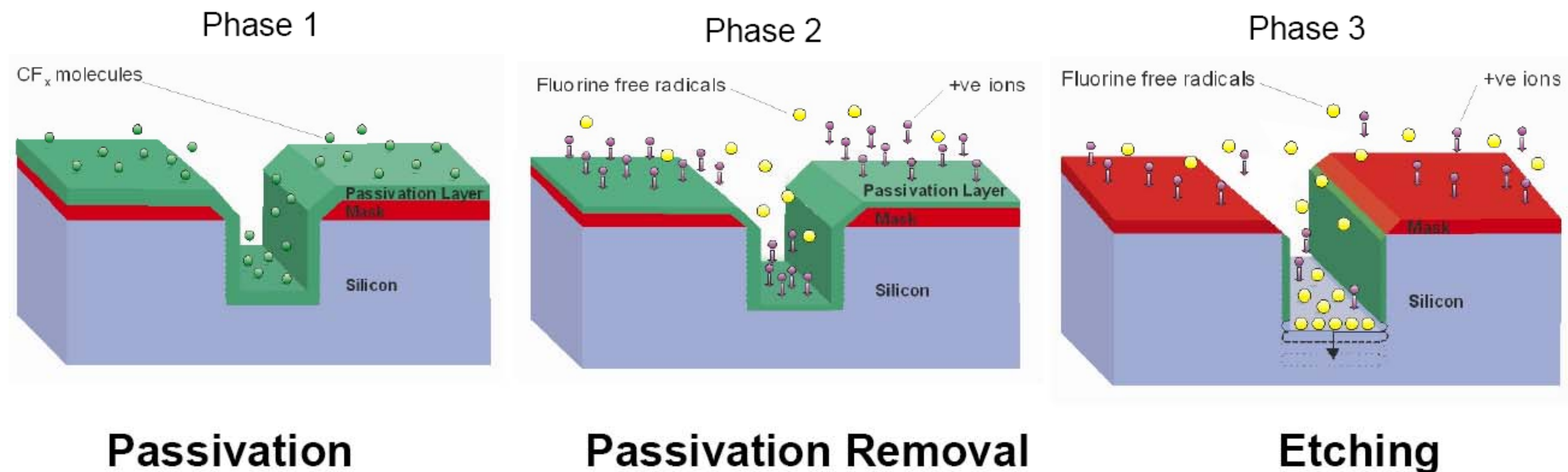
Deep Reactive Ion Etching (1)

- Uses high density plasma to alternatively etch silicon and deposit etch resistant polymer on sidewall
  - Unconstrained geometry 90° side walls
  - High aspect ratio 1:30
  - Easily masked (PR, SiO_2)
- Bosch process: sidewall passivation → etch → sidewall passivation → etch …



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Deep Reactive Ion Etching (2)

- Characteristics of the Deep RIE process
  - SF_6 flow: 30 ~ 150 sccm
  - C_4F_8 flow: 20 ~ 100 sccm
  - Etch cycle: 5 ~ 15 sec
  - Deposition cycle: 5 ~ 12 sec
  - Pressure: 0.25 ~ 10 Pa
  - Temperature: 20 ~ 80 ^{O}C
  - Etch rate: 1.5 ~ 4 um/min
  - Selectivity to resist mask: more than 75:1
  - Selectivity to oxide mask: more than 150:1
  - Sidewall angle: 90° ±2
  - Etch depth capability: up to 500 um

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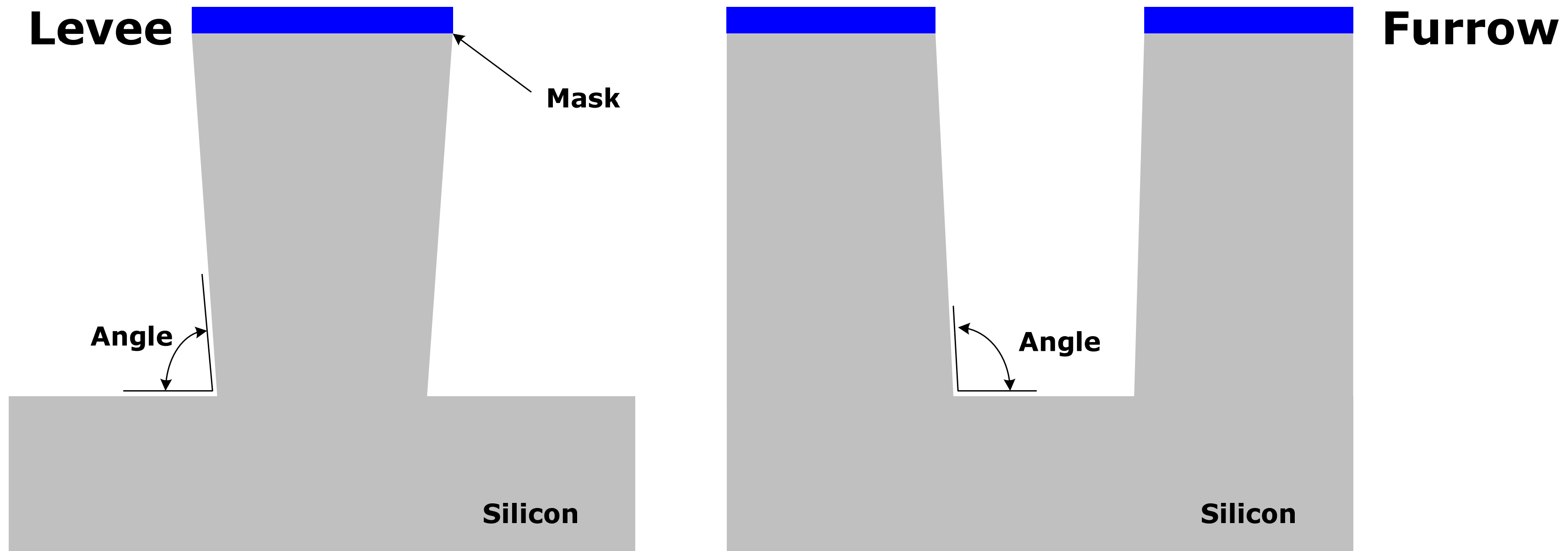
Deep Reactive Ion Etching (3)

- Fence (levee) structure and trench (furrow) structure have different etch side wall profile



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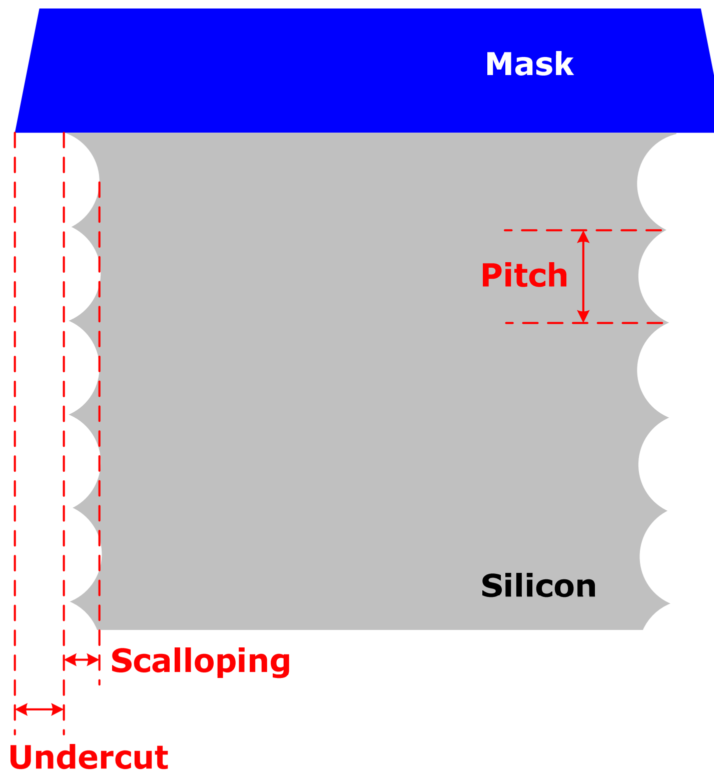
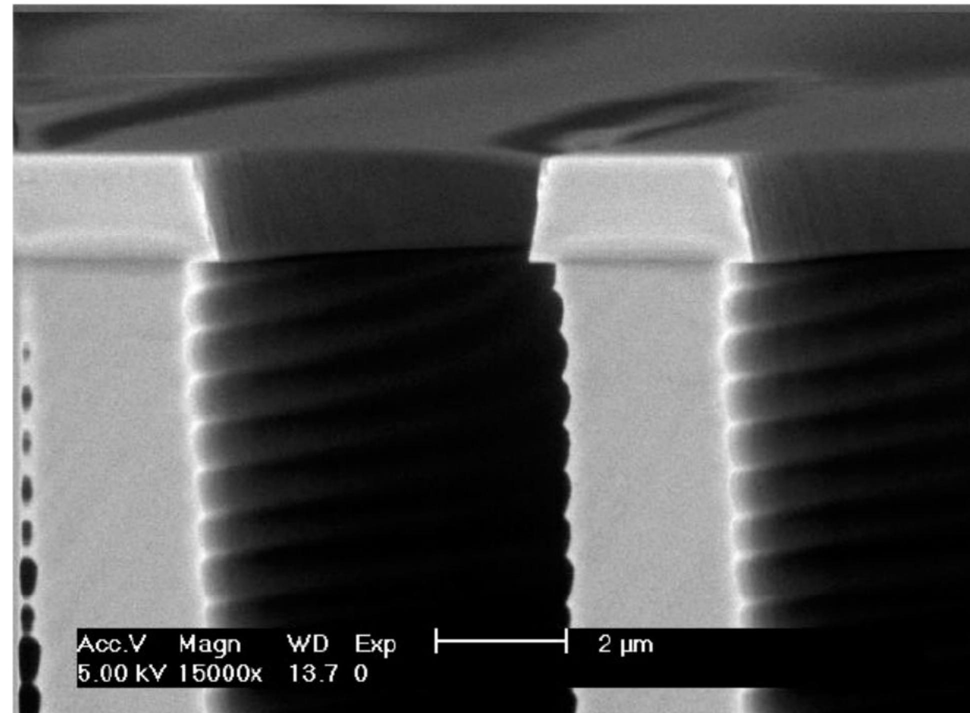
Deep Reactive Ion Etching (4)

- Characteristics of Bosch process
  - Scalloping
  - Under cut





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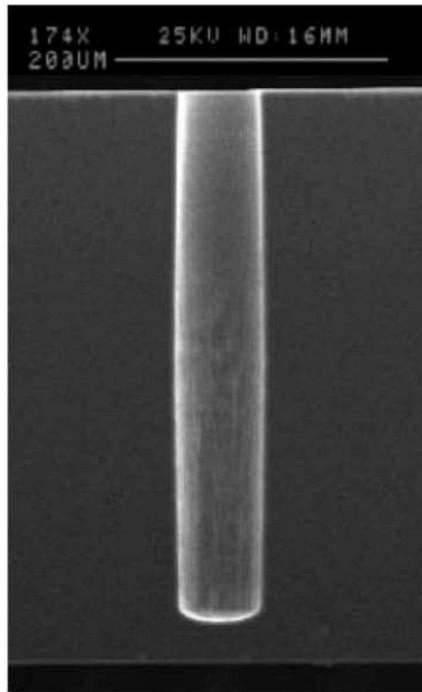
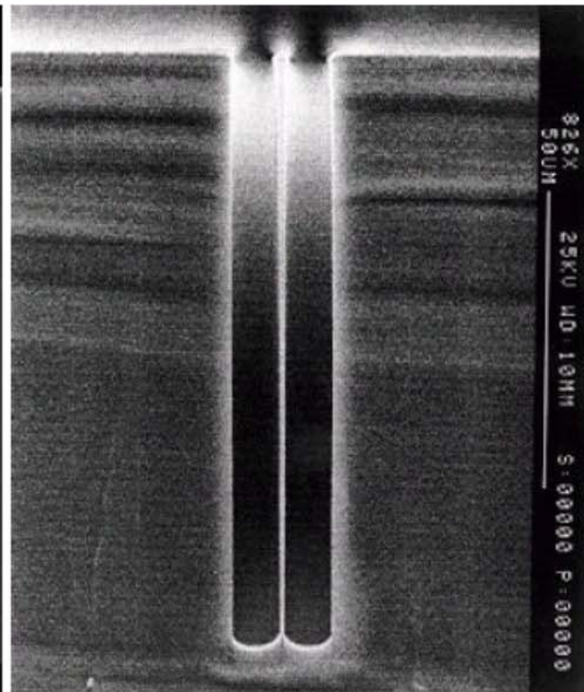
Deep RIE Example (1)

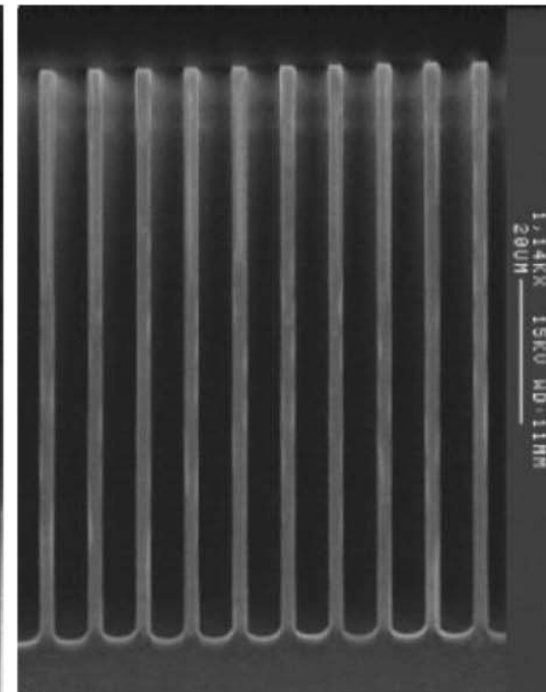
- Fabrication example (deep trench)



350μm-depth



100μm-depth



80μm-depth, 4.5μm space width, 2μm line width

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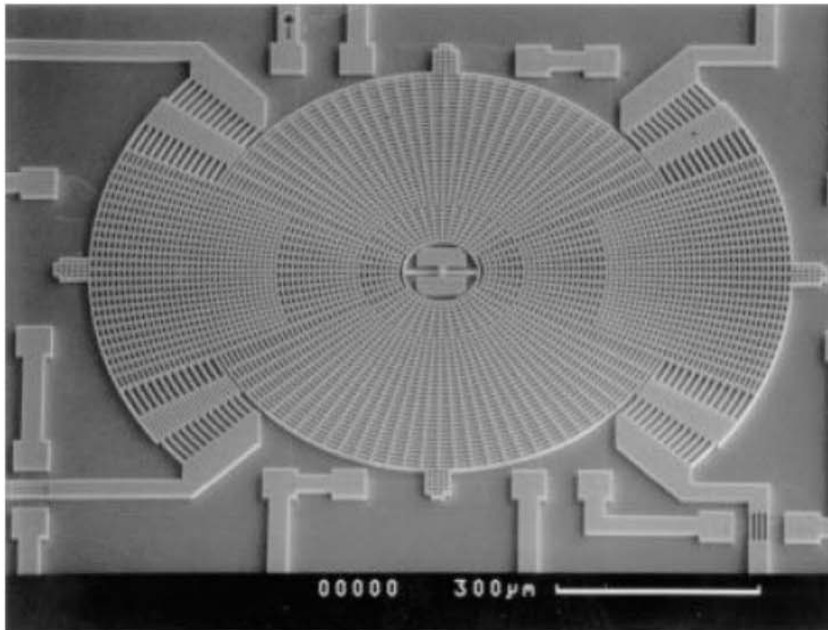
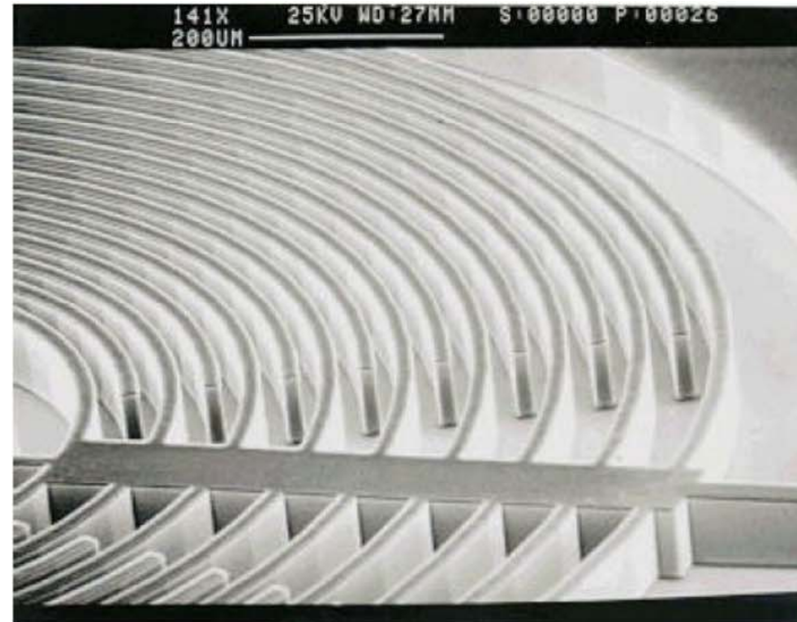
Deep RIE Example (2)

- Fabrication example (IMU device)



Gyroscope



Accelerometer (170㎛-depth)

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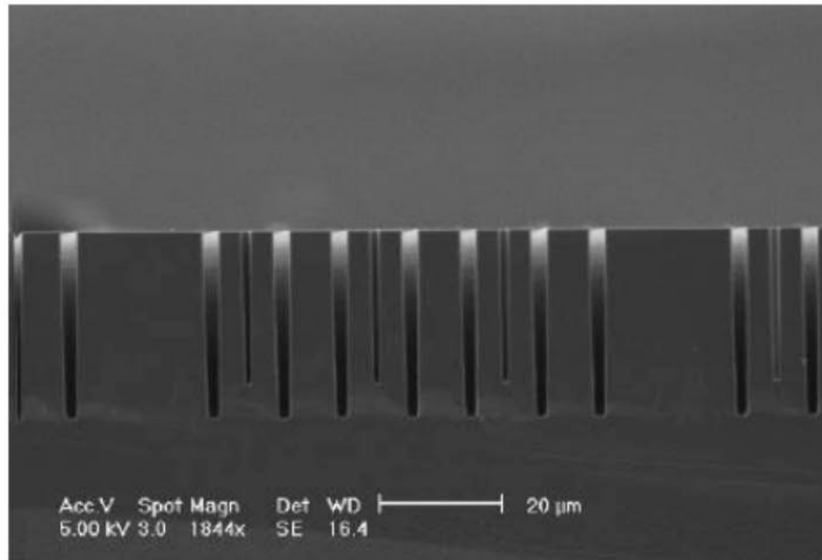
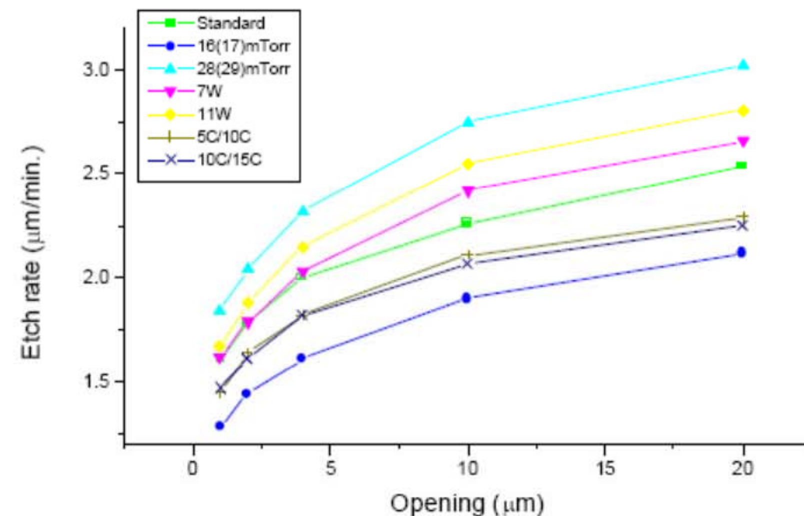
RIE Lag in Deep RIE Process

- RIE lag (microloading effect)
  - Etch rate of a wafer with a larger open area is different from the wafer with a smaller open area
  - Smaller hole has a lower etch rate than the larger holes
  - Etchants are more difficult to pass through the smaller hole
  - Etch byproducts are harder to diffuse out
  - Lower pressure can minimize the effect.





Plasma-Therm, SLR-7701-10R-B data

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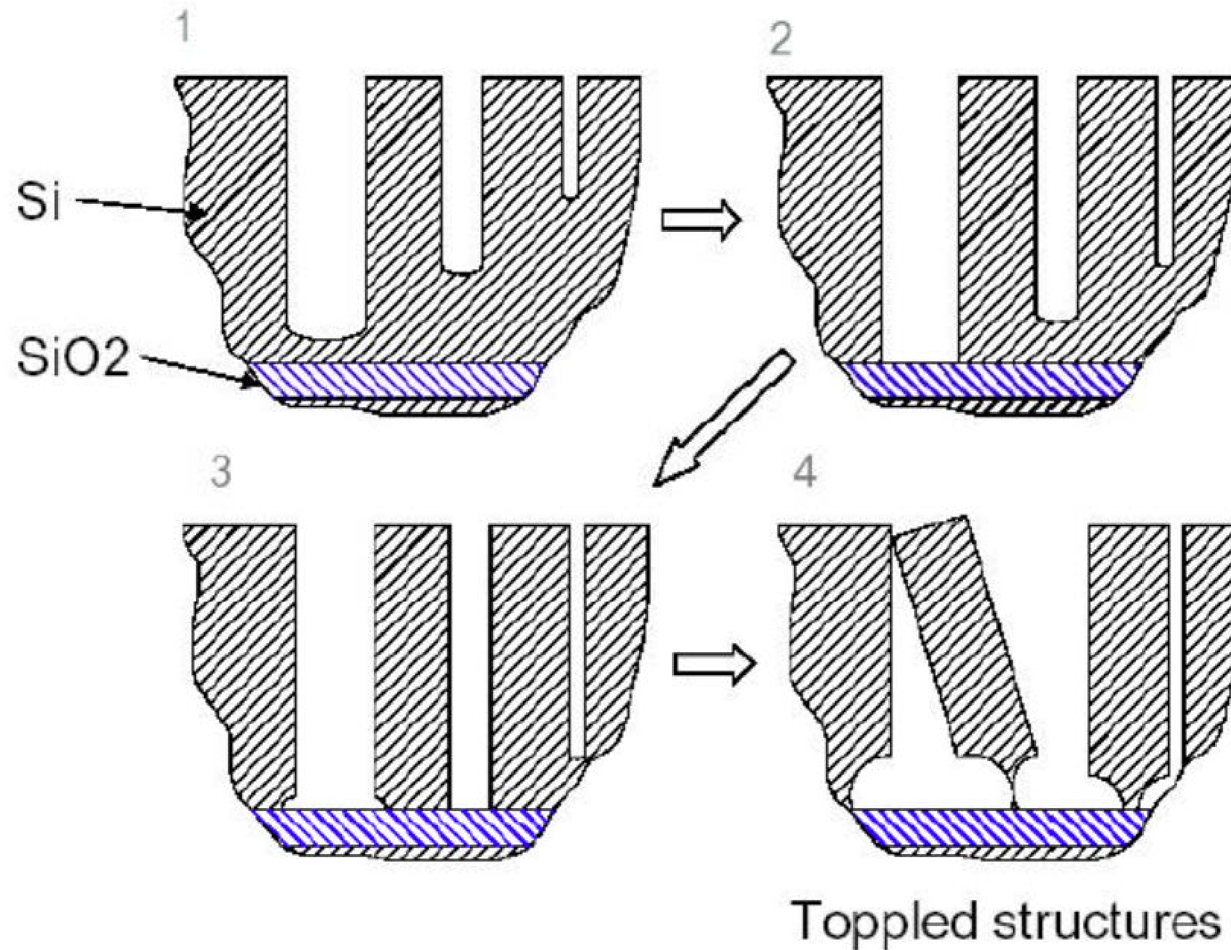
Footing in Deep RIE Process (1)

- Footing



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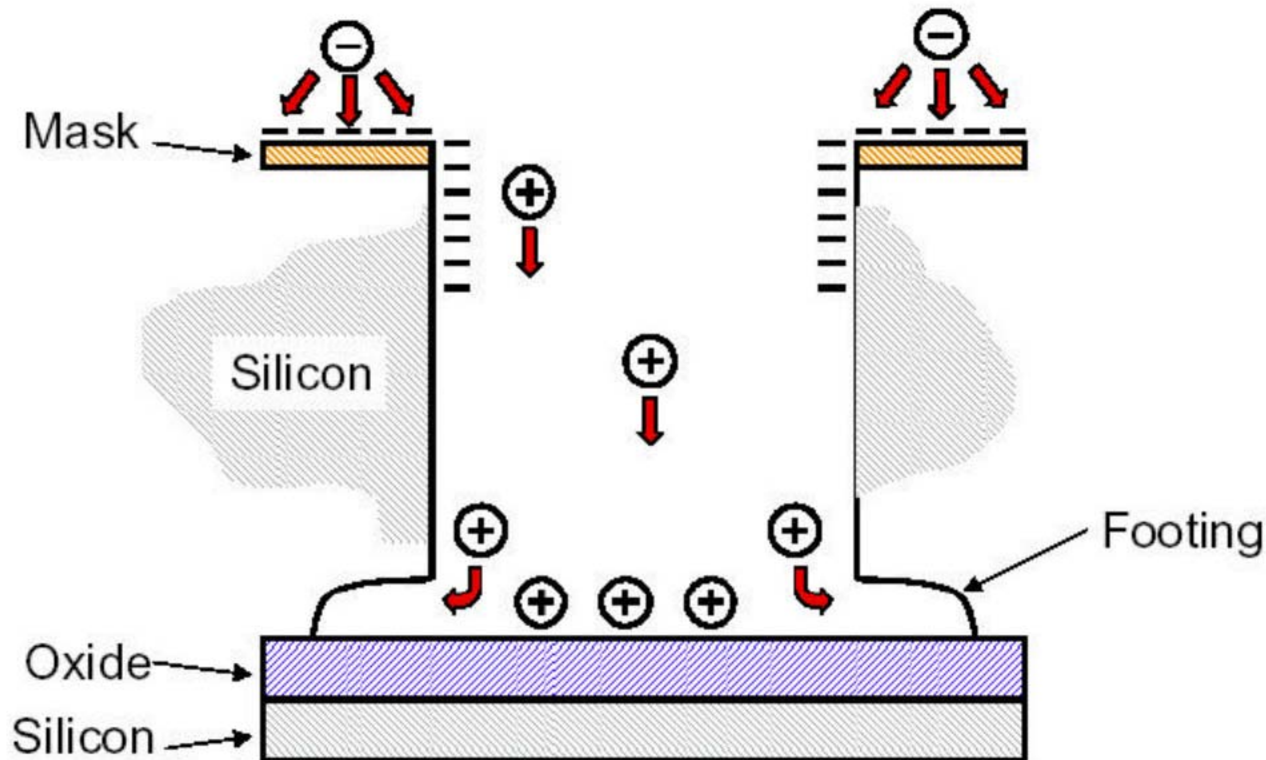
Footing in Deep RIE Process (2)

- Footing formation
  - There is notching at the foot of the silicon trench in a conventional deep RIE of SOI substrate due to charge accumulation at the base of the trench.



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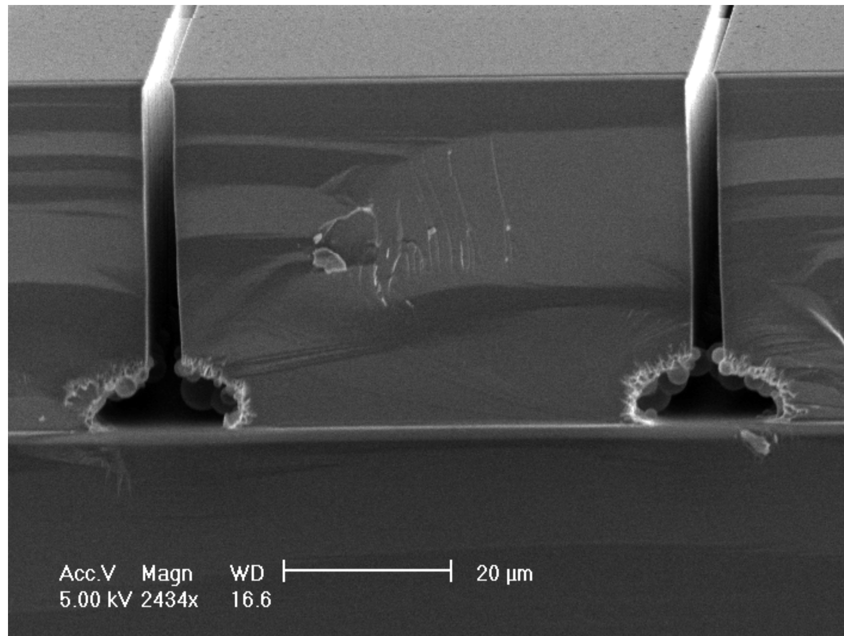
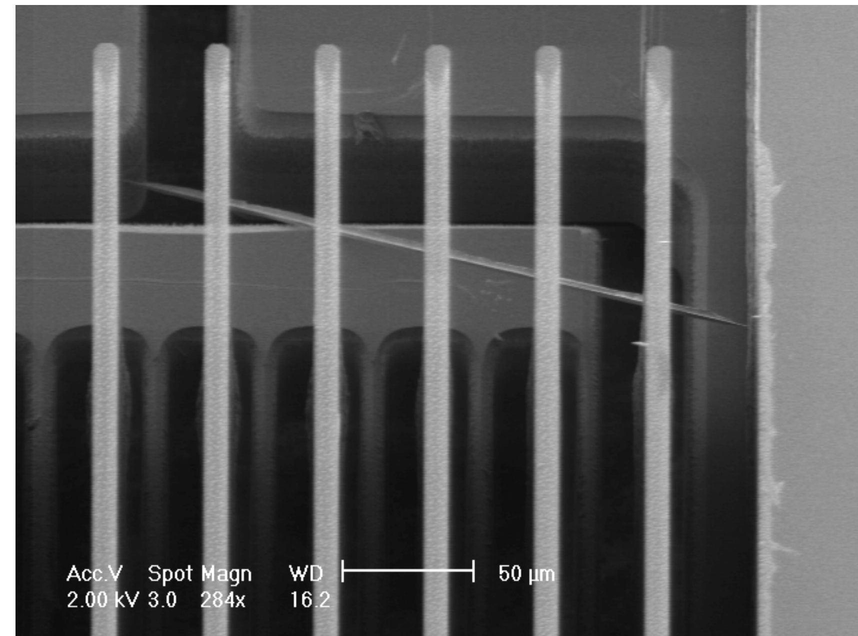
Footing in Deep RIE Process (3)

- Footing SEM pictures



Notching



Fragments

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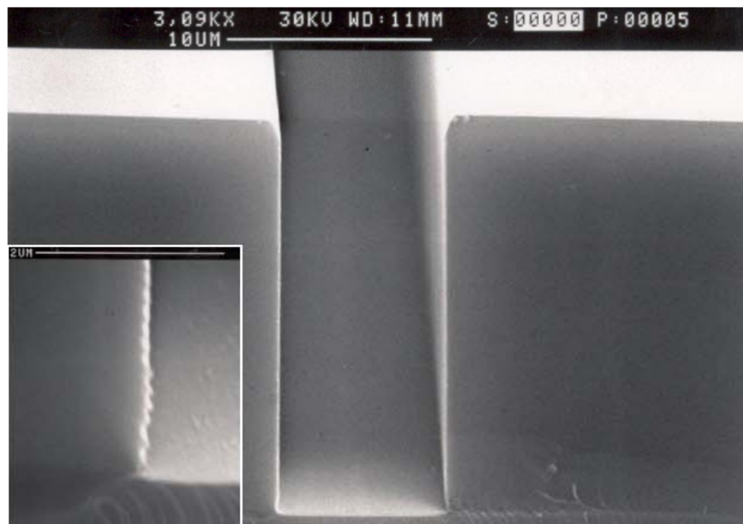
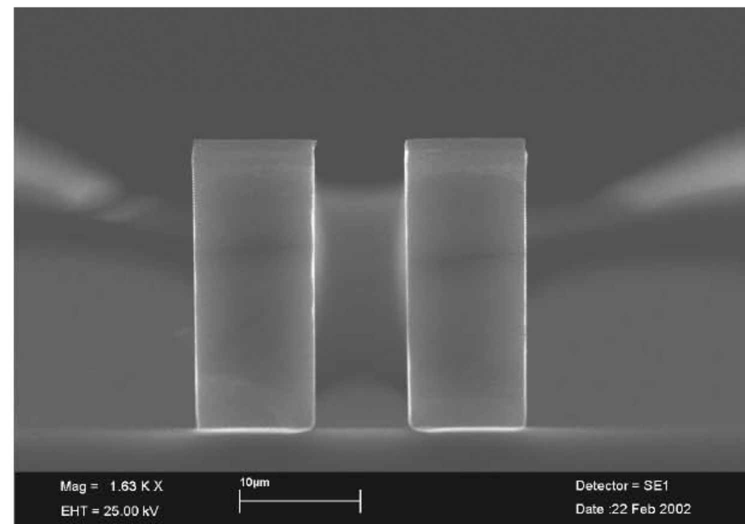
Reducing Footing Phenomenon in SOI Process

- Deep RIE with SOI kit (Surface Technology Systems, STS)
  - A conventional approach to reduce footing (notching) is to increase the passivation during the overetch
  - This increase process time and is only practical for similare feature sizes with short overetch time
  - **The SOI kit on the system controls the charging and hence broadens the process window significantly with out increased passivation**



Deep etched trench in 20 um SOI layer with good profile and notch control (8 um gap)



Isolated 10 um line features deep etched in a 20 um SOI layer with notch control (8 um gap centre, 500 um gap either side)

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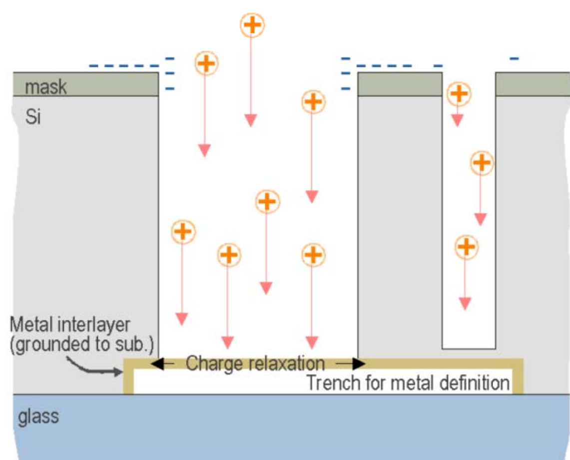
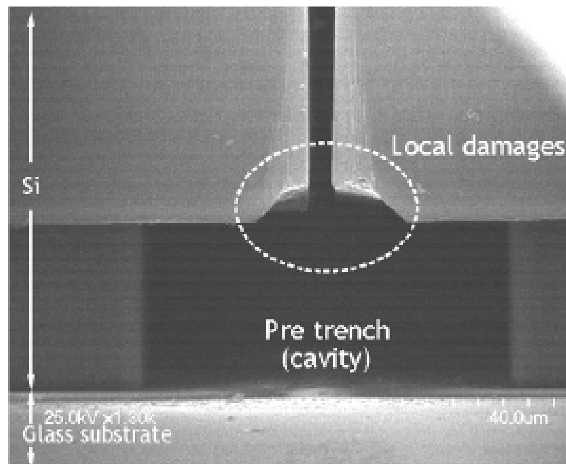
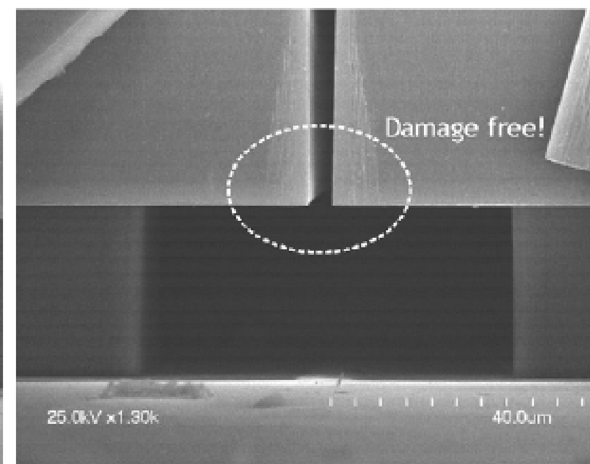
Reducing Footing Phenomenon in SOG Process

- Prevention method of a notching caused by surface charging
  - To prevent silicon from a notching in deep RIE process by introducing a self-aligned metal interlayer to a silicon/glass bonded fixture.
  - A metal interlayer prevents a charge buildup at the bottom of a silicon trench, therefore silicon structures do not suffer from charge-induced local damage.



An automatically aligned metal interlayer prevents silicon from notching by fast charge relaxation.





Test result for a simple trench: a 5 μm width silicon trench processed (Left picture) without a self-aligned metal interlayer (Right picture) with a self-aligned metal interlayer.

Dong-il "Dan" Cho **Nano/Micro Systems & Controls Lab.**
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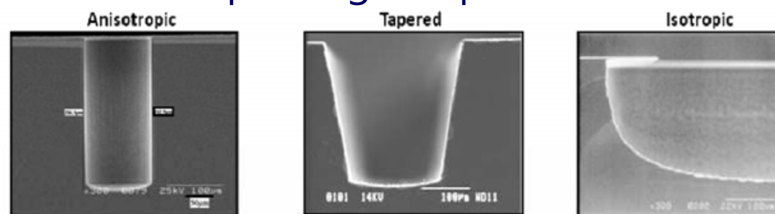
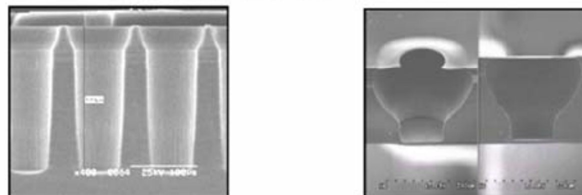
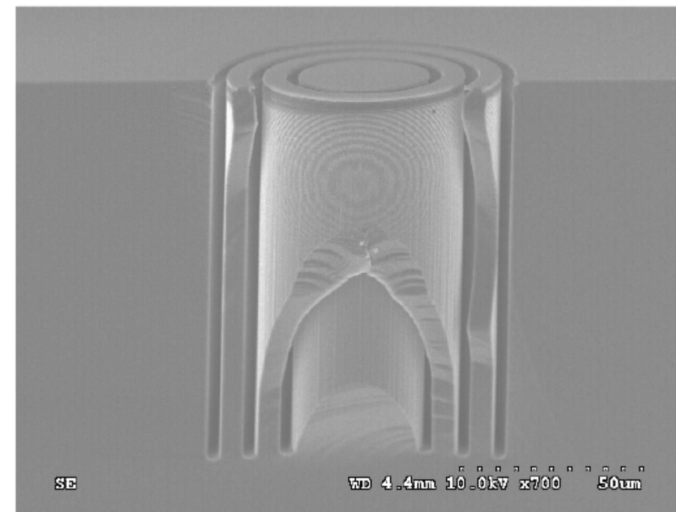
Latest Deep RIE in ALCATEL

- AMS 4200 for volume production cluster platform
  - Each process module is fitted with an Alcatel patented high-density ICP type plasma source.
  - The source is fixed on top of a diffusion chamber surrounded by a number of permanent magnets.
  - Achievements of the DRIE:
    - Profile control
    - High mask selectivity: >300:1
    - Super High Aspect Ratio: >100:1





A wide variety of basic profiles



Alcatel patented SHARP (Super High Aspect Ratio Process) allows an increase of the aspect ratio up to 110

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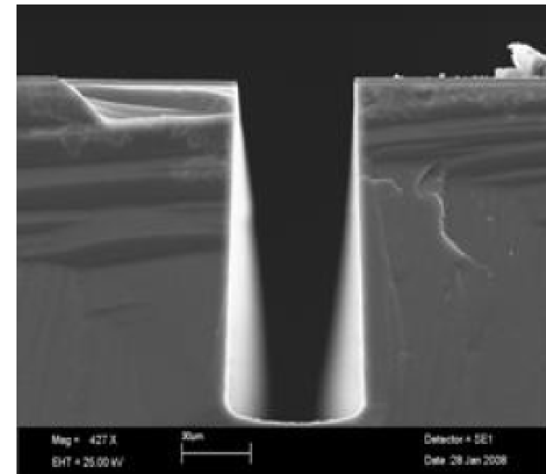
Latest Deep RIE in STS

- STS' Pegasus Systems
  - The Power Handling capability is improved
    - Improved Etch Rates
  - The plasma generation area is larger
    - Improved Etch Rates
    - Enhanced Etch Uniformity
  - Produces a neutral high radical density in the centre of the wafer and a uniform ion density across the whole wafer surface
    - Enhanced Etch Depth Uniformity
    - Improved Feature profile control
  - The STS Pegasus system offer full compatibility with CMOS fabs and foundries
    - No Electrostatic Damage
    - Excellent Particle Control
    - Low Ionic / Metal Contamination



ER	9.91μm/min
Profile	91.65 deg
Selectivity:PR	117:1

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Deep RIE I in ISRC (1)

- ICP deep silicon RIE (in MEMS area, for 4 inch wafer)
- Plasma-Therm, SLR-7701-10R-B
- Plasma source type: ICP (inductively coupled plasma)
- High aspect ratio up to 20~30
- Feature
  - 2 kW, ICP source and 500W bias power
  - gas line: C_4F_8, SF_6, Ar, O_2, NF_3, C_2F_6)

		Deposition	Etch A	Etch B
Time (sec)		5	3	5
Gas (sccm)	C_4F_8	100	0.5	0.5
	SF_6	0.5	50	100
	Ar	30	30	30
Power (W)	RF1 (bias)	1	13	13
	RF2 (source)	825	825	825
Pressure (mTorr)		22	23	23

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Deep RIE I in ISRC (2)

- Etch rate: 2.35 um/min (at 500 um opening)

- Under cut at the top of 4 um line & space: 0.4 um
- RIE lag (2 um/4 um): 24 % etch rate difference

- Selectivity to resist mask: 75:1
- Selectivity to oxide mask: 199:1

- Sidewall profile (levee): 88.5 $^{\circ}$
- Sidewall profile (furrow): 90 $^{\circ}$

- Etch depth capability: up to 500 um

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Deep RIE I in ISRC (3)

5.2 um

Acc.V Magn WD 5 µm
5.00 kV 4881x 22.0

74 um

Acc.V Magn WD 50 µm
5.00 kV 610x 22.0

7.6 um

Acc.V Magn WD 5 µm
5.00 kV 4881x 22.0

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Deep RIE II in ISRC (1)

- ICP deep silicon RIE II (in MEMS area, for 6 inch wafer)
- OERLIKON, Versaline
- Plasma source type: ICP (inductively coupled plasma)
- High aspect ratio up to 20~30
- Pump
  - Dry pump : Alcatel ADP122P 1,500ℓ/min
  - Turbo pump : Edwards STP-A1303CV 900ℓ/sec
- RF generator
  - PM, Coil : 2500W 2MHz)
  - Electrode : 600W, 13.56MHZ

		Deposition	Etch A	Etch B
Time (sec)		2	1.5	1
Gas (sccm)	C_4F_8	150	0	0
	SF_6	0	250	250
	Ar	30	30	30
Power (W)	RF1 (ICP)	2000	2000	2500
	RF2 (source)	10	150	10
Pressure (mTorr)		25	40	70

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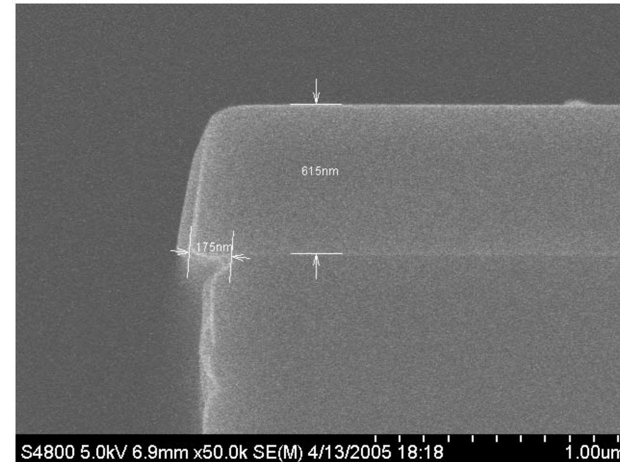
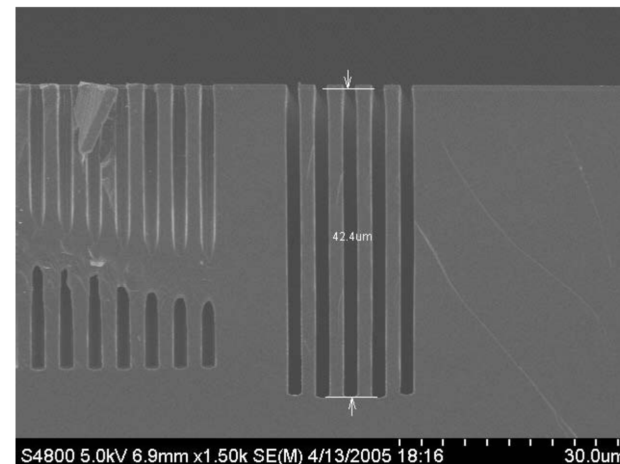
Deep RIE II in ISRC (2)

- Process parameter of High Rate 2 um recipe
  - Etch rate: 4 um/min
  - Aspect ratio: 25
  - Selectivity to resist mask: > 100:1
  - Selectivity to oxide mask: > 200:1
  - Uniformity: 1.2%
  - Verticality: 90°±1
  - Undercut: 150 nm
  - Scallop pitch: 160 nm
  - Scallop depth: 50 nm





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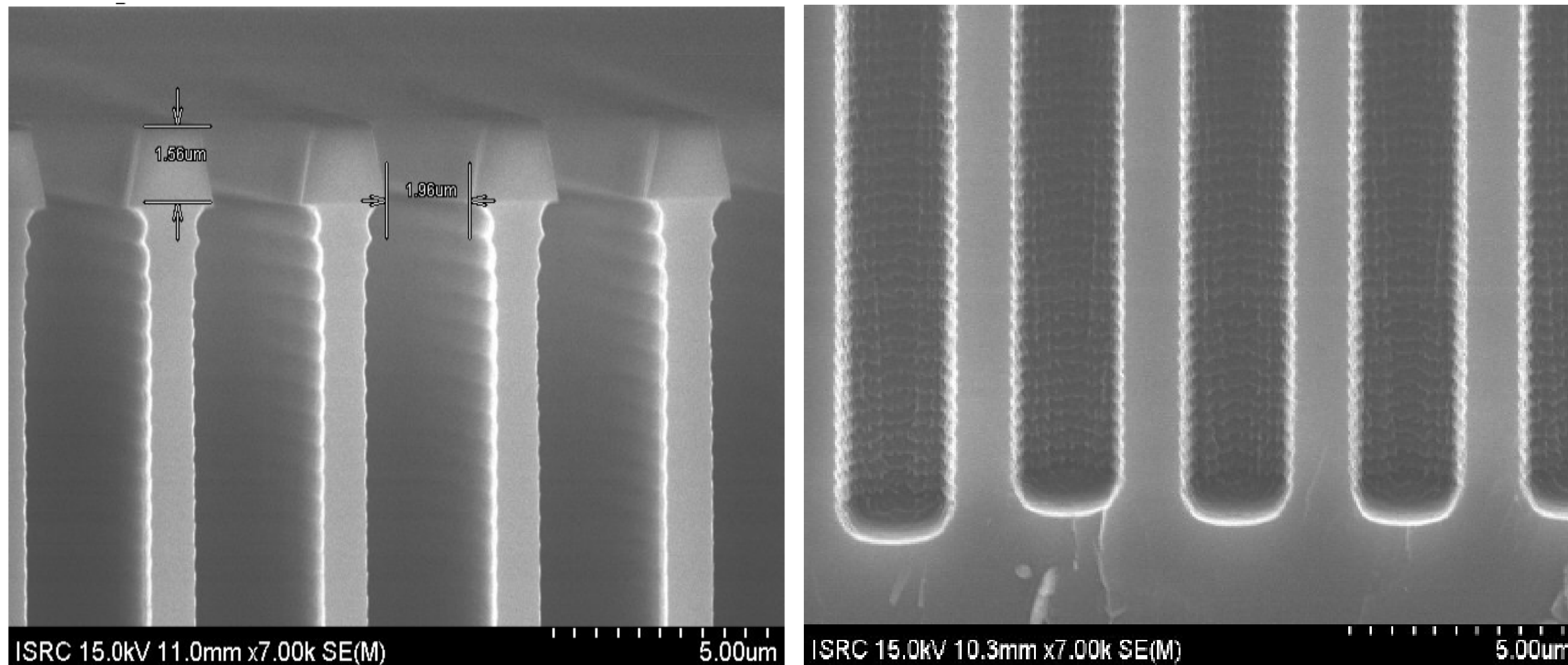
Deep RIE II in ISRC (3)

- Process results using 'SNU High Etch Rate 2 um' recipe



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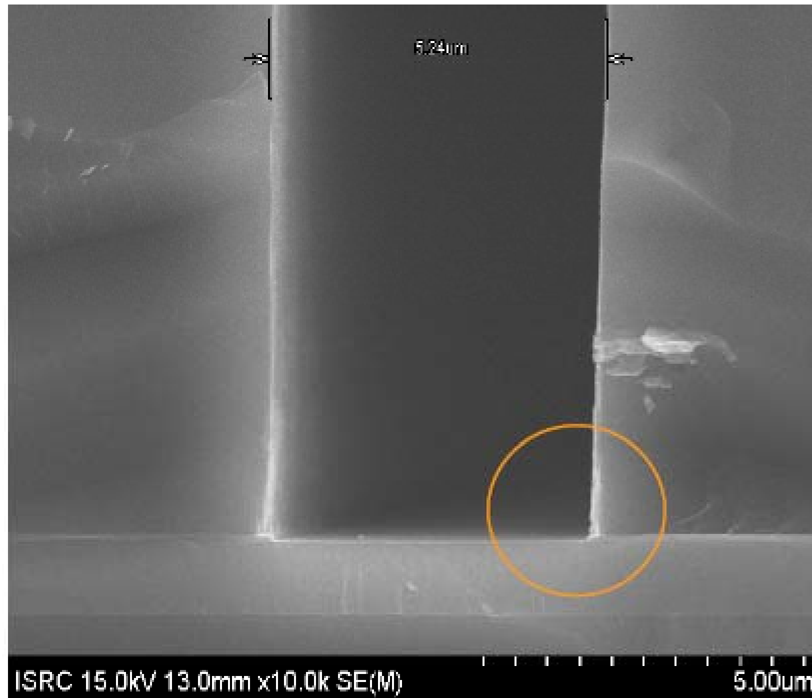
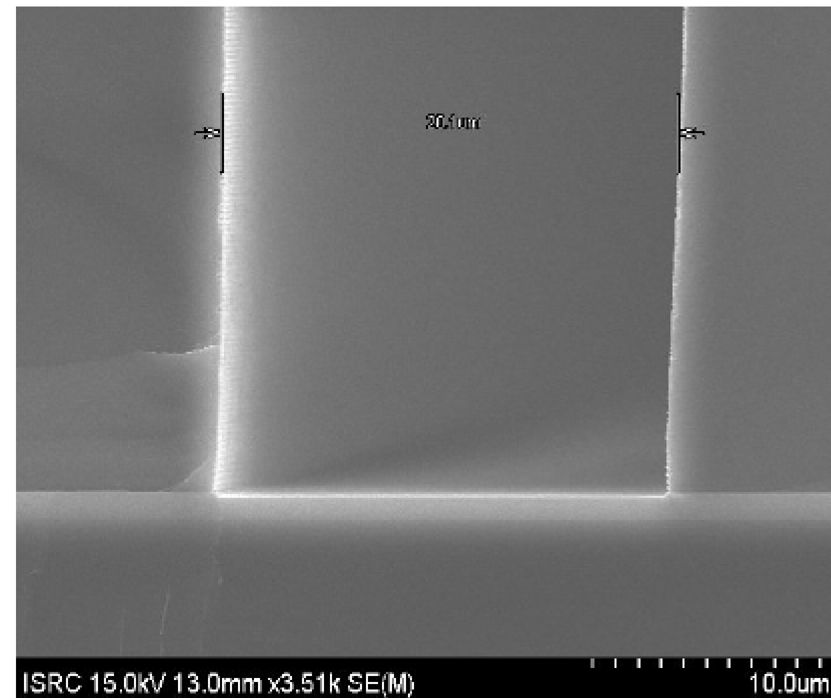
Deep RIE II in ISRC (4)

- Process results using 'SNU SOI' recipe
  - Anti-footing recipe for SOI process



5 um line width



20 um line width

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Reference

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Reference

7. S. Park, "Plasma-Therm Deep Silicon Etcher 공정개발 결과," Nov. 1999
8. Marc J. Madou, “Fundamentals of MICROFABICATION,” 2nd edition
9. J. D. Lee, “Silicon Integrated Circuit microfabrication technology,” 2nd edition

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RIE Principles (2)

- Basic steps in a plasma etching process

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