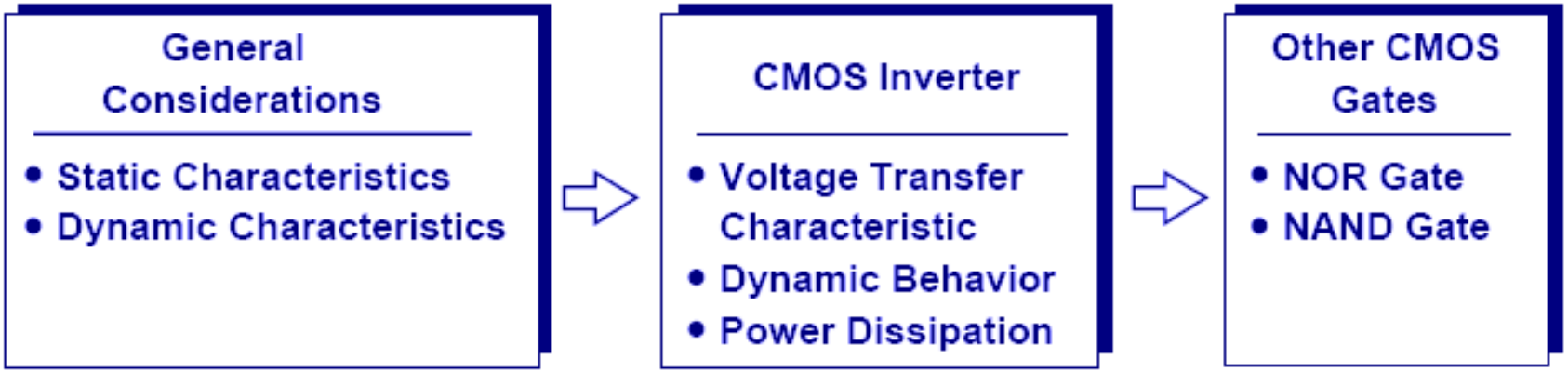
Chapter 15 Digital CMOS Circuits

- 15.1 General Considerations
- 15.2 CMOS Inverter
- 15.3 CMOS NOR and NAND Gates

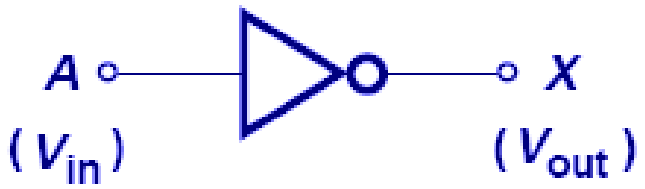
Chapter Outline



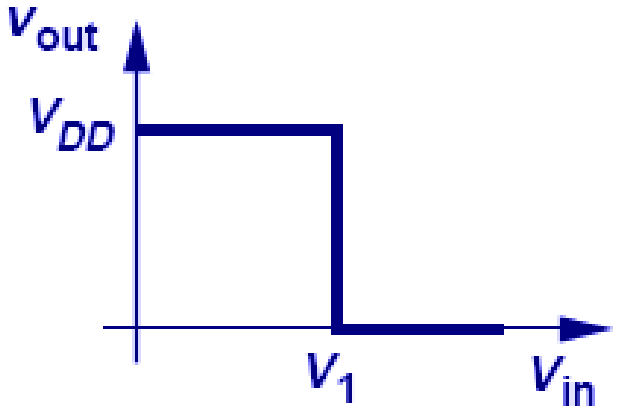
Following three important questions will be addressed

(1) What limits the speed of a digital gate?
(2) How much power does a gate consume while running at a certain speed?
(3) How much "noise" can a gate tolerate while producing a valid output?

Inverter Characteristic



(a)



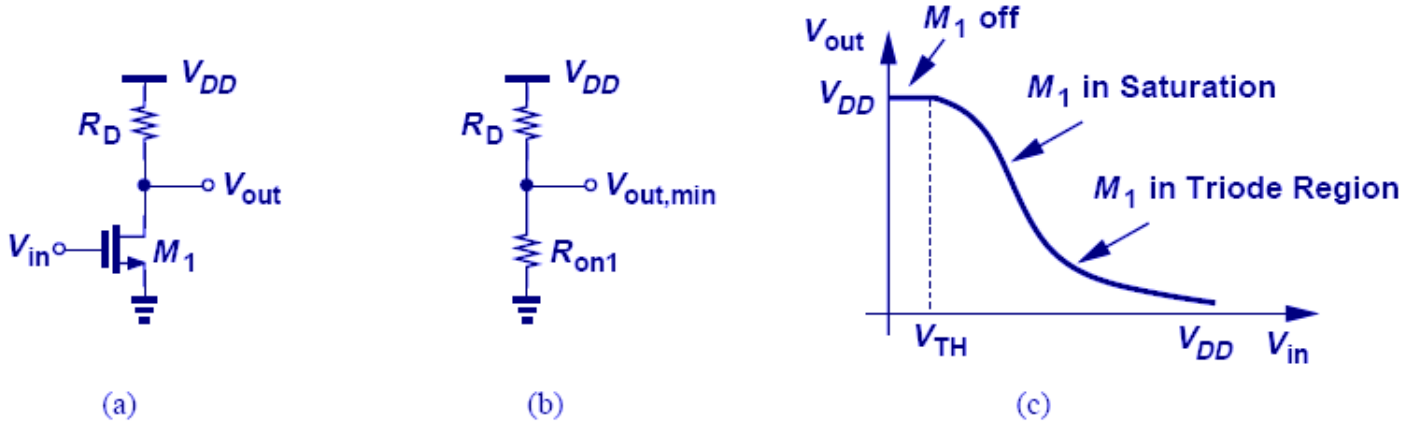
(b)

$$X = \overline{A}$$

- **An inverter outputs a logical “1” when the input is a logical “0” and vice versa.**

Examples 15.1 & 15.2: NMOS Inverter

$V_{DS} \geq V_{GS} - V_{TH}$: saturation, $V_{DS} < V_{GS} - V_{TH}$: linear



(a) (b) (c)

$V_{in} \leq V_{TH}$: $V_{out} = V_{DD}$

$V_{in} > V_{TH}$, $V_{out} > V_{in} - V_{TH}$: $V_{out} = V_{DD} - I_D R_D = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})^2$

$V_{in} > V_{TH}$, $V_{out} \leq V_{in} - V_{TH}$:

$$V_{out} = V_{DD} - I_D R_D = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D[2(V_{in} - V_{TH})V_{out} - V_{out}^2]$$

$$V_{out} = V_{in} - V_{TH} + \frac{1}{\mu_n C_{ox}\frac{W}{L}R_D} - \sqrt{(V_{in} - V_{TH} + \frac{1}{\mu_n C_{ox}\frac{W}{L}R_D})^2 - (\frac{2V_{DD}}{\mu_n C_{ox}\frac{W}{L}R_D})}$$

Example 15.1 & 15.2: NMOS Inverter (cont'd)

V_{out} is at the lowest when V_{in} is at V_{DD}.

$$\because I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}]$$

$$V_{out,min} = V_{DD} - R_D I_{D,max} \quad @ \text{ linear region}$$

$$= V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}[(V_{DD} - V_{TH})V_{out,min} - \frac{V_{out,min}^2}{2}]$$

If we neglect the second term in the square brackets, then

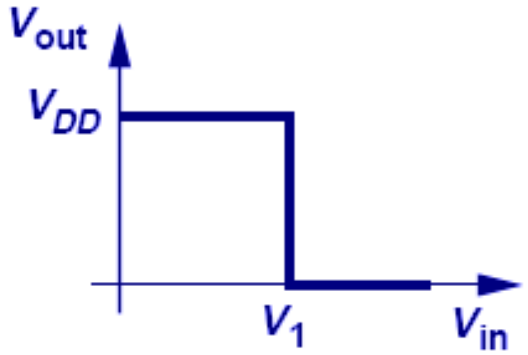
$$V_{out,min} \approx \frac{V_{DD}}{1 + \mu_n C_{ox} \frac{W}{L} R_D (V_{DD} - V_{TH})} = \frac{[1 + \mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{TH})]^{-1}}{R_D + [\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{TH})]^{-1}} V_{DD}$$

This is equivalent to viewing M1 as a resistor of value

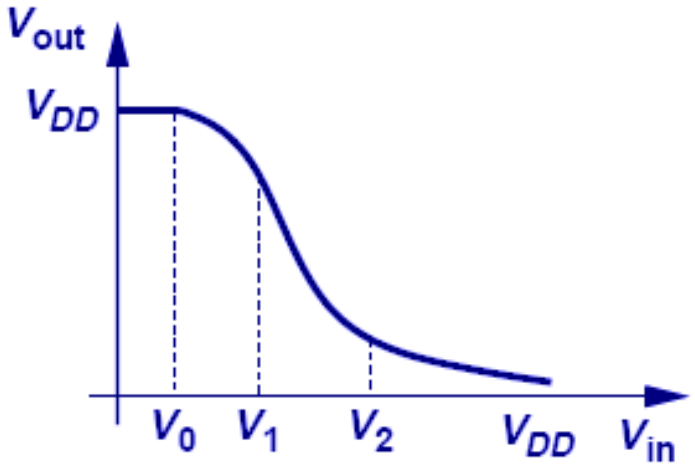
$$R_{on1} = [\mu_n C_{ox}(W/L)(V_{DD} - V_{TH})]^{-1}$$

- **The CS stage resembles a voltage divider between R_D and R_{on1} when M_1 is in deep triode region. It produces V_{DD} when M_1 is off.**

Transition Region Gain



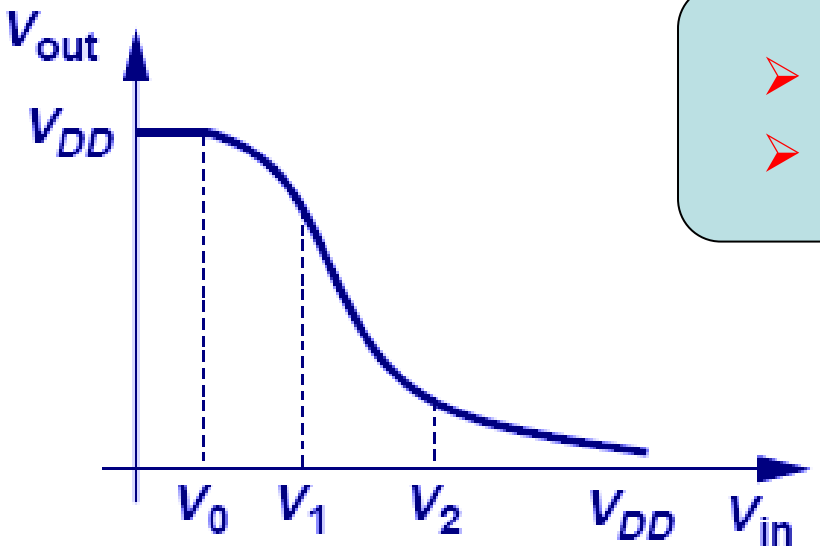
Infinite Transition Region Gain



Finite Transition Region Gain

- **Ideally, the VTC of an inverter has infinite transition region gain. However, practically the gain is finite.**

Example 15.3: Gain at Transition Region

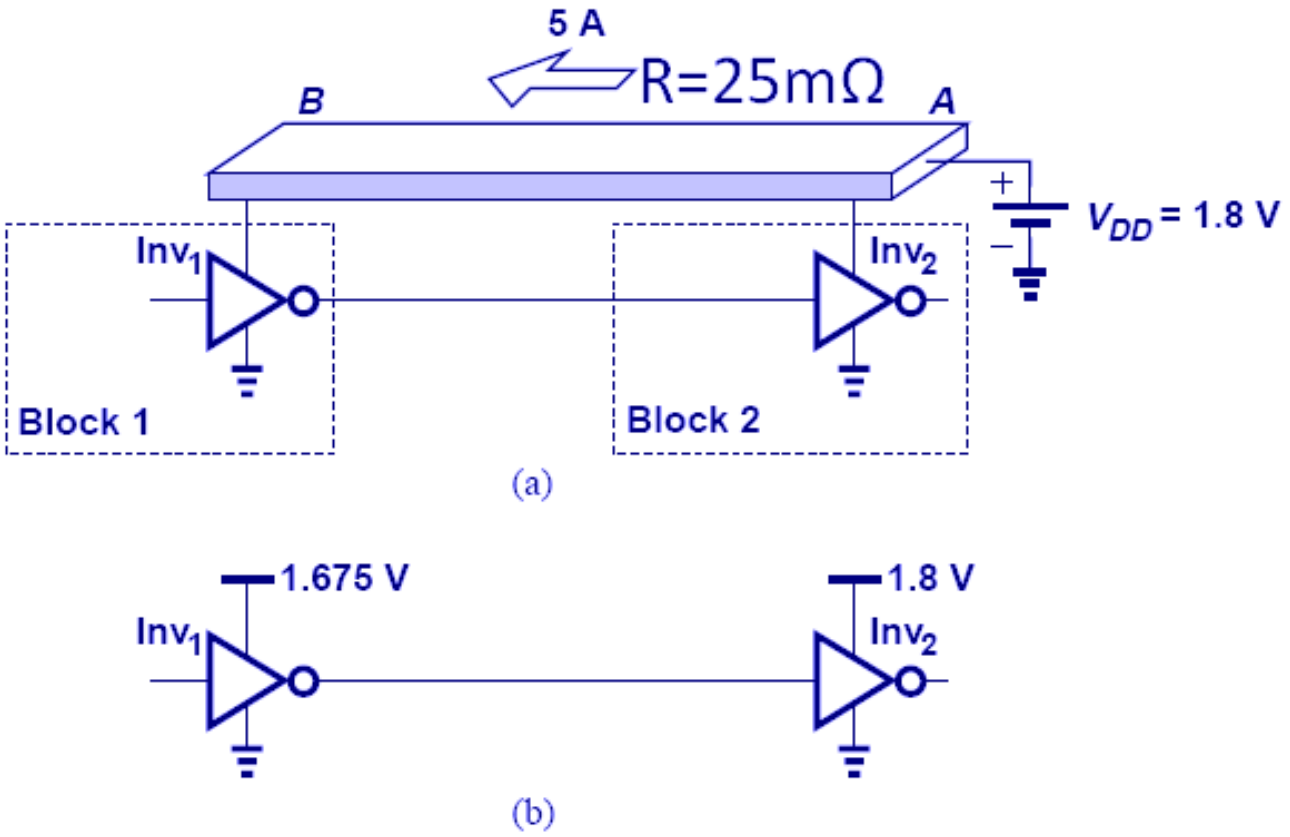


- Transition Region: 50 mV
- Supply voltage: 1.8V

$V_0 - V_2$: Transition Region

$$A_v = \frac{1.8}{0.05} = 36$$

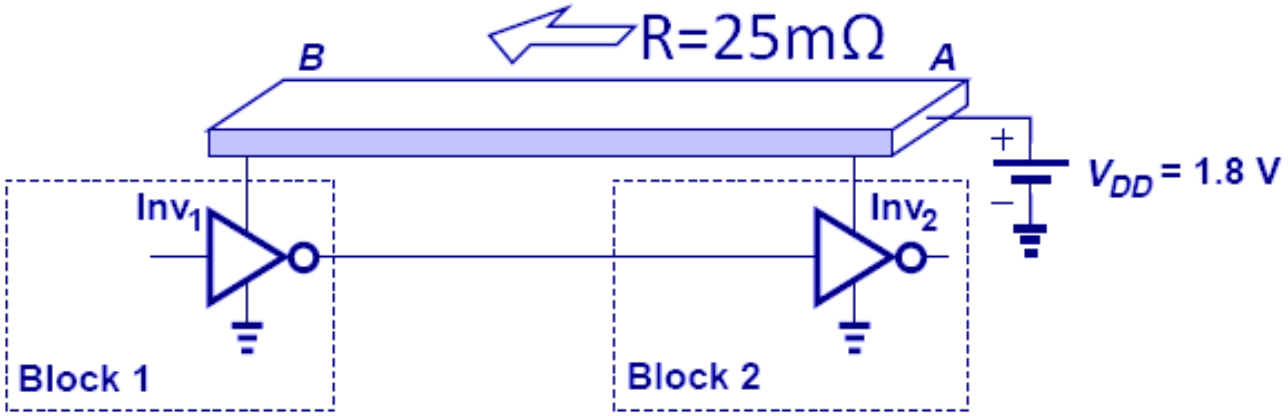
Logical Level Degradation



- **Since real power buses have losses, the power supply levels at two different locations will be different. This will result in logical level degradation.**

Example 15.4: Logical Level Degradation

If inverter Inv1 produces a logical ONE given by the local value of V_{DD}, determine the degradation as sensed by inverter Inv2.

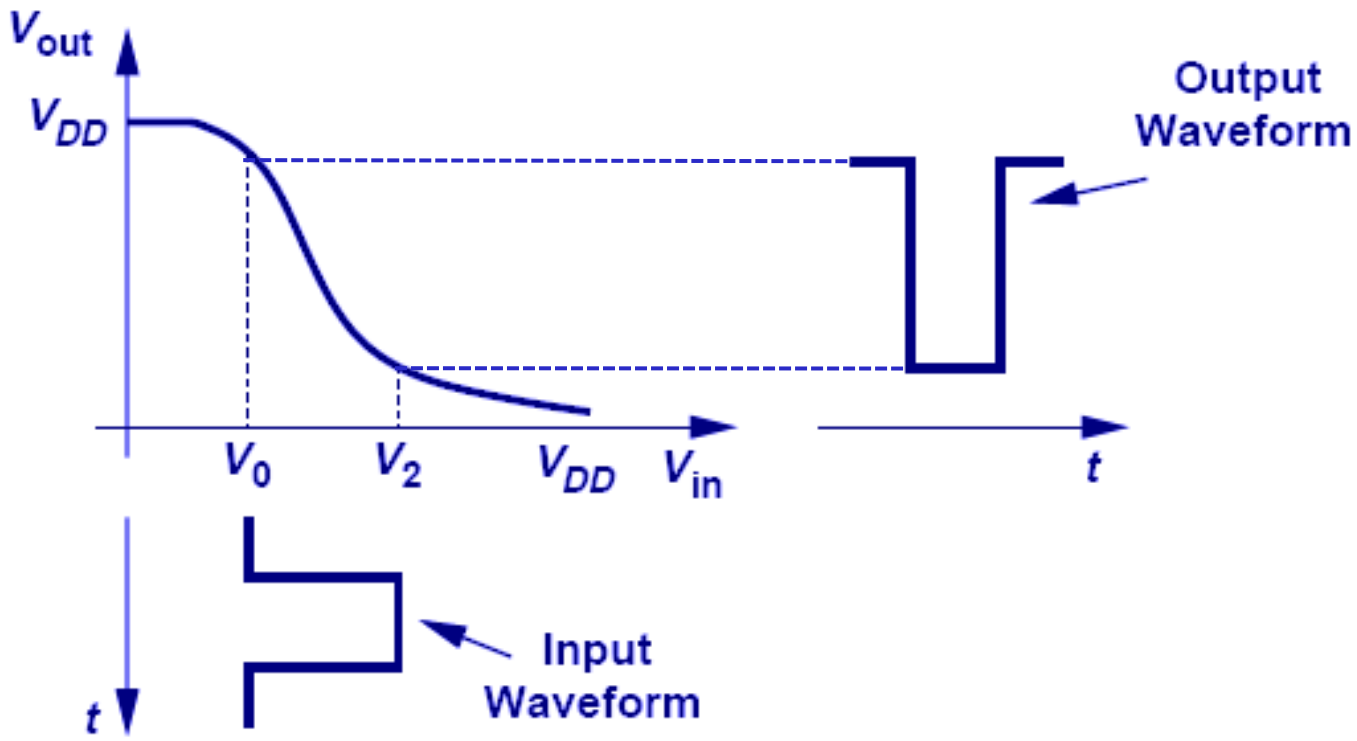


$$\Delta V = 5\text{A} \times 25\text{m}\Omega = 125\text{mV}$$

Supply B=1.675V

Supply A=1.8V

The Effects of Level Degradation and Finite Gain



- **In conjunction with finite transition gain, logical level degradation in succeeding gates will reduce the output swings of gates.**

Example 15.5: Small-Signal Gain Variation of NMOS Inverter

Sketch the small-signal voltage gain for the characteristic shown in Fig.15.4 as a function of V_{in}.

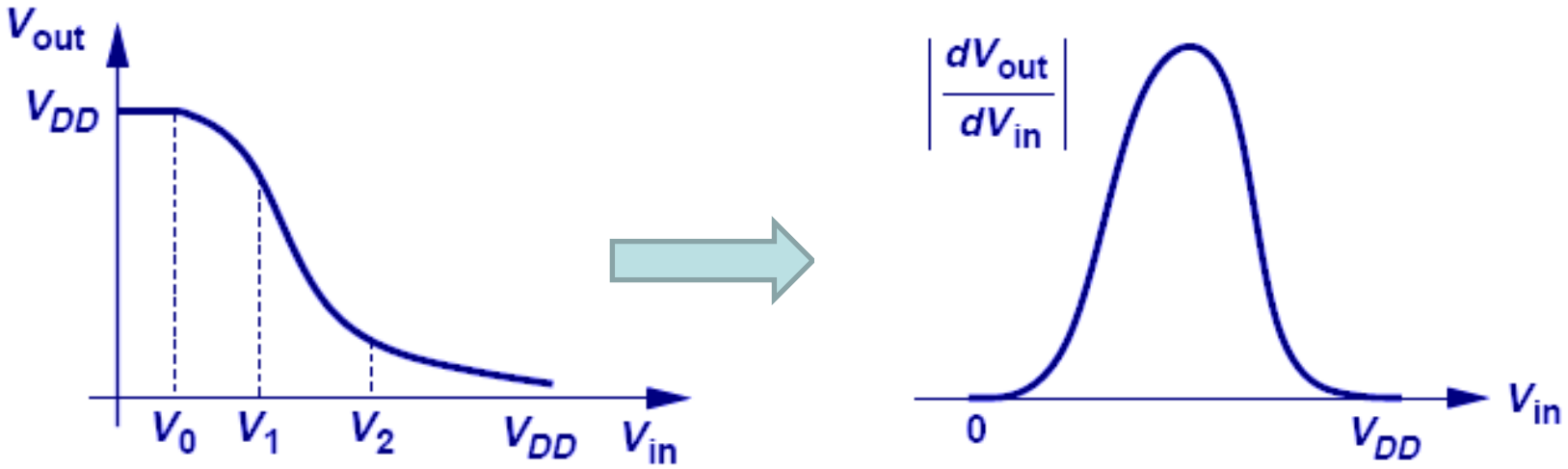
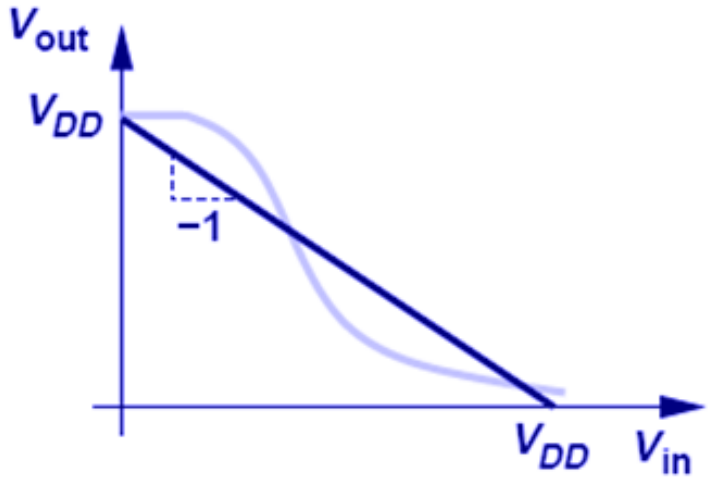


Fig.15.4

- **the small-signal gain is the largest in the transition region.**

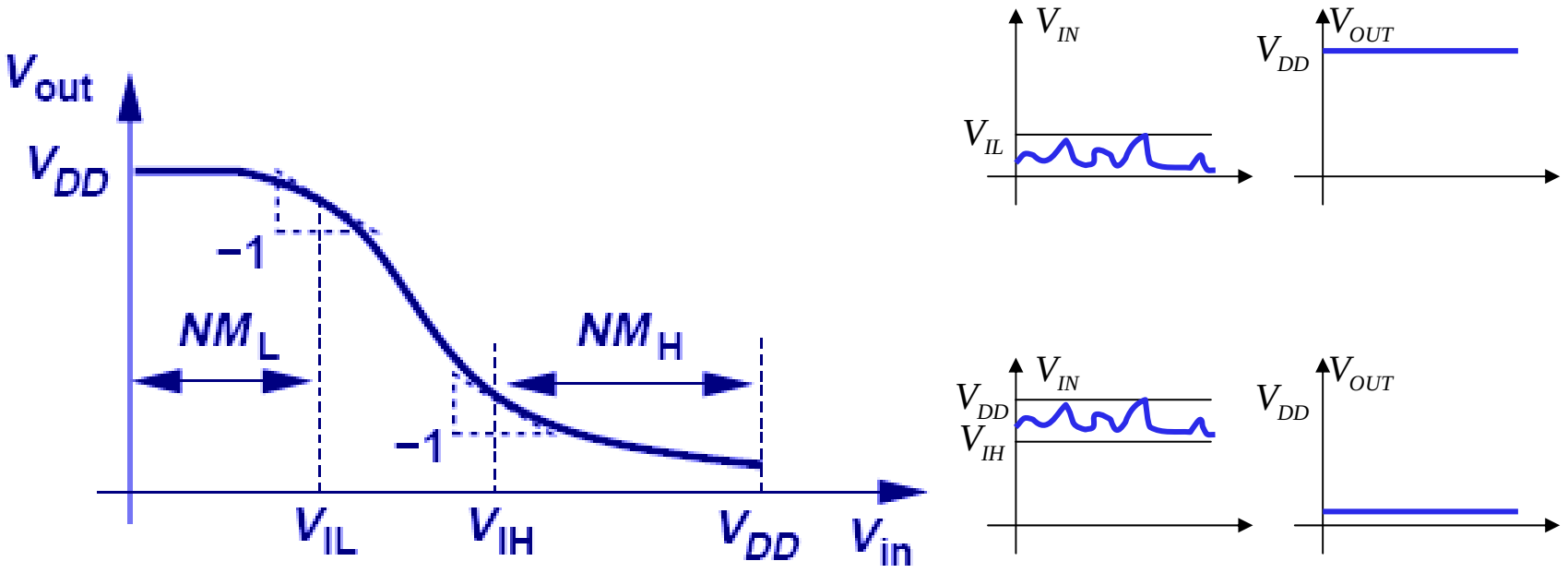
Example 15.6: Small-Signal Gain Above Unity

Prove that the magnitude of the small-signal gain obtained in Example 15.5 must exceed unity at some point.



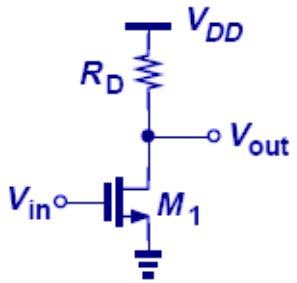
- **The transition region at the input spans a range narrower than 0 to V_{DD}.**

Noise Margin

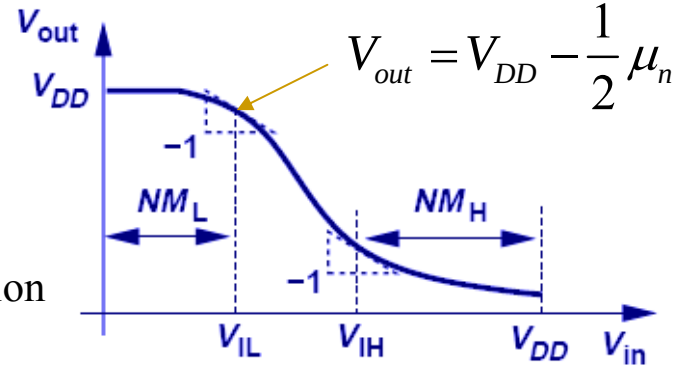


- **Noise margin is the amount of input logic level degradation that a gate can handle before the small-signal gain becomes -1.**

Example 15.7: NMOS Inverter Noise Margin



saturation region



$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2 R_D$$

When V_{in} is equal to V_{IL}, M1 is in saturation region. $V_{DS} > V_{GS} - V_{TH}$

1.Using the small-signal gain : $g_m R_D = \mu_n C_{ox}\frac{W}{L}(V_{IL} - V_{TH})R_D = 1$

2.Using differentiation : $\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_{IL} - V_{TH})R_D = -1$

$$NM_L = V_{IL} = \frac{1}{\mu_n C_{ox}\frac{W}{L}R_D} + V_{TH}$$

As V_{in} drives M_1 into the triode region (or linear region),

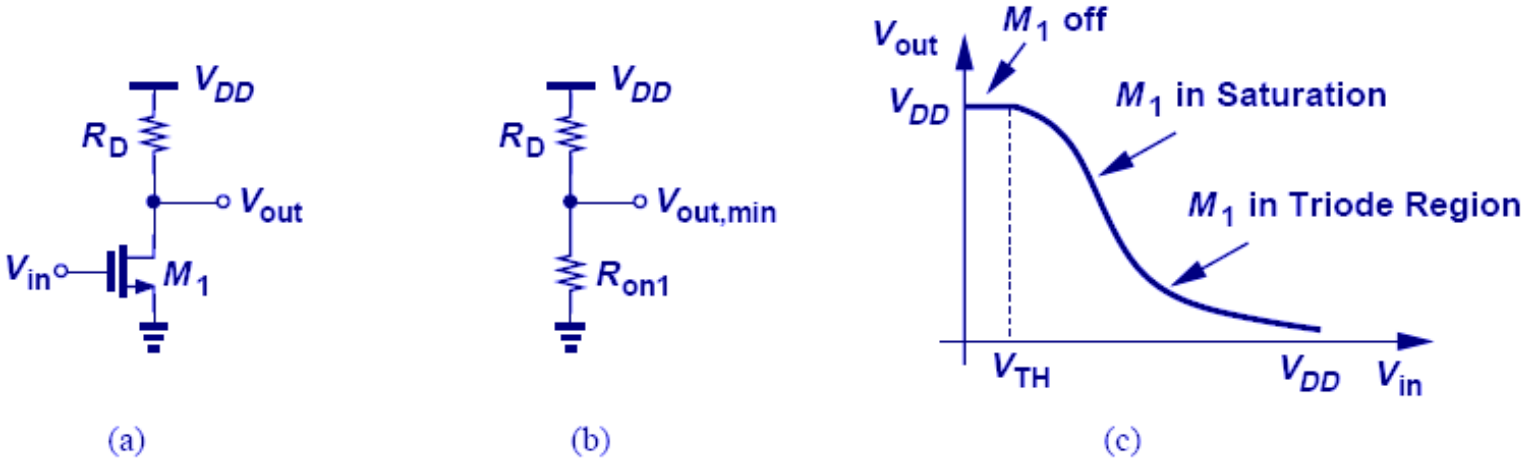
$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D\left[2(V_{in} - V_{TH})V_{out} - V_{out}^2\right]$$

$$\frac{\partial V_{out}}{\partial V_{in}} = -\frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D\left[2V_{out} + 2(V_{in} - V_{TH})\frac{\partial V_{out}}{\partial V_{in}} - 2V_{out}\frac{\partial V_{out}}{\partial V_{in}}\right] \quad \text{with } \partial V_{out}/\partial V_{in} = -1$$

$$V_{out} = \frac{1}{2\mu_n C_{ox}\frac{W}{L}R_D} + \frac{V_{in} - V_{TH}}{2} \longrightarrow V_{in} = V_{IH} \longrightarrow NM_H = V_{DD} - V_{IH}$$

Example 15.8: Minimum V_{out}

The output low level of an NMOS inverter is always degraded. Derive a relationship to guarantee that this degradation remains below $0.05V_{DD}$.



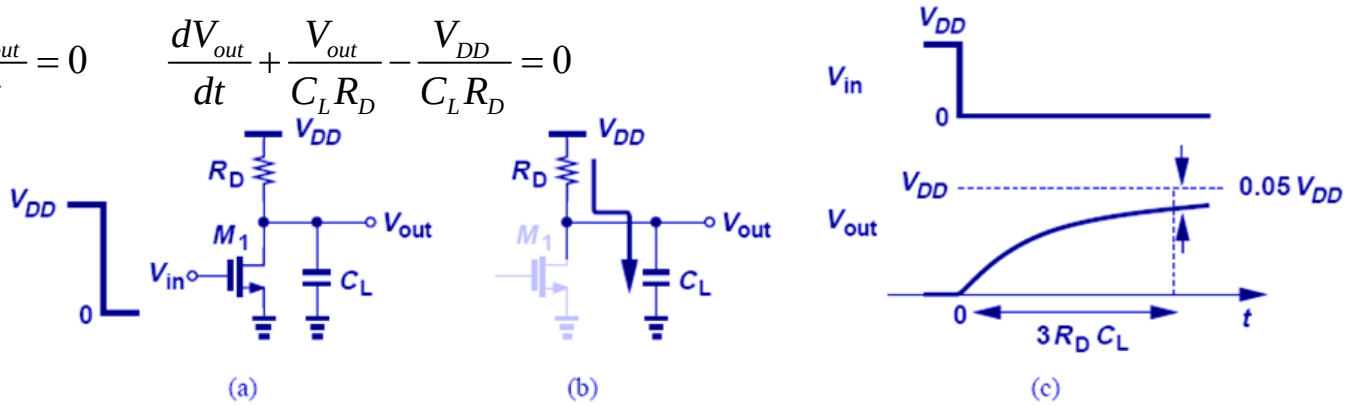
$$V_{out,min} \approx \frac{R_{on1}}{R_D + R_{on1}} V_{DD} \leq 0.05 V_{DD}$$

$$R_D \geq 19 R_{on1} = 19 \cdot [\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{TH})]^{-1}$$

Example 15.9: Dynamic Behavior of NMOS Inverter

$$-\frac{V_{DD}-V_{out}}{R_D}+C_L\frac{dV_{out}}{dt}=0 \qquad \frac{dV_{out}}{dt}+\frac{V_{out}}{C_L R_D}-\frac{V_{DD}}{C_L R_D}=0$$

$$V_{out}=A+Be^{-t/R_D C_L}$$



$$V_{out}(0^-)=V_{DD}-\mu_n C_{ox}\frac{W}{L}R_D(V_{DD}-V_{TH})V_{out}(0^-)R_D \quad \rightarrow V_{out}(0^-)=\frac{V_{DD}}{1+\mu_n C_{ox}\frac{W}{L}R_D(V_{DD}-V_{TH})}$$

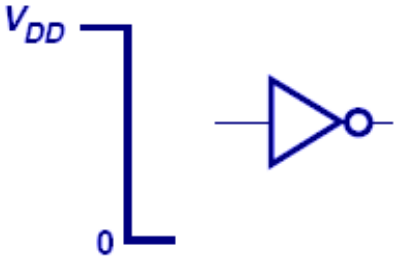
$$V_{out}(t)=V_{out}(0^-)+[V_{DD}-V_{out}(0^-)]\left(1-\exp\frac{-t}{R_D C_L}\right),\ t>0$$

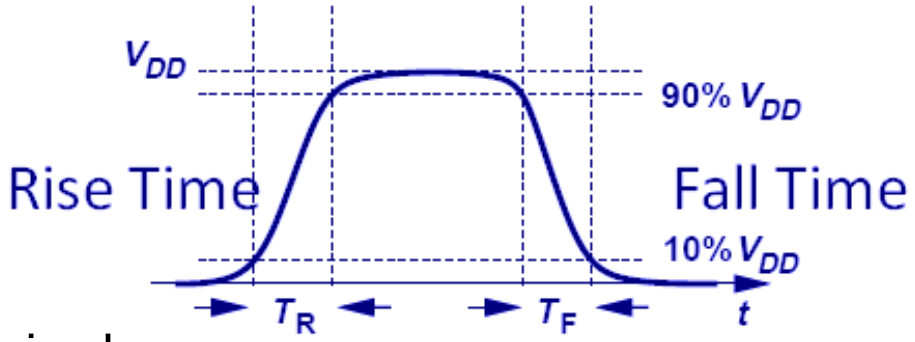
$$0.95V_{DD}=V_{out}(0^-)+[V_{DD}-V_{out}(0^-)]\left(1-\exp\frac{-T_{95\%}}{R_D C_L}\right) \quad \rightarrow T_{95\%}=-R_D C_L\ln\frac{0.05V_{DD}}{V_{DD}-V_{out}(0^-)}$$

Assuming $V_{DD}-V_{out}(0^-)\approx V_{DD}$, $T_{95\%}\approx 3R_D C_L$

- **Since digital circuits operate with large signals and experience nonlinearity, the concept of transfer function is no longer meaningful. Therefore, we must resort to time-domain analysis to evaluate the speed of a gate.**

Rise/Fall Time and Delay



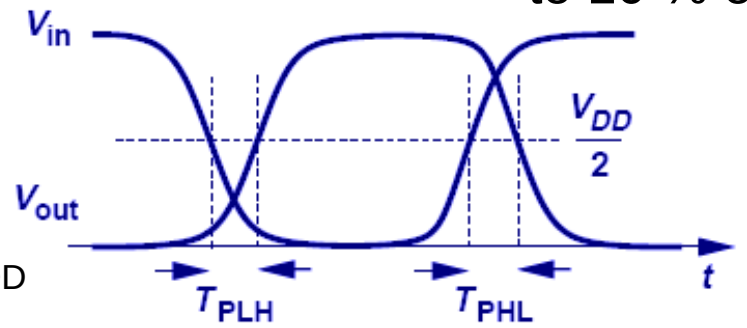


(a)

T_R: the time required for the output to go from 10% of V_{DD} to 90 % of V_{DD}

T_F: the time required for the output to go from 90% of V_{DD} to 10 % of V_{DD}

delay: the difference between the time points at which the input and the output cross 0.5 V_{DD}

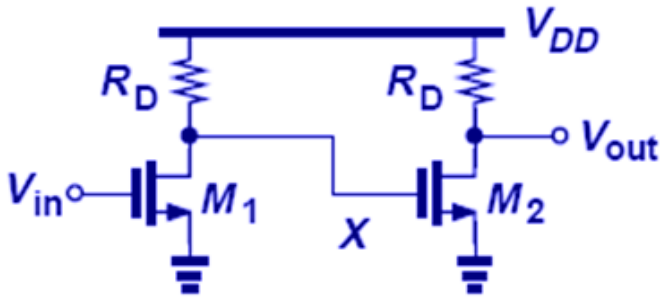


(b)

Delay

Example 15.10: Time Constant

Assuming a 5% degradation in the output low level, determine the time constant at node X when V_X goes from low to high.



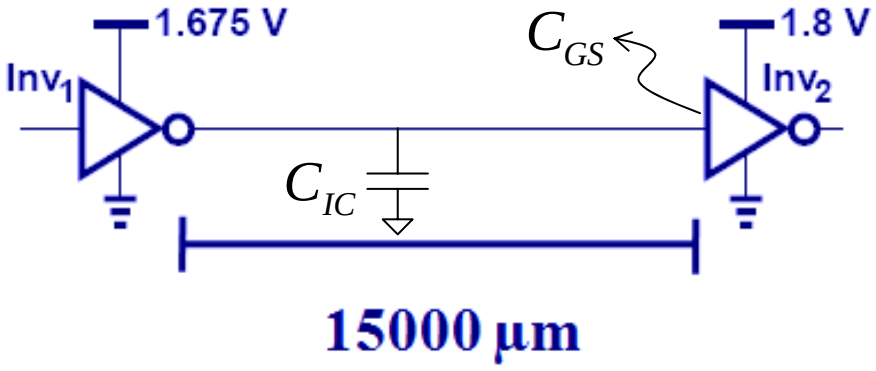
Assuming $C_X \approx WLC_{ox}$ and $R_D = 19R_{on1}$,

$$\tau = R_D C_X = \frac{19}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{TH})} \cdot WLC_{ox}$$

$$= \frac{19L^2}{\mu_n (V_{DD} - V_{TH})}$$

Example 15.11: Interconnect Capacitance

What is the interconnect capacitance driven by Inv_1?



$$\frac{C_{IC}}{C_{GS}} \approx 640$$

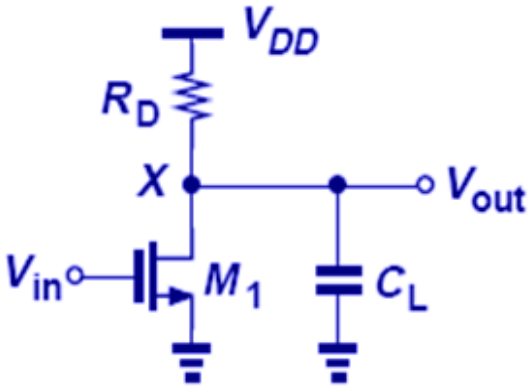
Wire Capacitance per Mircon: 50 aF/µm, (1aF=1x10^{-18}F)

Total Interconnect Capacitance: 15000×50×10^{-18} =750 fF

Equivalent to 640 MOS FETs with W=0.5µm, L=0.18µm, C_{ox} =13.5fF/µm^2

$$\because C_{GS} \approx WLC_{ox} = 1.17 \text{ fF}$$

Power-Delay Product



PDP has dimension of energy, i.e. it indicates how much energy is consumed for a logical operation

$$PDP = \text{Power} \cdot \frac{T_{PHL} + T_{PLH}}{2}$$

$$\approx (I_D V_{DD}) \cdot (R_D C_X) = \frac{V_{DD}^2}{R_D + R_{on1}} \cdot (R_D C_X) \text{ with } I_D = \frac{V_{DD}}{R_D + R_{on1}}$$

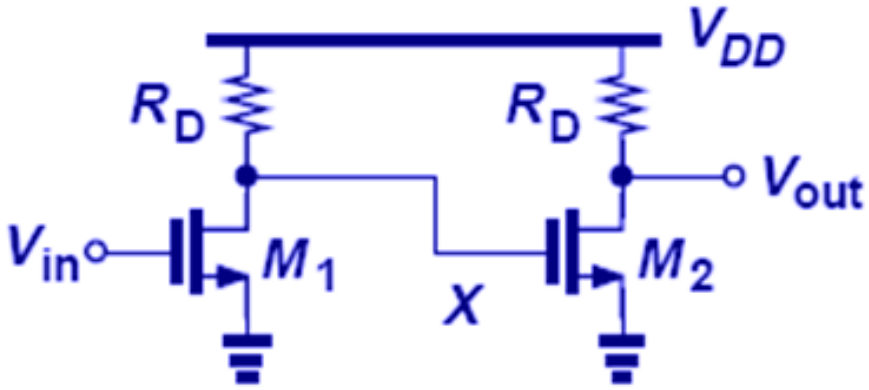
$$\approx (I_D V_{DD}) \cdot (R_D C_X) = \frac{V_{DD}^2}{R_D + R_{on1}} \cdot (R_D C_X)$$

$$\approx V_{DD}^2 C_X, \text{ since typically } R_D \gg R_{on1}.$$

- **The power delay product of an NMOS Inverter can be loosely thought of as the amount of energy the gate uses in each switching event.**

Example 15.12: Power-Delay Product

Assuming T_{PLH} is roughly equal to three time constants, determine the power-delay product for the low-to-high transitions at node X



T_{PLH}: Propagation delay time for the low-to-high transition

$$T_{PLH} \approx 3R_D C_X$$

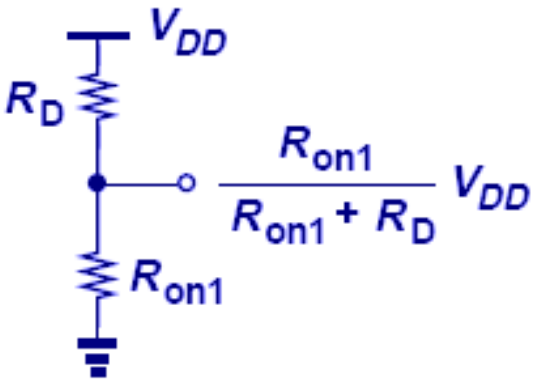
$$PDP = (I_D V_{DD})(3R_D C_X)$$

$$PDP = 3V_{DD}^2 WLC_{ox}$$

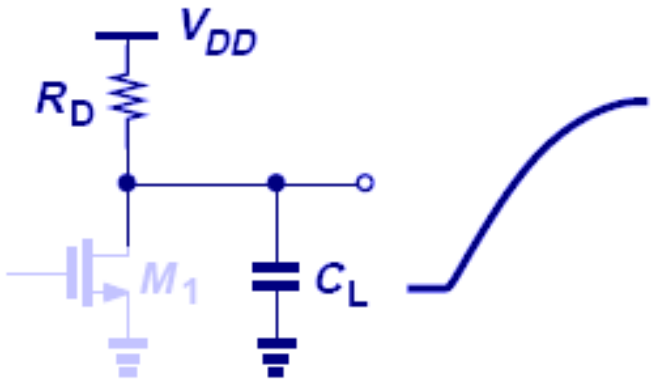
Summary

- Digital CMOS circuits account for more than 80% of the semiconductor market.
- The speed, power dissipation, and noise immunity of digital gates are critical parameters
- The input/output characteristic of a gate reveals its immunity to noise or degraded logical levels
- Noise margin is defined as the voltage degradation on the high or low levels that places the signal at the unit-gain point of the input/output characteristic
- The speed of gates is given by the drive capability of the transistors and the capacitances contributed by transistors and interconnecting wires
- The power-speed trade-off of gates is quantified by the power-delay product

Drawbacks of NMOS Inverter



(a)



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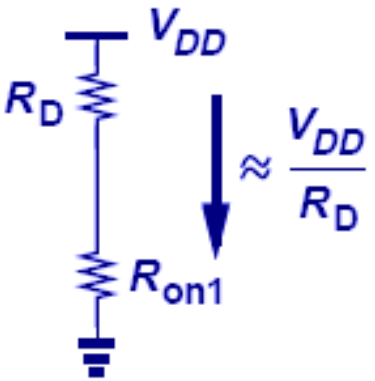


(c)

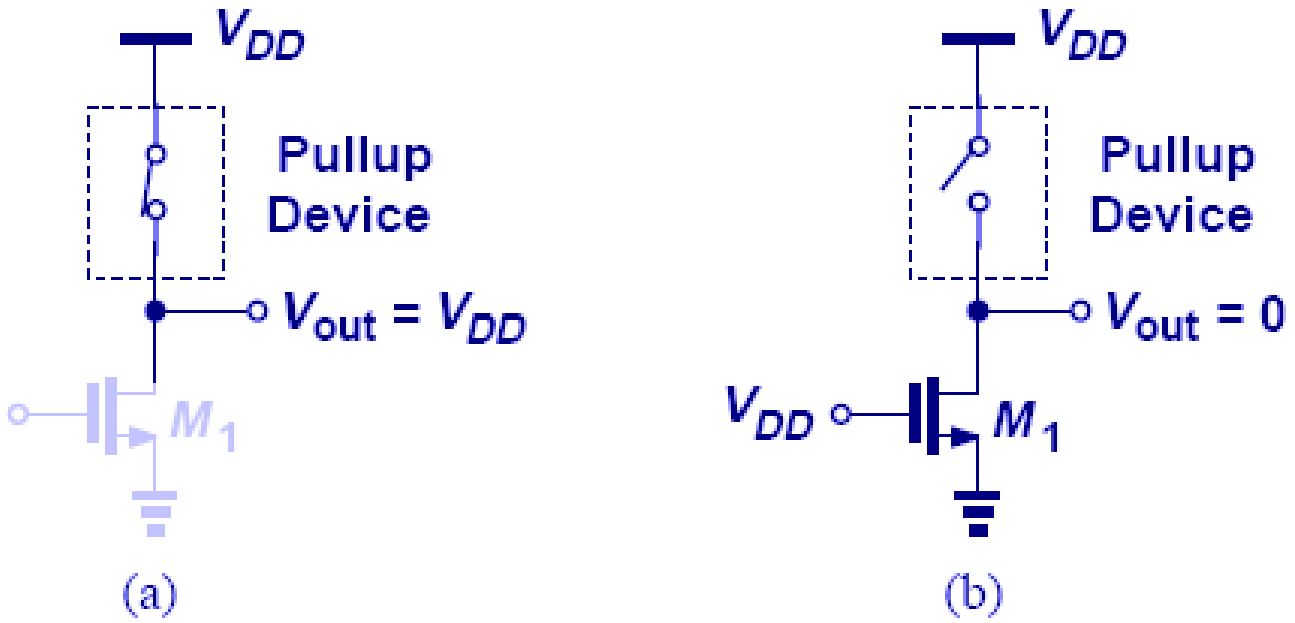
Risetime limitation due to R_D

Static power consumption during output level low

- **Because of constant R_D, NMOS inverter consumes static power even when there is no switching.**
- **R_D presents a tradeoff between speed and power dissipation.**

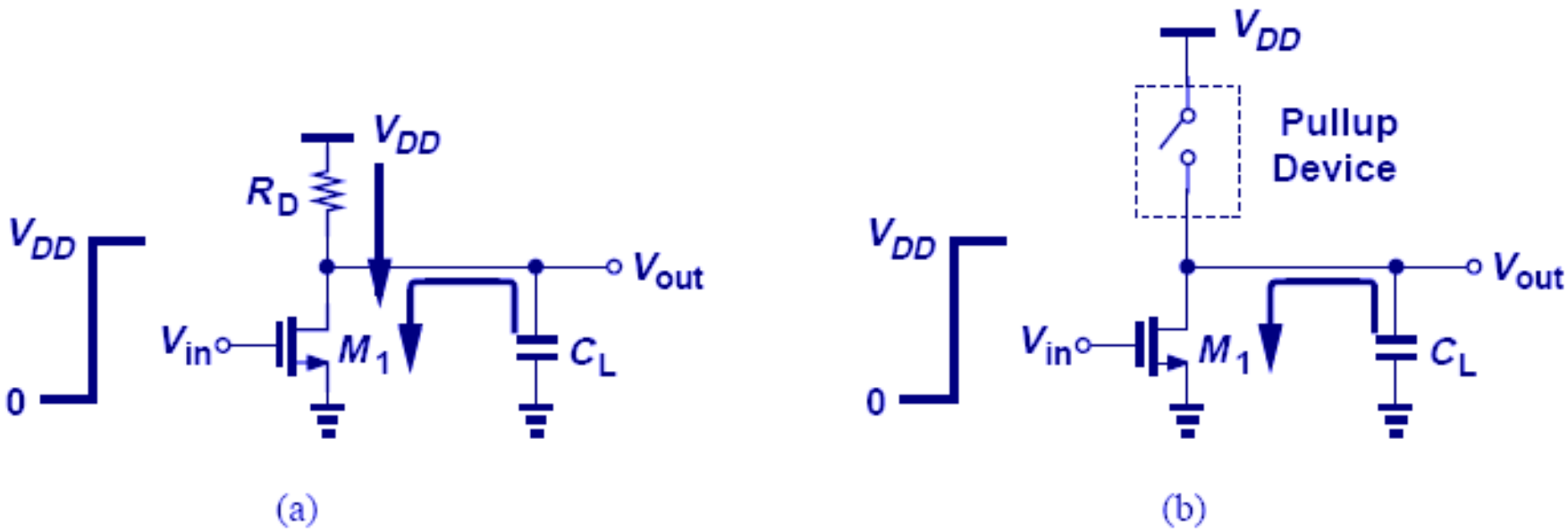
$$V_{DD}^2 / R_D$$

Improved Inverter Topology



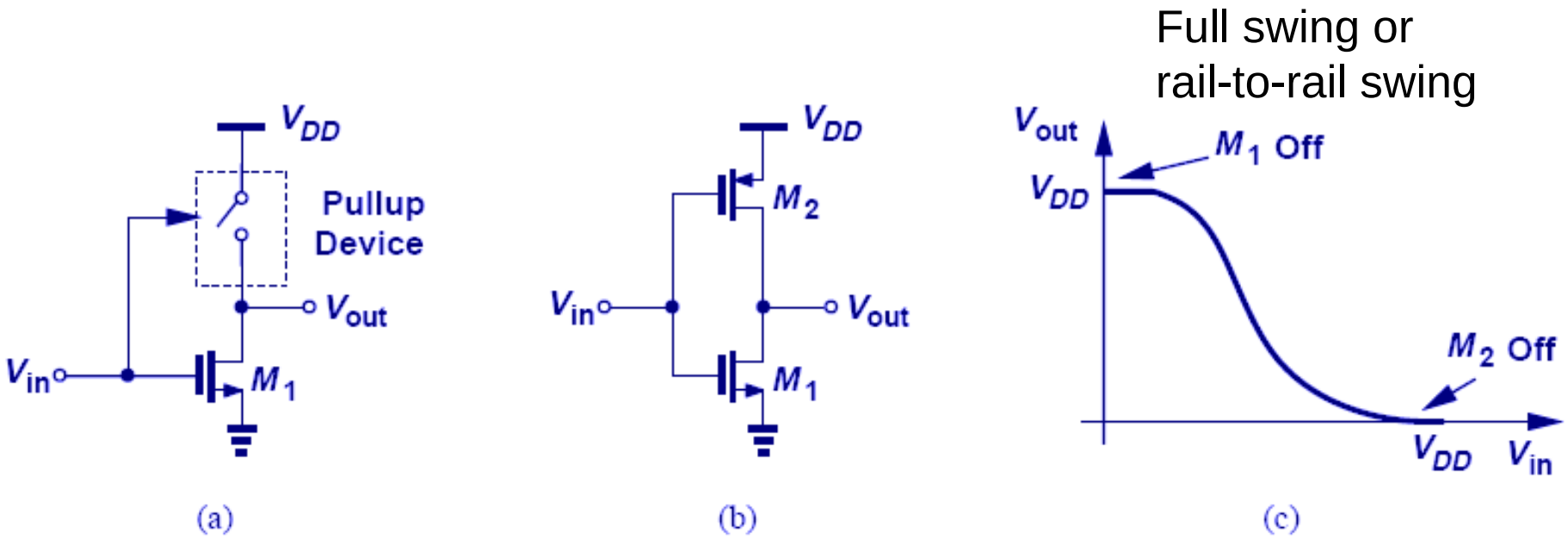
- **A better alternative would probably have been an "intelligent" pullup device that turns on when M_1 is off and vice versa.**

Improved Fall Time



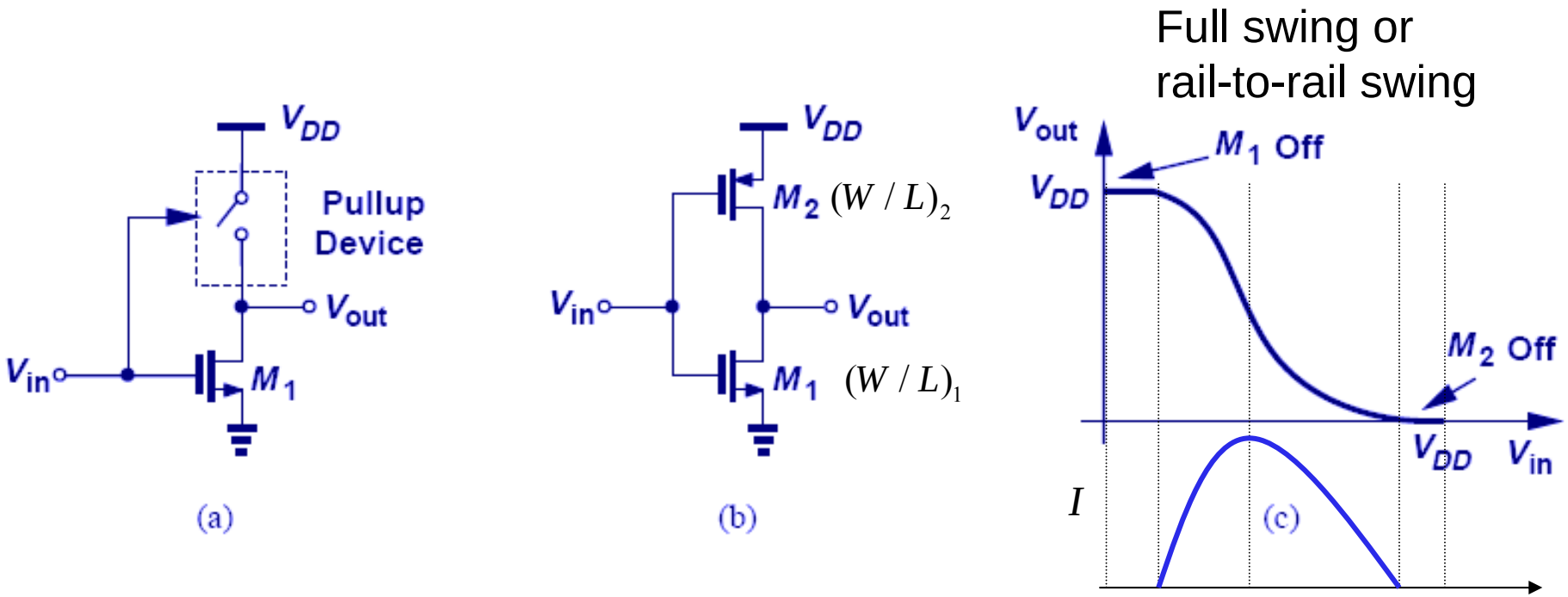
- **This improved inverter topology decreases fall time since all of the current from M_1 is available to discharge the capacitor.**

CMOS Inverter



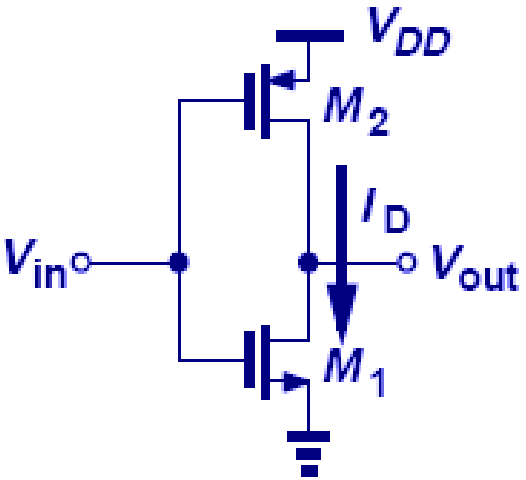
- **A circuit realization of this improved inverter topology is the CMOS inverter shown above.**
- **The NMOS/PMOS pair complement each other to produce the desired effects.**

CMOS Inverter

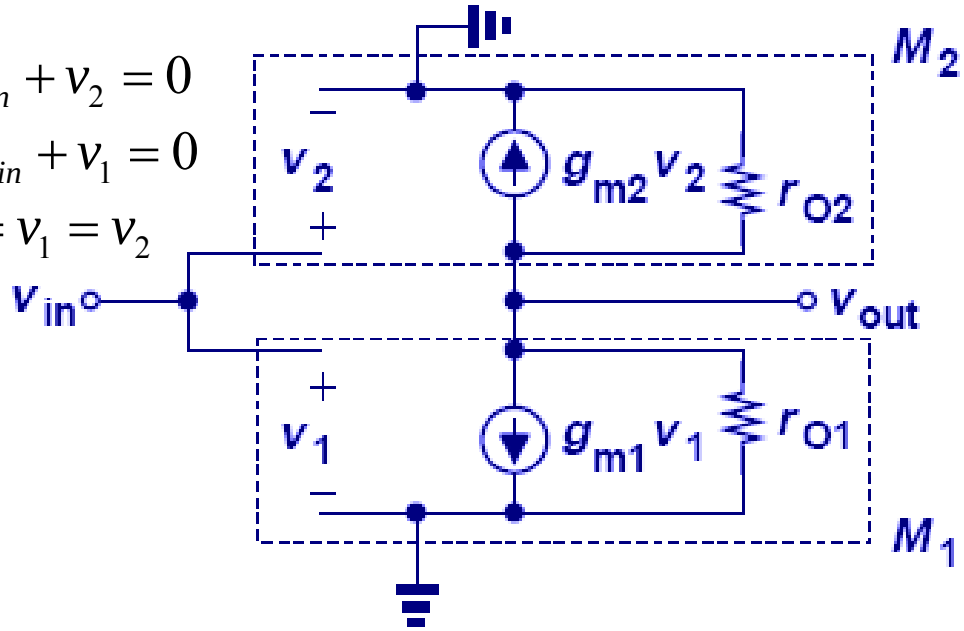


- **A circuit realization of this improved inverter topology is the CMOS inverter shown above.**
- **The NMOS/PMOS pair complement each other to produce the desired effects.**

CMOS Inverter Small-Signal Model



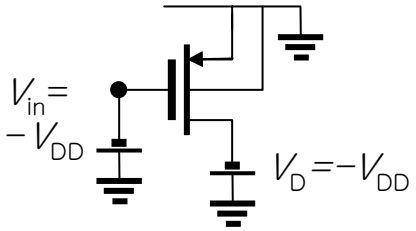
$$-v_{in} + v_2 = 0$$
$$-v_{in} + v_1 = 0$$
$$v_{in} = v_1 = v_2$$



$$\frac{v_{out}}{v_{in}} = -\left(g_{m1} + g_{m2}\right)\left(r_{O1} \| r_{O2}\right)$$

- **When both M_1 and M_2 are in saturation, the small-signal gain is shown above.**

Operation of PMOS Device

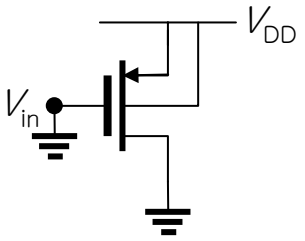


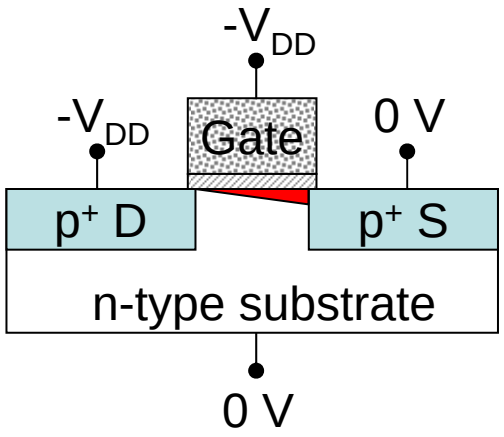
In saturation region

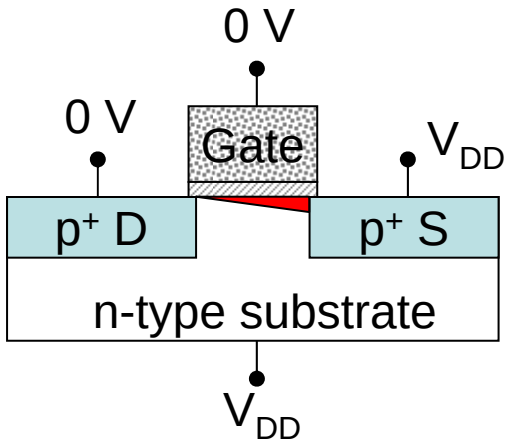
$$-V_{DS} \geq -V_{GS} - (-V_{TH})$$

$$V_{DS} \leq V_{GS} + V_{TH} \sim > 0$$

$$V_{DS} \leq V_{GS} + |V_{TH}|$$







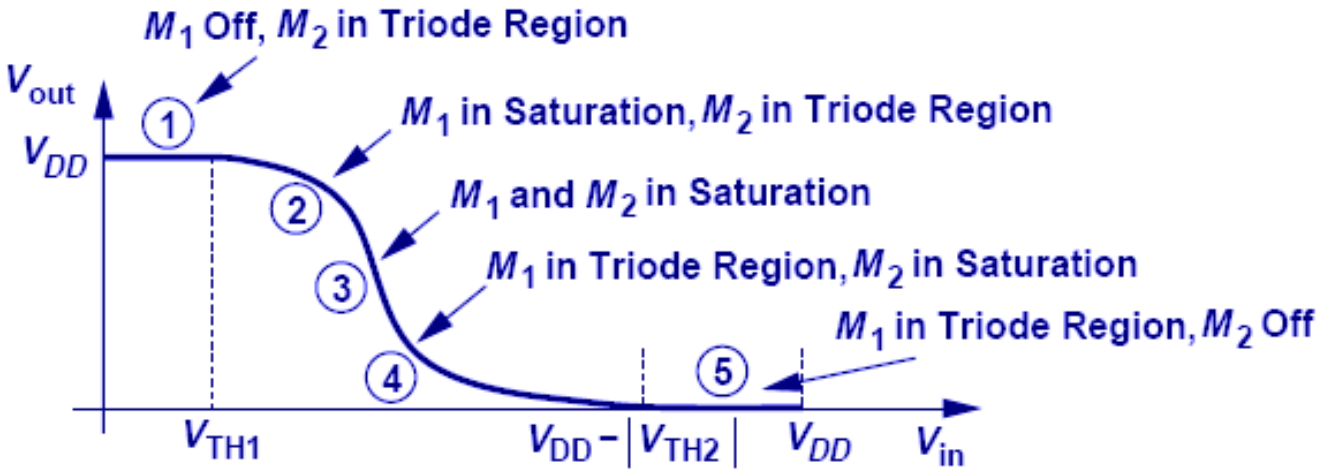
$$V_{GS} = V_G - V_S = 0 - V_{DD}$$

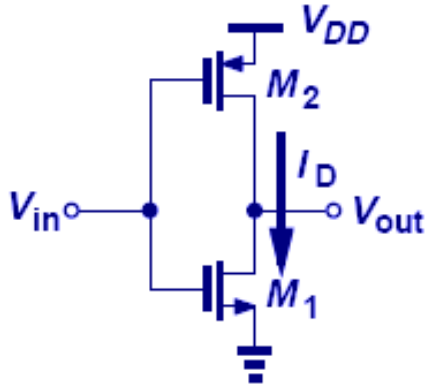
$$V_{DS} = V_D - V_S = 0 - V_{DD}$$

$$V_{GS} = V_G - V_S = -V_{DD} - 0$$

$$V_{DS} = V_D - V_S = -V_{DD} - 0$$

Voltage Transfer Curve of CMOS Inverter





Region 1: M_1 is off and M_2 is on. $V_{out}=V_{DD}$.

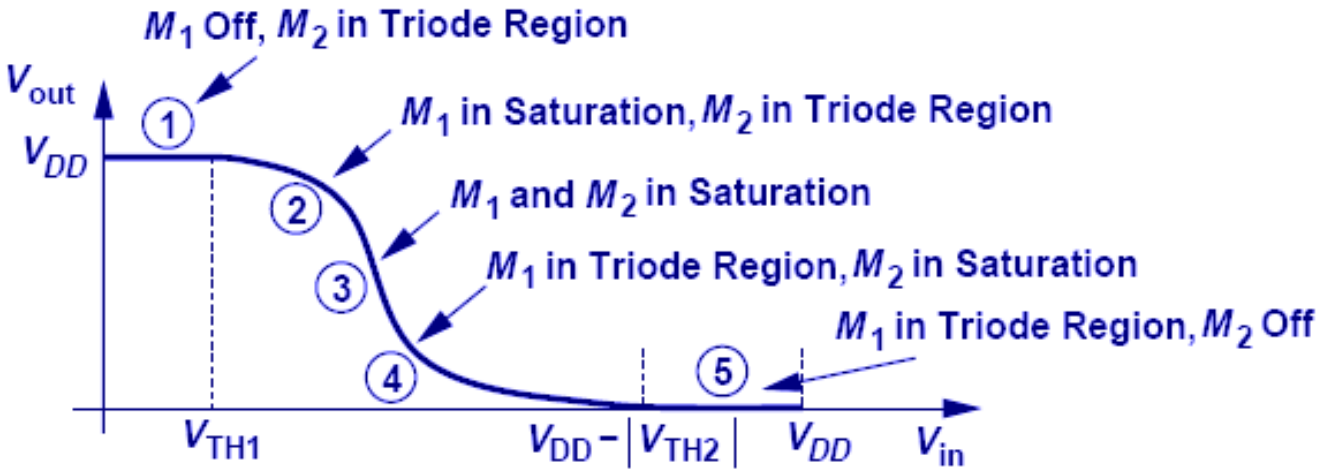
Region 2: M_1 is in saturation and M_2 is in triode region ($V_{in} \approx V_{TH1}+\Delta$).
Valid only when $V_{out} > V_{in} + |V_{TH2}|$.

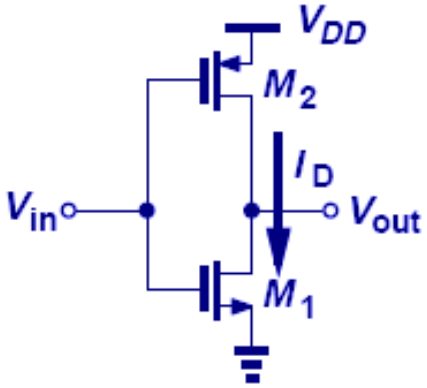
$V_{out} = V_{in} + |V_{TH2}| \rightarrow M_2$ is about to exit the triode region

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in}-V_{TH1})^2 = \mu_p C_{ox}\left(\frac{W}{L}\right)_2 \left[2(V_{DD}-V_{in}-|V_{TH2}|)(V_{DD}-V_{out})-(V_{DD}-V_{out})^2\right]$$

This quadratic equation can be solved in terms of $V_{DD}-V_{out} \rightarrow V_{out} = f(V_{in})$.

Voltage Transfer Curve of CMOS Inverter



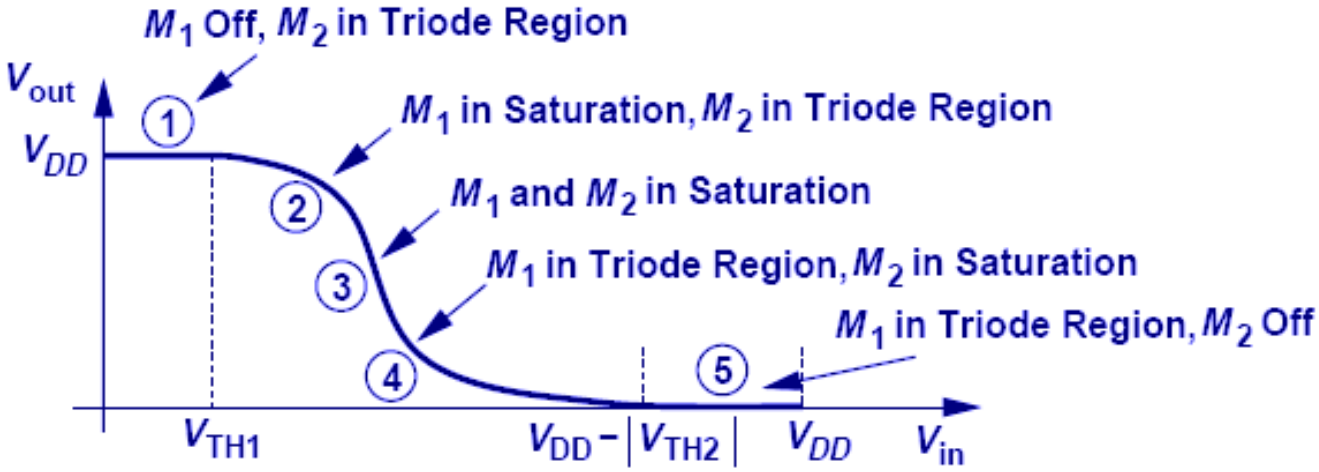


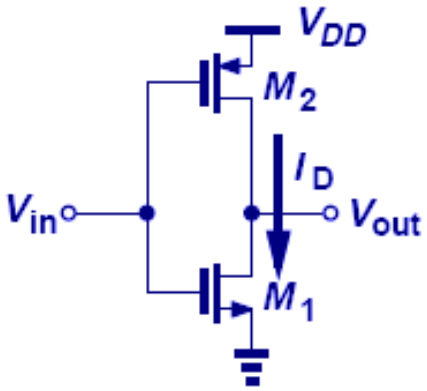
Region 3: M_1 and M_2 are in saturation. Apperas as vertical line assuming no channel-length modulation. Valid when $V_{in} - V_{TH1} \le V_{out} \le V_{in} + |V_{TH2}|$.

Solving $\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{in} - |V_{TH2}|)^2$,

$$V_{in} = \frac{\sqrt{\mu_n\left(\frac{W}{L}\right)_1}\cdot V_{TH1} + \sqrt{\mu_p\left(\frac{W}{L}\right)_2}\cdot(V_{DD} - |V_{TH2}|)}{\sqrt{\mu_n\left(\frac{W}{L}\right)_1} + \sqrt{\mu_p\left(\frac{W}{L}\right)_2}}$$

Voltage Transfer Curve of CMOS Inverter





Region 4: Similar to Region 2. M_1 is in triode region and M_2 is in saturation. Valid only when $V_{out} \leq V_{in} - V_{TH1}$.

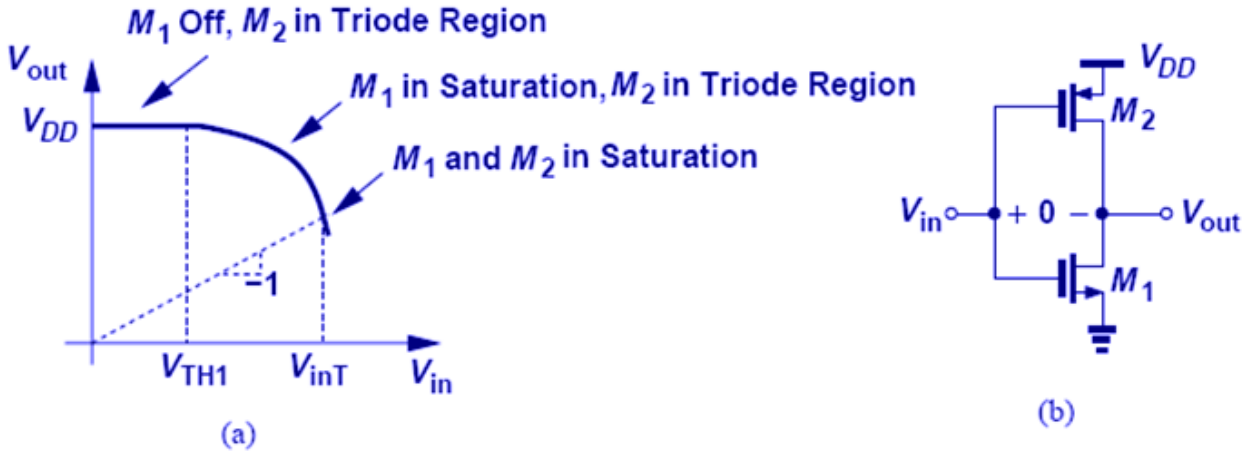
$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[2(V_{in}-V_{TH1})V_{out}-V_{out}^{\,2}\right]=\mu_p C_{ox}\left(\frac{W}{L}\right)_2(V_{DD}-V_{in}-|V_{TH2}|)^2$$

This quadratic equation can be solved in terms of $V_{DD}-V_{out} \rightarrow V_{out} = f(V_{in})$.

Region 5: M_1 is on and M_2 is off. V_{out}=0.

Example 15.14: Switching Threshold

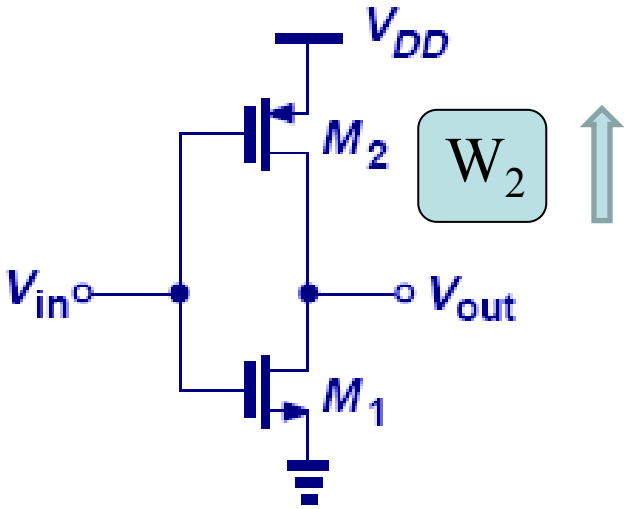
The switching threshold or the "trip point" of the inverter is when V_{out} equals V_{in}. Determine a relationship between $(W/L)_1$ and $(W/L)_2$ that sets the trip point of the CMOS inverter to $V_{DD}/2$, thus providing a "symmetric" VTC

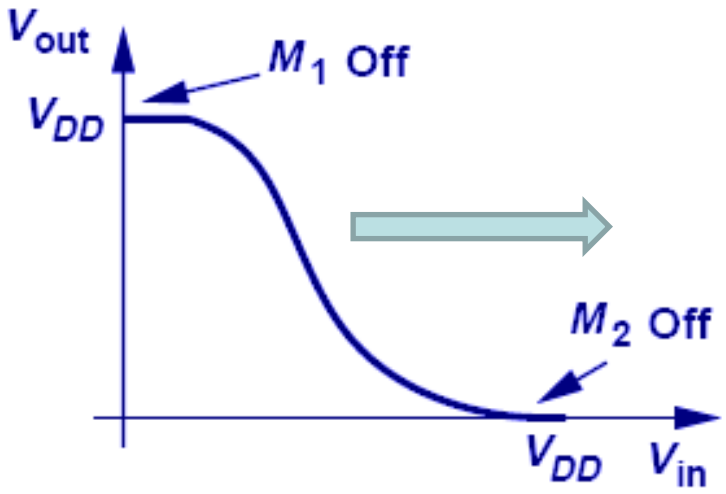


$$\mu_n C_{ox}\left(\frac{W}{L}\right)_1\left(\frac{V_{DD}}{2}-V_{TH1}\right)^2\left(1+\lambda_1\frac{V_{DD}}{2}\right)=\mu_p C_{ox}\left(\frac{W}{L}\right)_2\left(\frac{V_{DD}}{2}-|V_{TH2}|\right)^2\left(1+\lambda_2\frac{V_{DD}}{2}\right)$$

$$\text{Assuming } 1+\lambda_1\left(\frac{V_{DD}}{2}\right)\approx 1+\lambda_2\left(\frac{V_{DD}}{2}\right),\ \frac{W_1}{W_2}\approx\frac{\mu_p}{\mu_n} \qquad \mu_n\approx 2.5\mu_p,\ W_2\approx 2.5W_1$$

Example 15.15: VTC





- **As the PMOS device is made stronger, NMOS device requires higher input voltage to establish $I_{D1}=I_{D2}$. Thus, the VTC is shifted to the right.**

Noise Margins

V_{IL} is the low-level input voltage at which ($\delta V_{out}/\ \delta V_{in}$) = -1

In Region 2,

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in}-V_{TH1})^2 = \mu_p C_{ox}\left(\frac{W}{L}\right)_2 \left[2(V_{DD}-V_{in}-|V_{TH2}|)(V_{DD}-V_{out})-(V_{DD}-V_{out})^2\right]$$

Differentiating both sides with respect to V_{in},

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in}-V_{TH1}) =$$

$$\mu_p C_{ox}\left(\frac{W}{L}\right)_2 \left[-2(V_{DD}-V_{out})-2(V_{DD}-V_{in}-|V_{TH2}|)\frac{\delta V_{out}}{\delta V_{in}}+2(V_{DD}-V_{out})\frac{\delta V_{out}}{\delta V_{in}}\right]$$

With $\dfrac{\delta V_{out}}{\delta V_{in}} = -1$,

$$\mu_n\left(\frac{W}{L}\right)_1 (V_{in}-V_{TH1}) = \mu_p\left(\frac{W}{L}\right)_2 (2V_{out}-V_{in}-|V_{TH2}|-V_{DD})$$

Noise Margins

Assuming $a = \mu_n \left(\frac{W}{L}\right)_1 \Big/ \mu_p \left(\frac{W}{L}\right)_2$, we must solve

$a\left(V_{in} - V_{TH1}\right) = \left(2V_{out} - V_{in} - |V_{TH2}| - V_{DD}\right)$ and

$$\frac{a}{2}\left(V_{in} - V_{TH1}\right)^2 = \left[2\left(V_{DD} - V_{in} - |V_{TH2}|\right)\left(V_{DD} - V_{out}\right) - \left(V_{DD} - V_{out}\right)^2\right]$$

Deleting V_{out}, we get $A \cdot V_{in}^2 + B \cdot V_{in} + C = 0,$ where $A = \frac{1}{8}(a-1)(a+3),$

$$B = \frac{1}{4}(a+3)(V_{DD} - aV_{TH1} - |V_{TH2}|), C = -\frac{1}{8}[3(V_{DD} - |V_{TH2}|)^2 + 2aV_{TH1}(V_{DD} - |V_{TH2}|) - a(a+4){V_{TH1}}^2].$$

$$V_{IL} = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} = \frac{-B \pm \sqrt{\frac{1}{4}a(a+3)(V_{DD} - V_{TH1} - |V_{TH2}|)^2}}{2A}$$

$$= \frac{-\frac{1}{4}(a+3)(V_{DD} - aV_{TH1} - |V_{TH2}|) \pm \frac{1}{2}\sqrt{a(a+3)}(V_{DD} - V_{TH1} - |V_{TH2}|)}{2 \cdot \frac{1}{8}(a-1)(a+3)}$$

$$= \frac{2\sqrt{a}(V_{DD} - V_{TH1} - |V_{TH2}|)}{(a-1)\sqrt{a+3}} - \frac{(V_{DD} - aV_{TH1} - |V_{TH2}|)}{a-1}$$

Noise Margins

$$V_{IL} = NM_L = \frac{2\sqrt{a}\left(V_{DD} - V_{TH1} - |V_{TH2}|\right)}{(a-1)\sqrt{a+3}} - \frac{V_{DD} - aV_{TH1} - |V_{TH2}|}{a-1}, \text{ where } a = \frac{\mu_n \left(\frac{W}{L}\right)_1}{\mu_p \left(\frac{W}{L}\right)_2}.$$

Assuming symmetry, $(a = 1,\ V_{TH1} = |V_{TH2}| = V_{TH})$,

$$V_{IL} = NM_L = \frac{3}{8}V_{DD} + \frac{1}{4}V_{TH}.$$

Noise Margins

V_{IH} is the high-level input voltage at which ($\delta V_{out}/\delta V_{in}$) = -1.

$$V_{IH} = V_{DD} - V_{IL}\Big|_{a\to 1/a,\,V_{TH1}\to|V_{TH2}|,\,|V_{TH2}|\to V_{TH1}}$$

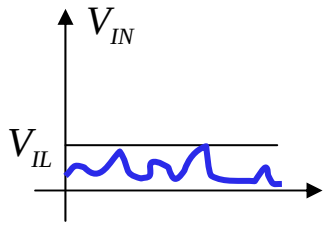
$$= \frac{2a\left(V_{DD} - V_{TH1} - |V_{TH2}|\right)}{(a-1)\sqrt{1+3a}} - \frac{V_{DD} - aV_{TH1} - |V_{TH2}|}{a-1}$$

Assuming symmetry, $V_{TH1} = |V_{TH2}| = V_{TH}$ and $\mu_n \left(\frac{W}{L}\right)_1 = \mu_p \left(\frac{W}{L}\right)_2$,

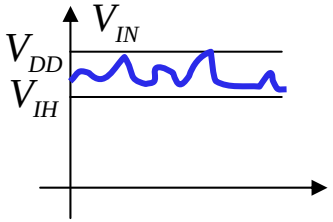
$$V_{IH} = \frac{5}{8}V_{DD} - \frac{1}{4}V_{TH}$$

$$NM_H = V_{DD} - V_{IH} = \frac{3}{8}V_{DD} + \frac{1}{4}V_{TH}$$

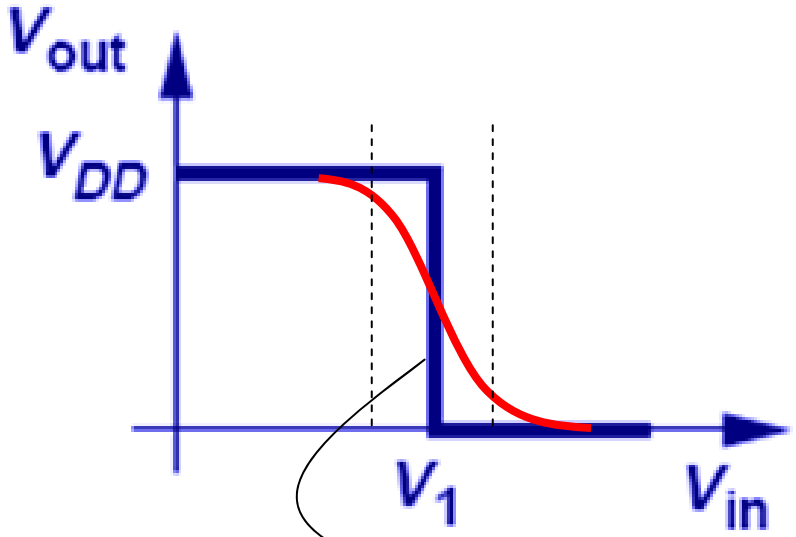
Example 15.17: Noise Margins of Ideal Inverter



$$NM_L = V_{IL}$$



$$NM_H = V_{DD} - V_{IH}$$

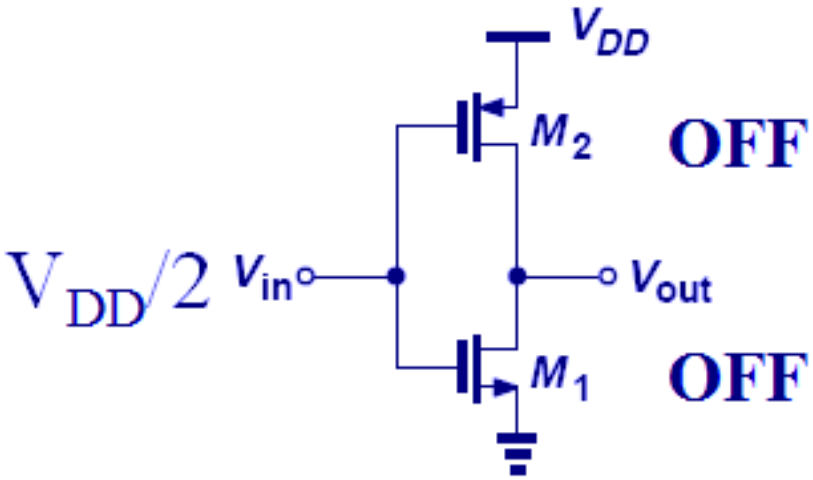


$$NM_{H,ideal} = NM_{L,ideal} = \frac{V_{DD}}{2}$$

$$\frac{1}{2}V_{DD} > \quad NM_L = NM_H = \frac{3}{8}V_{DD} + \frac{1}{4}V_{TH}$$

$$\because V_{TH} < \frac{1}{2}V_{DD}$$

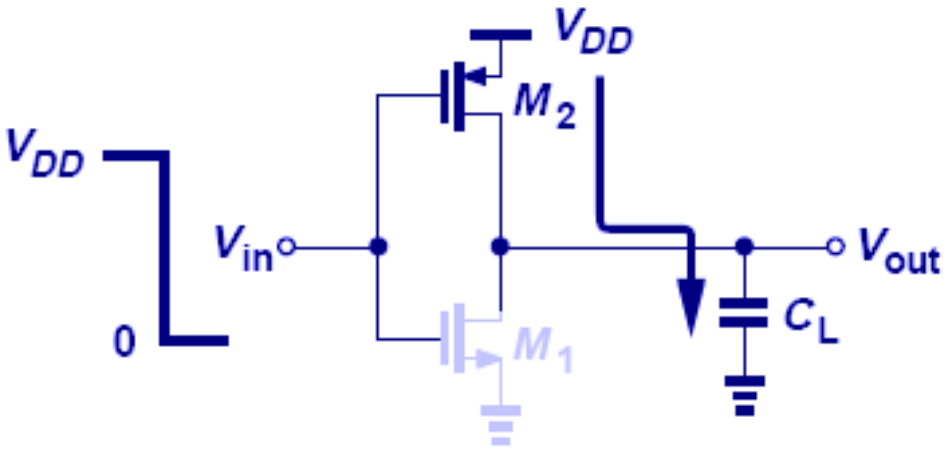
Example 15.18: Floating Output



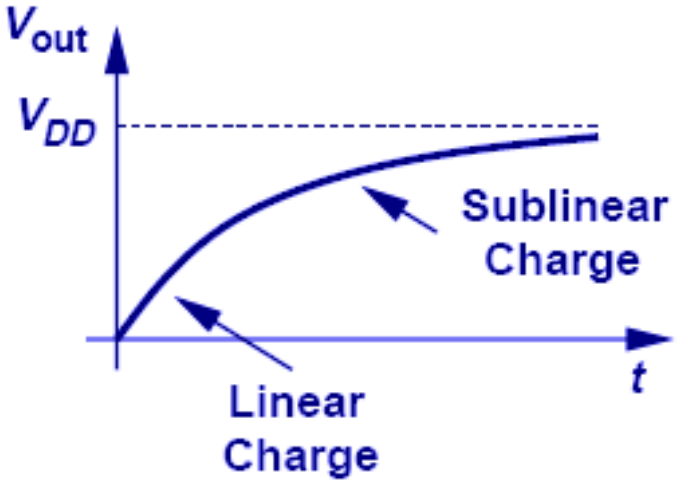
$$V_{TH1} > V_{DD}/2$$
$$|V_{TH2}| > V_{DD}/2$$

- When $V_{in}=V_{DD}/2$, M_1 and M_2 will both be off and the output floats.

Charging Dynamics of CMOS Inverter



(a)



(b)

- As V_{out} is initially charged high, the charging is linear since M_2 is in saturation. However, as M_2 enters the triode region the charge rate becomes sublinear.

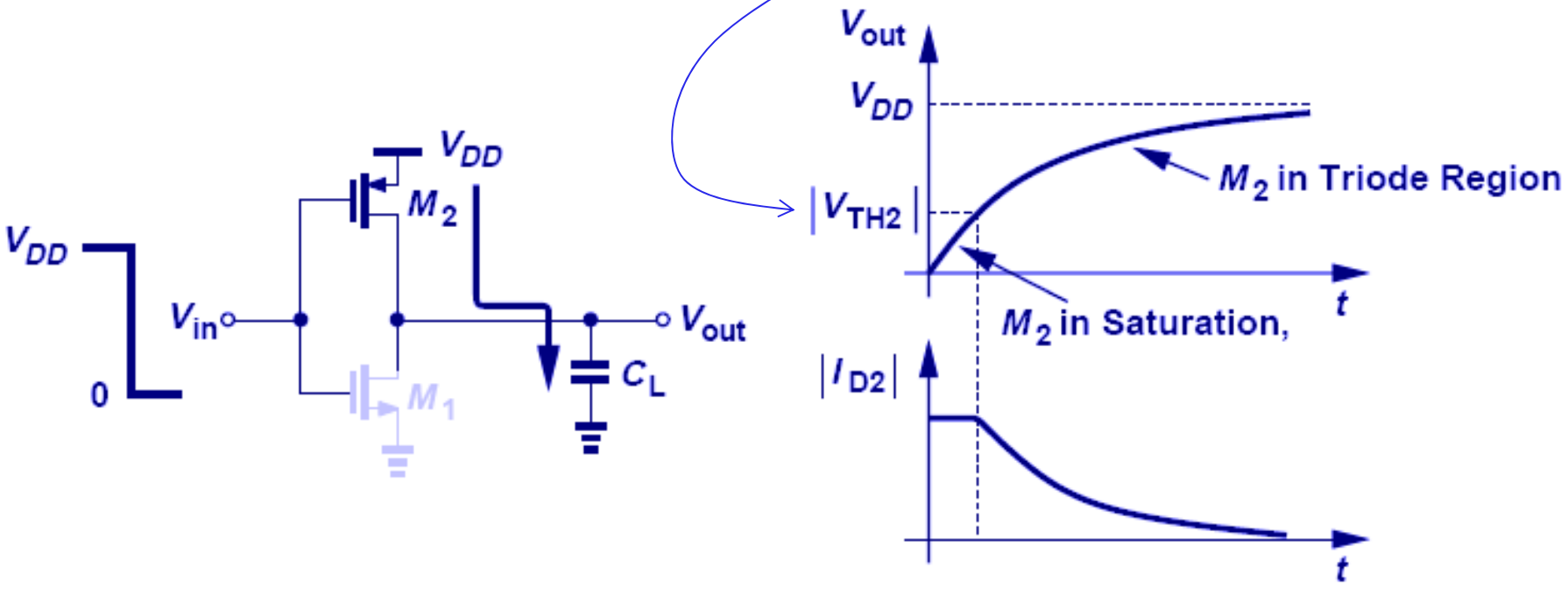
Example 15.19: Charging Current

In saturation region

$$V_{DS} \le V_{GS} + |V_{TH}|$$

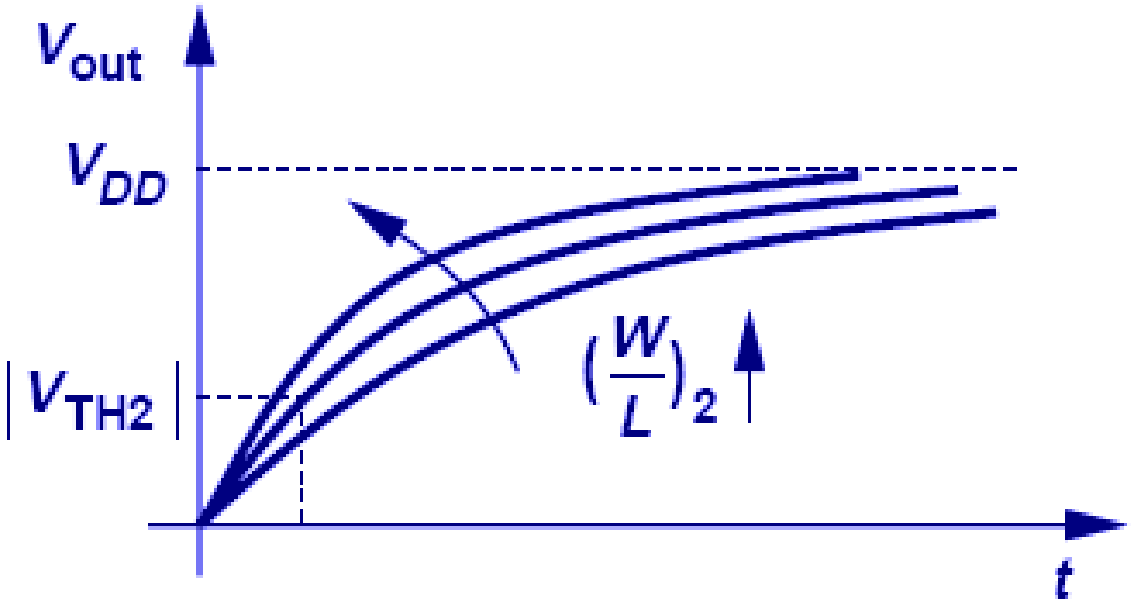
At boundary

$$|V_{TH2}| - V_{DD} \le 0 - V_{DD} + |V_{TH2}|$$



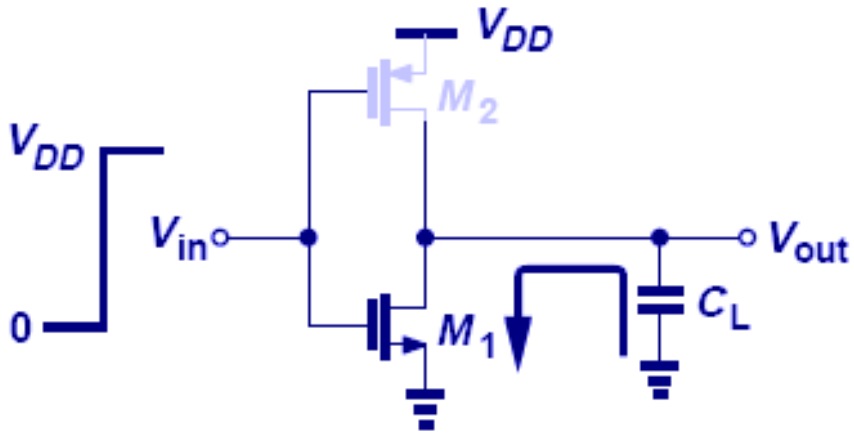
- The current of M_2 is initially constant as M_2 is in saturation. However as M_2 enters the triode region, its current decreases.

Example 15.20: Variation of Output Waveform

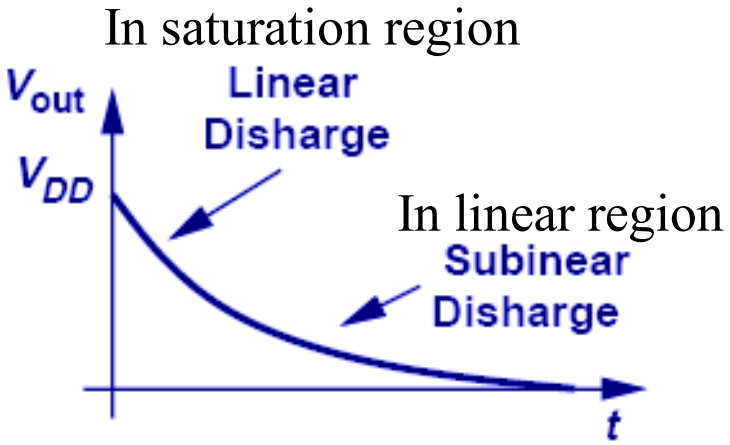


- **As the PMOS size is increased, the output exhibits a faster transition.**

Discharging Dynamics of CMOS Inverter



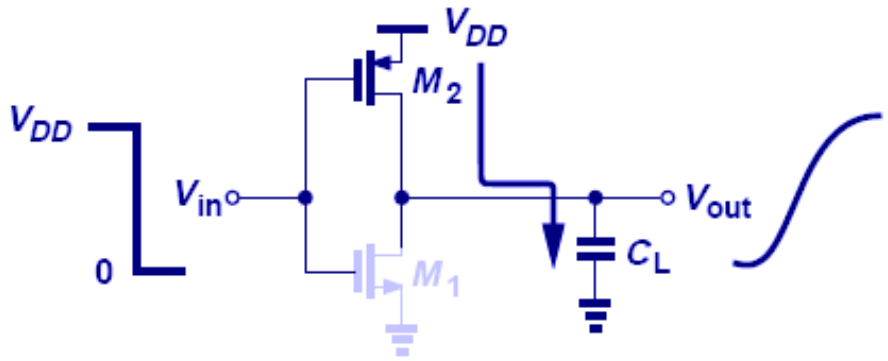
(a)

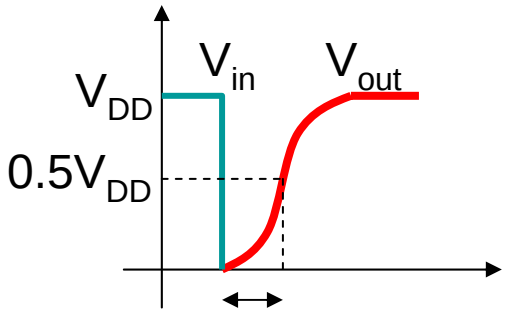


(b)

- **Similar to the charging dynamics, the discharge is linear when M_1 is in saturation and becomes sublinear as M_1 enters the triode region.**

Rise Delay





Initially, M_2 is in saturation,

$$|I_{D2}| = \mu_p C_{ox}\left(\frac{W}{L}\right)_2 \left(V_{DD} - |V_{TH2}|\right)^2$$

$$V_{out}(t) = \frac{|I_{D2}|}{C_L} t, \text{only up to } V_{out} = |V_{TH2}|.$$

$$\text{Thus, } T_{PLH1} = \frac{2|V_{TH2}|C_L}{\mu_p C_{ox}\left(\frac{W}{L}\right)_2 \left(V_{DD} - |V_{TH2}|\right)^2}$$

Rise Delay

Thereafter M_2 operates in the triode region,

$$|I_{D2}| = C_L \frac{dV_{out}}{dt}$$

$$\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2\left[2\left(V_{DD}-|V_{TH2}|\right)\left(V_{DD}-V_{out}\right)-\left(V_{DD}-V_{out}\right)^2\right] = C_L\frac{dV_{out}}{dt}$$

$$\frac{dV_{out}}{2\left(V_{DD}-|V_{TH2}|\right)\left(V_{DD}-V_{out}\right)-\left(V_{DD}-V_{out}\right)^2} = \frac{1}{2}\mu_p\frac{C_{ox}}{C_L}\left(\frac{W}{L}\right)_2 dt$$

Integrating from $V_{out} = |V_{TH2}|$ to $V_{DD}/2$, $\quad V_{DD}-V_{out} = u \qquad \int\frac{du}{au-u^2} = \frac{1}{a}ln\frac{u}{a-u}$

$$T_{PLH2} = \frac{C_L}{\mu_p C_{ox}\left(\frac{W}{L}\right)_2\left(V_{DD}-|V_{TH2}|\right)}\ln\left(3-4\frac{|V_{TH2}|}{V_{DD}}\right) = R_{on2}C_L\ln\left(3-4\frac{|V_{TH2}|}{V_{DD}}\right)$$

Thus,

$$T_{PLH} = T_{PLH1}+T_{PLH2}$$

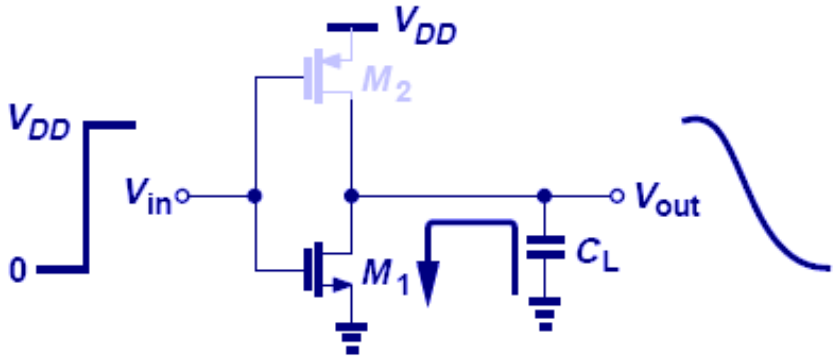
$$= R_{on2}C_L\left[\frac{2|V_{TH2}|}{V_{DD}-|V_{TH2}|}+\ln\left(3-4\frac{|V_{TH2}|}{V_{DD}}\right)\right]$$

Fall Delay

Similarly,

$$T_{PHL} = \frac{C_L}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[V_{DD} - |V_{TH1}|\right]}\left[\frac{2|V_{TH1}|}{V_{DD} - V_{TH1}} + \ln\left(3 - 4\frac{V_{TH1}}{V_{DD}}\right)\right]$$

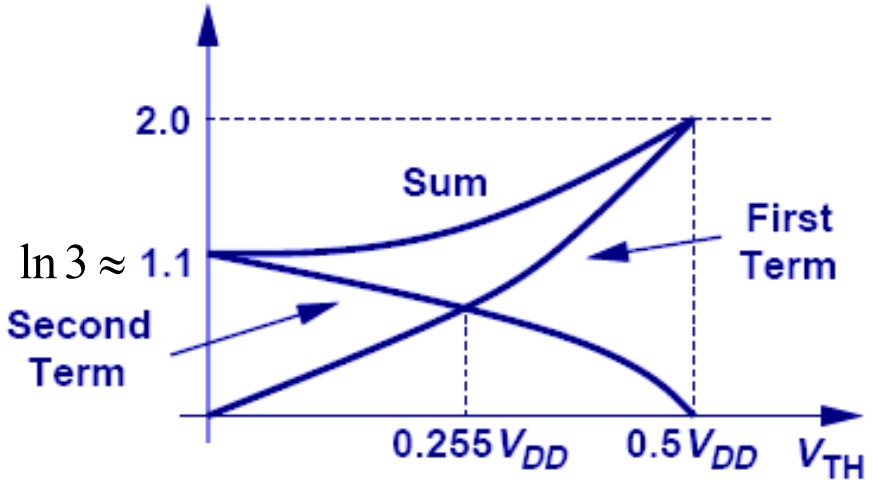
$$= R_{on1}C_L\left[\frac{2|V_{TH1}|}{V_{DD} - V_{TH1}} + \ln\left(3 - 4\frac{V_{TH1}}{V_{DD}}\right)\right]$$



Example 15.22: Delay vs. Threshold Voltage

Compare the two terms inside the square brackets as V_{TH1} varies from zero to $V_{DD}/2$

V_{TH} is zero, [ ] term is ln3

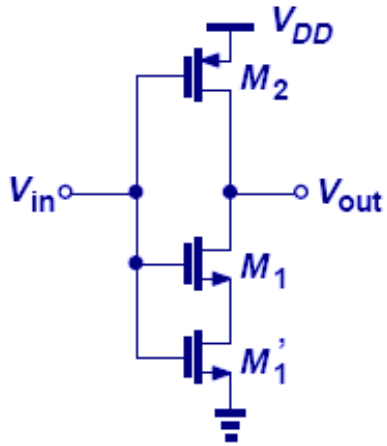


$$T_{PLH/HL} = \frac{C_L}{\mu_{p/n} C_{ox} \left(\frac{W}{L}\right)_{2/1} \left[V_{DD} - |V_{TH2/1}|\right]} \left[\frac{2|V_{TH2/1}|}{V_{DD} - V_{TH2/1}} + \ln\left(3 - 4\frac{V_{TH2/1}}{V_{DD}}\right)\right]$$

- **The sum of the 1st and 2nd terms of the bracket is the smallest when V_{TH} is the smallest, hence low V_{TH} improves speed.**

Example 15.23: Effect of Series Transistor

M_1' appears in series with M_1 and is identical to M_1. Explain what happens to the output fall time.

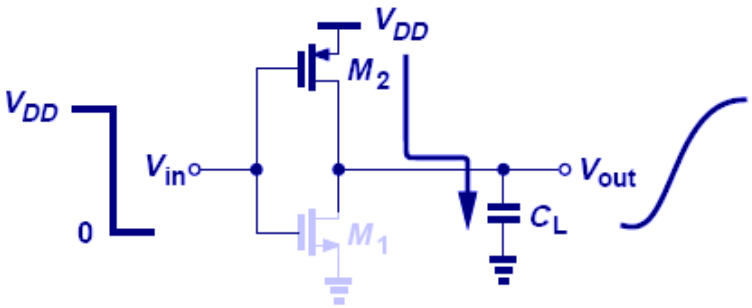


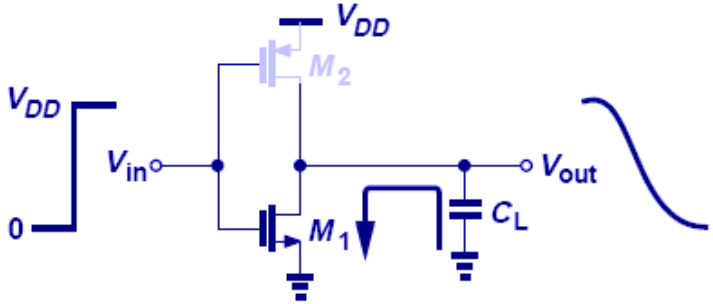
$$R_{on} = R_{on1} + R_{on1'}$$
$$= \frac{1}{\mu_n C_{ox}(\frac{W}{L})_1(V_{DD} - V_{TH1})} + \frac{1}{\mu_n C_{ox}(\frac{W}{L})'_1(V_{DD} - V'_{TH1})}$$
$$= 2R_{on1}$$

➢ **Since pull-down resistance is doubled, the fall time is also doubled.**

Power Dissipation of the CMOS Inverter

The PMOS also consumes power because it carries a finite current while a sustaining a finite voltage





Energy stored in C_L

$$E_1 = \frac{1}{2} C_L V_{DD}^2$$

Energy consumed by M_2 ($|V_{DS2}|$, $|I_{D2}|$)

$$E_2 = \int_{t=0}^{\infty} (V_{DD} - V_{out})(C_L \frac{dV_{out}}{dt}) dt$$

$$= C_L \int_{V_{out}=0}^{V_{out}=V_{DD}} (V_{DD} - V_{out}) dV_{out}$$

$$= \frac{1}{2} C_L V_{DD}^2$$

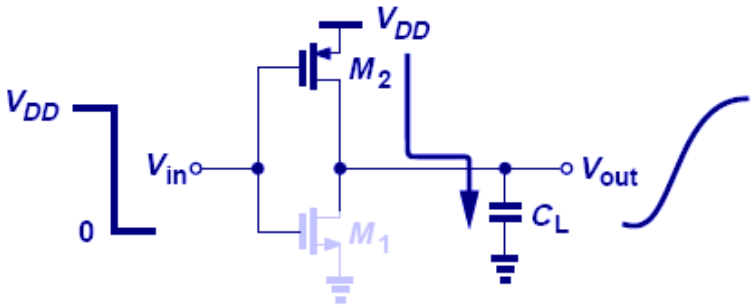
Thus, total energy consumed in one cycle is

$$E_{tot} = E_1 + E_2$$

$$= C_L V_{DD}^2$$

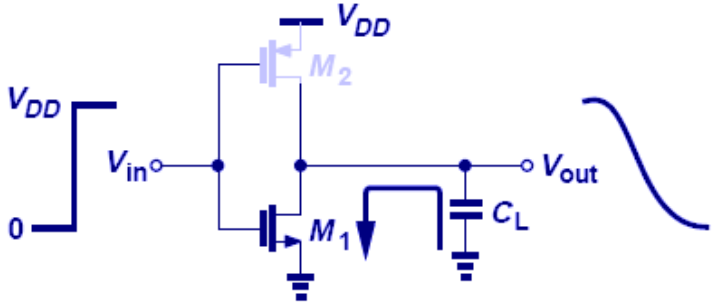
Power Dissipation of the CMOS Inverter

For a periodic input with frequency f_{in}, the average power drawn from V_{DD} is equal to



$$P_{Dissipation\_PMOS} = \frac{1}{2} C_L V_{DD}^2 f_{in}$$

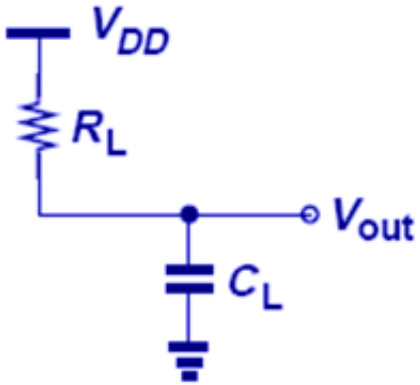
$$P_{supply} = C_L V_{DD}^2 f_{in}$$



$$P_{Dissipation\_NMOS} = \frac{1}{2} C_L V_{DD}^2 f_{in}$$

Example 15.24: Energy Calculation

Compute the energy drawn from the supply as $V_{out} = 0 \rightarrow V_{DD}$.



$$E_{stored} = \frac{1}{2} C_L V_{DD}^2$$

$$E_{dissipated} = \frac{1}{2} C_L V_{DD}^2$$

$$E_{drawn} = C_L V_{DD}^2$$

Energy stored in C_L

$$E_{stored} = \frac{1}{2} C_L V_{DD}^2$$

An energy consumed in R_1 while charging C_L

$$E_{dissipated} = \int_{t=0}^{\infty} (V_{DD} - V_{out})(C_L \frac{dV_{out}}{dt}) dt$$

$$= C_L \int_{V_{out}=0}^{V_{out}=V_{DD}} (V_{DD} - V_{out}) dV_{out}$$

$$= \frac{1}{2} C_L V_{DD}^2$$

Power Delay Product

The trade-off between the power dissipation and the speed

$$T_{PLH/HL} = \frac{C_L}{\mu_{p/n} C_{ox} \left(\frac{W}{L}\right)_{2/1} \left[V_{DD} - |V_{TH2/1}|\right]} \left[\frac{2|V_{TH2/1}|}{V_{DD} - V_{TH2/1}} + \ln\left(3 - 4\frac{V_{TH2/1}}{V_{DD}}\right)\right]$$

$$\because PDP = \text{Power} \cdot \frac{T_{PHL} + T_{PLH}}{2} \qquad \because R_{on2/1} = \frac{1}{\mu_{p/n} C_{ox} \left(\frac{W}{L}\right)_{2/1} \left[V_{DD} - |V_{TH2/1}|\right]}$$

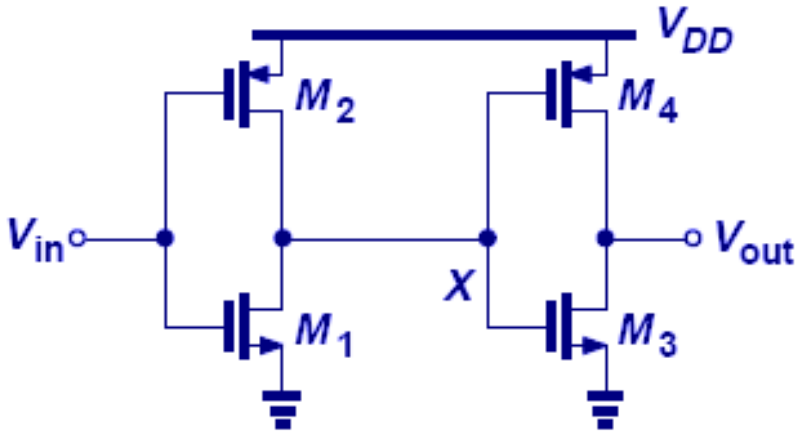
Assuming $T_{PHL} \approx T_{PLH}$, $R_{on1} \approx R_{on2}$

$$PDP = f_{in} R_{on1} C_L^2 V_{DD}^2 \left[\frac{2|V_{TH1}|}{V_{DD} - V_{TH1}} + \ln\left(3 - 4\frac{V_{TH1}}{V_{DD}}\right)\right]$$

The PDP is proportional to C_L^2, underlining the importance of minimizing capacitances in the circuit

Example 15.25: PDP

Consider a cascade of two identical inverters, where the PMOS device is three times as wide as the NMOS transistor to provide a symmetric VTC. For simplicity, assume the capacitance at node X is equal to $4WLC_{OX}$. Also, $V_{THN}=|V_{THP}| \approx V_{DD}/4$. Compute the PDP.



$$\left[\frac{2|V_{TH\,2/1}|}{V_{DD}-V_{TH\,2/1}}+\ln\left(3-4\frac{V_{TH\,2/1}}{V_{DD}}\right)\right]$$

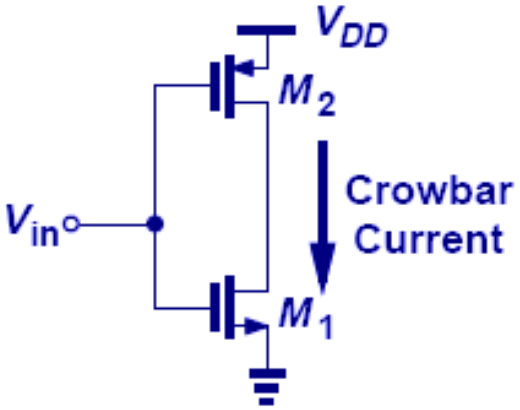
$$=\frac{2\times 0.25V_{DD}}{V_{DD}-0.25V_{DD}}+\ln\left(3-4\frac{0.25V_{DD}}{V_{DD}}\right)\approx 1.36$$

$$R_{on}=\frac{1}{\mu_n C_{ox}(\frac{W}{L})(V_{DD}-V_{TH})}$$

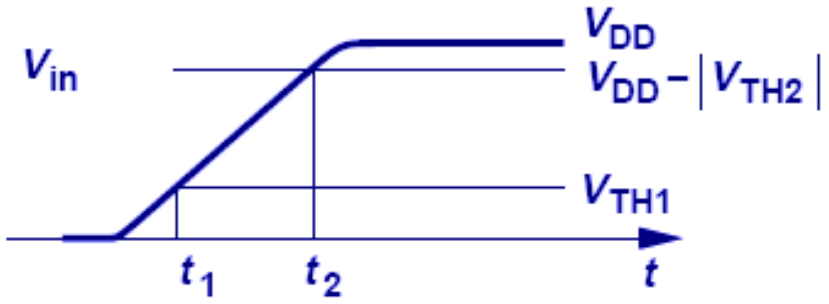
$$=\frac{4}{3}\frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)V_{DD}}$$

$$PDP=\frac{7.25WL^2C_{ox}f_{in}V_{DD}^2}{\mu_n}$$

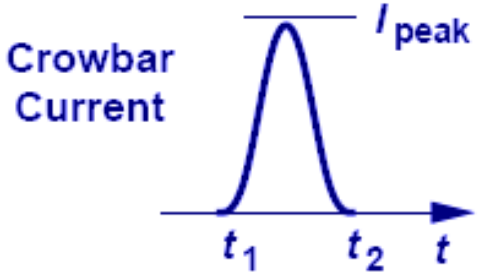
Crowbar Current

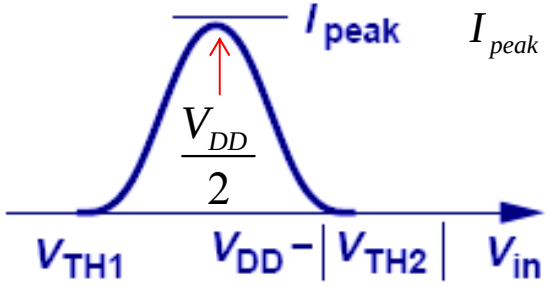


(a)



(b)



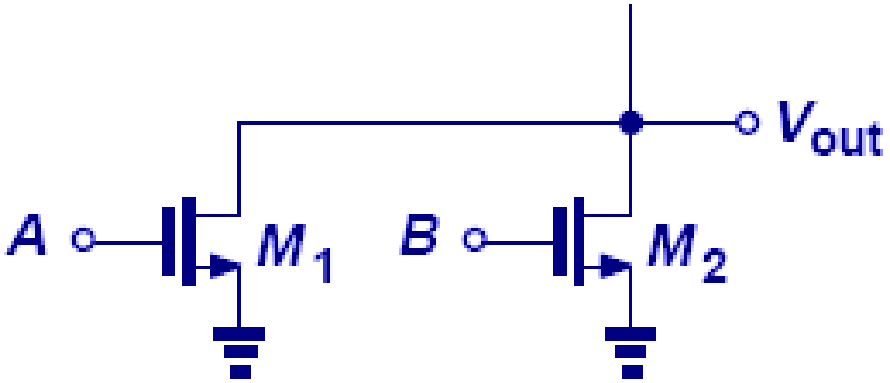


$$I_{peak} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(\frac{V_{DD}}{2} - V_{TH}\right)^2$$

(c)

- When V_{in} is between V_{TH1} and V_{DD}-$|V_{TH2}|$, both M_1 and M_2 are on and there will be a current flowing from supply to ground.

NMOS Section of NOR

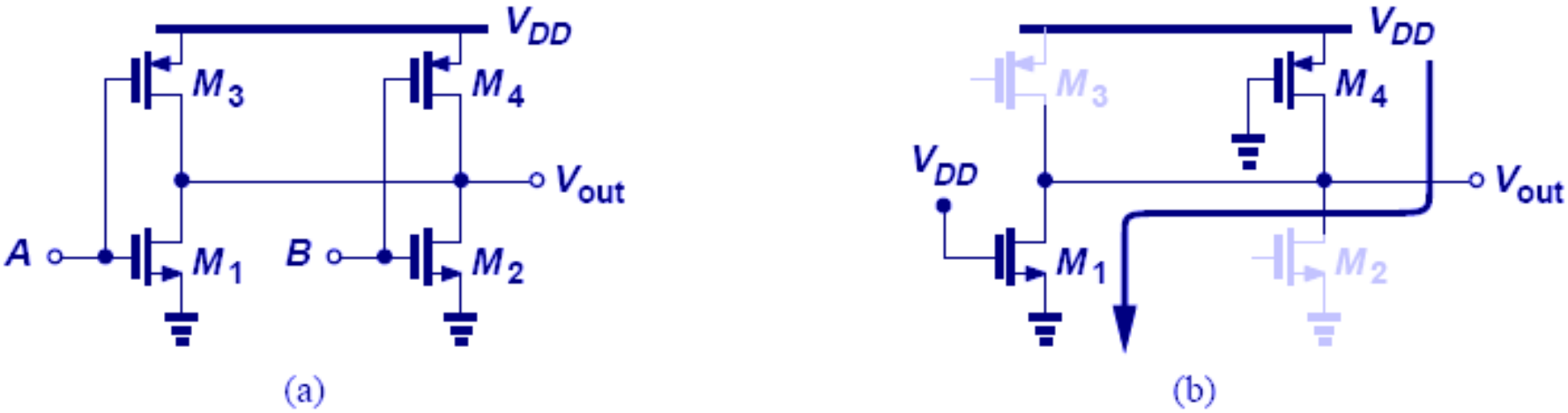


$$V_{out} = \overline{A + B}$$

A	B	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

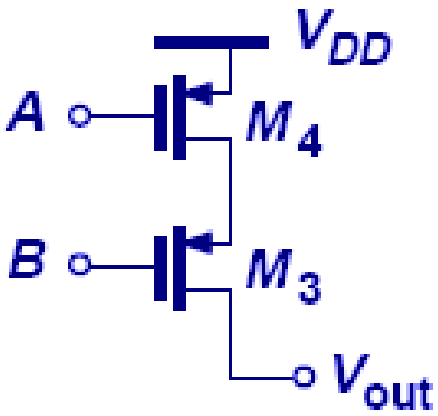
- **When either A or B is high or if both A and B are high, the output will be low. Transistors operate as pull-down devices.**

Example 15.26: Poor NOR



- **The above circuit fails to act as a NOR because when A is high and B is low, both M_4 and M_1 are on and produces an ill-defined low.**

PMOS Section of NOR

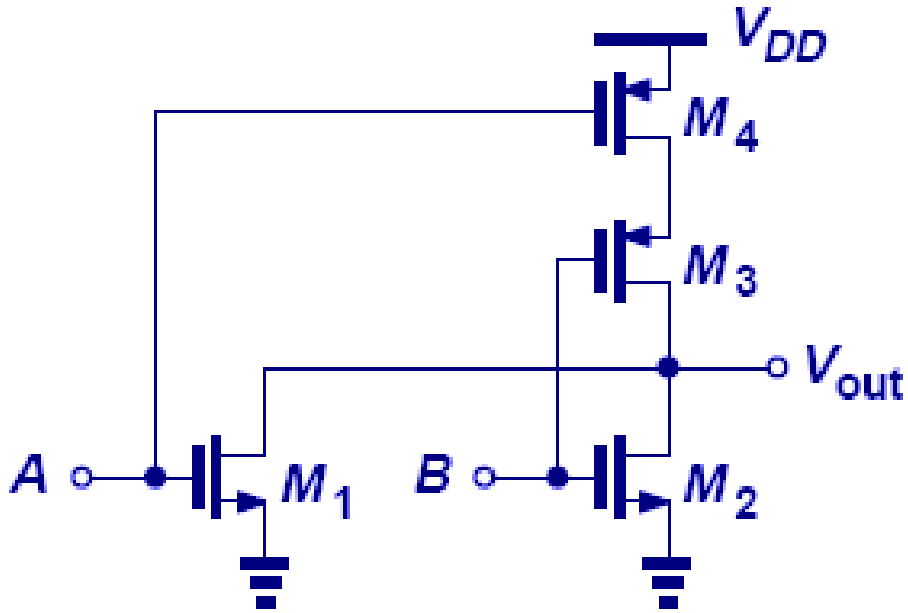


$$V_{out} = \overline{A + B}$$

A	B	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

- **When both A and B are low, the output is high. Transistors operate as pull-up devices.**

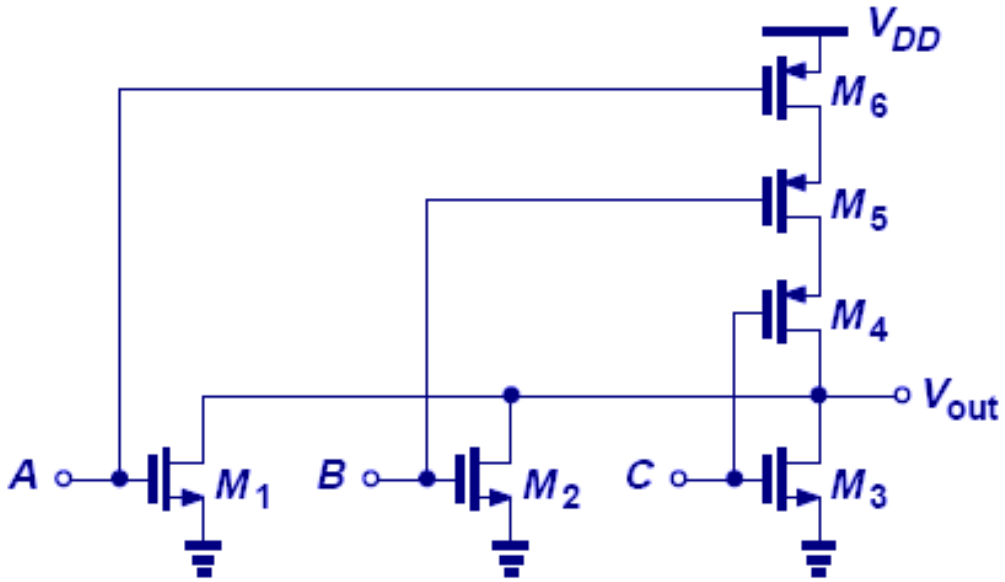
CMOS NOR



- **Combing the NMOS and PMOS NOR sections, we have the CMOS NOR.**

Example 15.27 & 15.28: Three-Input NOR

Select the relative widths of the transistors in the 3-input NOR gate for equal rise and fall times. Assume $\mu_n \approx 2\mu_p$ and equal channel lengths.



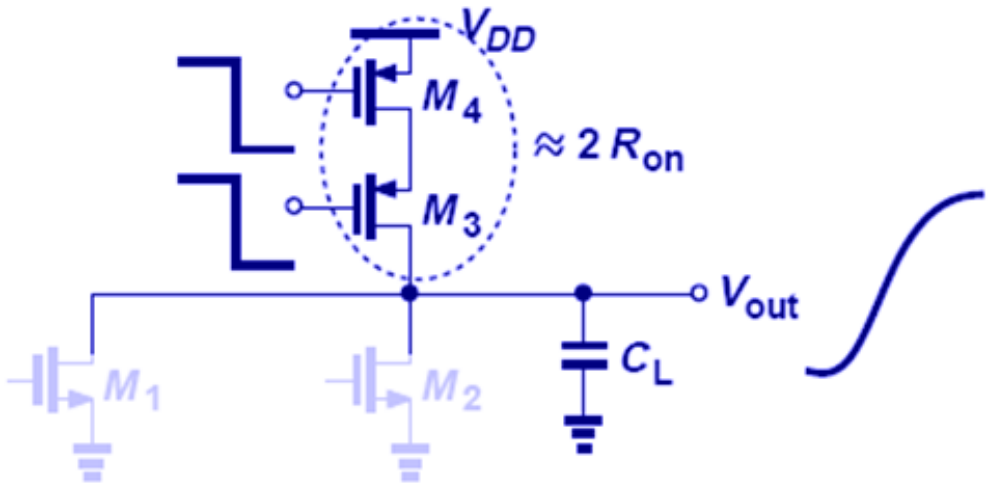
For equal rise & fall time, make the M_4-M_6 equivalent to one device with a width of W.

$W_1=W_2=W_3=W$
$W_4=W_5=W_6=6W$

$$V_{out} = \overline{A+B+C}$$

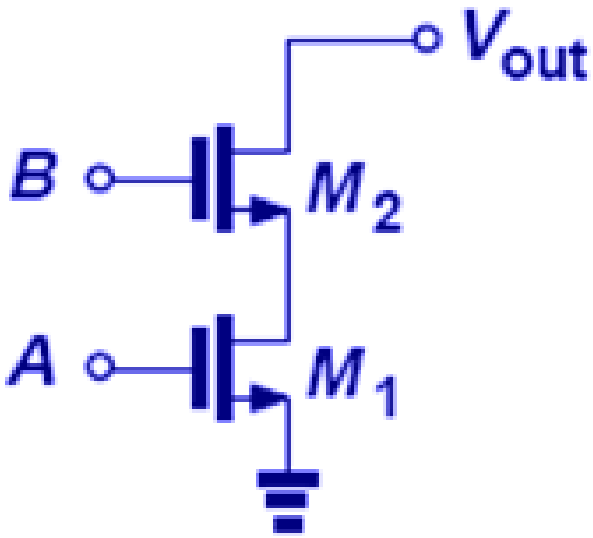
One gate presents a capacitance of $\sim 7WLC_{ox}$

Drawback of CMOS NOR



- Due to low PMOS mobility, series combination of M_3 and M_4 suffers from a high resistance, producing a long delay.
- The widths of the PMOS transistors can be increased to counter the high resistance, however this would load the preceding stage and the overall delay of the system may not improve.

NMOS NAND Section

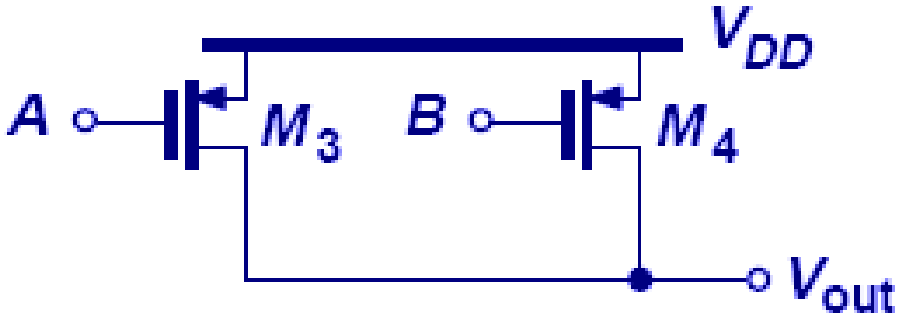


$$V_{out} = \overline{AB}$$

A	B	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

- **When both A and B are high, the output is low.**

PMOS NAND Section

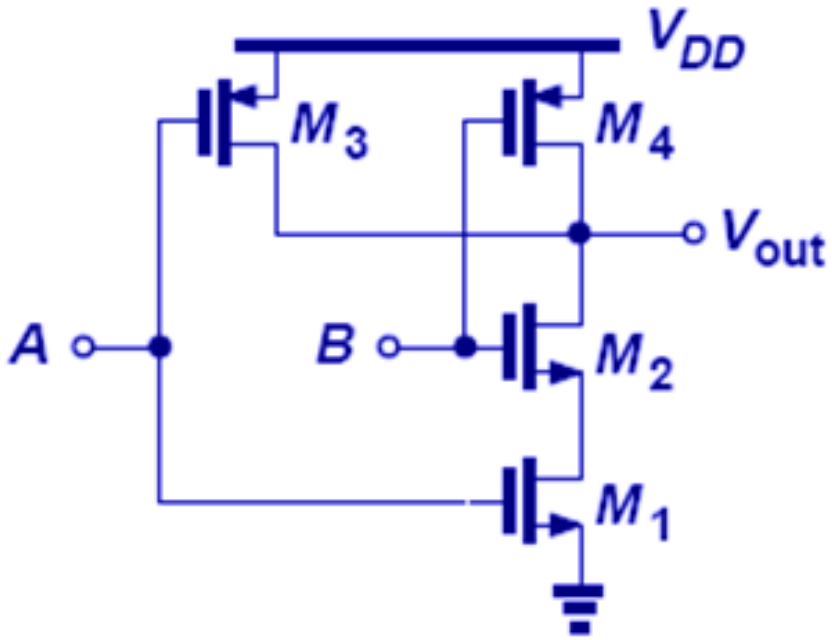


$$V_{out} = \overline{AB}$$

A	B	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

- **When either A or B is low or if both A and B are low, the output is high.**

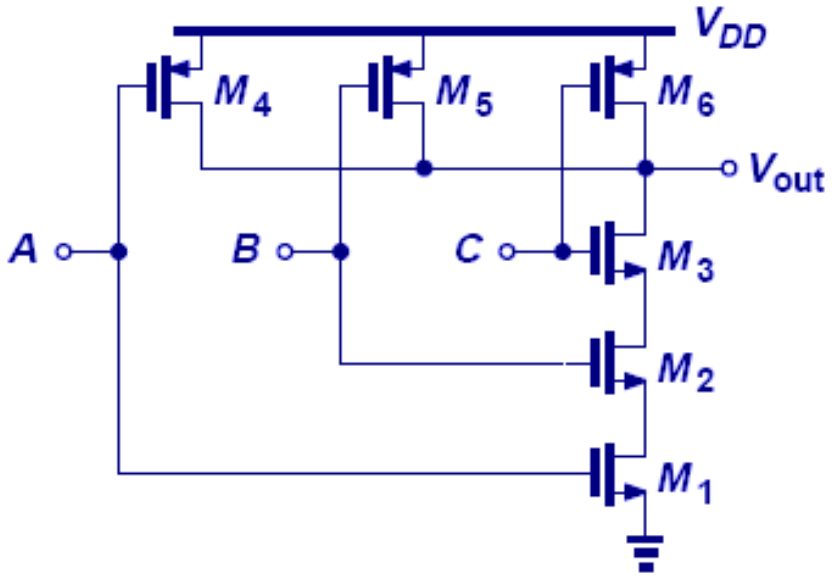
CMOS NAND



- **Just like the CMOS NOR, the CMOS NAND can be implemented by combining its respective NMOS and PMOS sections, however it has better performance because its PMOS transistors are not in series.**

Example 15.29: Three-Input NAND

Select the relative widths of the transistors in the 3-input NAND gate for equal rise and fall times. Assume $\mu_n \approx 2\mu_p$ and equal channel lengths.



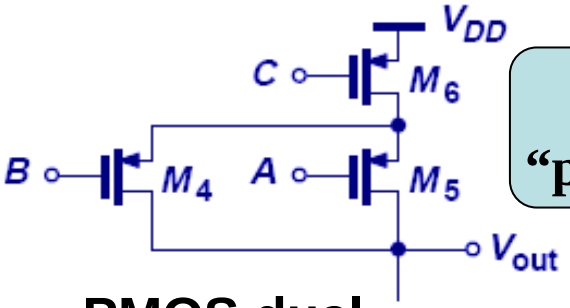
For equal rise & fall time, make the M_1-M_3 equivalent to one device with a width of W.

W_1=W_2=W_3=3W
W_4=W_5=W_6=2W

$$V_{out} = \overline{ABC}$$

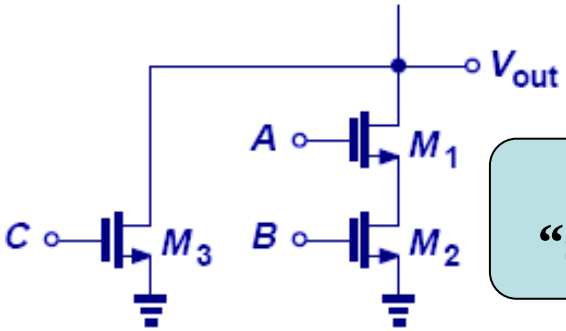
One gate presents a capacitance of $\sim 5WLC_{ox}$

Example 15.30: NMOS and PMOS Duality

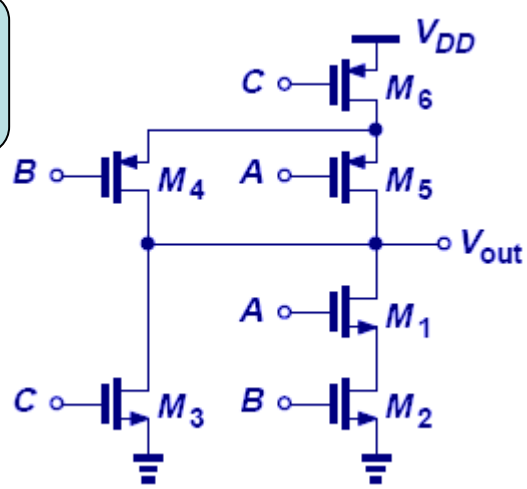


PMOS dual

C is in "series" with the "parallel" combination of A and B



C is in "parallel" with the "series" combination of A and B



CMOS realization

$$V_{out} = \overline{AB + C}$$

- **In the CMOS philosophy, the PMOS section can be obtained from the NMOS section by converting series combinations to the parallel combinations and vice versa.**

Summary

- The CMOS inverter is an essential building block in digital design. It consumes no power in the absence of signal transitions.
- The NMOS and PMOS devices in an inverter provide “active” pull-down and pull-up currents and hence enhance each other’s operation.
- The average power dissipated by a CMOS inverter is equal to $f_{in}C_LV_{DD}^2$.
- Based on the CMOS inverter, other gates such as NOR and NAND gates can be derived. These gates also have zero static power.