Micro Electro Mechanical Systems for mechanical engineering applications

Lecture 3:
MEMS fabrication I: bulk micromachining (2)

Kahp-Yang Suh

Assistant Professor
SNU MAE
sky4u@snu.ac.kr

Micromachining

Process Type	Examples
Lithography	photolithography, screen printing, electron-beam lithography, x-ray lithography
Thin-Film Deposition	chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), sputtering, evaporation, spin-on application, plasma spraying, etc.
Electroplating	blanket and template-delimited electroplating of metals
Directed Deposition	electroplating, stereolithography, laser-driven chemical vapor deposition, screen printing, transfer printing
Etching	plasma etching, reactive-ion enhanced (RIE) etching, deep reactive ion etching (DRIE), wet chemical etching, electrochemical etching, etc.
Directed Etching	laser-assisted chemical etching (LACE)
Machining	drilling, milling, electric discharge machining (EDM), diamond turning, sawing, sand blasting, etc.
Bonding	fusion bonding, anodic bonding, adhesives, etc.
Surface Modification	wet chemical modification, plasma modification
Annealing	thermal annealing, laser annealing

Bulk micromachining process for high aspect ratio structures

- Merits of single crystal silicon high aspect ratio structures

  - High sensitivity
  - Large force
  - Free from residual stress and stress gradient

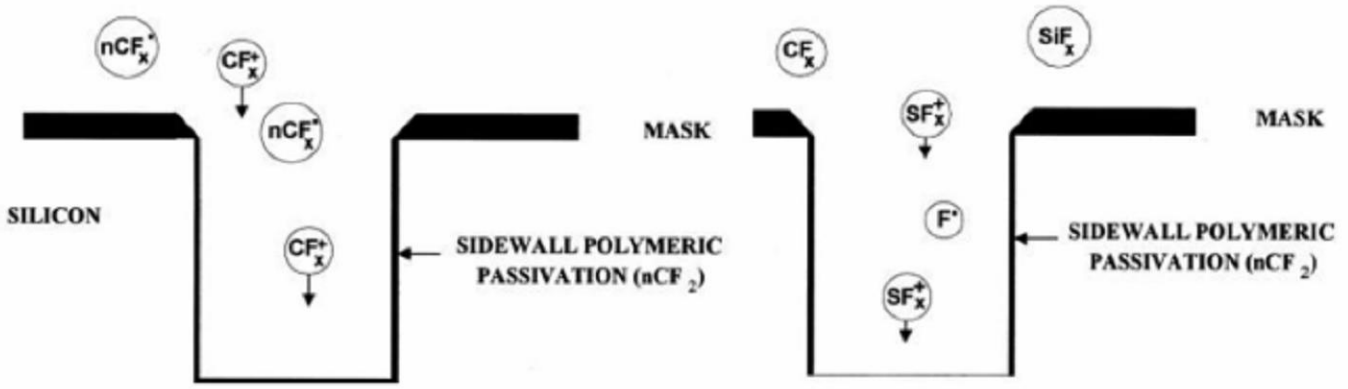
- Deep reactive ion etching (Deep RIE)

- LIGA process (Lithographie, Galvanoformung, Abformung)
  or (lithography, galvanoforming, molding)

- Other methods

Deep Reactive Ion Etching (Deep RIE) (1)

- Uses high density plasma to alternatively etch silicon and deposit etch resistant polymer on sidewall
  - Unconstrained geometry 90° side walls
  - High aspect ratio 1:30
  - Easily masked (PR, SiO_2)
- Bosch process: sidewall passivaiton → etch → sidewall passivaiton → etch …



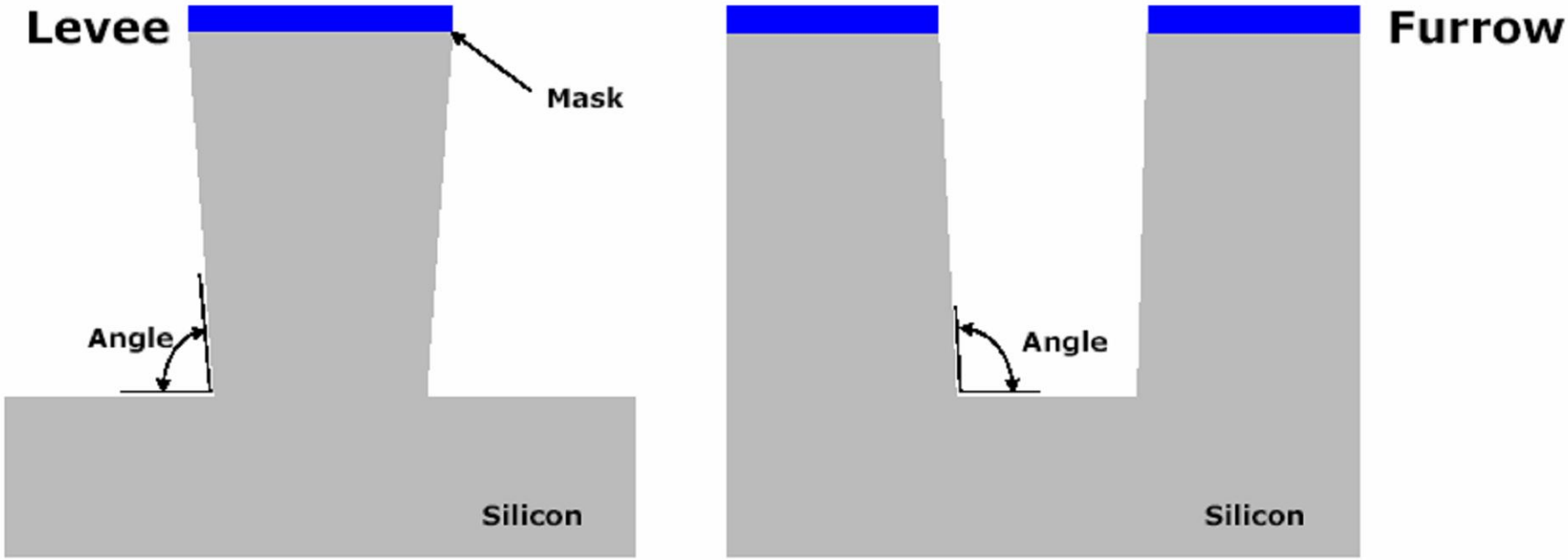
ASE process deposition step ASE process etch step

Deep Reactive Ion Etching (Deep RIE) (2)

- Characteristics of the Deep RIE process
  - SF6 flow: 30 ~ 150 sccm
  - C4F8 flow: 20 ~ 100 sccm
  - Etch cycle: 5 ~ 15 sec
  - Deposition cycle: 5 ~ 12 sec
  - Pressure: 0.25 ~ 10 Pa
  - Temperature: 20 ~ 80 ^{o}C
  - Etch rate: 1.5 ~ 4 um/min
  - Selectivity to resist mask: more than 75:1
  - Selectivity to oxide mask: more than 150:1
  - Sidewall angle: 90^{o} ±2
  - Etch depth capability: up to 500 um

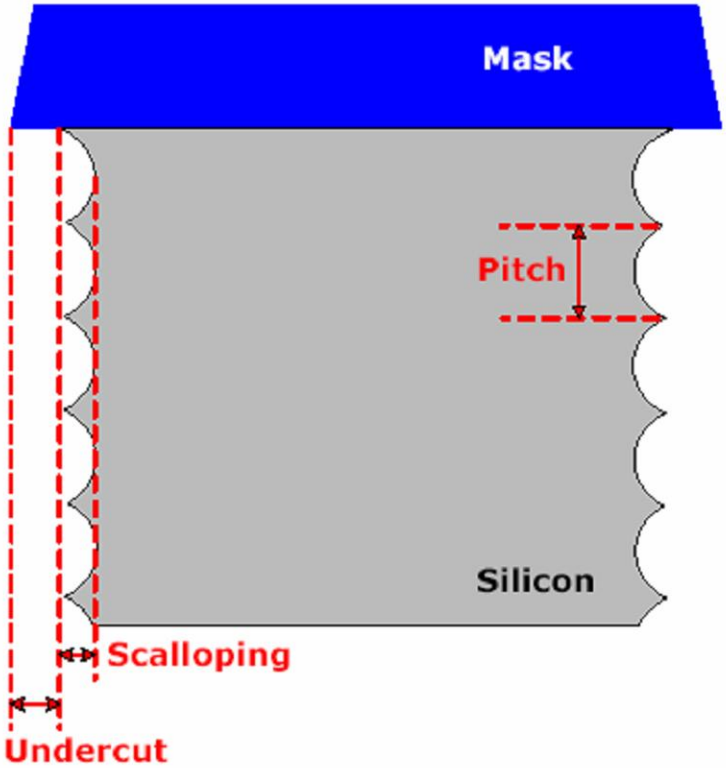
Deep Reactive Ion Etching (Deep RIE) (3)

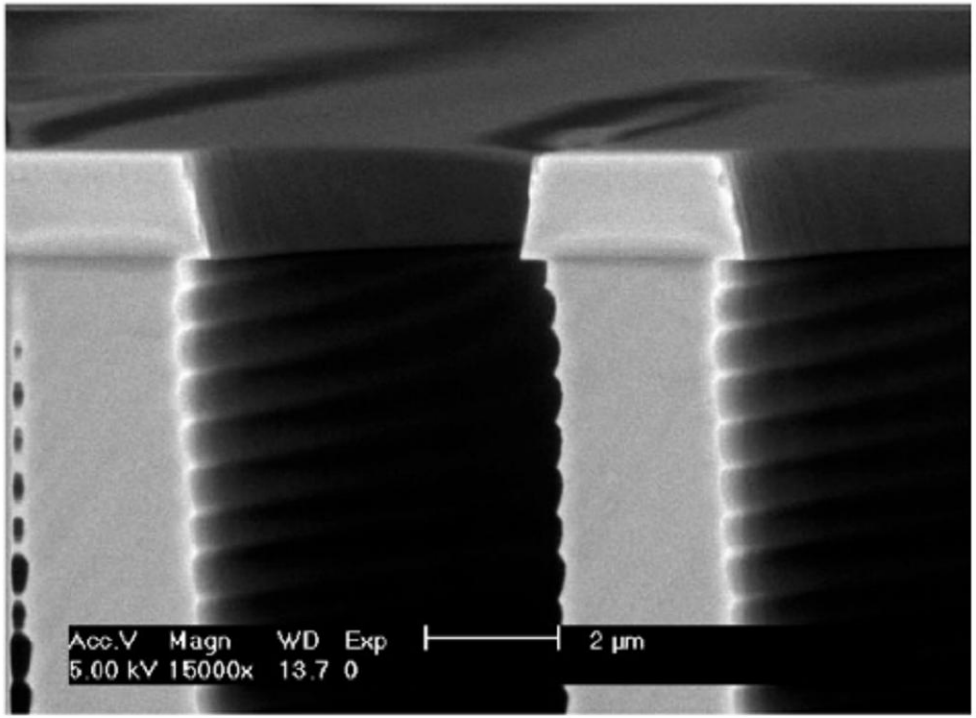
- Fence (levee) structure and trench (furrow) structure have different etch side wall profile



Deep Reactive Ion Etching (Deep RIE) (4)

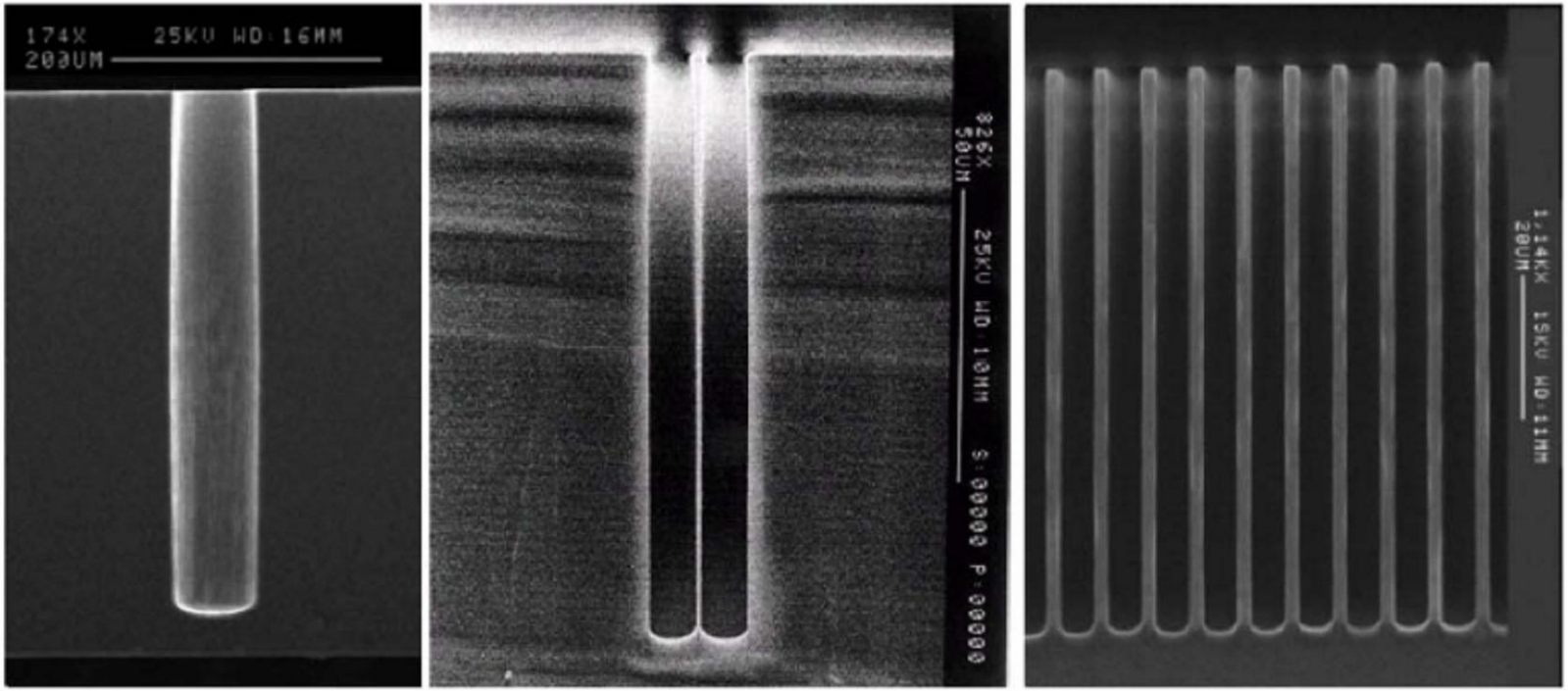
- Characteristics of Bosch process
  - Scalloping
  - Under cut





Deep RIE Fabrication example (1)

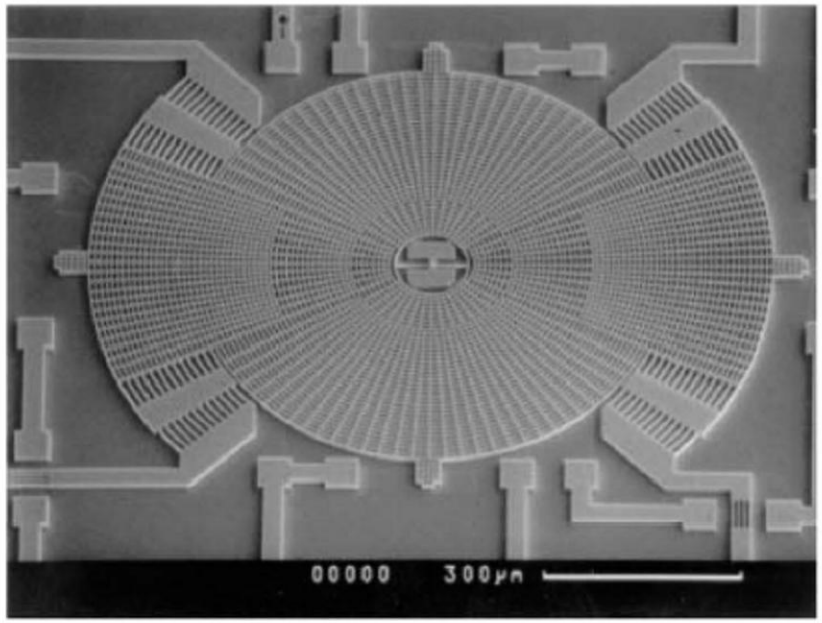
- Fabrication example (deep trench)



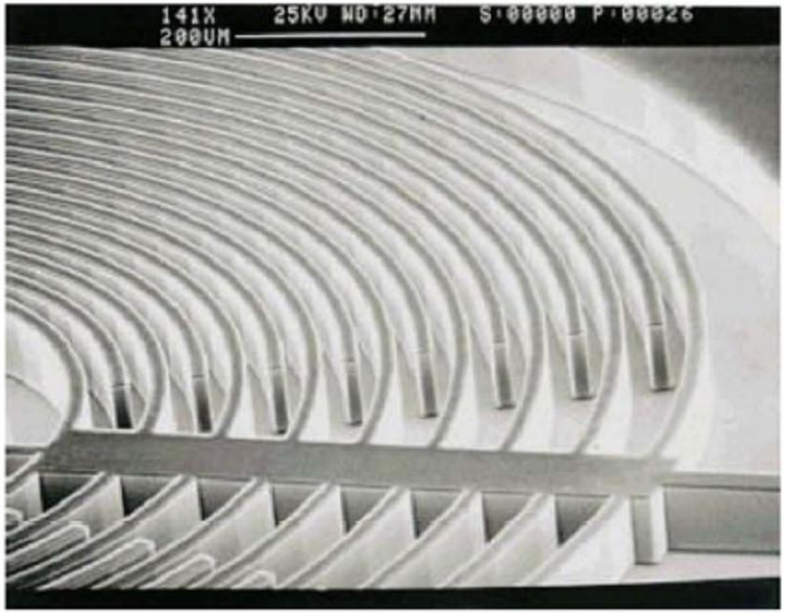
350㎛-depth　　100㎛-depth　　80㎛-depth, 4.5㎛ space width, 2㎛ line width

Deep RIE Fabrication example (2)

- Fabrication example (IMU device)



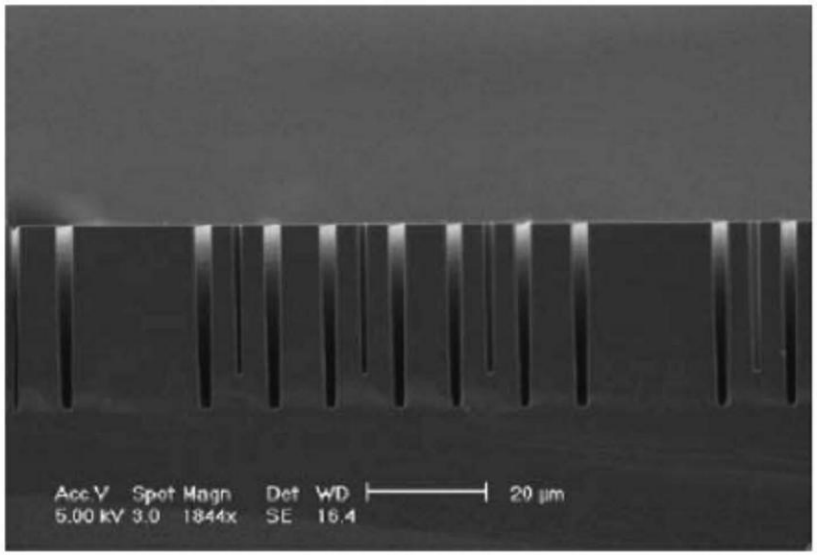
Gyroscope

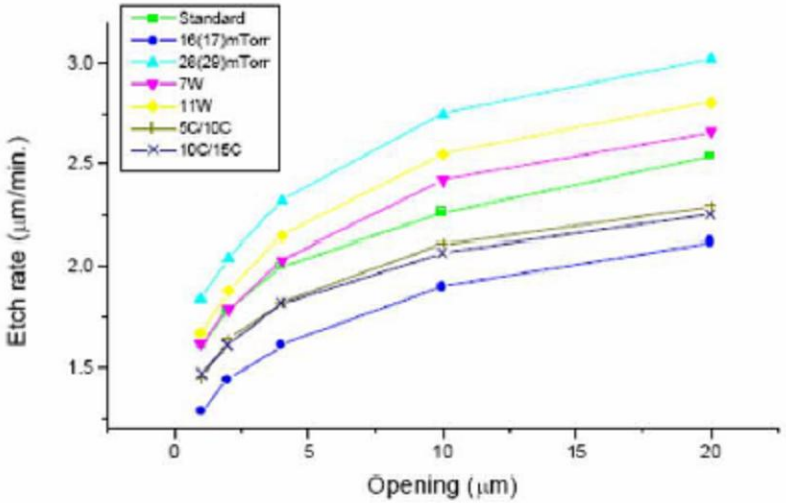


Accelerometer (170㎛-depth)

RIE lag in Deep RIE process

- RIE lag (microloading effect)
  - Etch rate differs from the area of opening

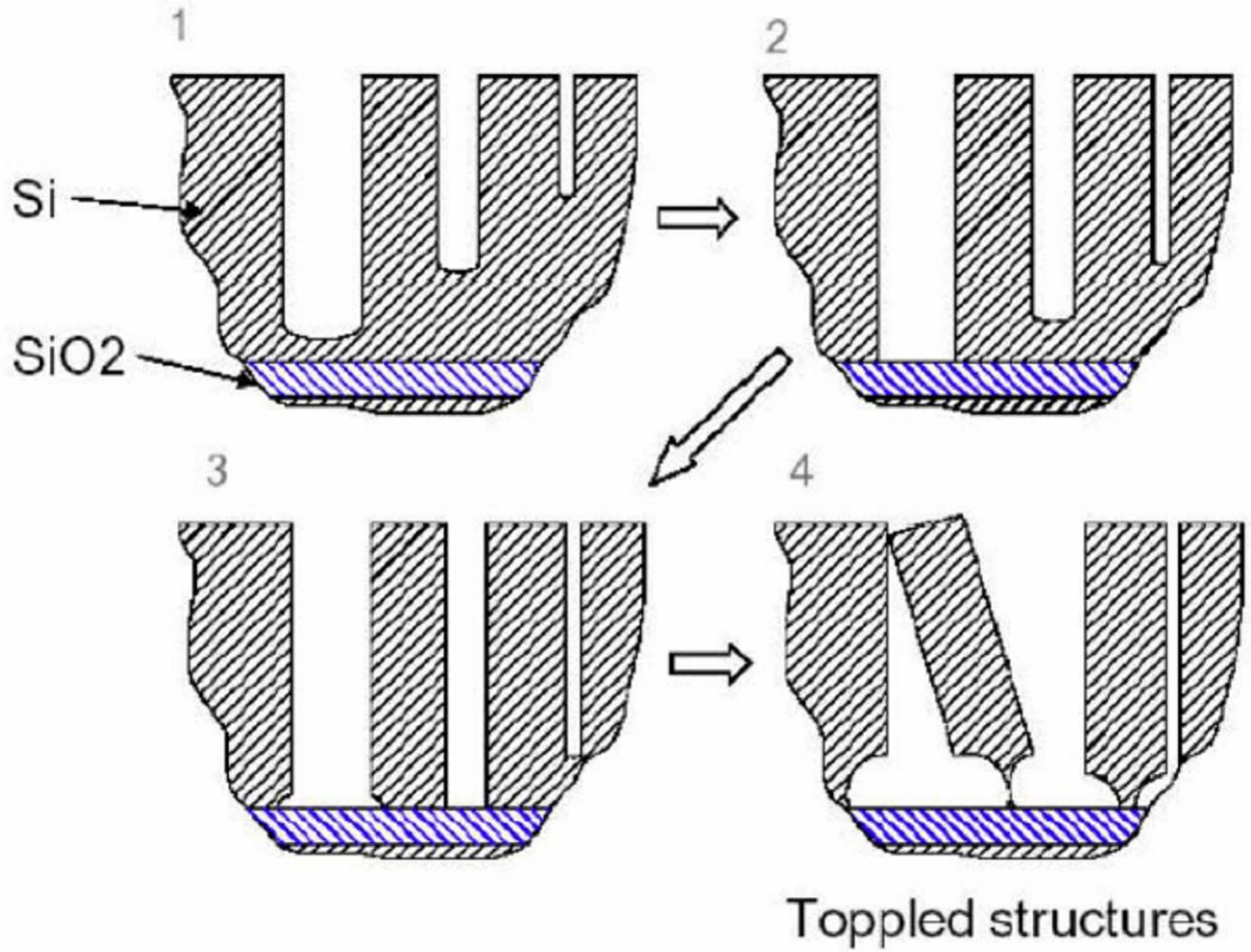




Plasma-Therm, SLR-7701-10R-B data

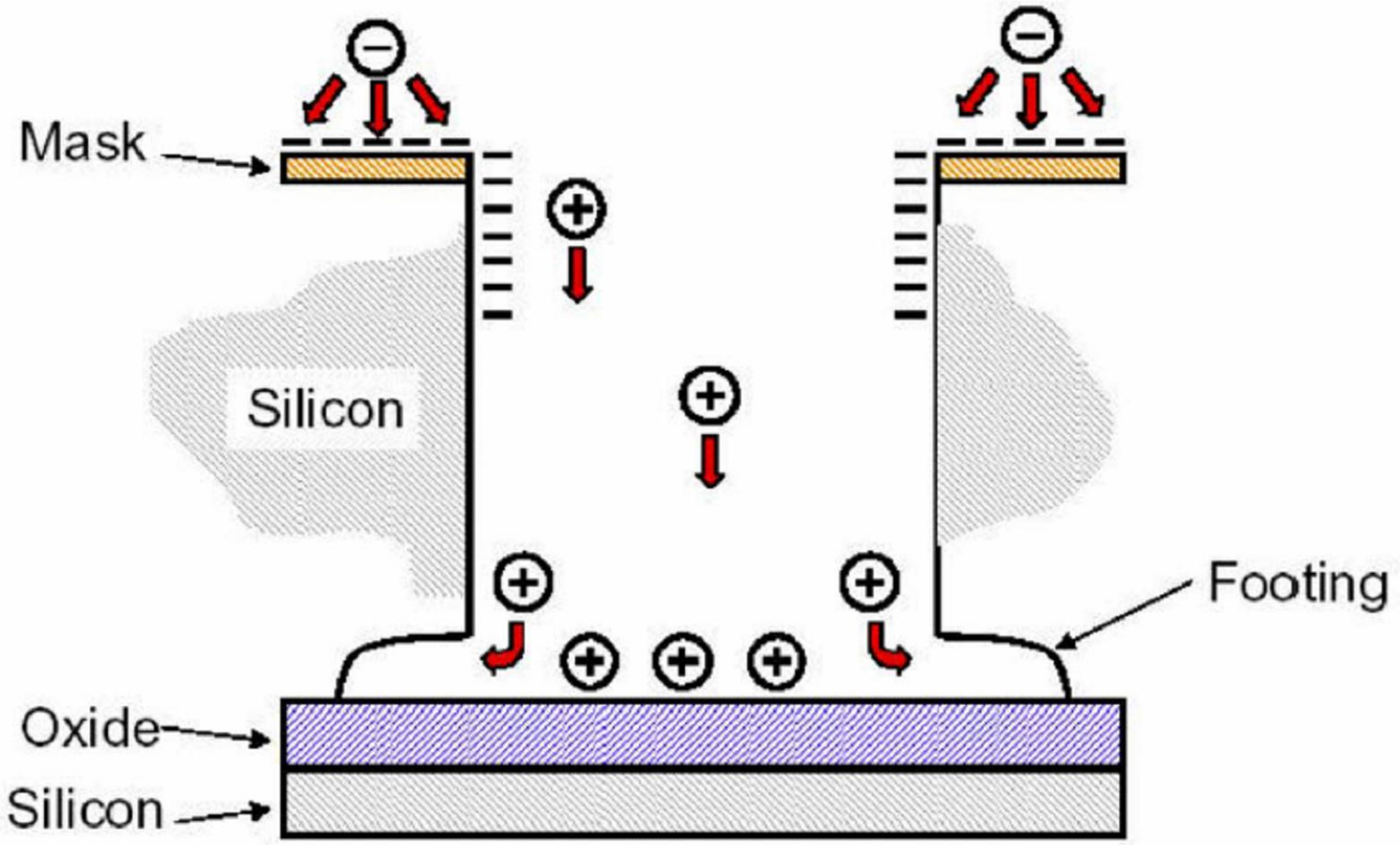
Footing in Deep RIE process (1)

- Footing



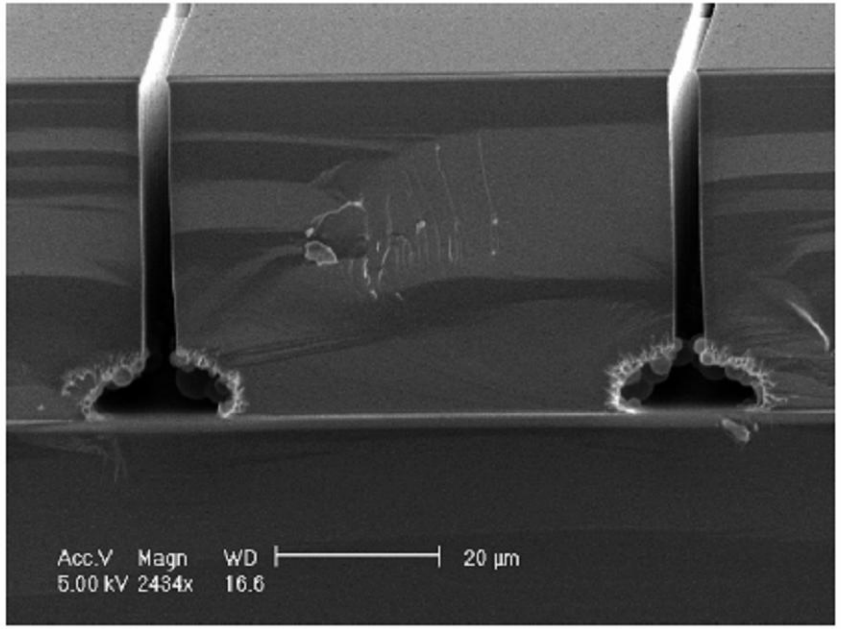
Footing in Deep RIE process (2)

- Footing formation

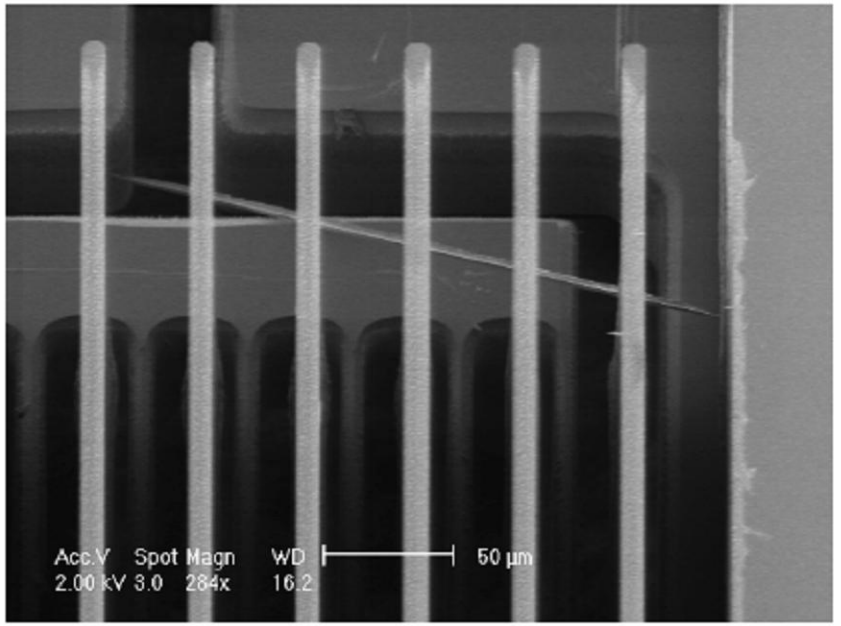


Footing in Deep RIE process (3)

- Footing SEM pictures



Notching



Fragments

LIGA process (1)

- The LIGA process was developed at the IMT (Institute of Microstructure Technology), in the early eighties under the leadership of Dr. W. Ehrfeld.
- LIGA is a German acronym for *Lithographie, Galvanoformung, Abformung* (lithography, galvanoforming, molding)
- High aspect ratio > 20
- High accuracy < 0.5 μm
- High uniformity

LIGA process (2)

- **Deep X-ray lithography and mask technology**

- Heights of up to 1 mm and a lateral resolution down to 0.2 μm.

- Walls are smooth and parallel to each other.

- Mask is a very thin metal foil (e.g., Ti, Be). Absorbers consist of a thick layer of Au.

- **Electroforming**

- Metal structures are generated from the plastics structure.
  Ex) Ni, Cu, Au, or alloys.

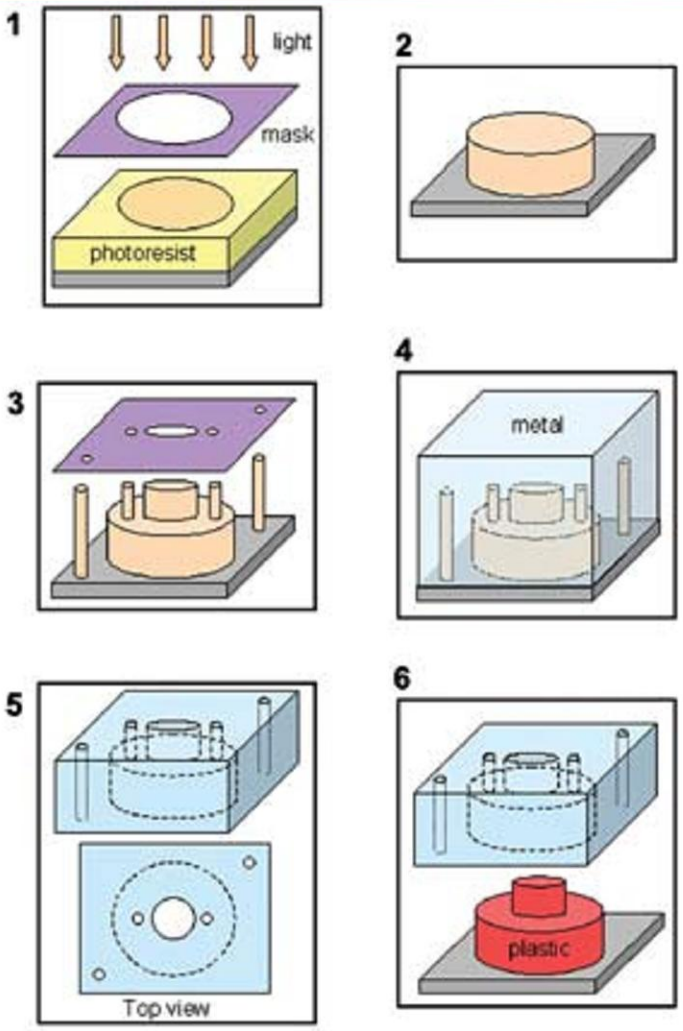
- Direct use or tools for secondary plastics molding.

- **Plastics molding**

- Low-cost mass production by the LIGA process.

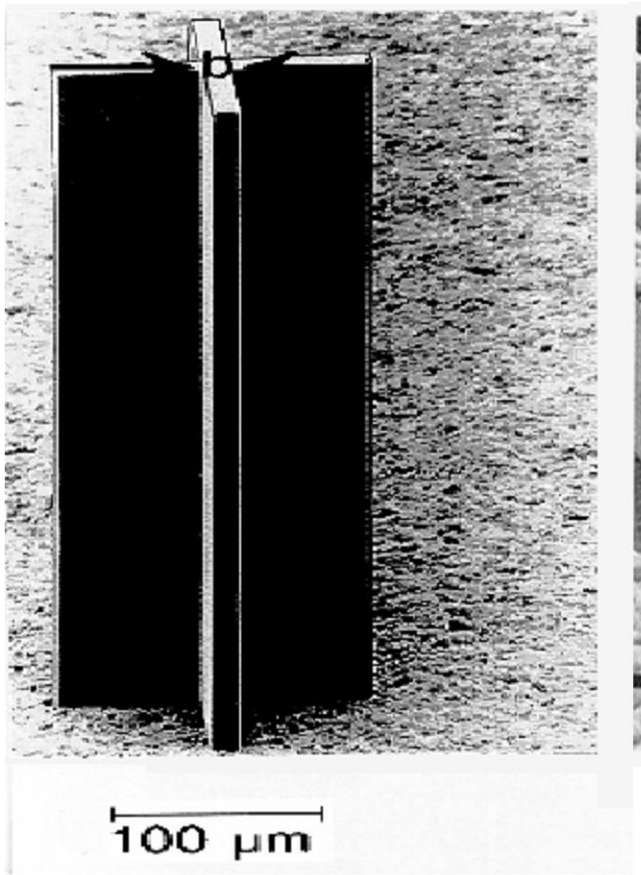
- Various polymers are used.

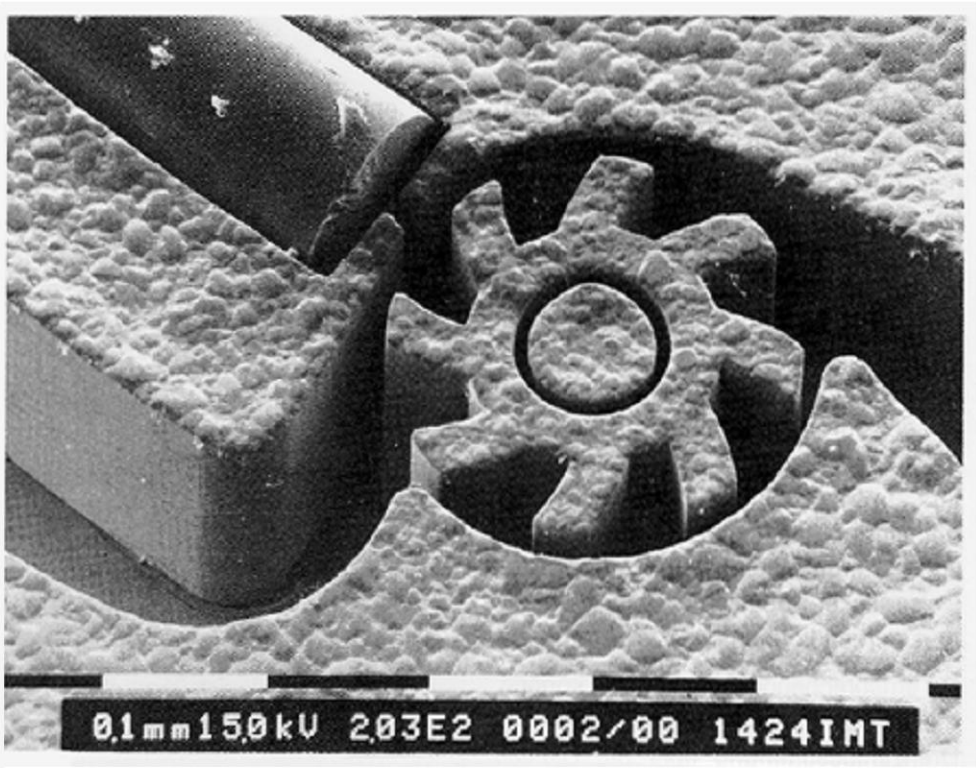
LIGA process (3)



(1) Epoxy resin is selectively cured by X-ray light beamed through a mask.
(2) Uncured epoxy is etched away.
(3) Subsequent masking steps produce additional features.
(4) Metal is then electroformed over the cured epoxy to form a mold half.
(5) The metal mold is ground to the correct height, and the epoxy is dissolved away, leaving a cavity and ejector holes.
(6) The tool is ready to mold parts.

Example by LIGA





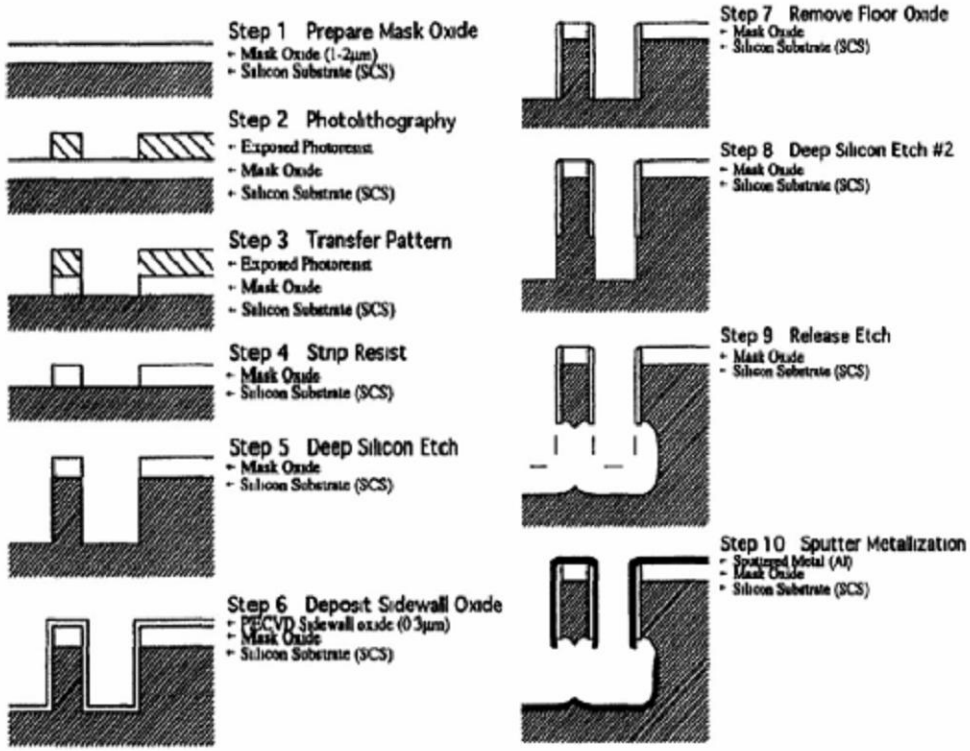
Other methods

- Fabrication process
  - SCREAM process (Cornell University)
  - SIMPLE process (Delft University of Technology)
  - Dissolved wafer process (University of Michigan)
  - HARPSS process (University of Michigan)
  - SBM process (Seoul National University)
  - SOG process
  - **SOI process**
  - Post CMOS micromachining processing (Carnegie Mellon University)

SCREAM process

- **S**ingle **C**rystal **R**eactive **E**tching and **M**etallization

- Multiple isotropic and anisotropic etching
- Low temperature etching and deposition
- Limitation on the structural width
- Complicated process involving several film deposition and etching step

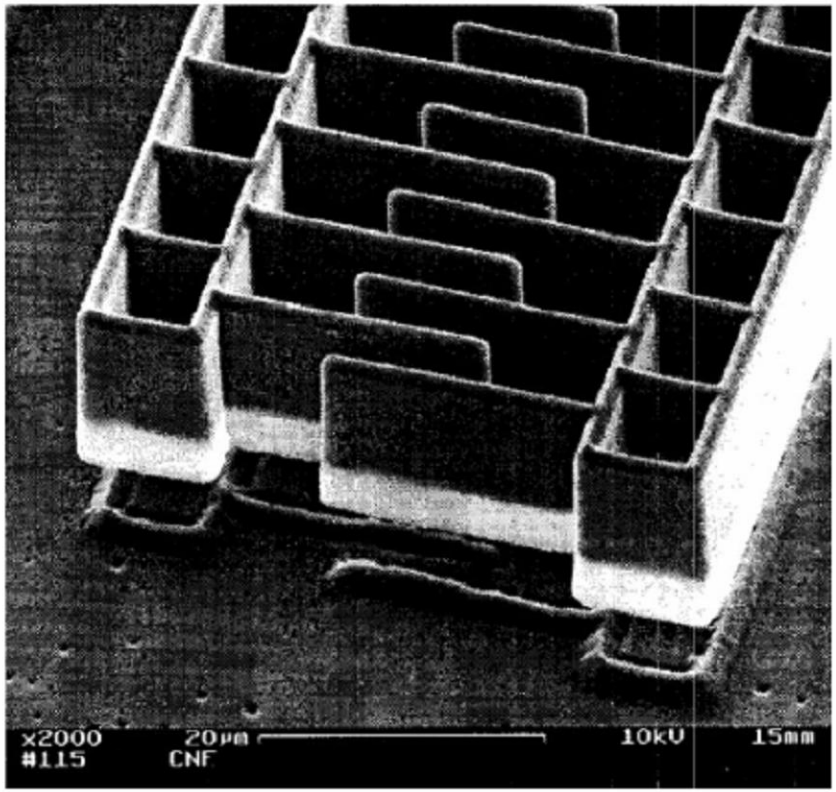


Fabrication Process

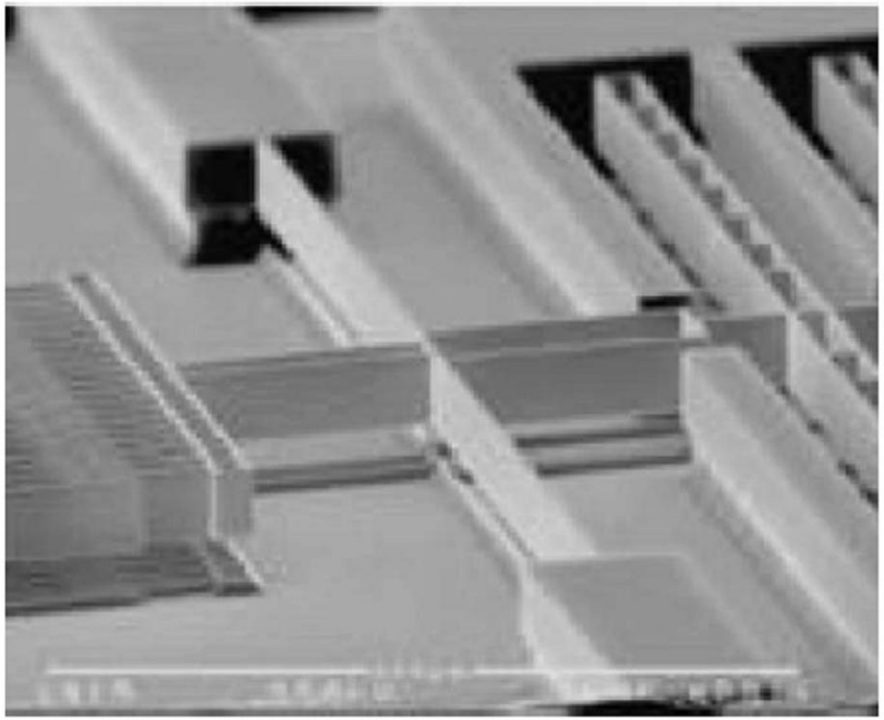
Ref.) K. A. Shaw, et. Al., *Sens. Actuators A*, vol. 40, p. 63-70, 1994

Example by SCREAM process

- SCREAM process example



Fabricated SCREAM comb drive

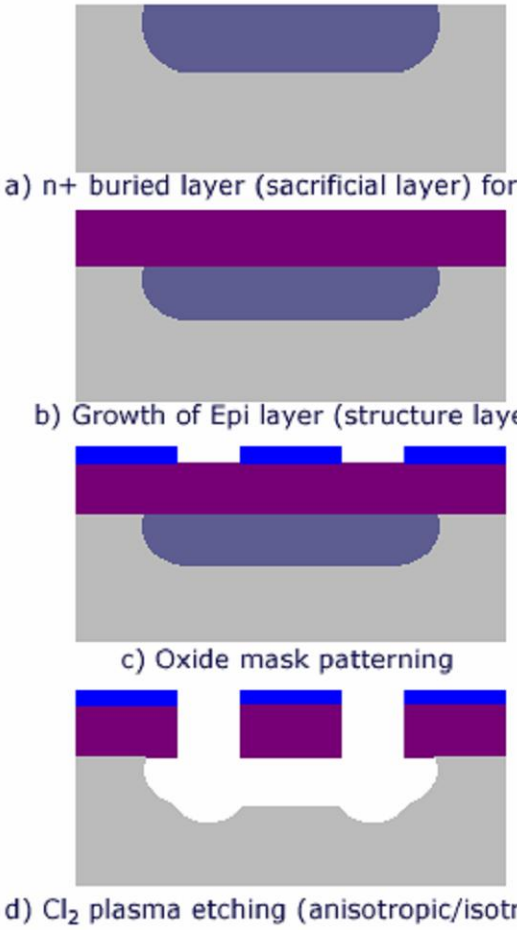


XYZ-stage for MEMS STM

SIMPLE process

- **SI**licon **M**icromachining by single step **PL**asma **E**tching process
- An n^+ buried layer is formed on the substrate before the growth of a lightly n-doped epitaxial layer
- Cl_2 based plasma etches epitaxial layer anisotropically but lateral etching occurs in n^+ buried layer

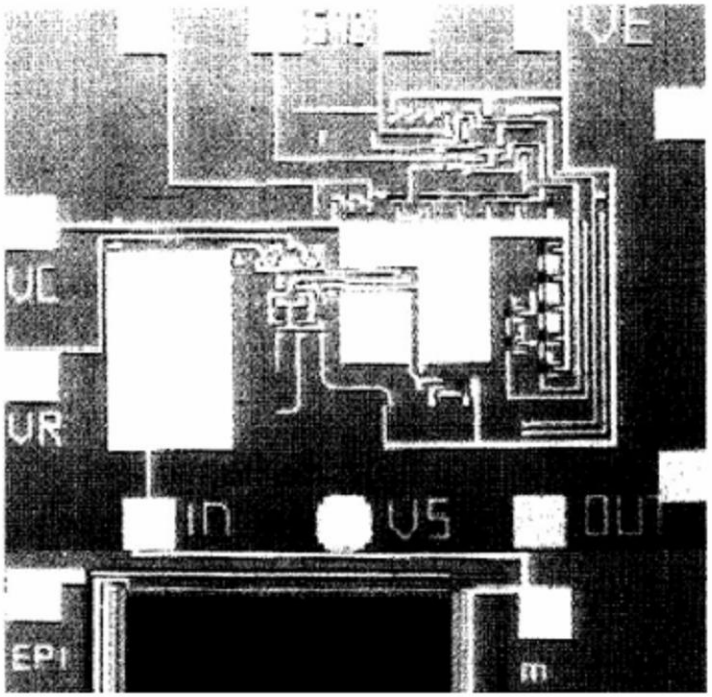
  → free-standing single crystalline silicon microstructures can be patterned and released
- The lateral etch rate of the n^+ buried layer is dependent on doping concentration



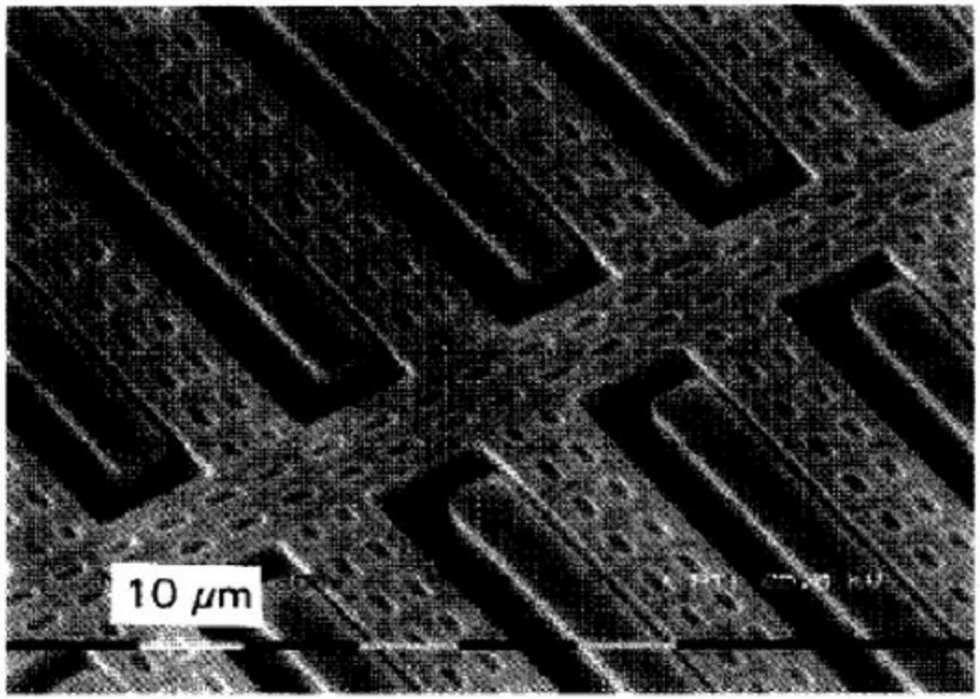
Ref.) Y. X. Li, et. al.,MEMS'95, pp. 398-403, 1995

Example by SIMPLE process

- SIMPLE process example



Accelerometer with on chip read-out circuit



Comb drive of the accelerometer

HARPSS process

- **H**igh **A**spect **R**atio combined **P**oly and **S**ingle crystalline **S**ilicon
- Produce 10~100 um thick poly-Si and single crystalline Si microstructures with simple fabrication process
- HAR poly-Si structures are created by refilling 100 μm trenches with poly-Si

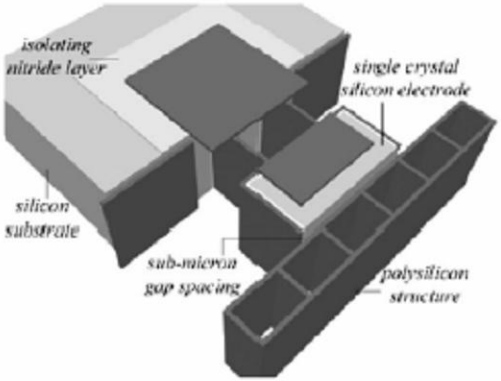
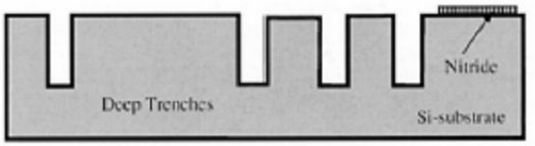
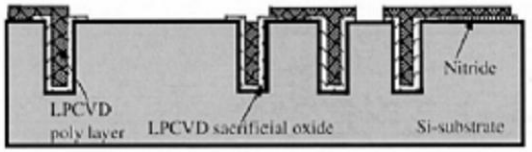


Fig. 1. View of a thick single-crystal silicon electrode separated from a trench-refilled polysilicon structure by submicrometer capacitive gap in the HARPSS process.

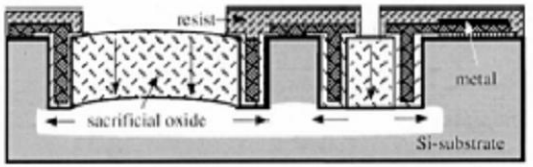
Ref.) F. Ayazi, K.Najafi, JMEMS, Vol. 9, No. 3, pp. 288-294, 2000



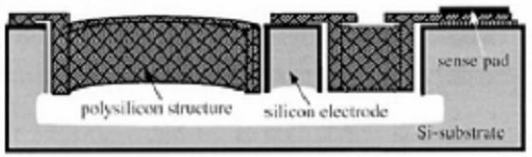
a) Deposit and pattern the isolating nitride layer;
b) dry etch deep trenches to define the main body structure.



c) Deposit LPCVD sacrificial oxide and dope surface of the oxide; d) refill trenches with LPCVD polysilicon; e) etch back poly; f) pattern oxide; g) deposit, dope and pattern poly.



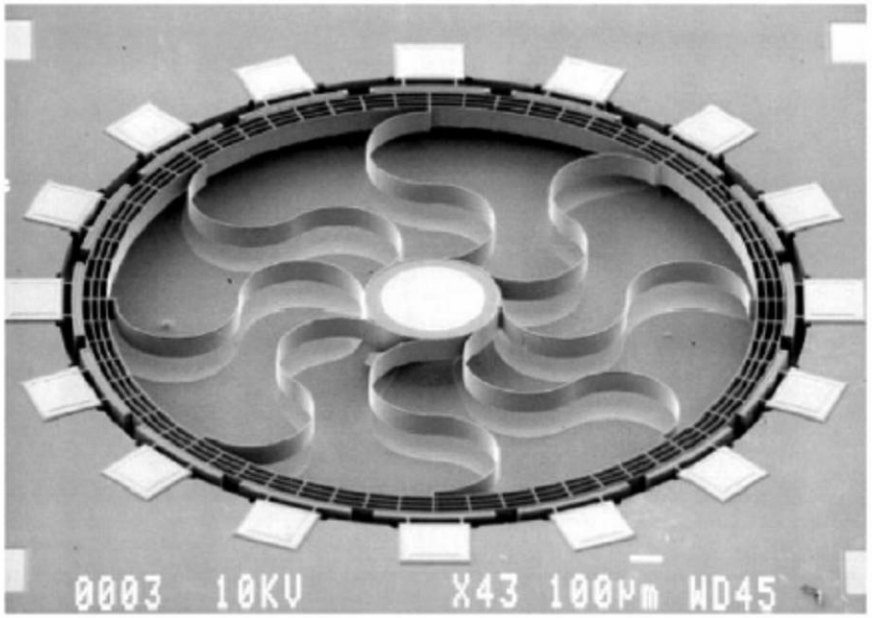
h) Deposit and pattern Cr/Au; i) SF_6 deep dry directional etch + undercut to release silicon structures/electrodes (thick resist used as a mask);



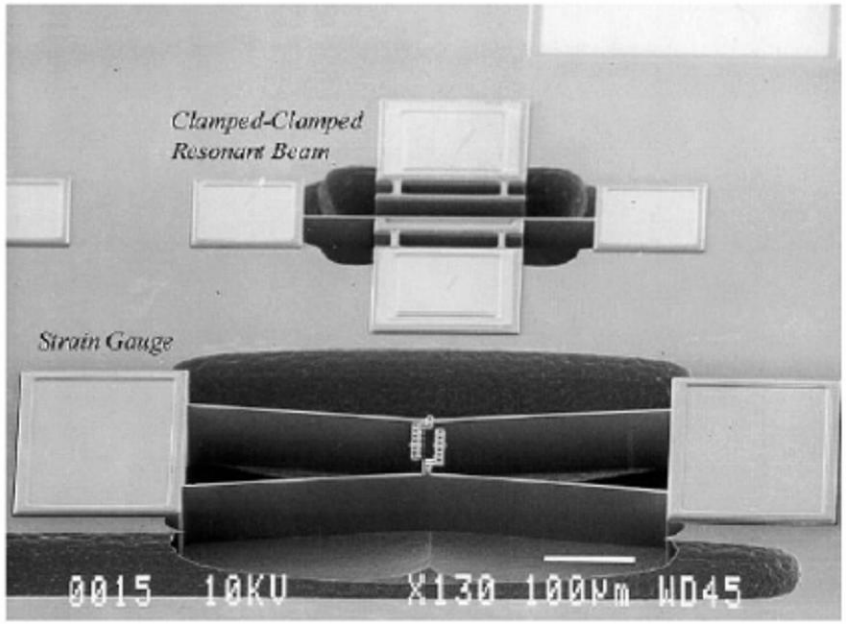
j) Strip resist; k) etch the sacrificial oxide layer to completely release the structure.

Example by HARPSS process

- HARPSS process example



Ring gyroscope fabricated by HARSS process

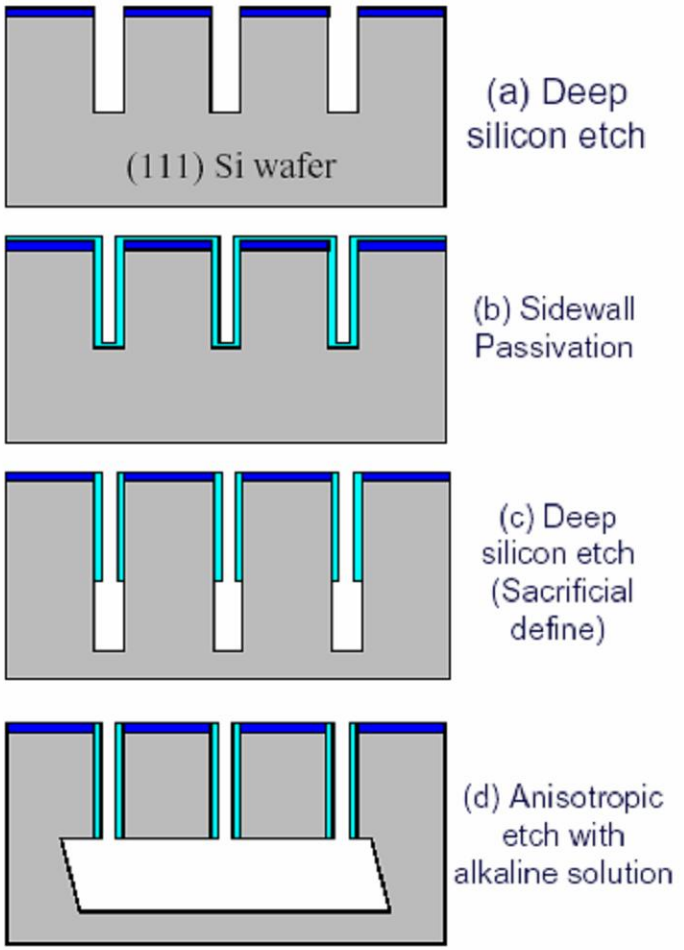


Bent beam strain gauge and resonant beam

SBM process

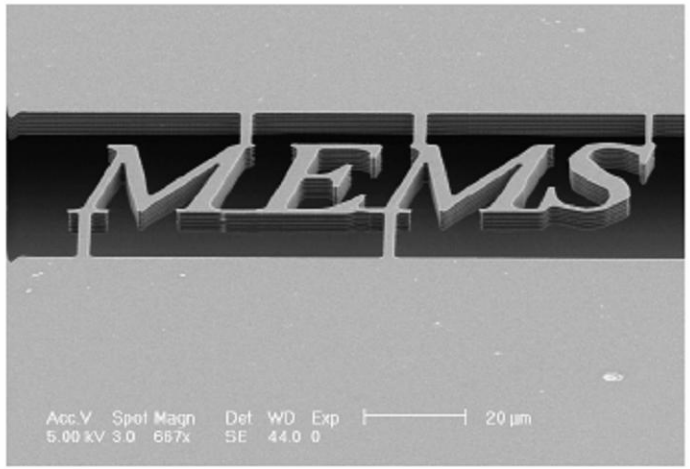
- **S**acrificial **B**ulk **M**icromachining
- (111) single crystal silicon is used
- Arbitrary shapes can be patterned by RIE (surface micromachining)
- Sacrificial release using alkaline etchants (bulk micromachining)
- High aspect ratio structures using deep RIE
- Combines the advantages of deep RIE, SURFACE micromachining and BULK micromachining

Ref.) S. Lee, S. Park, and D. Cho, JMEMS, Vol. 8, no. 4, pp. 409-416, 1999

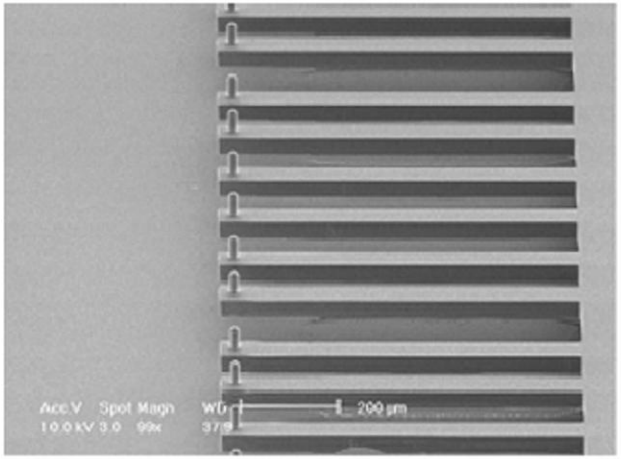


Example by SBM process

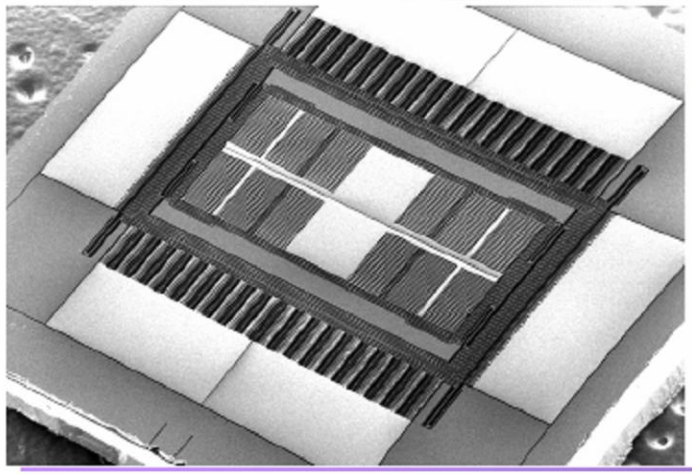
- SBM process example



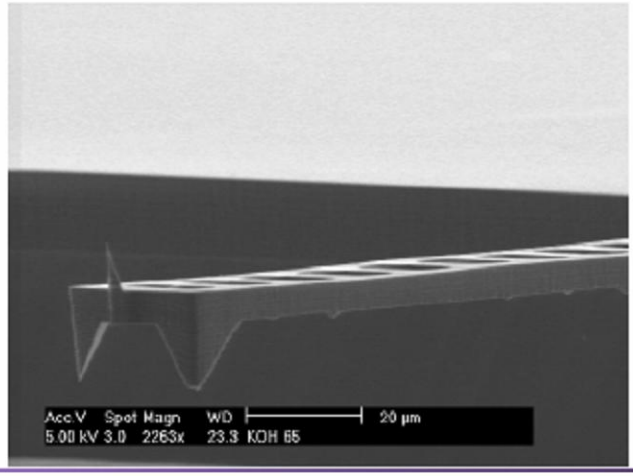
Released silicon structure



Microprobe array



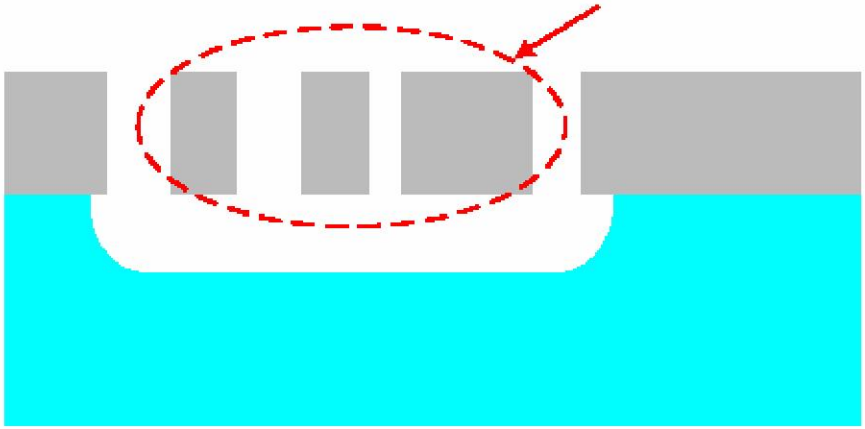
Z-axis gyroscope



Silicon nano probe

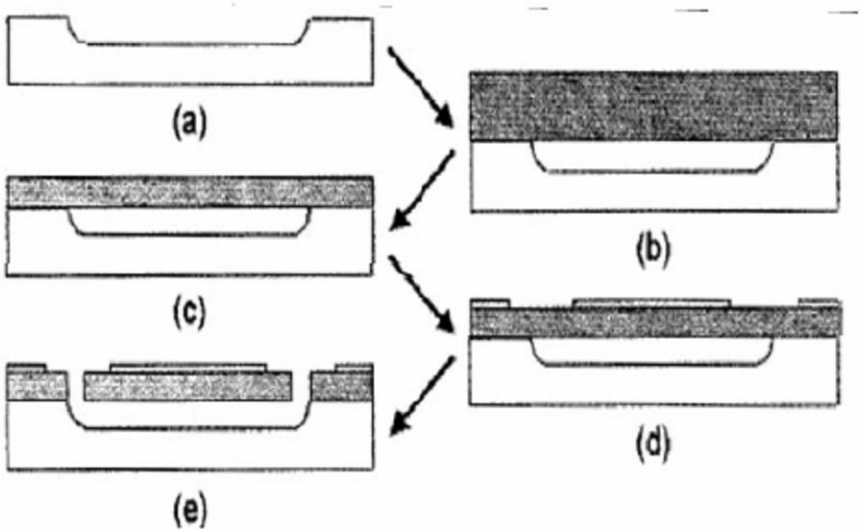
SOG process

- **S**ilicon **O**n **G**lass process
- The Process is combined with deep silicon RIE, glass wet etch, and bonding process between silicon wafer and glass wafer
- Structure are defined by deep Si RIE
- Moving structure are released by glass wet etching

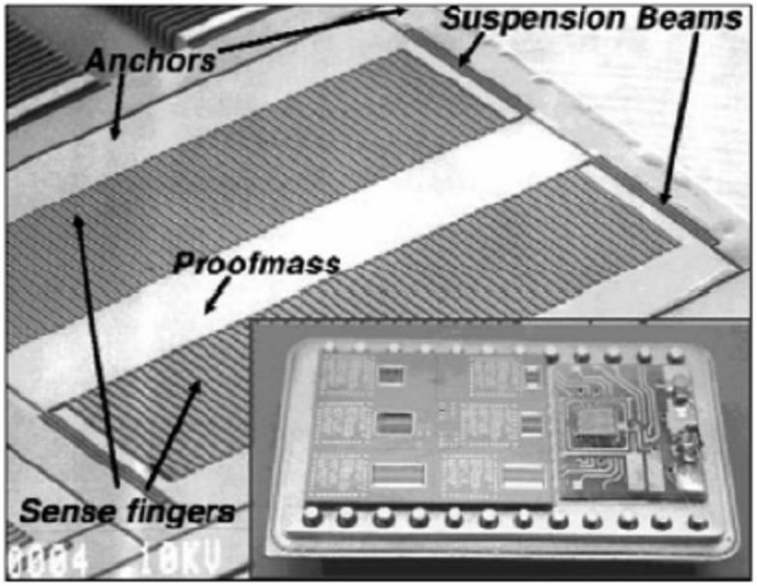


Example by SOG process (1)

- SOG process example (1)
  - SOG lateral micro-accelerometer (University of Michigan)



Fabrication process

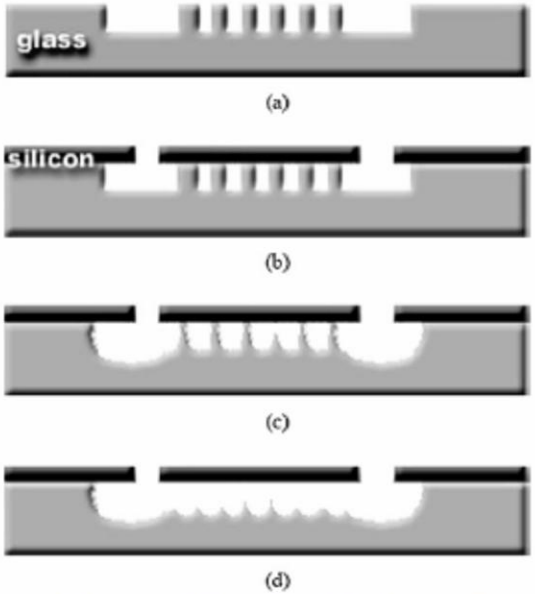


Fabricated micro-accelerometer

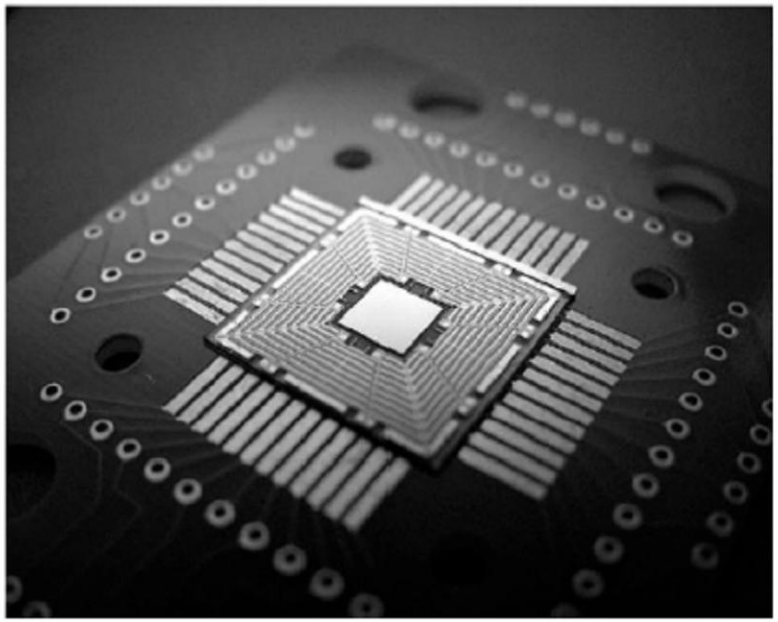
Ref.) C. Junseok, H. Kulah, and K. Najafi, MEMS'02, pp. 623-626, 2002

Example by SOG process (2)

- SOG process example (2)
  - Silicon micro XY stage (MiSA SNU)
  - uCARP (Micro Channel Assisted Release Process) is proposed to release the large plate structure



Micro Channel Assisted Release Process

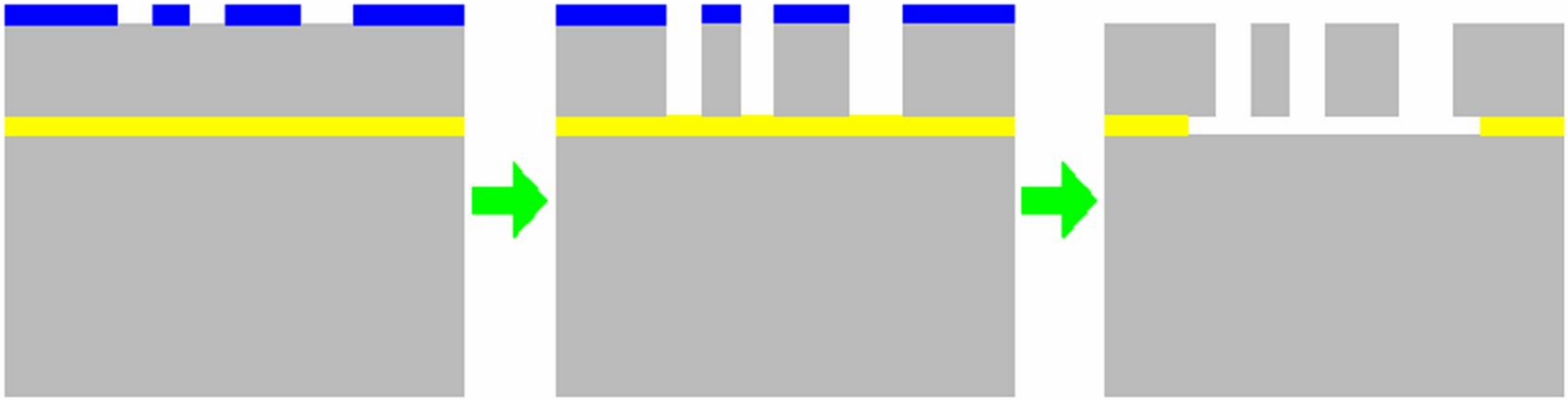


Fabricated micro XY-stage (PCB packaged)

Ref.) C. Kim, H. Jeong, J. Jeon, and Y. Kim, JMEMS, Vol. 12, No. 4, pp. 470-478, 2003

SOI process (1)

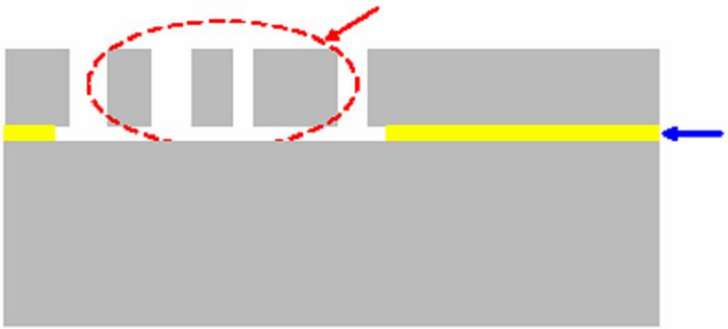
- **S**ilicon **O**n **I**nsulator process
  - Dry anisotropic etching to etch a pattern into the silicon layer on top of the insulator
  - Structures are released by etching the sacrificial buried oxide insulator layer, which displays a thickness with a high reproducibility (400±5 nm) and uniformity (<±5 nm)



Typical SOI Process

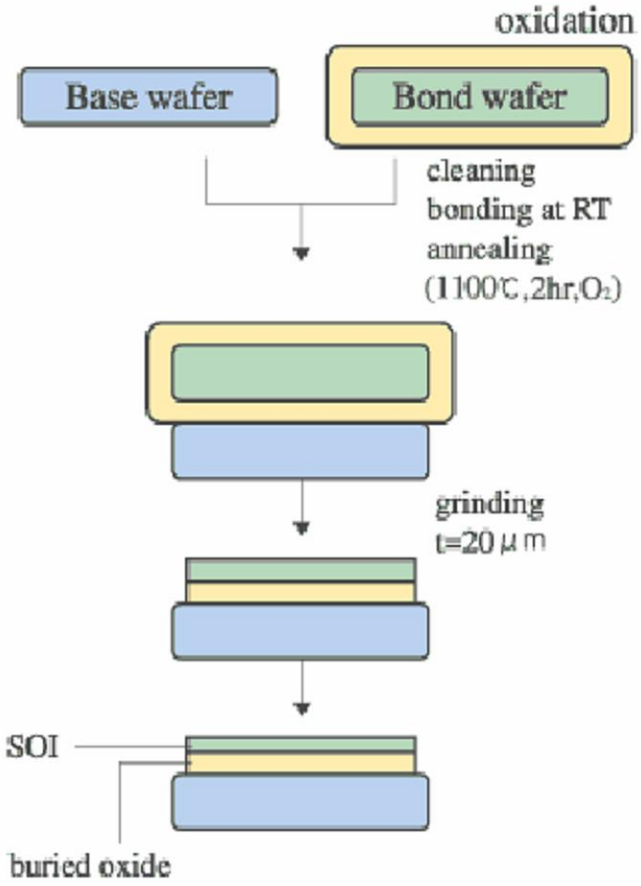
SOI process (2)

- SOI process advantages
  - CMOS compatibility
  - Buried oxide as sacrificial and insulating layer as excellent etch stop
  - Freedom of shape in xy dimensions and continually improving dry etching techniques, resulting in larger high aspect rations and higher features
  - Dramatic reduction of process steps as the SOI wafer comes with several embedded process steps



SOI wafer (1)

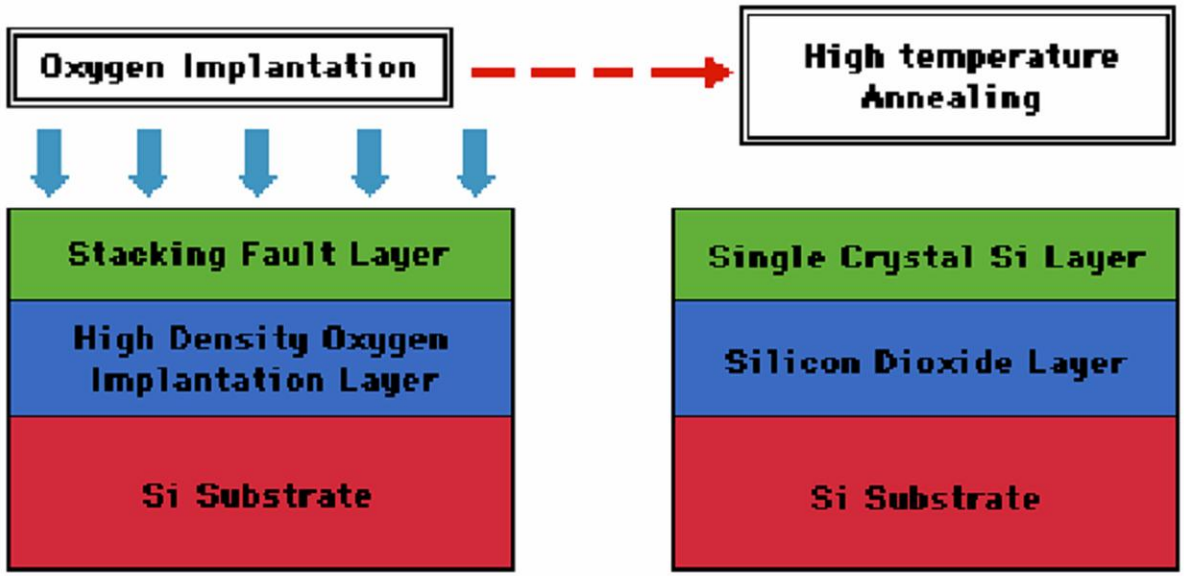
- SOI (Silicon On Insulator) wafer
  - In SOI, bulk silicon wafers are replaced with wafer that have three layers
    - A thin surface layer of silicon (from a few hundreds angstroms to several micron meters)
    - An underlying layer of insulating material → buried oxide or BOX
    - A support or handle silicon wafer
  - Typical SIO dimensions
    : 10~100 um/0.25~2 um/400 um
  - SOI in MEMS
    - Fewer process steps are needed for feature isolation
    - Parasitic capacitance is reduced
    - Power consumption is lowered



Bonded wafer production

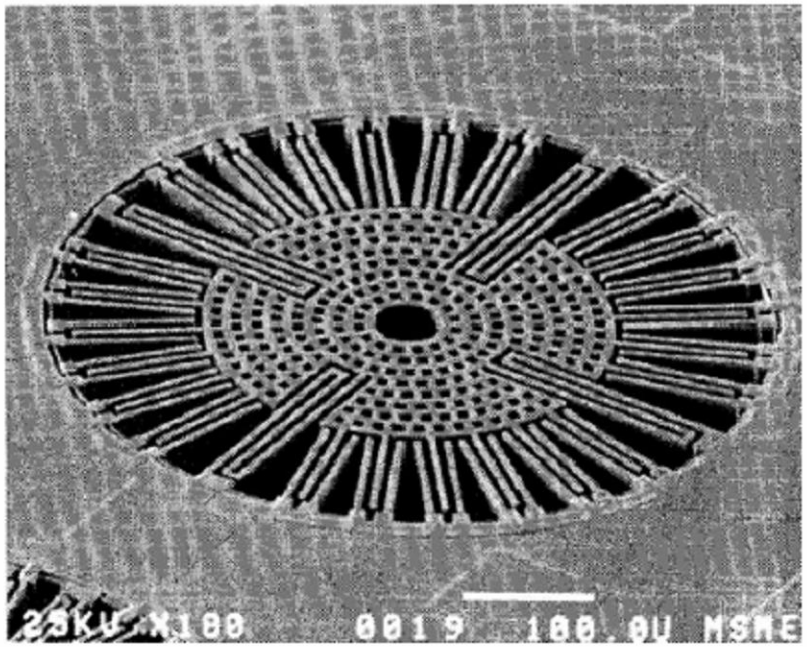
SOI wafer (2)

- SIMOX (Separation by IMplanted OXygen)
  - Oxygen Implantation into Si Substrate
  - High temperature Annealing
  - Silicon + Oxygen → Silicon Dioxide Layer
  - Typical SIMOX dimensions: 1~10 um/0.1~0.4 um/400 um

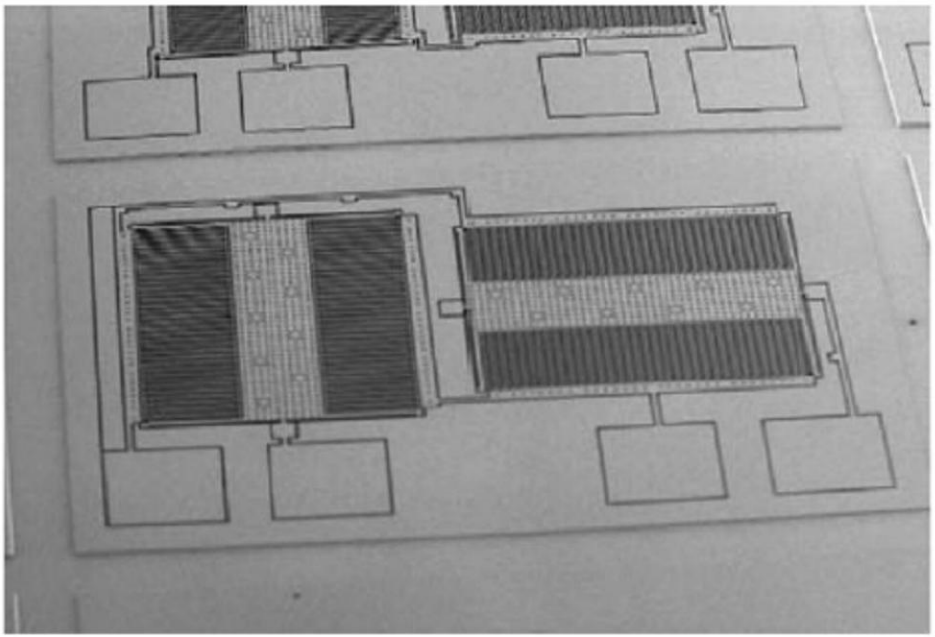


Example by SOI process (1)

- IMU sensor



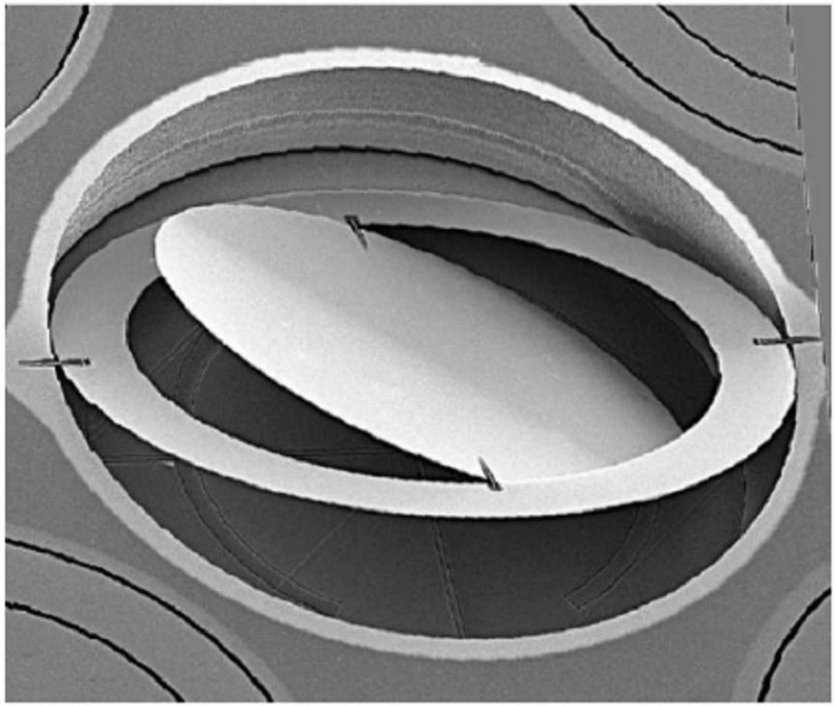
SOI accelerometer
(UC Berkeley)



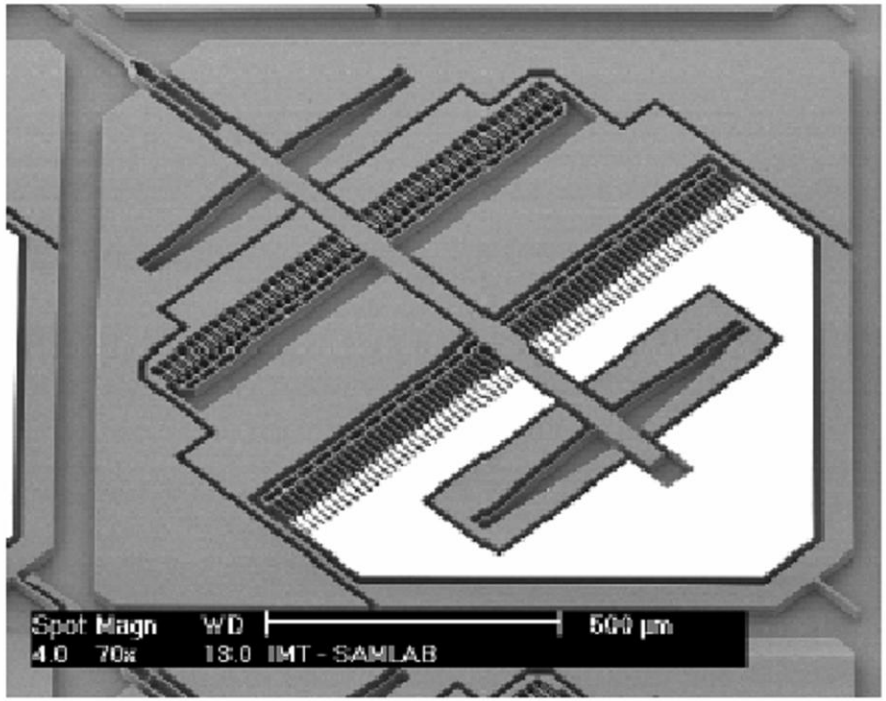
Twin axis accelerometer using SOI wafer
(TRONIC'S Microsystems)

Example by SOI process (2)

- Optical MEMS



Silicon tilting mirror
(Lucent Technologies)



On/off optical switch
(Neuchatel Univ.)