ELPL Embedded Low-Power Laboratory

Embedded System Application

4190.303C

2010 Spring Semester

On-board Signal Integrity and DDR2 Bus (SSTL) Specification

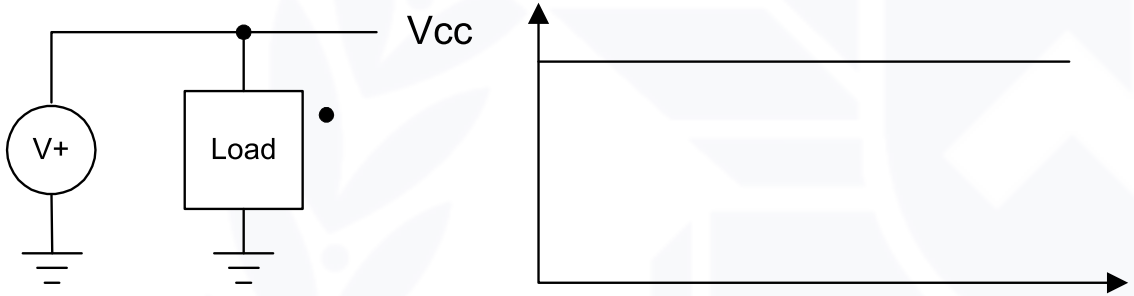
Naehyuck Chang
Dept. of EECS/CSE
Seoul National University
naehyuck@snu.ac.kr

Agenda

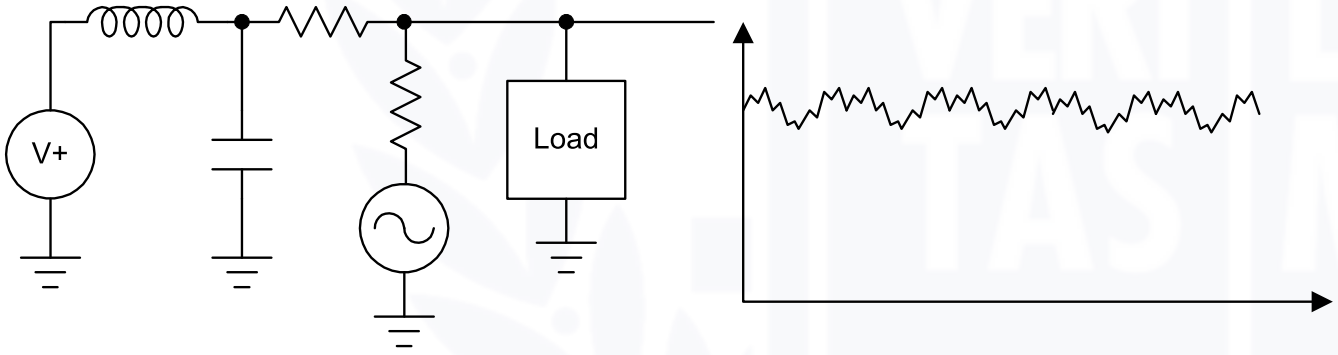
- Power Integrity
- Definition of high-speed signaling
- Controlled impedance lines
- Transmission line effect
- Reflection
- Termination
- Crosstalk
- DDR2 bus specification

Power Integrity

- Before we mention signal integrity
  - Power integrity first



a) Ideal power source: zero line impedance



b) Realistic power source: non-zero line impedance

Power Integrity

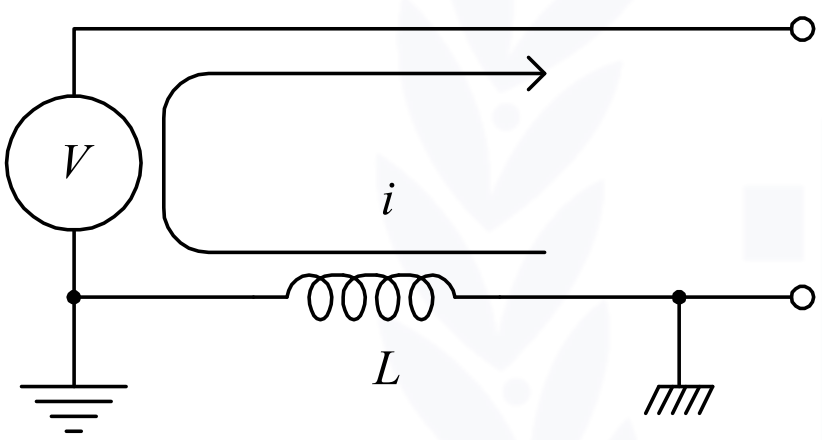
- Why power integrity?
  - Power supply impedance
    - Resistive component
    - Inductive component

$$V_{drop} = iR + L\frac{di}{dt}$$

- 20 A current with DC resistance 0.05 Ω
  - Yields 1 V IR drop
  - TTL operating range is 4.75 V to 5.25 V
- 0.1 A current change in 2 ns with 500 nH
  - Yields 25 V L di/dt drop!
  - In practice, yields much less voltage drop since 500nH prevents 0.1 A current change itself in 2 ns

Power Integrity

- Ground bounce
  - Digital logic gate is a differential amplifier
  - Reference is GND
  - Earthquake!



V

$v = V - L\frac{di}{dt}$

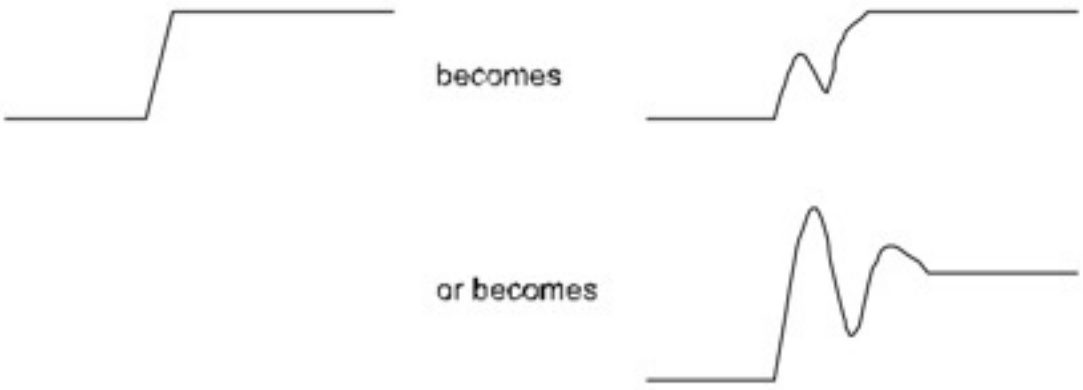
$L\frac{di}{dt}$

Definition of high-speed signaling

- DDR2 data transfer bandwidth
  - Even SDRAM data transfer speed is 133 MHz

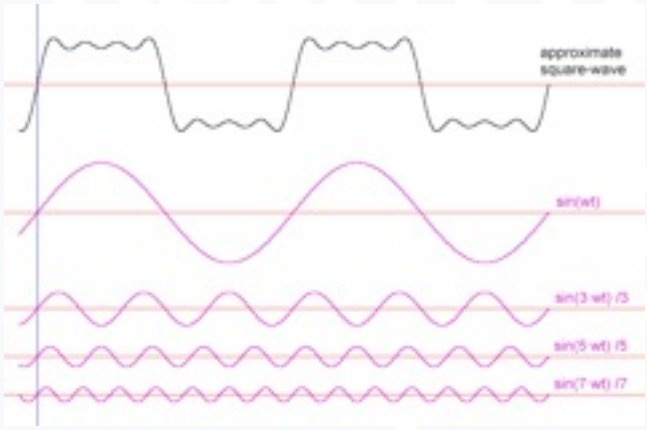
Memory	Clock Frequency	Data Rate
DDR200	100 MHz	200 MHz
DDR266	133 MHz	266 MHz
DDR333	167 MHz	333 MHz
DDR400	200 MHz	400 MHz

- High-speed signaling causes signal integrity problem



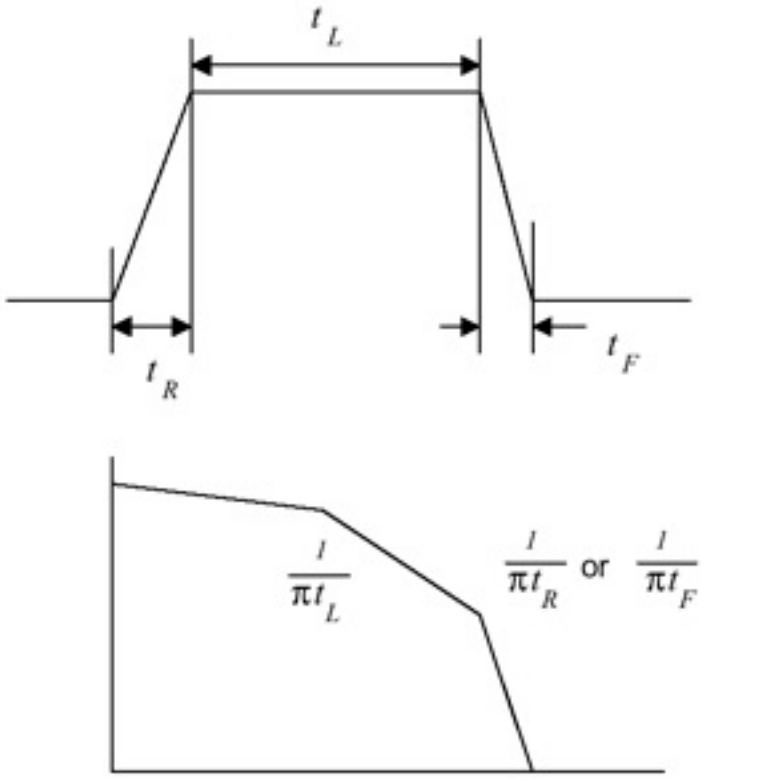
Definition of high-speed signaling

- Speed is one of the most important design factor
  - Hundreds of MHz data transfer clocks are widely available
- Definition of high-speed signaling?
  - Is there a clear threshold of high-speed signaling?
  - Is 2 GHz a high frequency?
  - Is 100 KHz not so much a high frequency?
  - What about 10 MHz?
- Questions from my neighborhood professors
  - Laboratory equipments for digital system design
- Before we answer the question...
  - Digital systems do not use sine wave!
  - Demand for short propagation delay
    - Fast edge rate is required
- What is a square wave?
  - Collection of independent sine waves



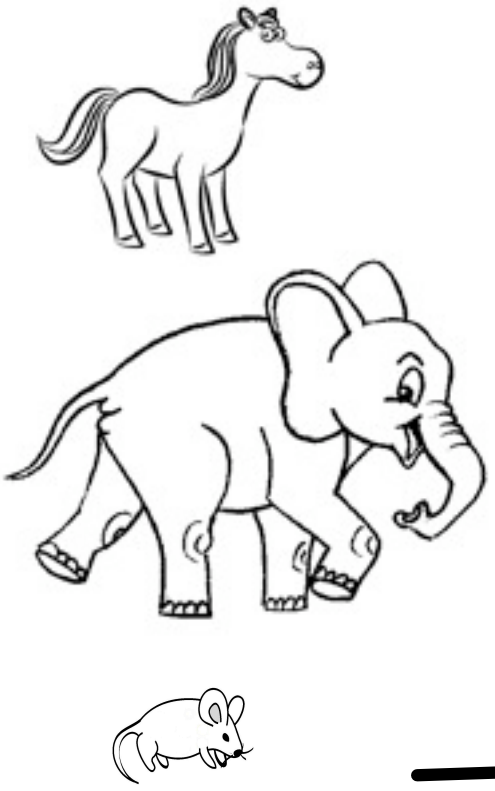
Definition of high-speed signaling

- Power spectrum of a square wave
  - Knee frequency
- Frequency components that determines the knee frequency
  - Rise time (t_R)
  - Fall time (t_F)
  - Pulse width (t_L)
  - Usually t_F is the shortest components
- Below the knee frequency,
  - High power distribution
  - More information to be delivered
  - Should be carefully handled
- Above the knee frequency,
  - We might ignore them



Definition of high-speed signaling

- Signal integrity

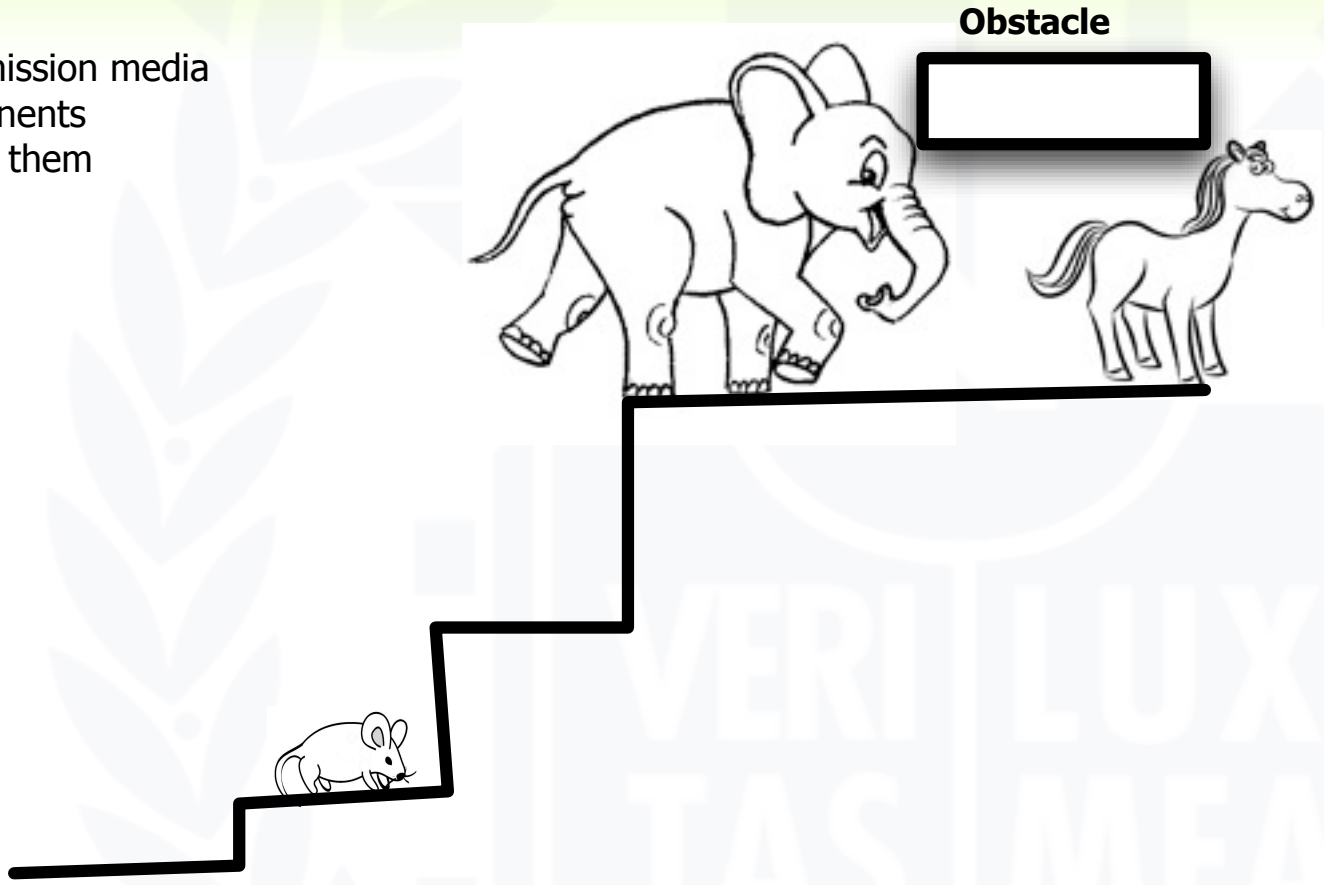


Animal march

Stair cases

Definition of high-speed signaling

- Signal integrity
  - Improper transmission media may lose components or incur delay of them
  - Blur the march!

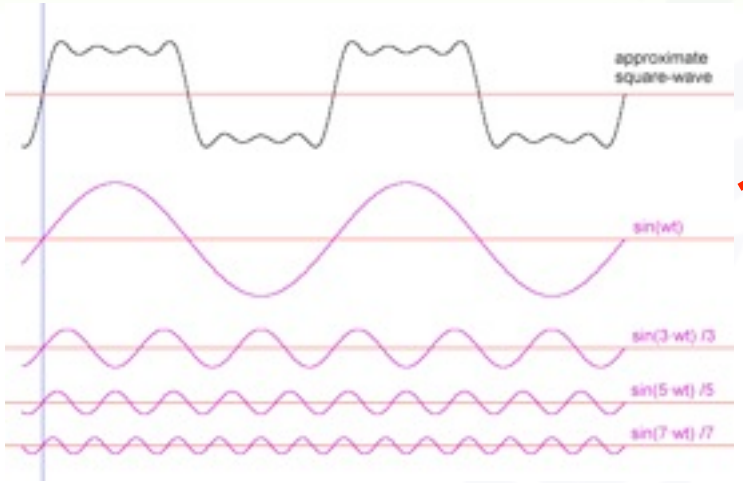


Animal march

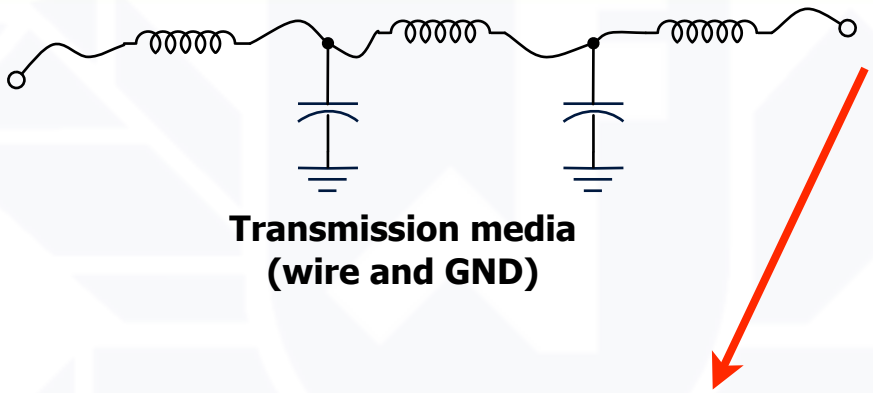
Stair cases

Definition of high-speed signaling

- Signal integrity



Square wave input



Transmission media (wire and GND)

Passed

Passed but delayed

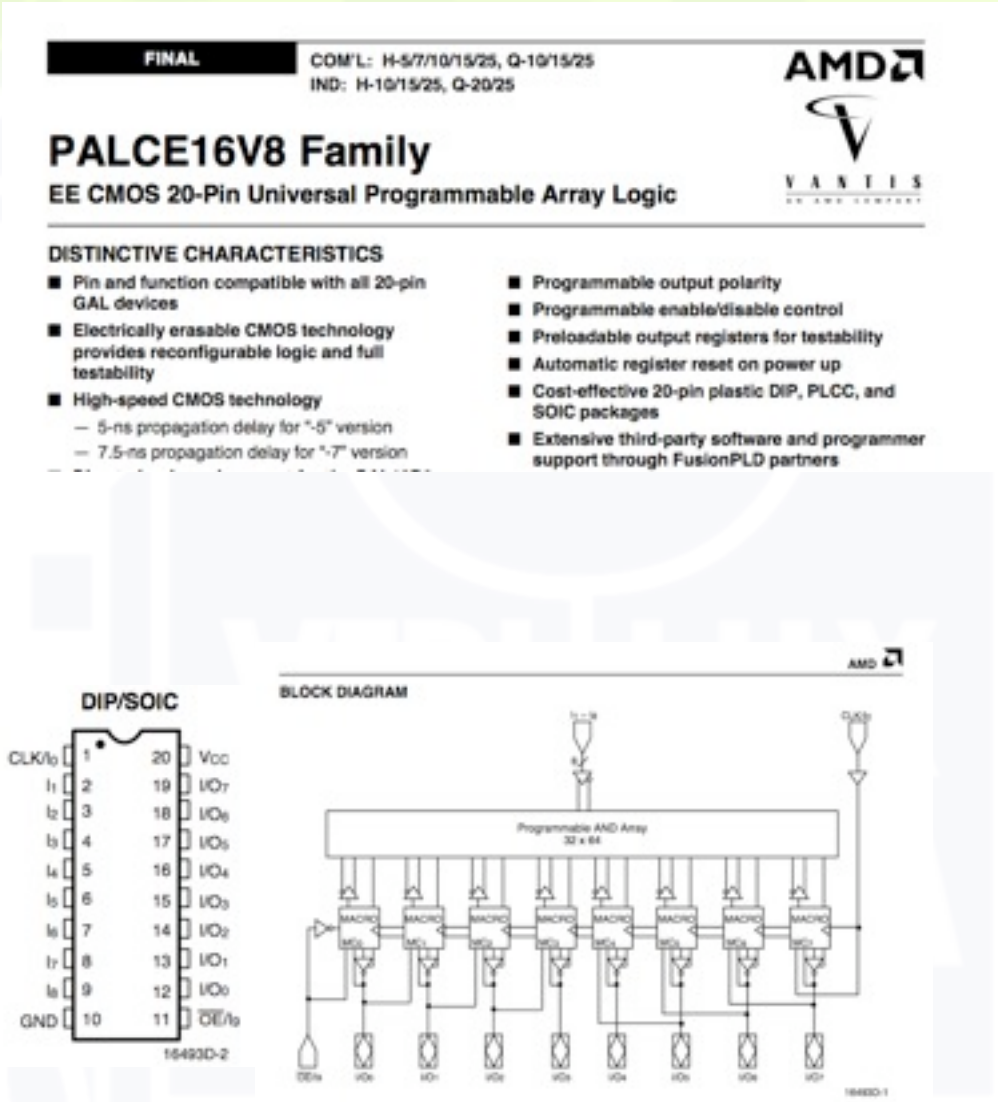
Shrunk and delayed

Lost

Square wave output

Definition of high-speed signaling

- Example
  - PALCE16V8: t_F = 2 ns
  - f_N = 1/(π × 2 ns) = 160 MHz
  - f_N = 0.5/(2 ns) = 250 MHz
- We should take care of frequency components up to 250 MHz **regardless of the clock frequency!**
  - Base frequency is not generally important
- Modern semiconductor chips are designed to operate in a high clock frequency
  - Use of the device implies your design is subject to high-speed signaling



FINAL

COM'L: H-5/7/10/15/25, Q-10/15/25
IND: H-10/15/25, Q-20/25

AMD

VANTIS

PALCE16V8 Family

EE CMOS 20-Pin Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- Pin and function compatible with all 20-pin GAL devices
- Electrically erasable CMOS technology provides reconfigurable logic and full testability
- High-speed CMOS technology
  - 5-ns propagation delay for "-5" version
  - 7.5-ns propagation delay for "-7" version
- Programmable output polarity
- Programmable enable/disable control
- Preloadable output registers for testability
- Automatic register reset on power up
- Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages
- Extensive third-party software and programmer support through FusionPLD partners

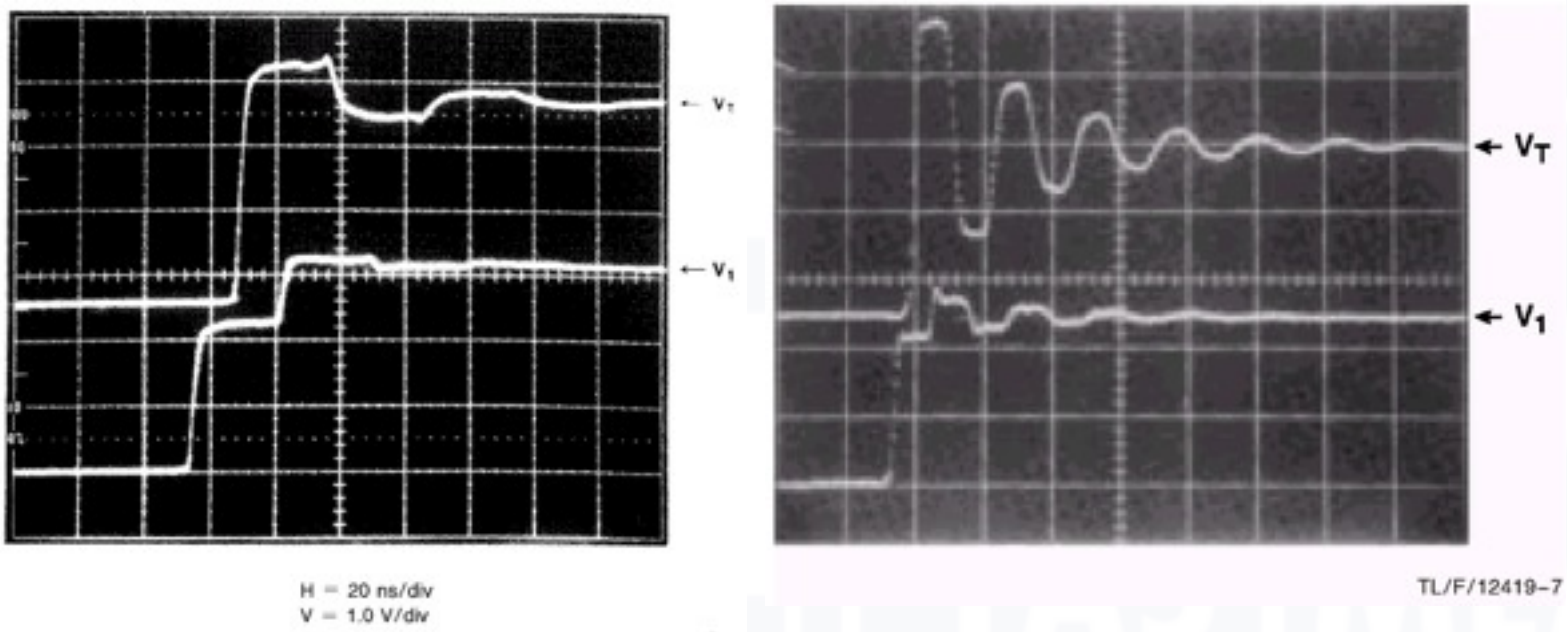
DIP/SOIC

16493D-2

BLOCK DIAGRAM

Definition of high-speed signaling

- Is signal integrity assured if the parasitic inductance and capacitance are virtually eliminated within the frequency range of interest?
  - The answer is negative because wave reflection



Wave distortion by reflection

Definition of high-speed signaling

- Lumped circuits
  - The differential equations obtained for the circuit using KVL and/or KCL (i.e., loop or nodal analysis) involve only one variable: time
  - Assuming that the entire circuit is at a single point in space, or equivalently, that the travel time of the electric signal is negligible
- No more lumped circuits
  - A distributed circuit is one for which the travel time of the electric signal between the components cannot be neglected
  - The voltages and currents in such a circuit are functions of position as well as time

Definition of high-speed signaling

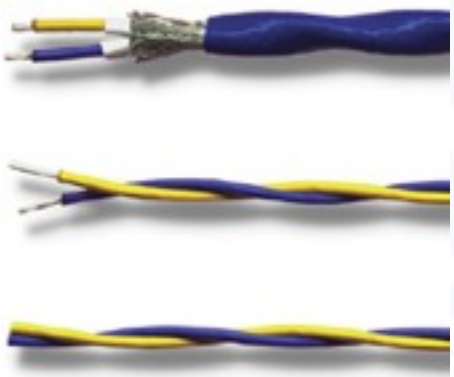
- Distinguish between a lumped and a distributed circuit
  - **Rise time versus travel time**
  - Period versus travel time
  - Component size versus wavelength
  - Rule of thumb
    - $t_R/t_{PD} > 6$ → definitely lumped
    - $t_R/t_{PD} < 2.5$ → definitely distributed

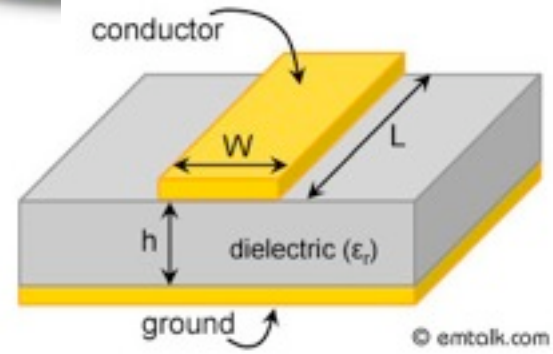
Definition of high-speed signaling

- Lumped components with all dimensions much smaller than λ
  - Resistors, capacitors, inductors, etc.
- Distributed components with one dimension either comparable to or greater than λ, and other dimensions much smaller than λ
  - Coaxial cables, hollow waveguides, handset antennas for wireless communications, etc.
- Distributed components with all dimensions much greater than λ
  - Graded index optical fibers, reflector antennas, etc.

Controlled Impedance Line

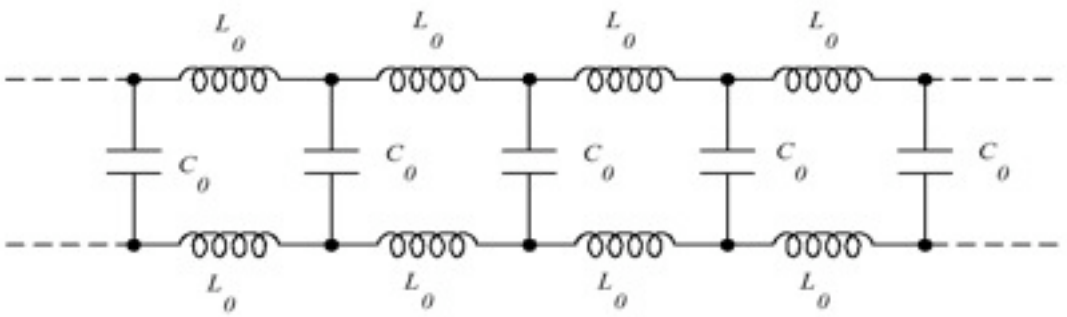
- Controlled Impedance Line
  - A uniform transmission line consists of two (or more) parallel conductors separated by a vacuum or other insulating material
  - The cross-section of a uniform transmission line is small compared to λ and does not change over the length of the transmission line which is (usually much) greater than 0.1λ





Controlled Impedance Line

- Controlled Impedance Line
  - Inductance and capacitance are evenly distributed along the length of the line



- Inductance and capacitance are evenly distributed along the length the line
- Z_0: AC resistance, unit is Ω

$$Z_0 = \sqrt{\frac{L_0}{C_0}}$$

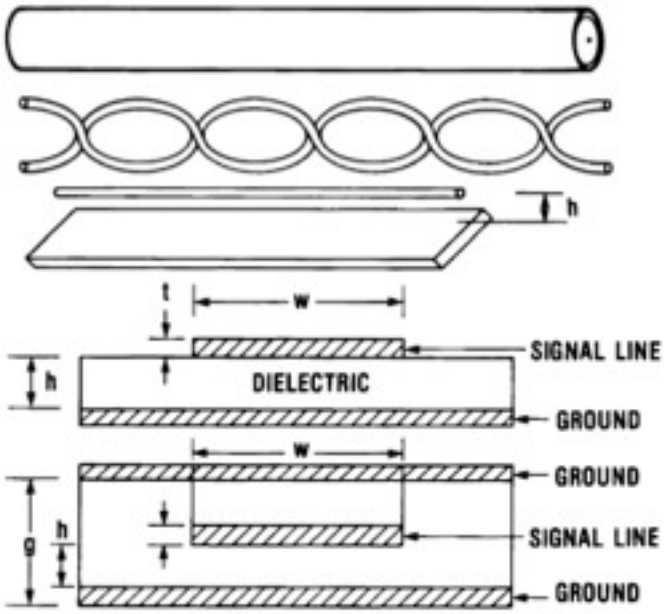
L_0: Signal line inductance in Henrys per unit length
C_0: Signal line capacitance in Farads per unit length

- t_{PD}: propagation delay

$$t_{PD} = \sqrt{L_0 C_0}$$

Controlled Impedance Line

- Typical impedance of controlled impedance lines

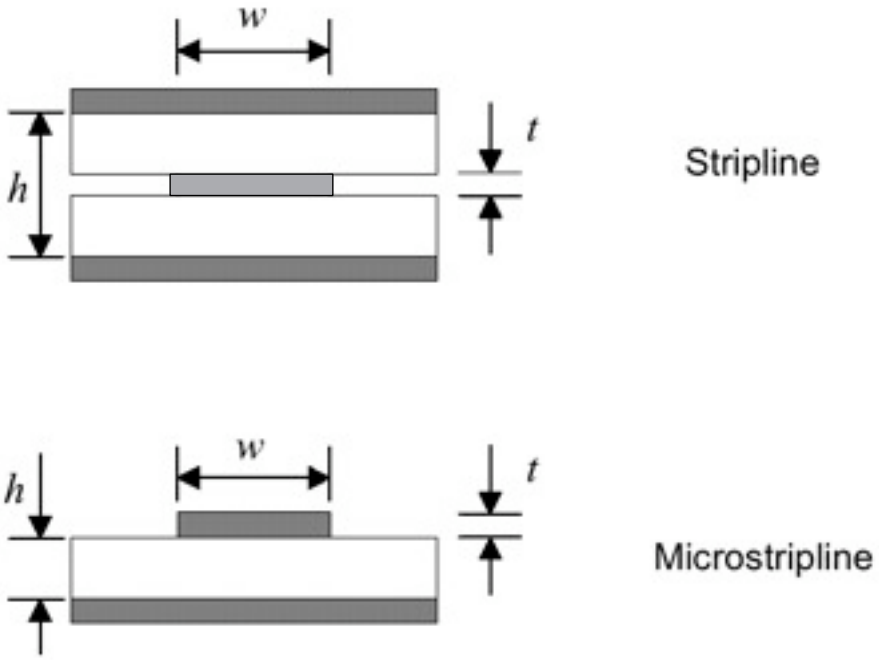


COAXIAL CABLE	Z_o = 50, 75, 125Ω
TWISTED PAIR	Z_o = 50 TO 100Ω
WIRE OVER GROUND	$Z_o = \frac{60}{\sqrt{\epsilon_R}} \ln\left(\frac{4h}{d}\right)$ TYPICALLY Z_o = 120 TO 200Ω
MICROSTRIPLINE	$Z_o = \frac{87}{\sqrt{\epsilon_R + 1.41}} \ln\left(\frac{5.98}{0.8w + t}\right)$ TYPICALLY Z_o = 50 TO 100Ω
STRIPLINE	$Z_o = \frac{60}{\sqrt{\epsilon_R}} \ln\left[\frac{4b}{0.67\pi w(0.8 + \frac{t}{w})}\right]$ $\frac{w}{(b-t)} < 0.35$ AND $t/b < 0.25$ TYPICALLY Z_o = 30 TO 80Ω

AN008424-1

Controlled Impedance Line

- Stripline and microstripline



Controlled Impedance Line

- Example of a microstripline on an epoxy-laminated fiberglass printed circuit board
  - A common material is epoxy-laminated fiberglass, which has an average dielectric constant of 5

$$Z_0 = \frac{87}{\sqrt{\varepsilon_R + 1.41}} ln \frac{5.98h}{0.8w + t} \Omega$$

$$t_{PD} = 1.017\sqrt{0.457\varepsilon_R + 0.67}\ ns/ft$$

$$C_0 = 1000\frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

Controlled Impedance Line

- Example of a microstripline on an epoxy-laminated fiberglass printed circuit board
  - Copper thickness is 1 mil
  - Track width is 8 mils (typically 8 to 15 mils)
  - Layer separation is 30 mils

$$Z_0 = \frac{87}{\sqrt{5}+1.41} ln \frac{5.98 \times 0.03}{0.8 \times 0.001 + 0.01} \Omega = 67.05\,\Omega$$

$$t_{PD} = 1.017\sqrt{0.457 \times 5 + 0.67}\; ns/ft = 1.75\; ns/ft$$

$$C_0 = 1000\frac{1.75}{67.05}\; pF/ft = 26.1\; pF/ft$$

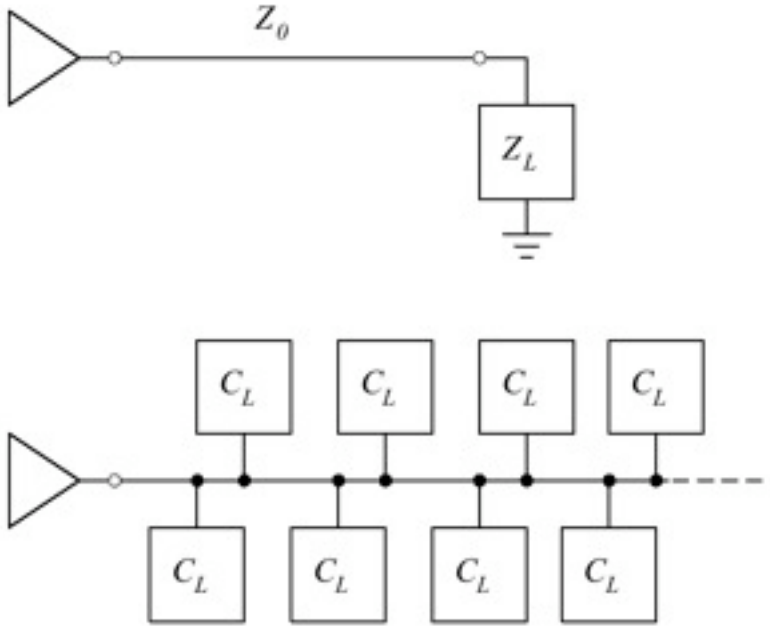
$$L_0 = 67.05^2 \times 26.1\; pF/ft = 117\; pH/ft$$

Controlled Impedance Line

- Lumped or distributed load
  - New parameter CL: added capacitance in Farads per unit length
  - DRAM: 4 to 12 pF

$$Z_0 = \frac{Z_0}{\sqrt{1 + \frac{C_L}{C_0}}} \Omega$$

$$t_{PD} = t_{PD}\sqrt{1 + \frac{C_L}{C_0}}\ ns/ft$$



Controlled Impedance Line

- Example
  - Input capacitance is 5 pF, and clearance is 200 mil

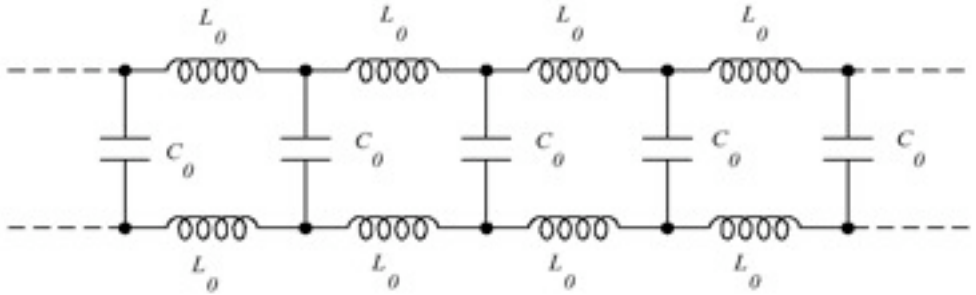
$$C_L = \frac{5\,pF}{0.5\,in\frac{1\,ft}{12\,in}} = 120\,pF/ft$$

$$Z_0 = \frac{67.05}{\sqrt{1+\frac{120\,pF/ft}{26.1\,pF/ft}}} = 28.34\,\Omega$$

$$t_{PD} = 1.75\,ns/ft\sqrt{1+\frac{120\,pF/ft}{26.1\,pF/ft}} = 4.14\,ns/ft$$

Transmission Line Effect

- Transmission lines
  - Connections capable of carrying a signal between a transmitter and a receiver
    - Telecom-based cables operating over long distances
    - Travel time is long
    - This impedance of the wire is extremely important, as any mismatch within the transmission path will result in a reduction in quality of the signal
    - Controlled impedance line should be used for transmission lines



- PCB tracks
  - At low frequencies, a PCB track may be an ideal circuit without resistance, capacitance or inductance
  - At high frequencies, a PCB track is a transmission line
    - $t_r/t_d < 2.5$

Transmission Line Effect

- Transmission line effects
  - Mismatched impedance results in signal reflection
- CMOS digital logic gates are basically impedance mismatched devices
  - Input impedance is very high
  - Output impedance is very low
  - C.f., emitter coupled logic
- If the interconnect between two CMOS gates is a transmission line, signal reflection occurs

Reflection

- Maximum transfer of energy
  - The load impedance is equal the source impedance
    - $Z_0 = Z_L$
- The waveform at the load
  - Sum of originally generated signal and the reflection from the load
- Recall reflection in physics
  - Generate a wave on a string
  - Reflection from an open end
    - Generates a reflected wave of a 180 degree phase shift
  - Refection from a fixed end
    - Generates a reflected wave of the same phase

Reflection

- Appearance of the waveform depends on
  - Mismatch of the load
  - Line impedance Z_0
  - The ratio of the signal-transition time, t_R to the propagation delay of the line
    - t_R / t_{PD}
- The amount of overshoot usually varies proportionally with the signal-line length until $t_R / t_{RD} = 1$

Reflection

- The overshoot is as much as the original transition
- Rule of Thumbs again
  - A signal line is considered as a transmission line when $t_R/t_{PD} \leq 1/4$
  - More conservative rule is $t_R/t_{PD} \leq 1/8$

PI6C20400
1:4 Clock Driver for Intel PCI Express Chipsets

Symbol	Parameters	Min	Max.	Units
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V)	175	700	ps
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation		125	ps

Reflection

- Example
- t_R (ns), line length (in) with the condition of t_R/t_{PD} = 1/4

t_R (ns)	Line length (in)	
	Lumped load	Distributed load
5	8.5	3.6
3	5.1	2.17
2	3.4	1.4
1	1.7	0.75

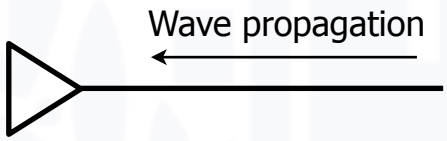
Reflection

- Qualifying reflection
  - Reflection coefficient
    - Z0 is the transmission line impedance
    - ZL is the load impedance

$$K_R = \frac{Z_L - Z_0}{Z_L + Z_0}$$

- Short load
  - Load is a CMOS logic gate output
    - Ideal CMOS logic gate output impedance is 0

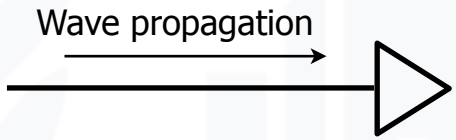
$$K_R = \frac{0 - Z_0}{0 + Z_0} = -1$$



Reflection

- Open load
  - Load is a CMOS logic gate input
    - Ideal CMOS logic gate input impedance is ∞

$$K_R = \frac{\infty - Z_0}{\infty + Z_0} = 1$$



Reflection

- Real case example: CMOS GAL PALCE16V8 and microstripline
  - Z_0 ranges from 30 to 150 Ω
  - Input impedances range from 10 K to 100 KΩ
  - Driver's output impedance
    - Rough approximation

$$Z_S = \frac{V_{OL}}{I_{OL}} = \frac{0.2\,V}{24\,mA} = 8.3\,\Omega$$

  - Since input impedance 100K Ω, K_R at load:

$$K_R = 1$$

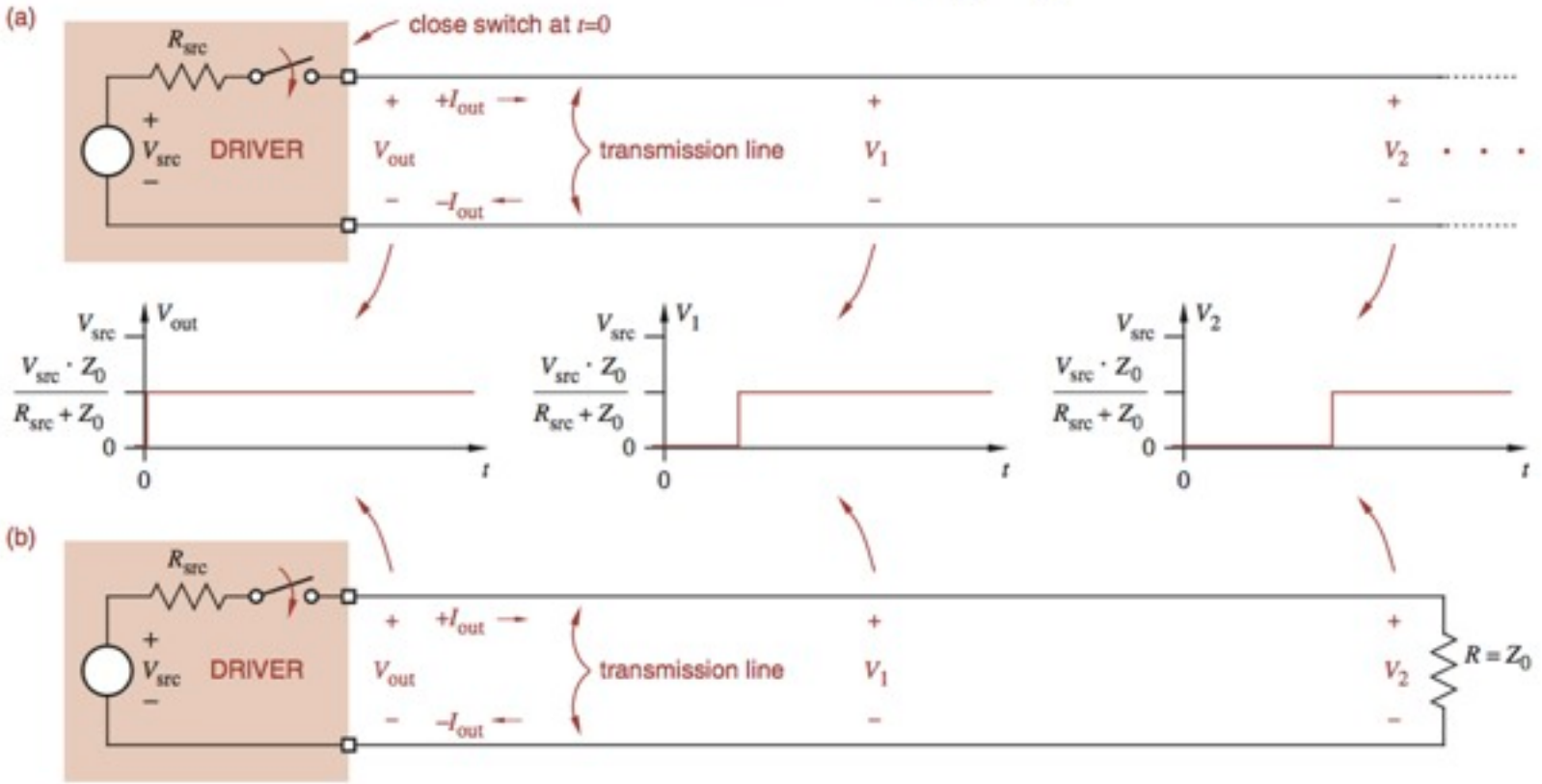
  - Since Z_0 = 67 Ω, K_R at source:

$$K_R = \frac{8.3 - 67}{8.3 + 67} = -0.78$$

Reflection

- Wave propagation

$$V_{out} = V_{src} \cdot \frac{Z_0}{R_{src} + Z_0}$$



Reflection

- Wave propagation (incident wave)
  - Driver generates 3.5 V $\Rightarrow$ 0.2 V

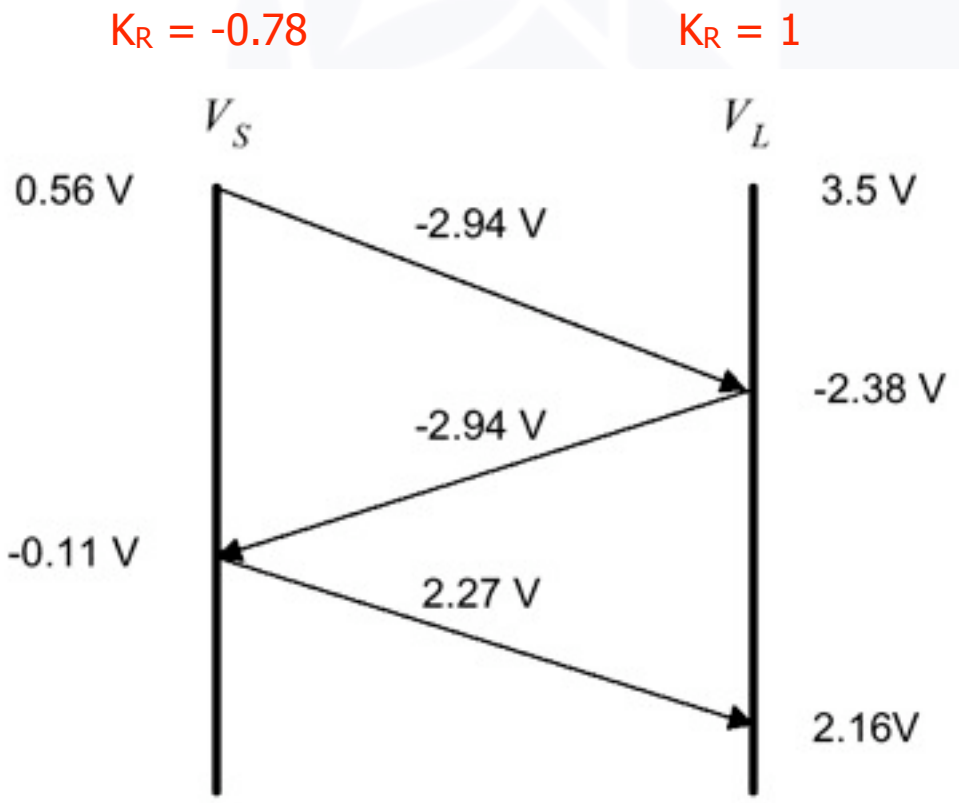
$$\Delta_V = \frac{(0.2\,V - 3.5\,V)Z_0}{Z0 + Z_s} = \frac{-3.3\,V \times 67\,\Omega}{67\,\Omega + 8.3\,\Omega} = -2.94\,V$$

  - Resultant signal, V_S:

$$V_S = 3.5\,V + \Delta_V = 0.56V$$

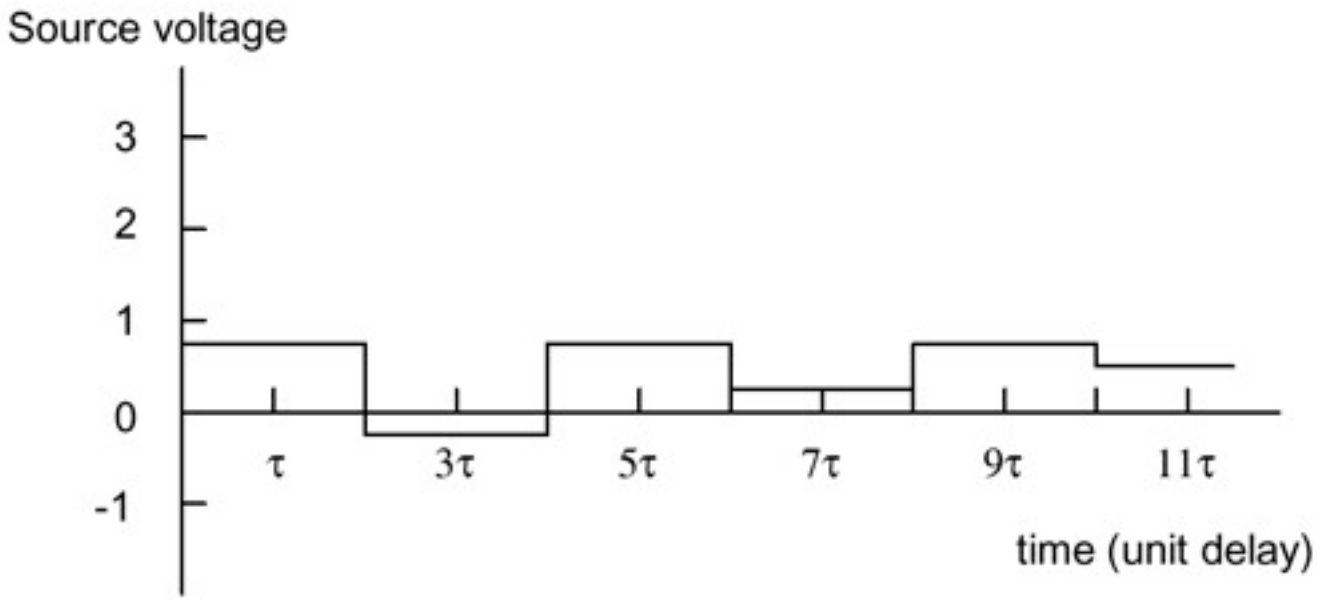
Reflection

- Lattice diagram with superposition theory



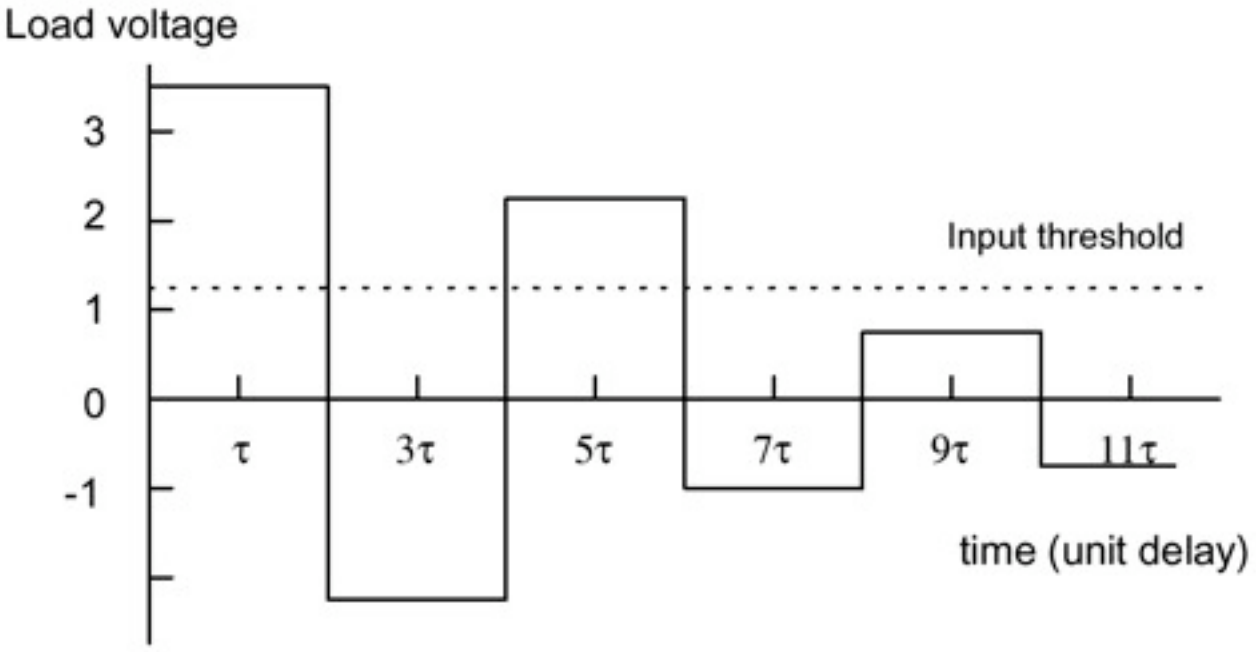
Reflection

- Settling time and delay: source voltage



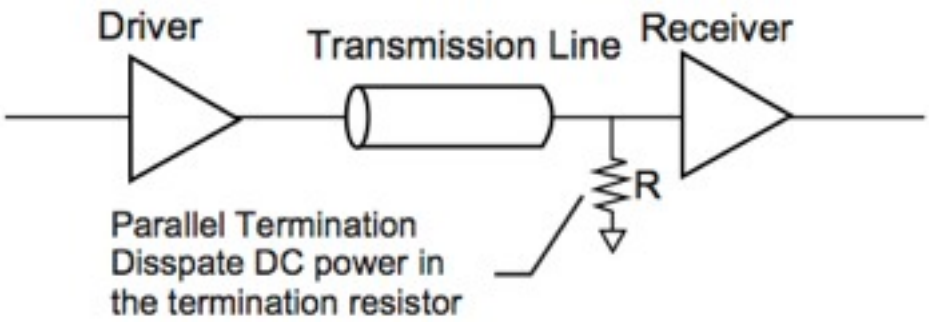
Reflection

- Settling time and delay: source voltage



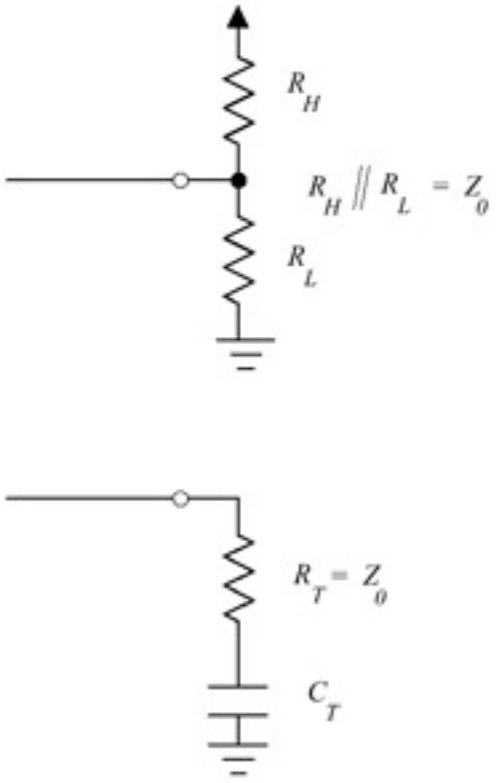
Termination

- Reflections are eliminated when $Z_L = Z_0$
- How to make $Z_L = Z_0$?
- Parallel termination (end termination)
  - Reduce Z_L to Z_0 : eliminate the first reflection
    - Placing parallel register with the load current drain is high for the HIGH-output state
    - Terminating to Vcc helps since I_{OL} is usually high than I_{OH}, but normally not enough
    - Termination to a DC reference voltage: 50 register to 3 V reference



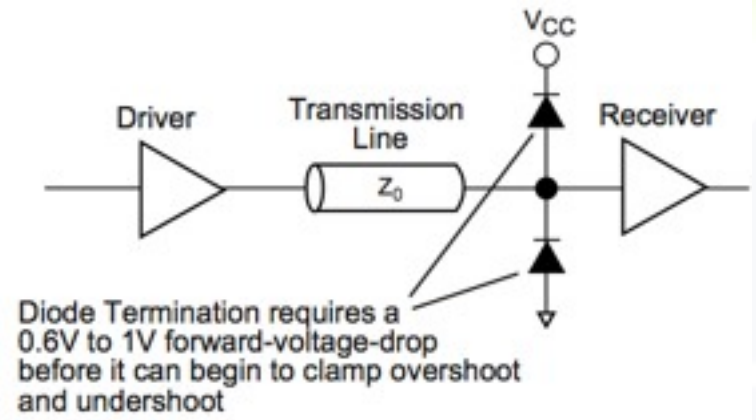
Termination

- Parallel termination (end termination)
  - Drawbacks
    - Too much DC current
- Variations
  - Split termination
    - Reduce the maximum DC current by half
    - Does not use the same value of the pull up and pull down resistors to maintain default voltage level not close to 1/2 VDD, e.g, 220/330 or 330/470
  - AC termination
    - Use of a capacitor to cut the DC current during steady state
    - Determination of the capacitance is critical because it affects the slew rate variation



Termination

- Variations
  - Diode termination
    - Does not involve load impedance nor does it consume DC power
    - Forward- voltage-drop of 0.6V to 1V
    - Less effective as the logic voltage level moves to a lower voltage such as 2.5V and 1.8V
  - Active termination
    - Use of an active termination device
    - Cost



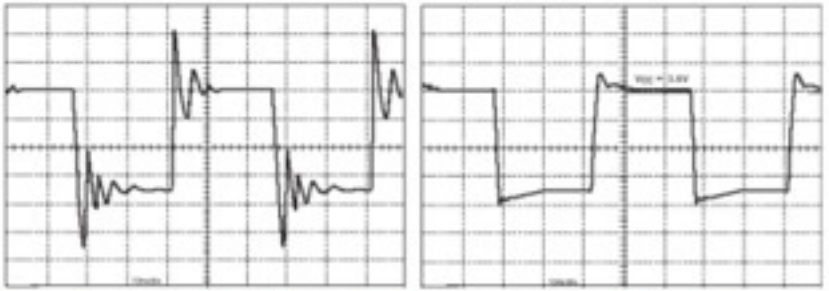
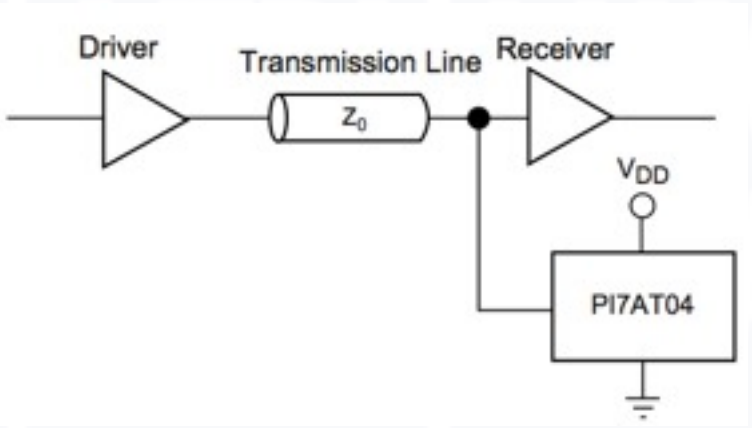


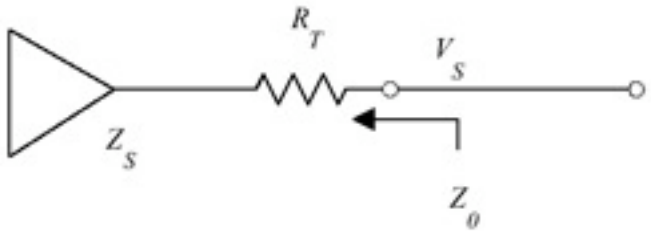
Figure 6. Signal with overshoot and undershoot when not using the PI7AT04.

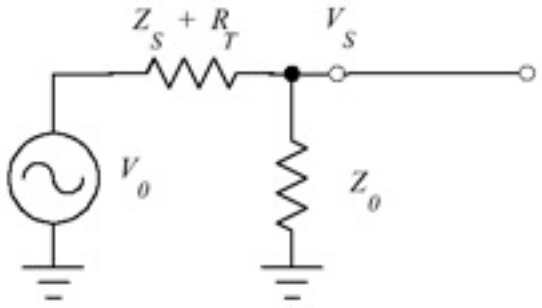
Figure 7. Overshoot and undershoot are reduced when using the PI7AT04



Termination

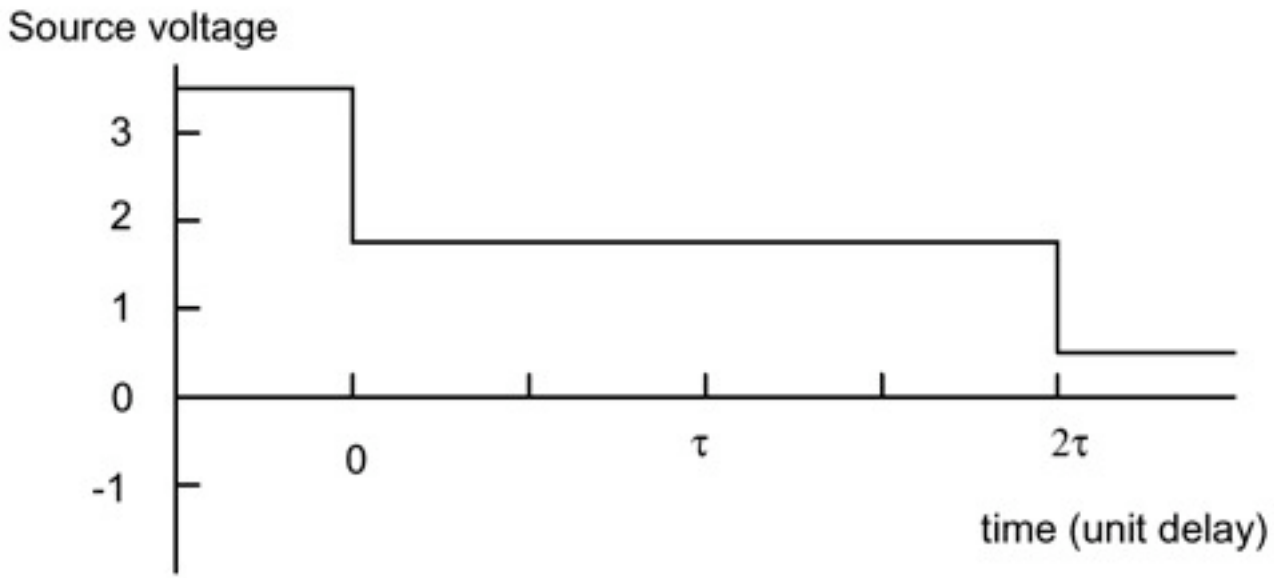
- Source termination methods: $Z_L = Z_0$
- How to make $Z_S = Z_0$?
  - Increase Z_S to Z_0 : eliminate the second reflection
    - placing a series register with the source: best for a lumped load
    - Since the load is open, ΔV reflects from the load to the source
    - There is no second reflection
    - Risky approach for a distributed load because of the intermediate voltage
    - The device close to the driver has a valid input after a return trip; However, it is popular for a DRAM array





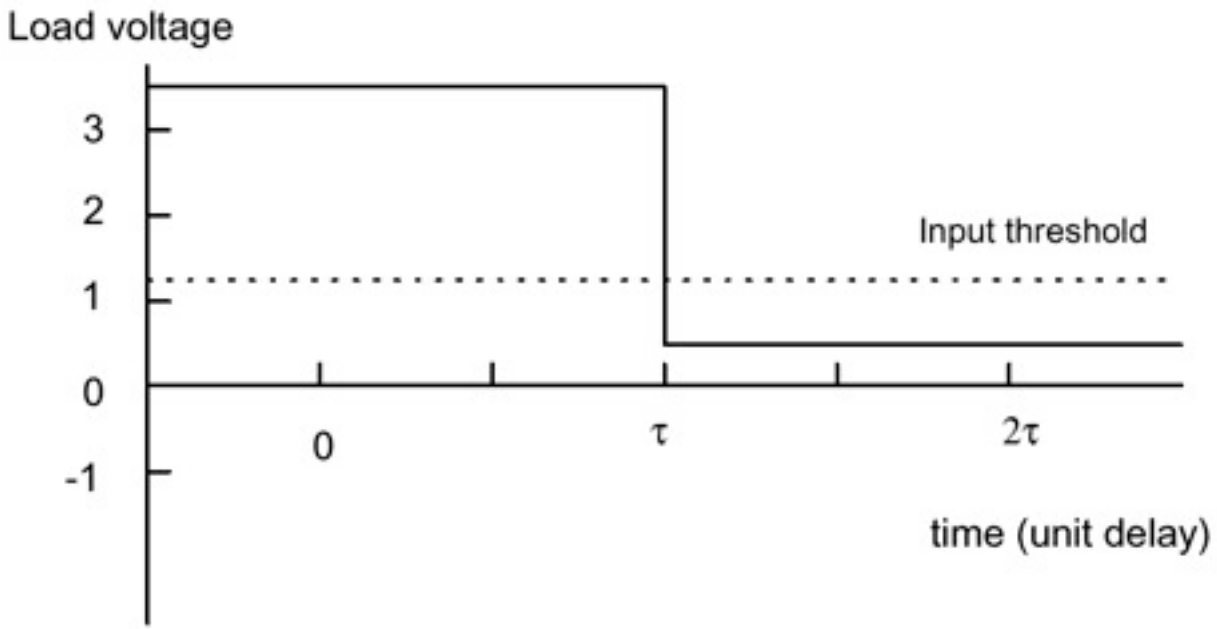
Termination

- Source termination
  - Settling time and delay: source voltage



Termination

- Source termination
  - Settling time and delay: load voltage

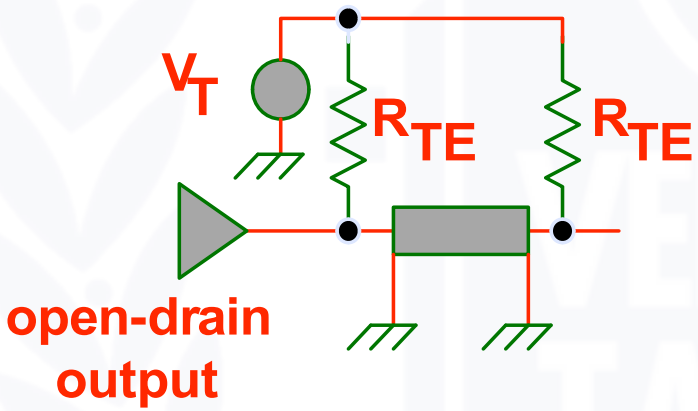


Termination

- Source termination
  - Choose R_T such that $R_T + Z_S < Z_0$
    - Reduce the additional delay by making the intermediate voltage below the threshold level
    - This is not an exact match, thus inducing ringing, but tolerable
    - Generally, exact match is difficult, because HIGH-impedance and LOW-impedance are different: for PALCE16V8, 50 Ω and 8 Ω, respectively

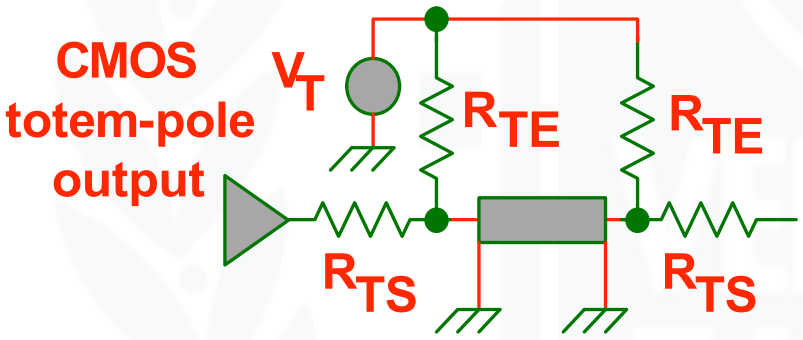
Termination

- Industrial standards that include termination resistors as default
  - GTL+
    - Processors to memory controllers
    - Intel Pentium™ processor
    - 3.3V supply
    - Open-drain output end-terminated to 1.5V
    - CMOS and BiCMOS versions



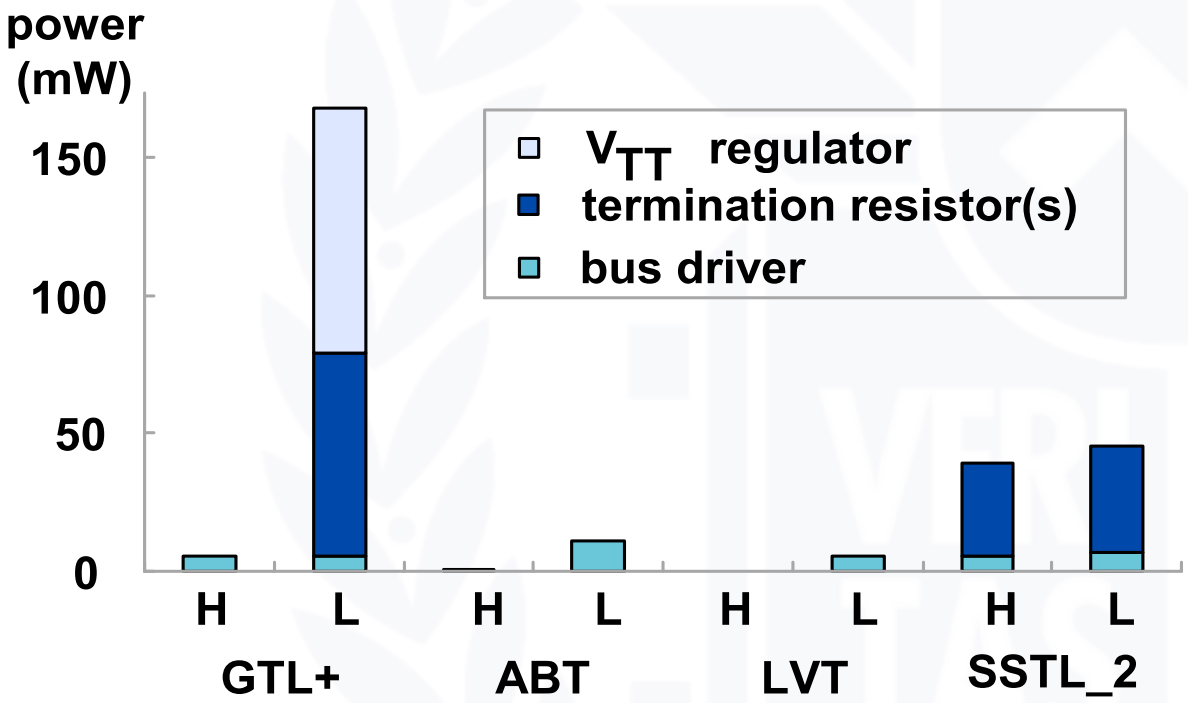
Termination

- Industrial standards that include termination resistors as default
  - SSTL_2
    - Memory controllers to DDR SDRAM arrays
    - 2.5V CMOS totem-pole terminated to 1.25V
    - CMOS technology
    - CMOS totem-pole



Termination

- Static power consumption

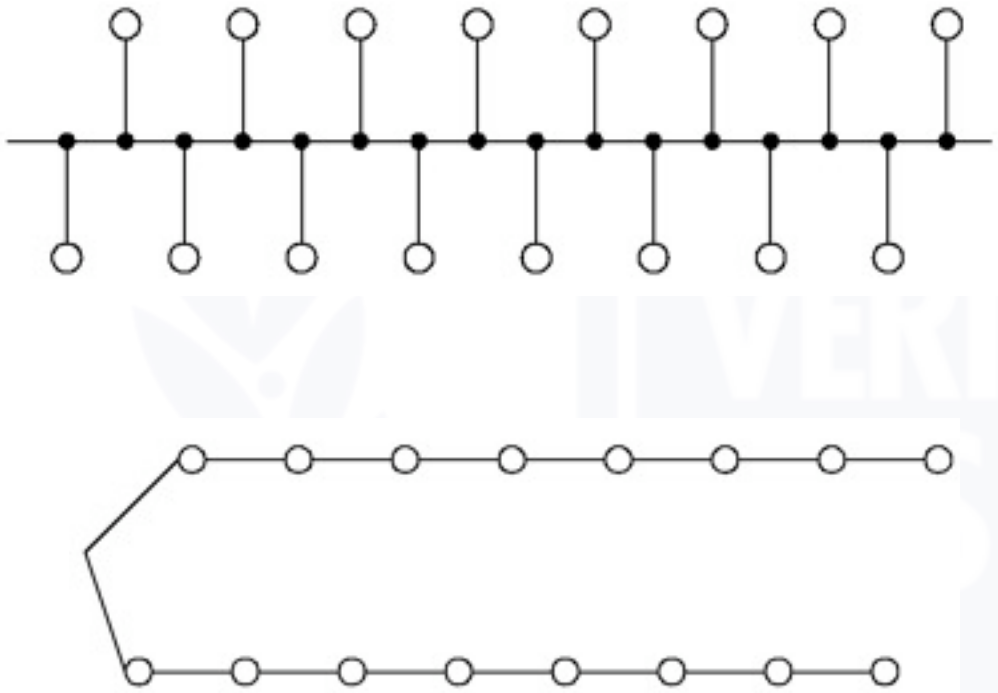


Termination

- Layout rules for transmission lines
  - Do not make discontinuity
    - Discontinuities are points where the impedance of the signal line changes abruptly
    - The formula of K_R is valid as well for the discontinuities
    - Avoid bend of tracks and vias
    - Smoothing the bends
    - Reduce excessive vias

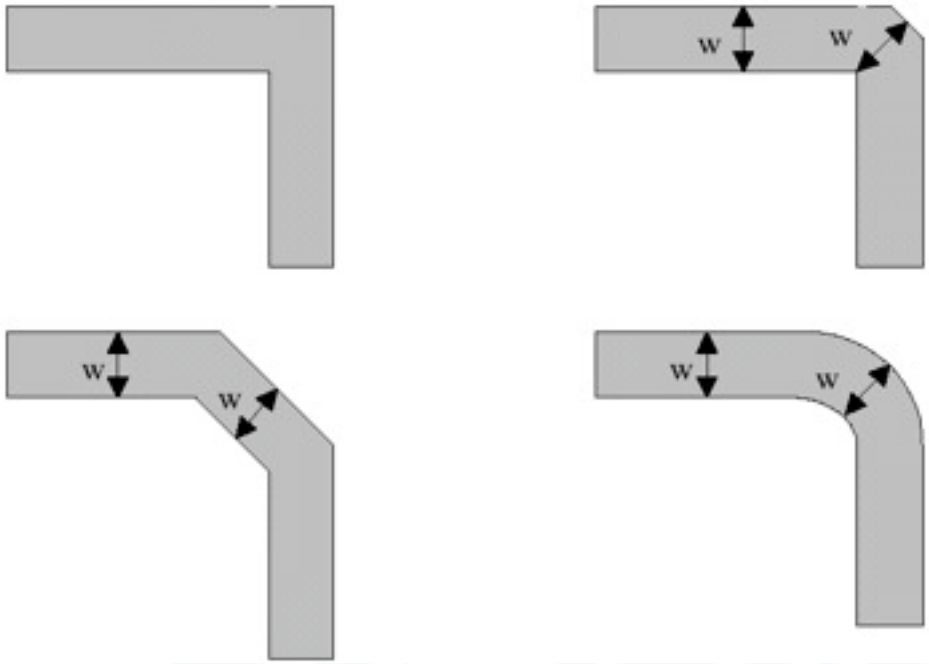
Termination

- Layout rules for transmission lines
  - Do not use stubs or Ts
    - Stub or Ts can be noise sources
    - Terminate individually long stubs
    - Do not make stubs



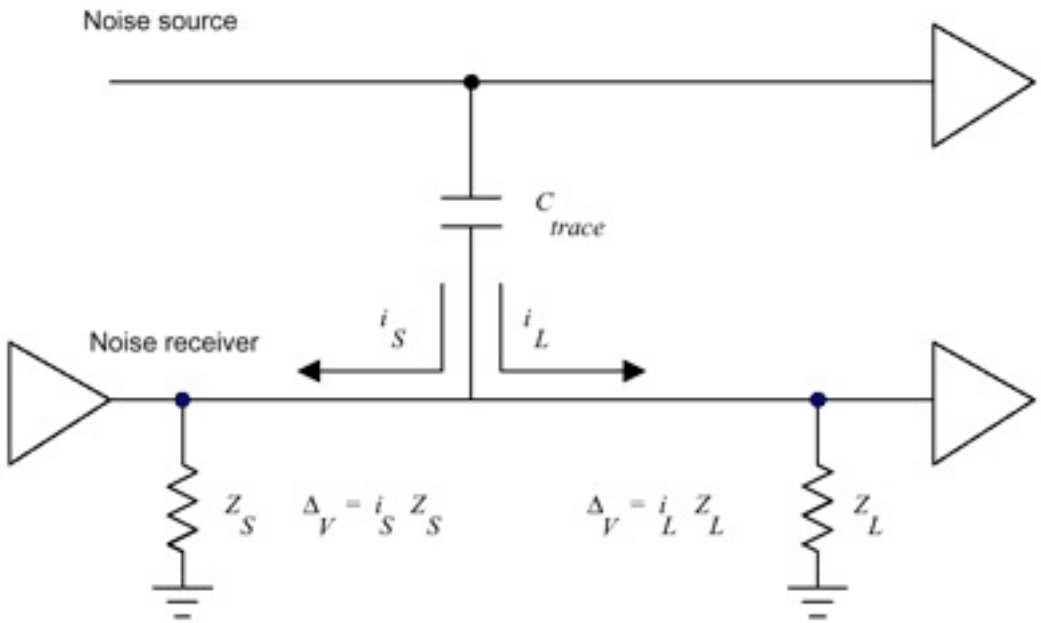
Termination

- Layout rules for transmission lines
  - Soothing the bends



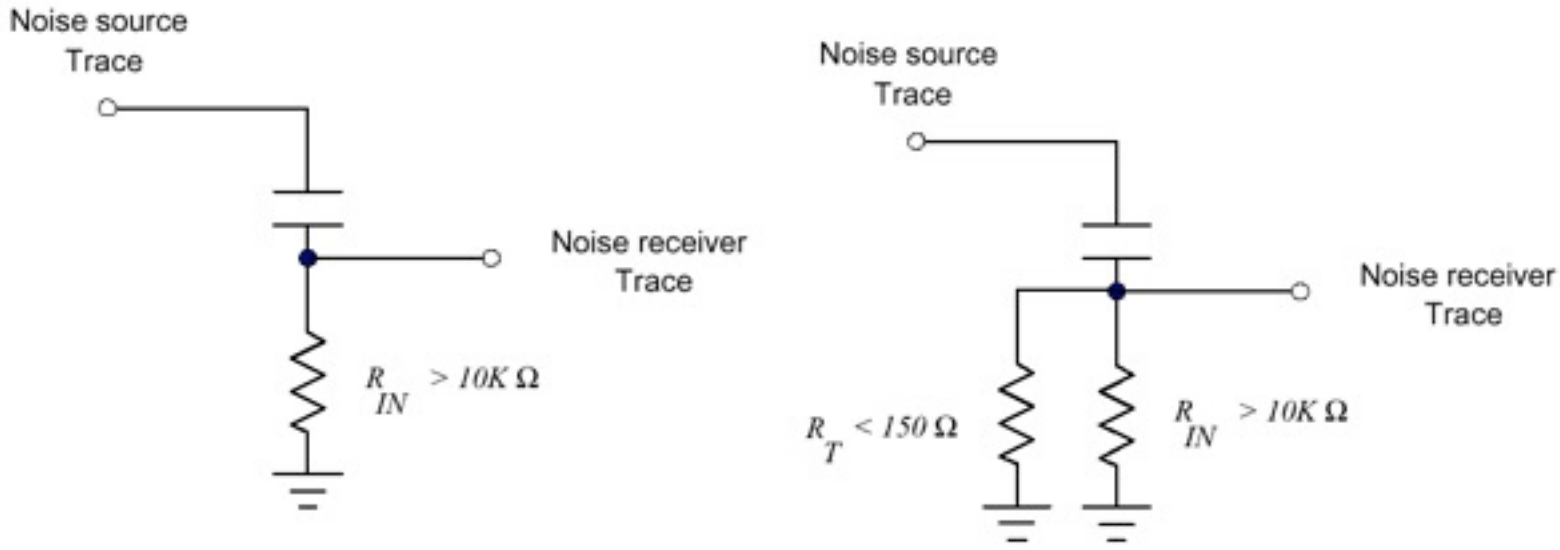
Crosstalk

- Capacitive crosstalk
  - Capacitive coupling induced by closely located lines
    - Current injection to a transmission line



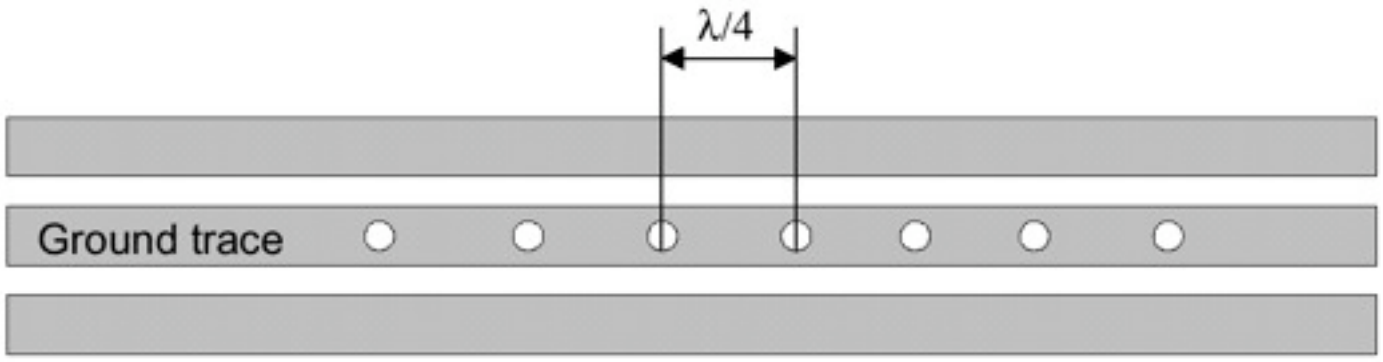
Crosstalk

- Capacitive crosstalk
  - Termination reduces the noise



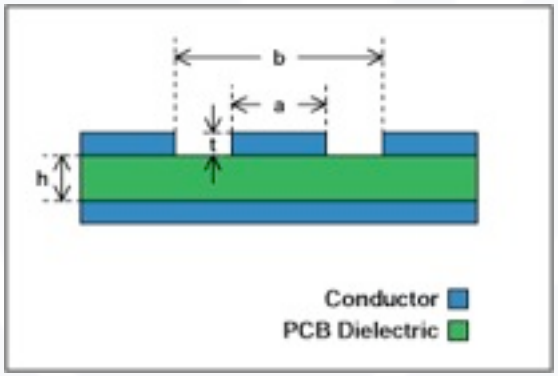
Crosstalk

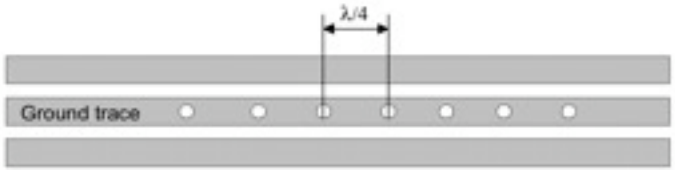
- Capacitive crosstalk
  - Separation helps to reduce the crosstalk
  - Isolation
    - Put a ground trace between the coupled traces should be a solid ground

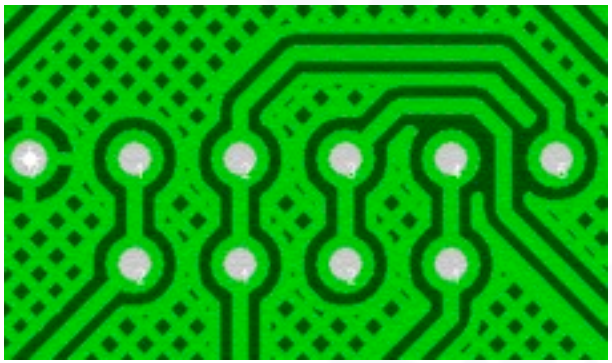


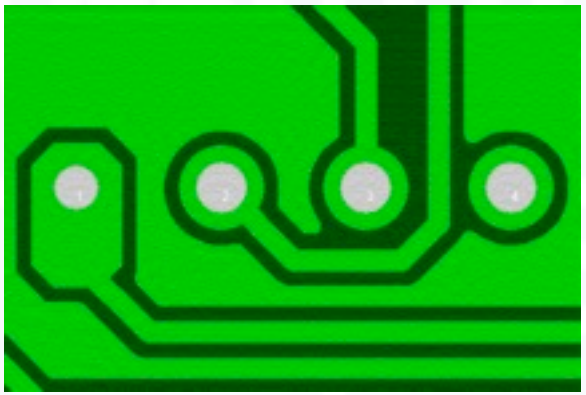
Crosstalk

- Coplanar waveguide
  - Often used in RF circuits
  - Often can be seen with copper pour
  - Hard to control line impedance for multi-layer PCBs
    - Does not recommend
    - To make isolation, dense ground vias should be applied









Crosstalk

- Capacitive crosstalk example
  - Wavelength

$$\lambda = \text{velocity} \times \text{period} = \frac{1}{t_{PD}} \frac{1}{\text{freq}}$$

  - Maximum frequency of interest

$$f_{MAX} = \frac{1}{1.25\,ns \times \pi} = 255\,MHz$$

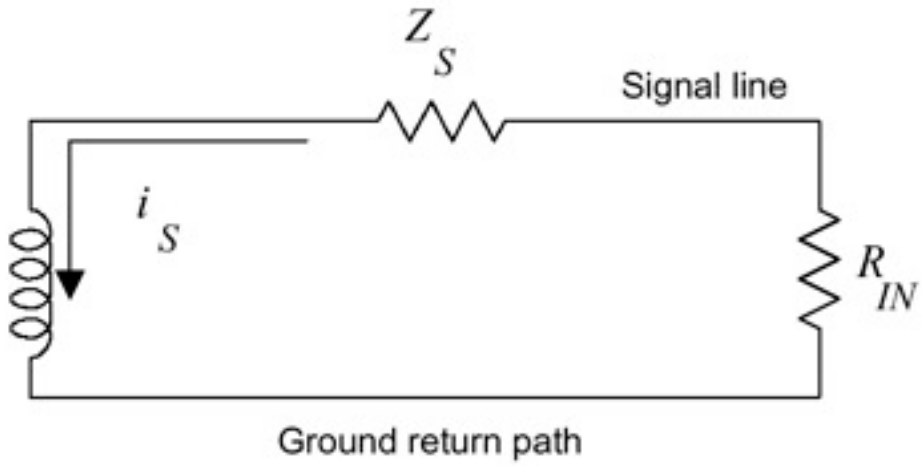
  - Distance

$$\lambda = \frac{1}{255\,MHz} \frac{1}{4.14\,ns/ft} \frac{12\,in}{ft} = 11.4\,in$$

$$\lambda/4 = \frac{11.4\,in}{4} = 2.8\,in$$

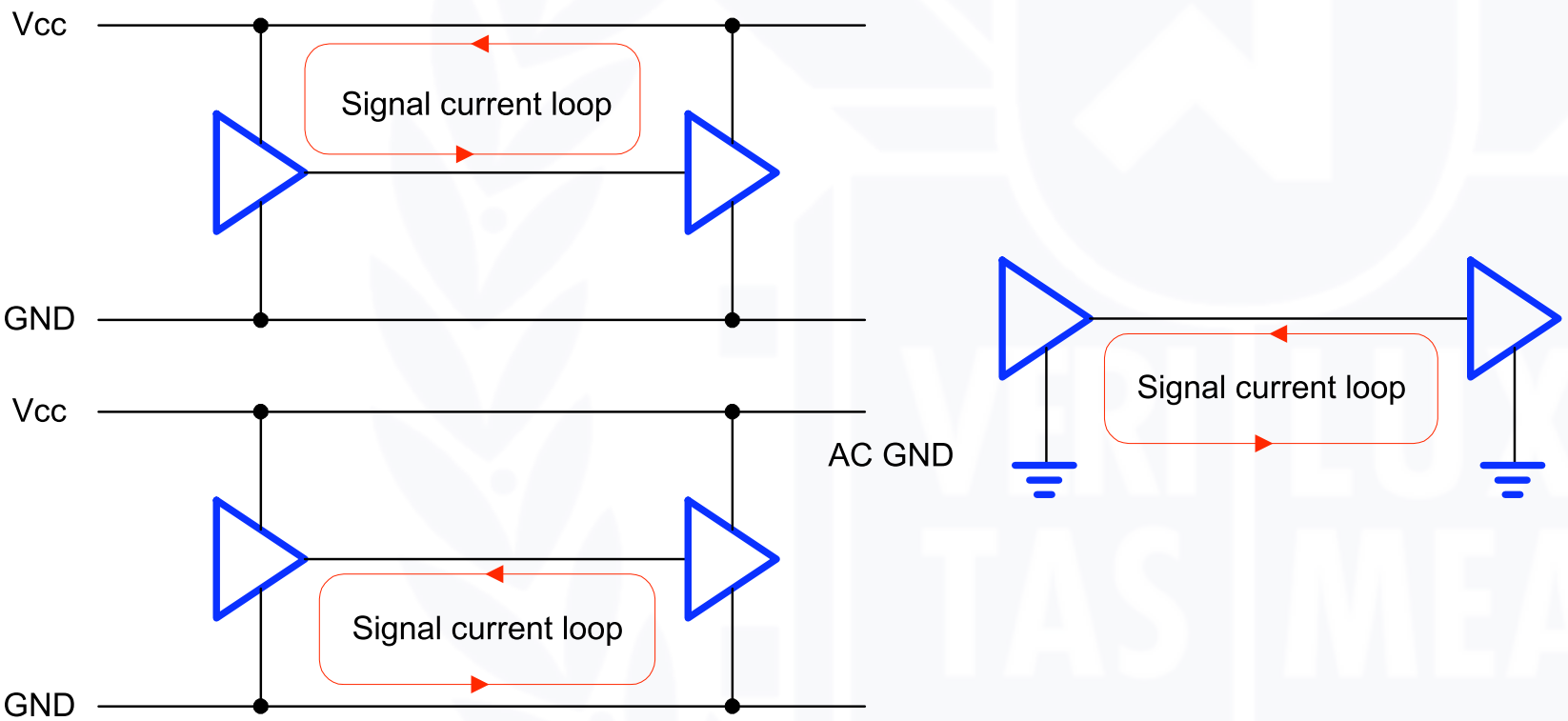
Crosstalk

- Inductive crosstalk
  - Coupling of signals between the primary and secondary coils
    - Natural loops by signals and their return paths
    - Artificial loops
    - Amount of the coupled signal depends on the size of the loops and their proximity
    - The size of the signal at the load, increases with the load impedance



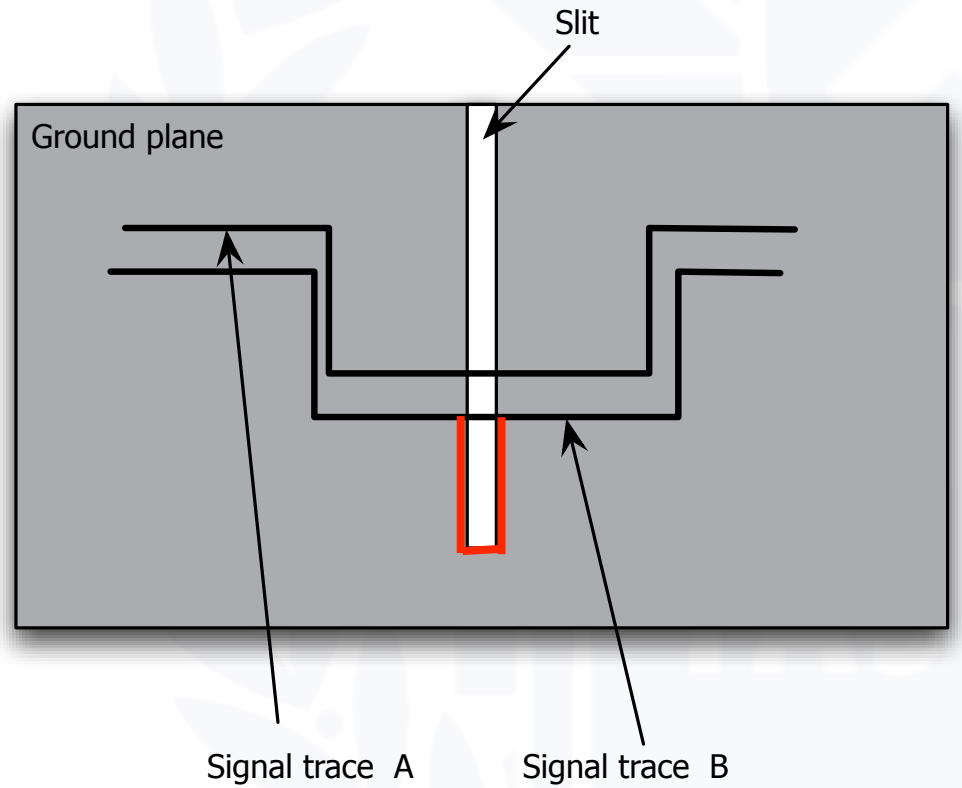
Crosstalk

- Inductive crosstalk
  - VCC and GND are signal return paths



Crosstalk

- Inductive crosstalk
  - Signal traces A and B will be coupled by the same return path



Crosstalk

- Solution
  - Artificial loop
    - Open it
  - Natural Loop
    - Keeping the load impedance low
  - R_T is usually 30 Ω to 150 Ω
    - This reduce the voltage at least two orders of magnitude

Crosstalk

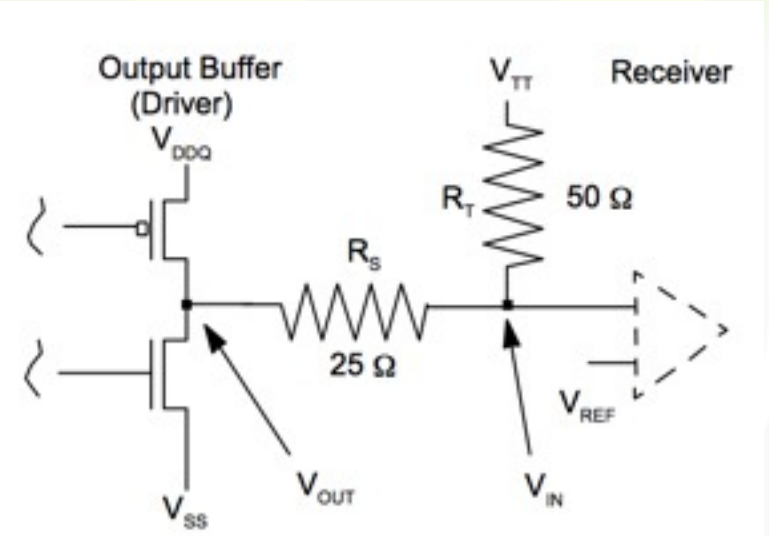
- Summary
  - Both capacitive and inductive crosstalk increase with load impedance
    - should be terminated
  - Keeping the signal separated reduces capacitive coupling
  - Capacitive coupling can be reduced by isolation with ground trace
  - Inductive crosstalk can be reduced by minimizing loop size
  - Inductive crosstalk is induced by shared common path

DDR2 Bus Specification

- SSTL (Stub series termination logic)
  - Attaining 200 MHz maximum frequency
  - V_{IH} and V_{IL} are V_{REF}+200 mV and V_{REF}–200 mV, respectively
    - This 400-mV input voltage swing allows much faster than the standard 1.2-V difference in LVTTL levels where V_{IH} and V_{IL} equal 2 V and 0.8 V, respectively

DDR2 Bus Specification

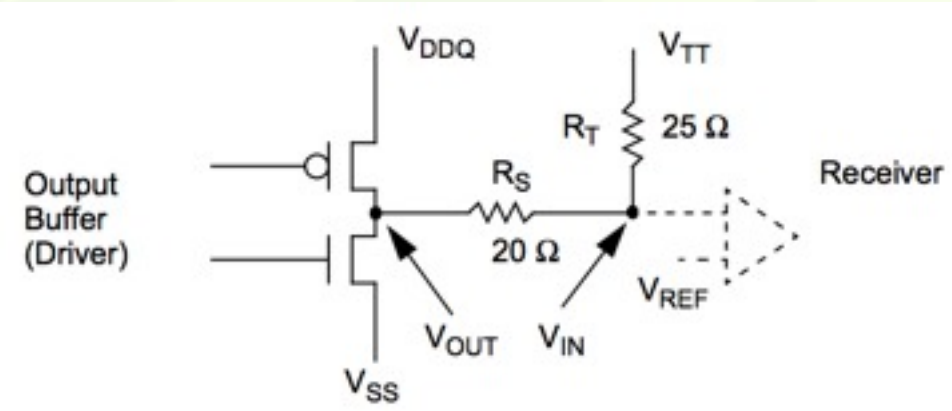
- SSTL
  - SSTL_2
    - DDR I memory
    - V_{DDQ} = 2.5 V, V_T = 0.5 x V_{DDQ}



Symbol	Parameter	Min.	Nom	Max.	Units	Notes
V_{DD}	Device supply voltage	V_{DDQ}		n/a	V	1
V_{DDQ}	Output supply voltage	2.3	2.5	2.7	V	1
$V_{REF(DC)}$	Input reference voltage	1.13	1.25	1.38	V	2, 3
V_{TT}	Termination voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	4

DDR2 Bus Specification

- SSTL
  - SSTL_18
    - DDR II memory
    - V_{DDQ} = 1.8 V, V_T = 0.5 x V_{DDQ}



Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
V_{DDQ}	Output supply voltage	1.7	1.8	1.9	V	
V_{REF}	Input reference voltage	833	900	969	mV	1, 2
V_{TT}	Termination voltage	V_{REF} - 40	V_{REF}	V_{REF} + 40	mV	3