Lecture 8. Special Topics: Design Trade-Offs in LC-Tuned Oscillators

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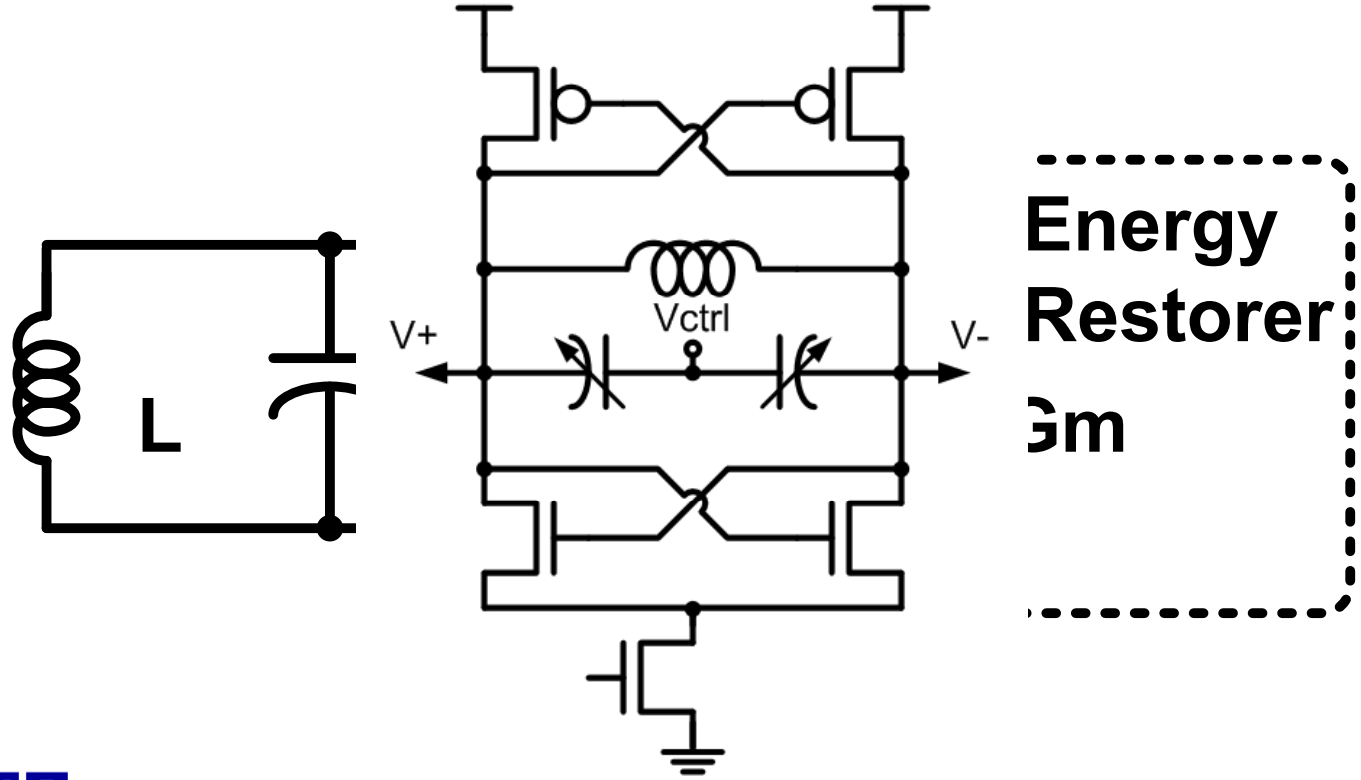
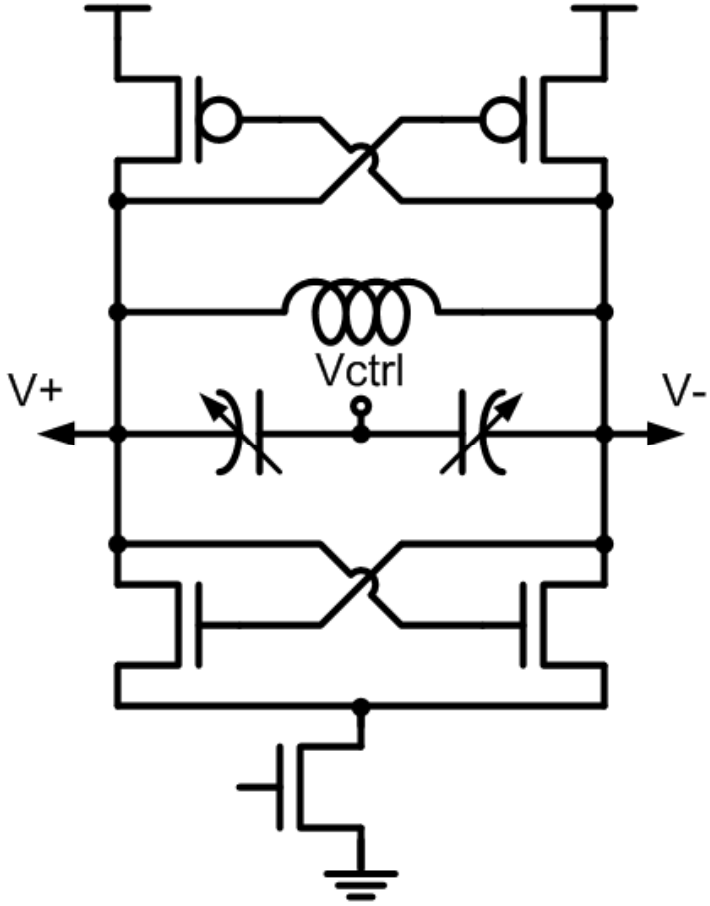
Tuned Oscillator Basic

- LC resonant tank resonates at ω_o = 1/sqrt(LC)
- Oscillation is sustained if –Gm = 1/R



Review: Performance Metrics for LC Osc.

- Performance Metrics
  - Phase noise/jitter
  - Frequency tuning range
  - Power dissipation
  - Supply/substrate noise sensitivity
  - Output swing
  - …



Phase Noise

- A clock signal *v(t)* can be expressed by its amplitude *A*, nominal frequency f_0 and its phase noise $\phi(t)$:

$$v(t) = A \cdot sin(2\pi f_0 t + \phi(t))$$

- Phase noise $S_\phi(f)$ is a power-spectral density (PSD) of the instantaneous phase $\phi(t)$:
  - Describes how close v(t) is to a perfectly periodic waveform
- In measurements, $S_\phi(f)$ is approximated by the PSD of the signal *v(t)*:

$$\mathcal{L}(\Delta f) := 4S_v(f_0 + f_m)/A^2$$

Lecture Outline

- Understanding the origins of phase noise/jitter
  - LTI phase noise theory (high-Q on-chip resonators)
  - LTV phase noise theory (1/f noise up-conversion)
  - NTV phase noise theory (voltage-limiting; AM-to-PM conversion)

- Optional topics regarding optimal LC oscillator designs
  - Wide tuning range
  - Multiphase clock generation
  - Optimization

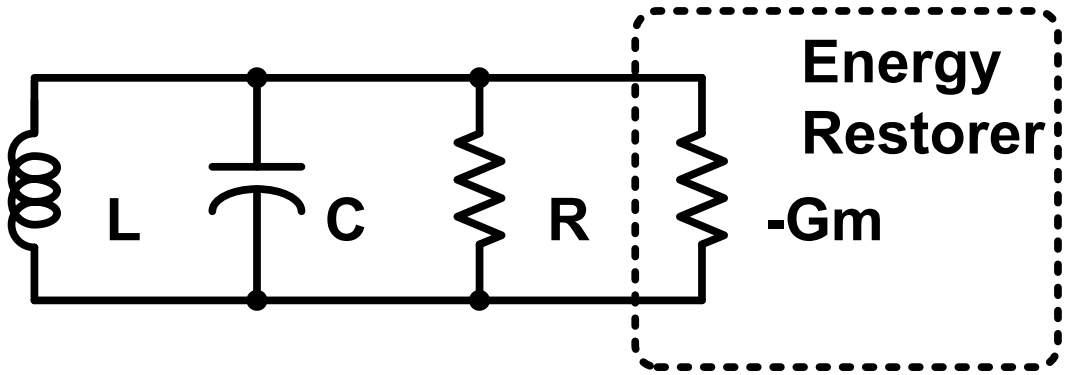
LTI Phase Noise Theory

LTI Phase Noise Theory (1)

- Noise sources in an LC oscillator: R and –Gm

$$\frac{i_{n,total}^2}{\Delta f} = \frac{i_{n,R}^2 + i_{n,Gm}^2}{\Delta f} = \frac{4kT}{R}(1+\gamma) \quad (\because -Gm = R)$$

  - Thermal noise where γ is the excess noise factor for the active devices
  - γ for a MOS device is 2/3 for long-channel, 1~4 for short-channel devices



LTI Phase Noise Theory (2)

- Impedance Z of the parallel RLC near ω_o:

$$Z(\omega_0 + \Delta\omega) = \frac{\omega_0 R}{2Q\Delta\omega}$$

- Phase noise at offset $\Delta\omega$:

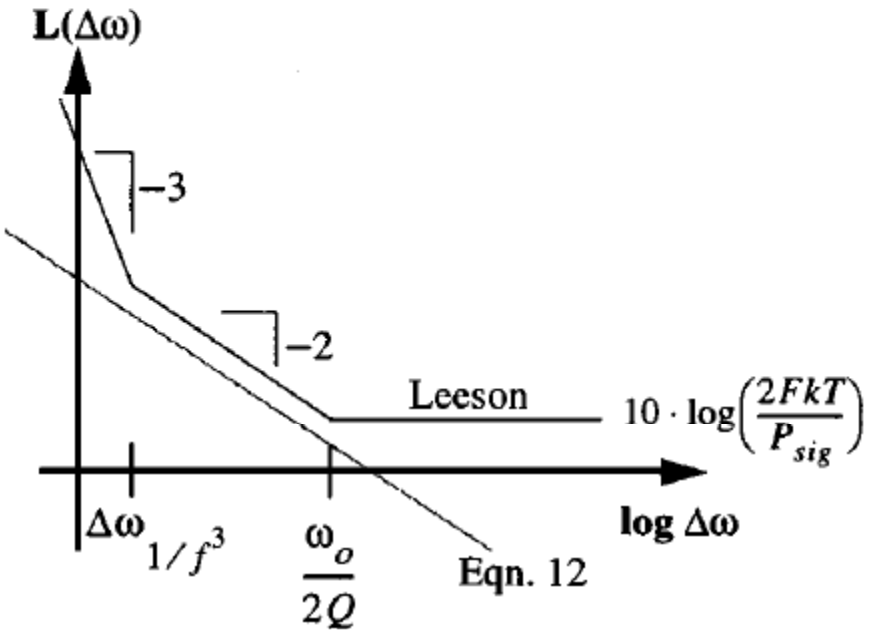
$$\mathcal{L}(\Delta\omega) = 10 \cdot log\left(\frac{i_n^2}{\Delta f} \cdot |Z(\omega_0 + \Delta\omega)|^2 \cdot \frac{1}{2P_{sig}}\right)$$

$$= 10 \cdot log\left(\frac{2kT(1+\gamma)}{P_{sig}} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)$$

- White noise translates to $1/f^2$ phase noise
- High Q and large P_{sig} desired for low phase noise

Leeson's Formula

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot log\left[\frac{2FkT}{P_{sig}}\left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right]$$



- In addition to thermal noise contribution ($1/f^2$), the formula also includes:
  - 1/f-noise contribution ($1/f^3$)
  - Buffer noise

Phase Noise vs. Power

- Shunt N identical LC VCOs in parallel
  - Power is doubled; phase noise is halved
  - R is halved; L is halved; C is doubled
  - Q, ω_o, and output swing remain unchanged
- But, scaling I_{bias} only doesn't always improve your VCO phase noise
  - In fact, it can get worse (voltage-limiting)

Figure-of-Merit (FOM)

- $\mathcal{L}\{\Delta\omega\}$ normalized to $\Delta\omega/\omega_o$ and P_{sig}

$$\mathrm{FOM} = -\mathcal{L}\{\Delta\omega\} - 10 \cdot log\left(\left(\frac{\Delta\omega}{\omega_0}\right)^2 \cdot \frac{P_{sig}}{kT}\right)$$

$$= 10 \cdot log\left(\frac{2Q^2}{1+\gamma}\right)$$

- Indicates the qualities of the tank (Q) and the energy restorer (γ)
- Typical ranges of FOM: 0 ~ 20dB
  - Q/sqrt(1+γ) of 0.7 ~ 7

Clock Jitter Definitions

- Suppose $\{t_n\}$ is a sequence of rising transition times from a clock with the nominal period of T (=$1/f_0$)
- Absolute jitter (a.k.a. aperture jitter):

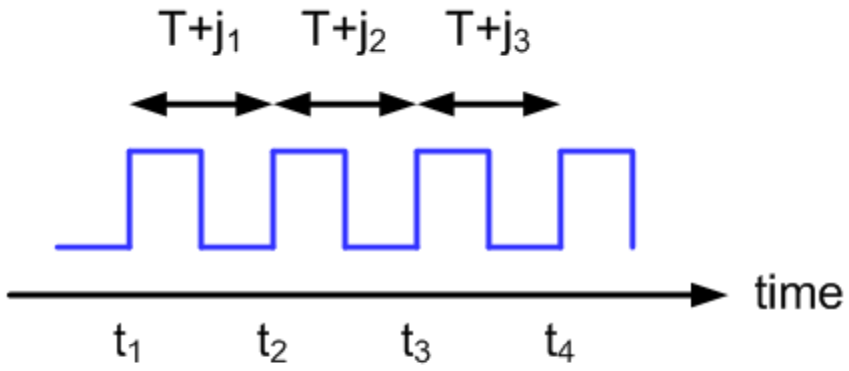
$$\{t_n - nT\}$$

Absolute jitter in radians: $\{\theta_n := 2\pi f_0 \cdot (t_n - nT)\}$

- Relation with phase noise:

$$\sigma_{abs}^2 = \frac{1}{2\pi f_0^2} \int_{-f_0/2}^{f_0/2} S_\theta(f) df$$

where $S_\theta(f) \approx S_\phi(f)$



D. Lee, "Analysis of Jitter in Phase-Locked Loops," TCASII, Nov. 2002

Clock Jitter Definitions (2)

- Period jitter (a.k.a. cycle-to-cycle jitter):

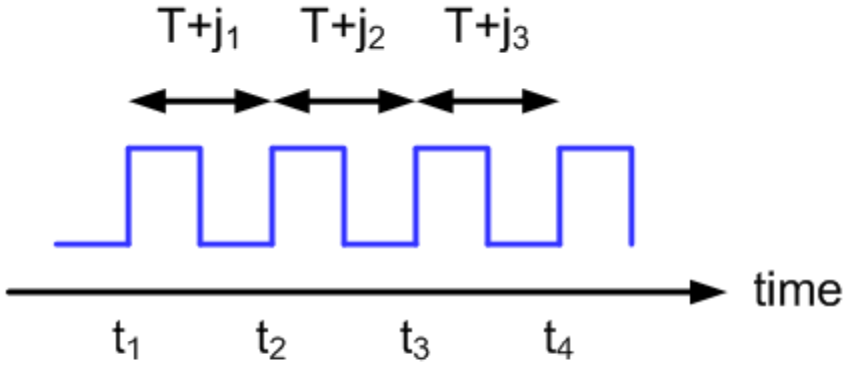
$$\{j_n := t_{n+1} - t_n - T\}$$

- Jitter over k periods (a.k.a. long-term jitter):

$$\{j_n(kT) := t_{n+k} - t_n - kT\}$$

- Relation with phase noise:

$$\sigma_J^2(kT) = \frac{1}{(\pi f_0)^2} \cdot \int_{-f_0/2}^{f_0/2} sin^2(\pi f k T) \cdot S_\theta(f) df$$



Long-Term Jitter of an Oscillator

- Another way of defining the long-term jitter is by the standard deviation of phase difference between time τ:

$$\sigma_\tau^2 = \sigma_J^2(\tau) = \mathbb{E}\left[\left(\phi(t+\tau) - \phi(t)\right)^2\right] / \omega_0^2$$

- Assuming thermal noise only (1/f^2 noise):

$$\sigma_\tau = \kappa \cdot \sqrt{\tau}$$

where

$$\kappa = \Delta\omega/\omega_0 \cdot 10^{\mathcal{L}\{\Delta\omega\}/20}$$

Typical CMOS LC Oscillator

- 2.5GHz, 1mW LC VCO with FOM=17dB

$$\kappa = \Delta\omega/\omega_0 \cdot 10^{\mathcal{L}\{\Delta\omega\}/20}$$
$$= \sqrt{FOM \cdot \frac{P_{sig}}{kT}}$$

- Cycle-to-cycle jitter (τ=T_{period}): 5.8fs,rms
- PLL with BW=1MHz (τ=1/2πBW): 115fs,rms

Clock Jitter Definitions (3)

- Adjacent period jitter (a.k.a. cycle-to-cycle jitter):

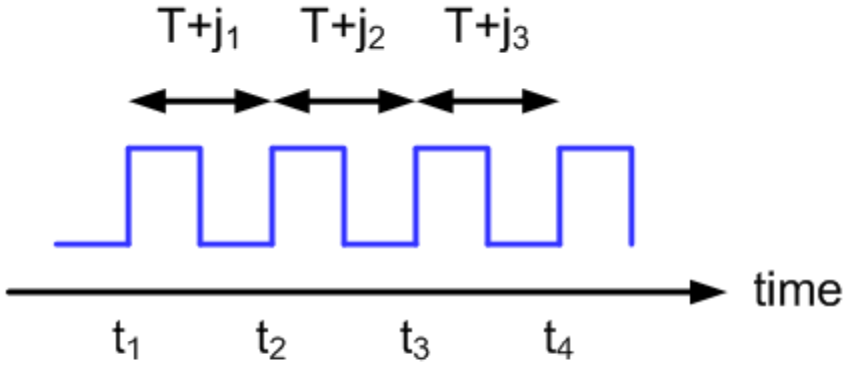
$$\{\Delta j_n := j_{n+1} - j_n = (t_{n+2} - t_{n+1}) - (t_{n+1} - t_n)\}$$

- Adjacent period jitter over k periods:

$$\{\Delta j_n(kT) := t_{n+2k} - 2t_{n+k} - t_n\}$$

- Relation with phase noise:

$$\sigma^2_{\Delta J}(kT) = \frac{4}{(\pi f_0)^2} \cdot \int_{-f_0/2}^{f_0/2} sin^4(\pi f k T) \cdot S_\theta(f) df$$



Relationship Among Clock Jitters

- Relation between period jitter and adjacent period jitter:

$$\sigma_{\Delta J}^2(kT) = 4\sigma_J^2(kT) - \sigma_J^2(2kT)$$

- And some known inequalities:

$$\sigma_J(kT) \leqslant 2 \cdot \sigma_A$$

$$\sigma_{\Delta J}(kT) \leqslant 4 \cdot \sigma_A$$

$$\sigma_{\Delta J}(kT) \leqslant 2 \cdot \sigma_J(kT)$$

$$\sigma_J(2kT) \leqslant 2 \cdot \sigma_J(kT)$$

D. Lee, “Analysis of Jitter in Phase-Locked Loops,” TCASII, Nov. 2002

Quality Factor

- General definition of the Q-factor:

$$Q = 2\pi \cdot \frac{energy\ stored}{energy\ loss\ in\ one\ oscillation\ cycle}$$

- For a parallel RLC tank:

$$\begin{aligned} Q &= 2\pi \cdot \frac{average\ magnetic\ energy + average\ electric\ energy}{energy\ loss\ in\ one\ oscillation\ cycle}\Big|_{\omega=\omega_0} \\ &= 2\pi \cdot \frac{peak\ magnetic\ energy}{energy\ loss\ in\ one\ oscillation\ cycle}\Big|_{\omega=\omega_0} = \frac{R}{\omega_0 L} \\ &= 2\pi \cdot \frac{peak\ electric\ energy}{energy\ loss\ in\ one\ oscillation\ cycle}\Big|_{\omega=\omega_0} = \omega_0 RC \\ &= \frac{R}{\sqrt{L/C}} \end{aligned}$$

Quality Factor (2)

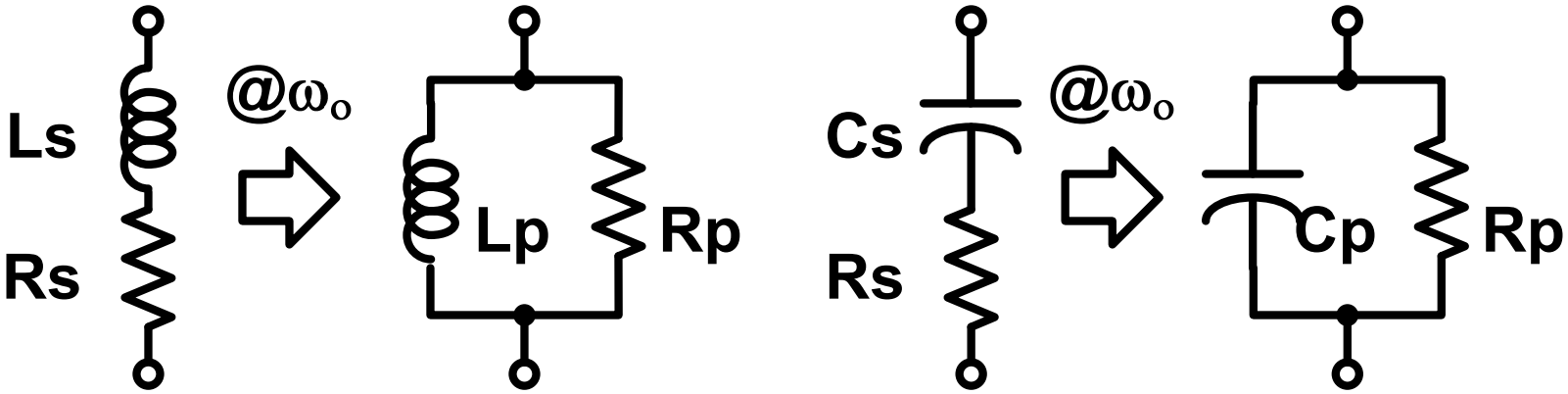
- Q of inductor: $Q_L = \omega_o L_S / R_S$

$$L_P = L_S \cdot (Q_L^2+1)/Q_L^2, \quad R_P = R_S \cdot (Q_L^2+1)$$

- Q of capacitor: $Q_C = 1/\omega_o R_S C_S$

$$C_P = C_S \cdot Q_C^2/(Q_C^2+1), \quad R_P = R_S \cdot (Q_C^2+1)$$

- Q of RLC: $Q_L \,||\, Q_C$



Start-Up Condition

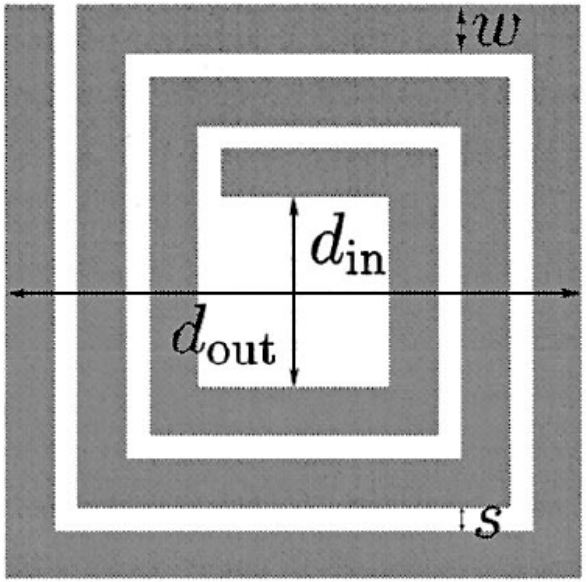
- Oscillation starts if $-Gm > 1/R_{tank}$
- Assuming that inductor loss (R_s) dominates:

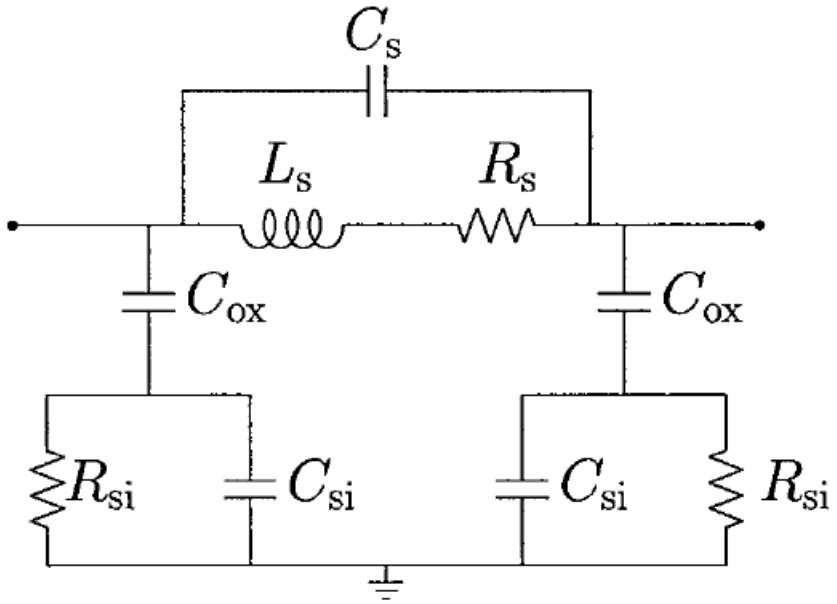
  $1/R_{tank} \approx 1/R_s \cdot 1/((\omega_o L_s/R_s)^2+1) \approx R_s/(\omega_o L_s)^2$

- Worst-case start-up is at the lowest ω_o!
  - Don't reset your VCO to the lowest Vctrl

Spiral Inductor

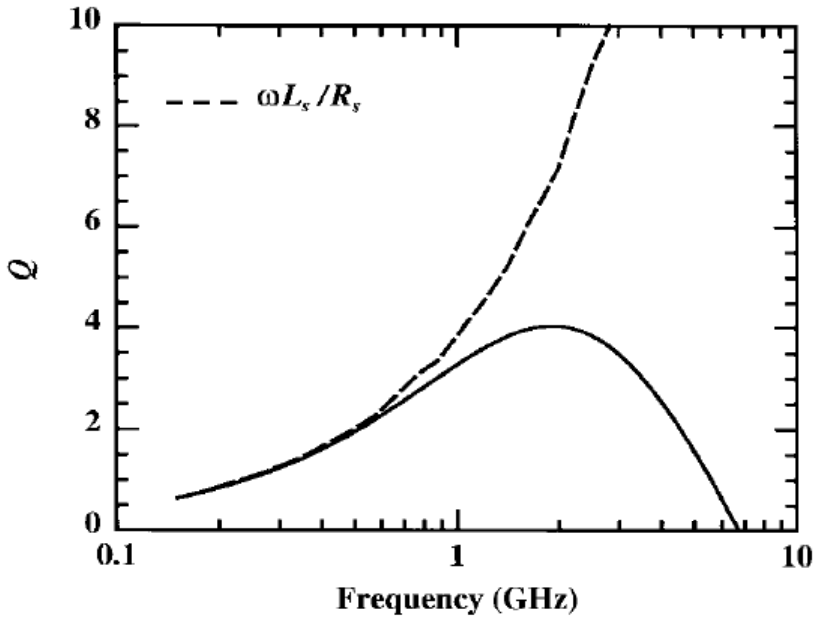
- Minimize R_s for highest Q (dc, skin-effect)
- Use top metal for low C_{ox} and high $f_{self\text{-}resonant}$
- PGS removes substrate uncertainties

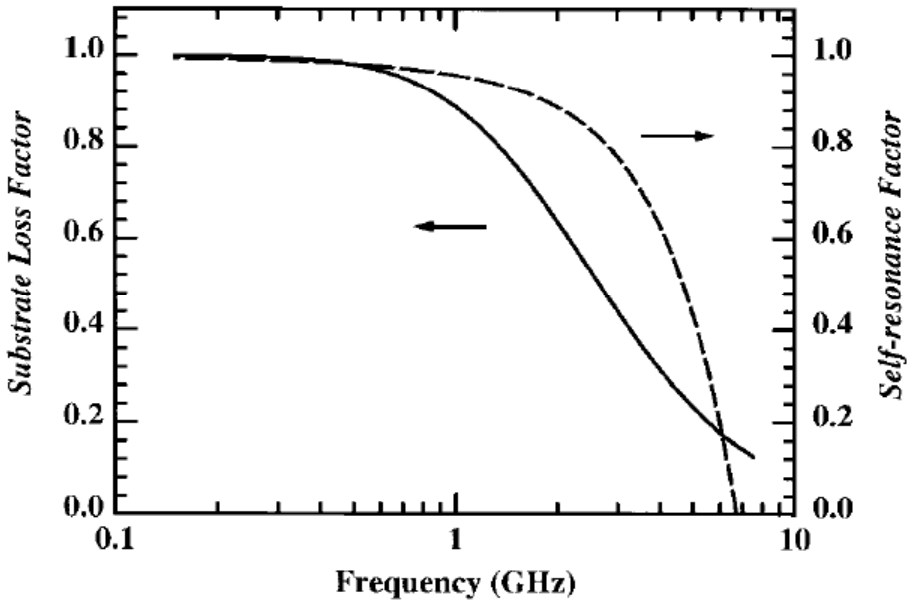




Spiral Inductor Q

- $Q = \omega_o L_s / R_s \cdot$ (substrate loss factor) $\cdot$ (self-resonance factor)

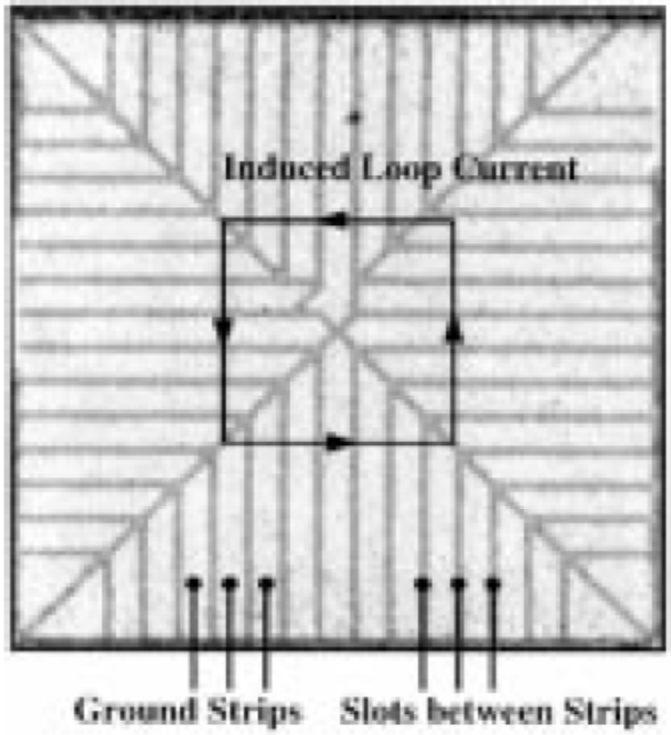




[Yue98]

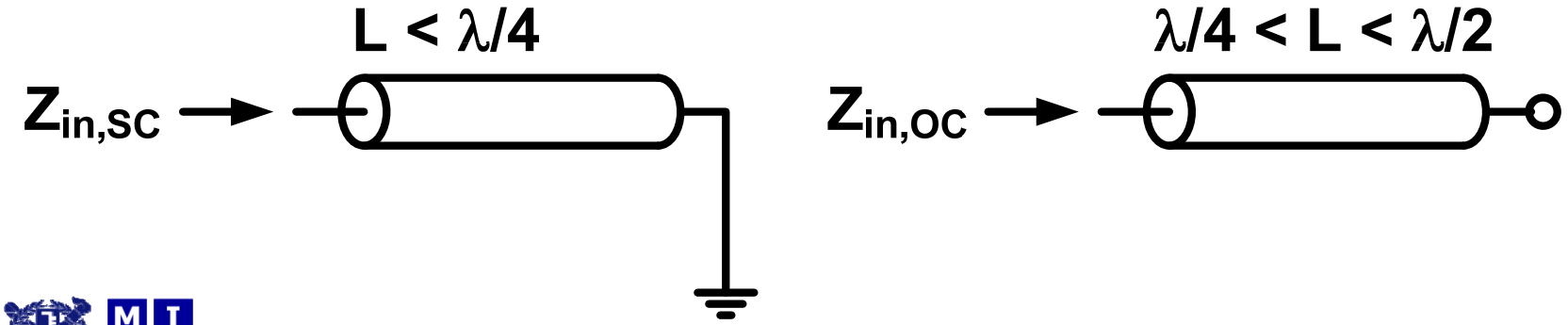
Patterned-Ground Shield (PGS)

- Shields the electric field of the inductor from the lossy substrate
  - Can't shield the magnetic field
- Patterned in order to prevent eddy current loss
  - High resistance along the induction loop
- Alleviates uncertainty in substrate modeling



Transmission Lines

- Distributed element with $\gamma = \alpha + j\beta$
- Short-circuited T/L: $Z_{in,SC} \approx jZ_o \cdot \tan(\beta L)$
  - Inductive for $L < \lambda/4$
- Open-circuited T/L: $Z_{in,OC} \approx -jZ_o \cdot \cot(\beta L)$
  - Inductive for $\lambda/4 < L < \lambda/2$
- $Q = \beta/2\alpha$ where $\alpha = R_S/Z_o$

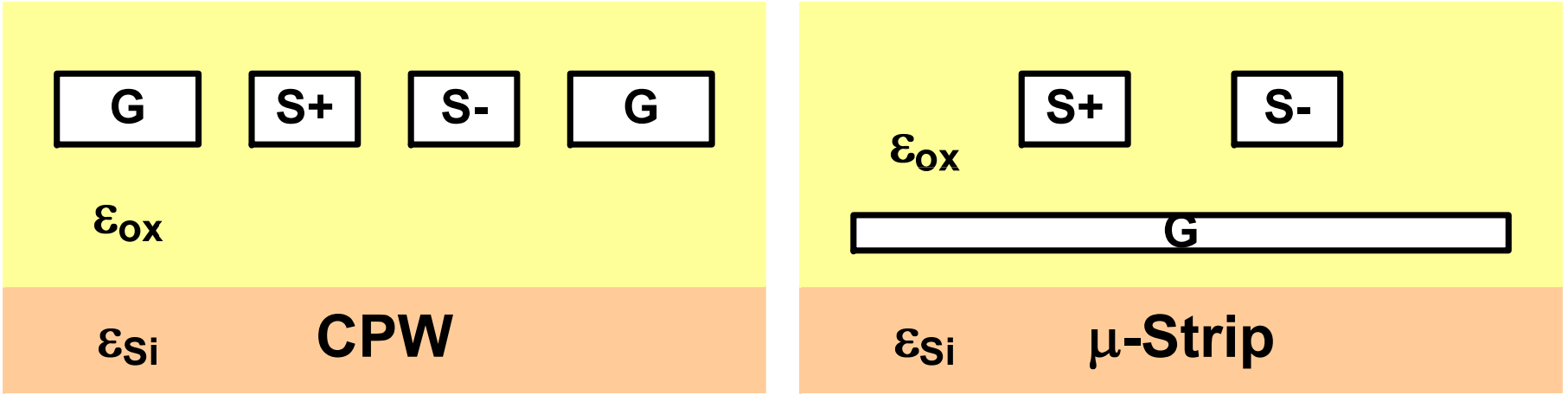


Spiral L vs. Transmission Line

- Spiral inductors:
  - High L per area
  - Open-field structure
- Transmission lines:
  - Closed-field structure; less coupling, higher Q
  - Higher accuracy in L
  - Lengthy at low frequencies

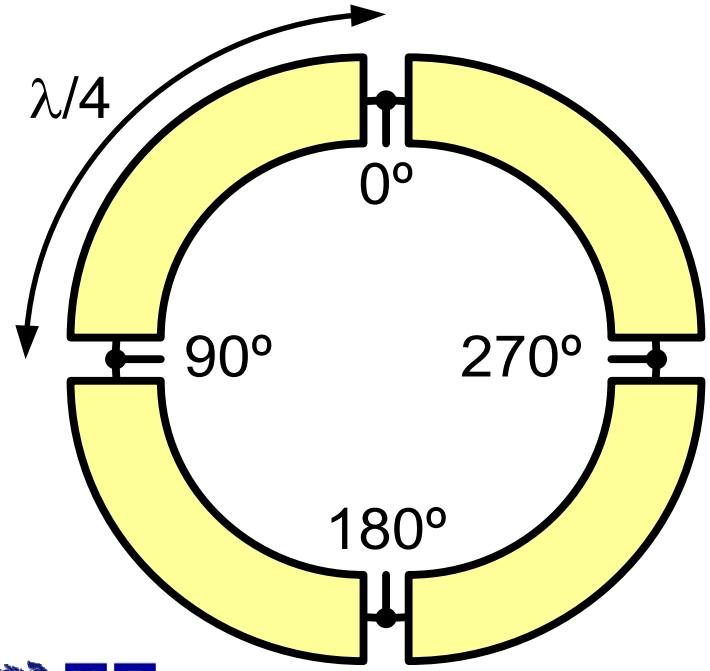
CPW vs. Microstrip

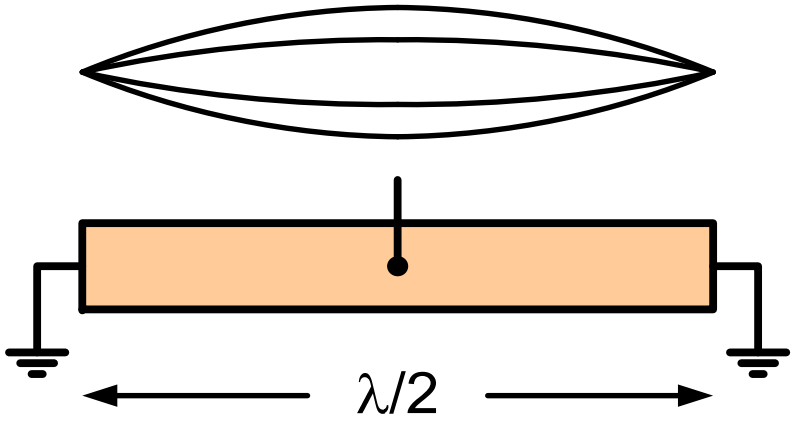
- CPW: Higher $Z_0 \Rightarrow$ higher Q and large L
  - Dimensions are set by lithography not by oxide thickness; less process sensitive
- Microstrip: inherent shield to the substrate
  - Insensitive to substrate parameters



Traveling vs. Standing Wave

- Both are equivalent to $\lambda/4$ short-circuited T/L
- [Wood01], [O'Mahony03], [Ham04]



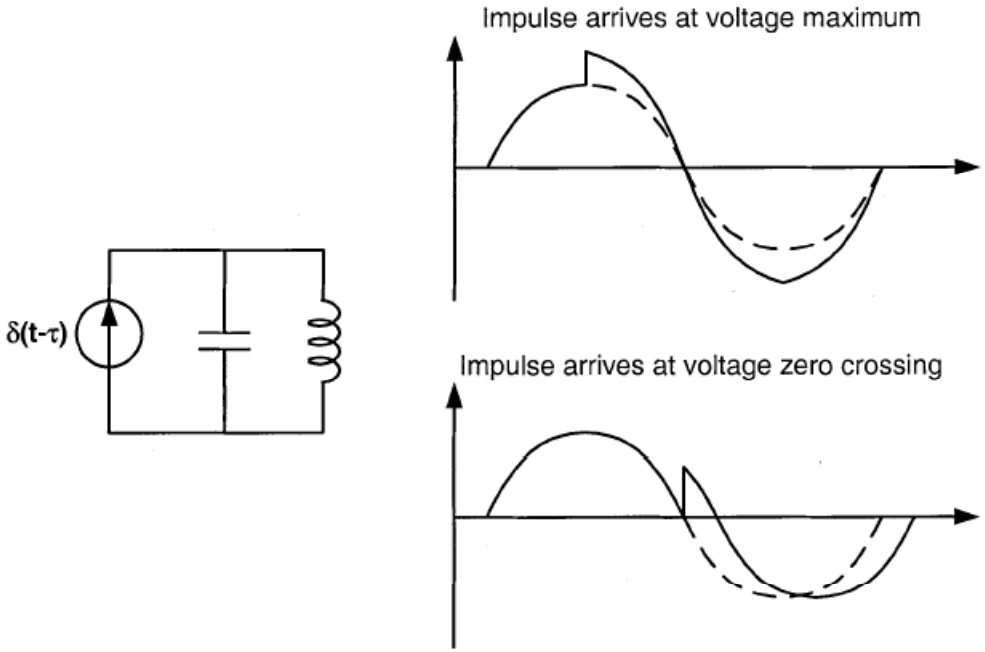


LTV Phase Noise Theory

LTV Phase Noise Theory

- VCO response depends on when noise hits
- Hajimiri ISF: linear, but time-varying response

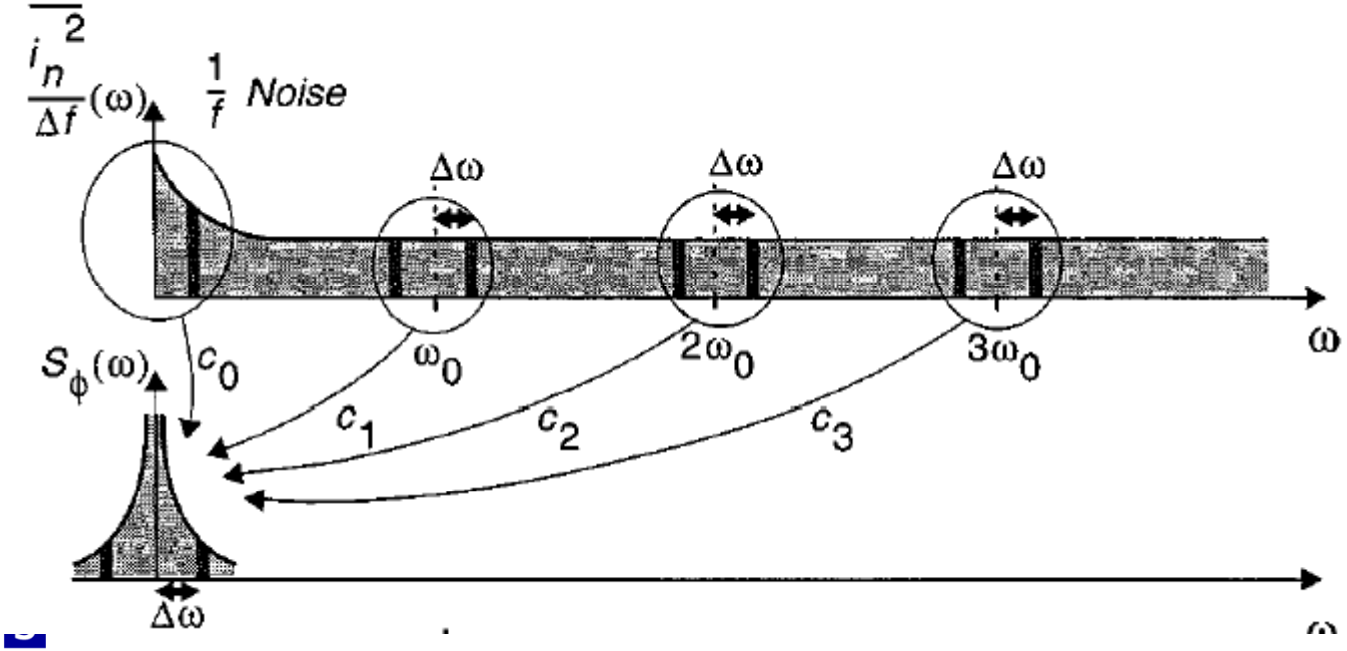
$$h_\phi(t,\tau) = \Gamma(\omega_o\tau)/q_{max} \cdot u(t-\tau)$$



Periodic ISF: Noise Folding

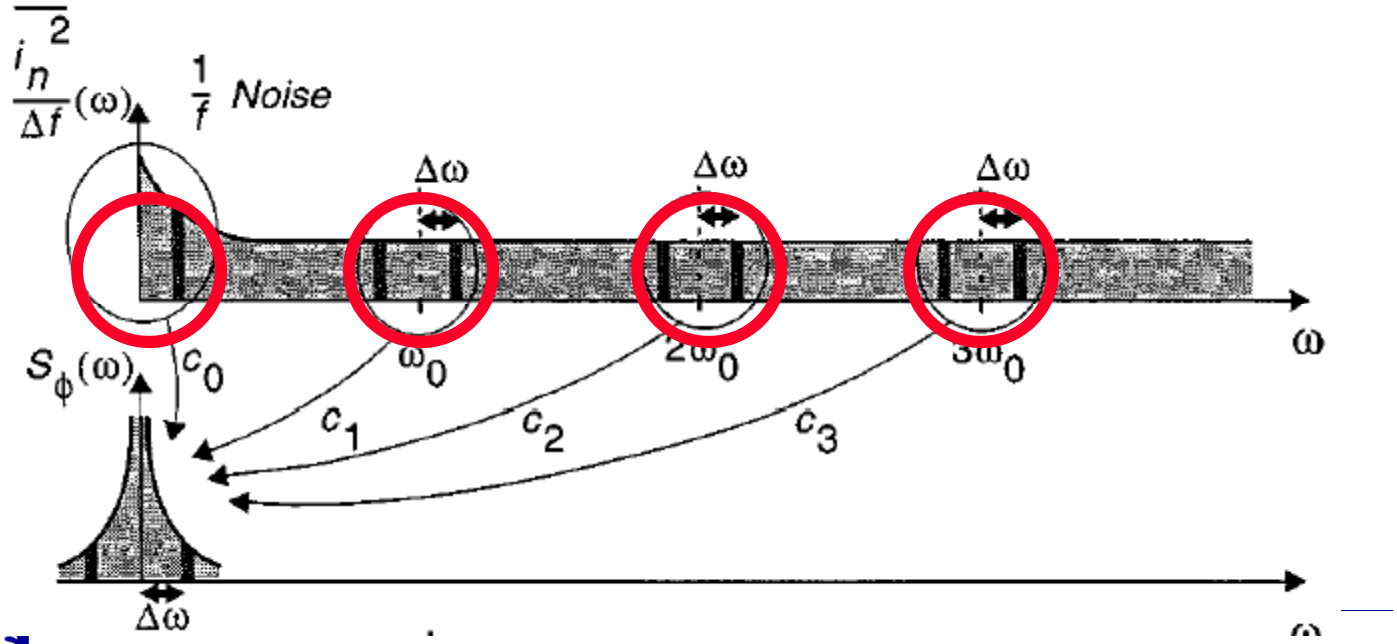
- $\phi(t) = \int h_\phi(t,\tau) \cdot i(\tau)\, d\tau = \int \Gamma(\omega_o \tau)/q_{max} \cdot i(\tau)\, d\tau$ – (*)
- $\Gamma(\cdot)$ is periodic; expanded to Fourier series:

  $\Gamma(\omega_o \tau) = c_0/2 + \sum c_n \cdot \cos(n\omega_o \tau)$
- Noise at $n \cdot \omega_o + \Delta\omega$ folds down to $\Delta\omega$



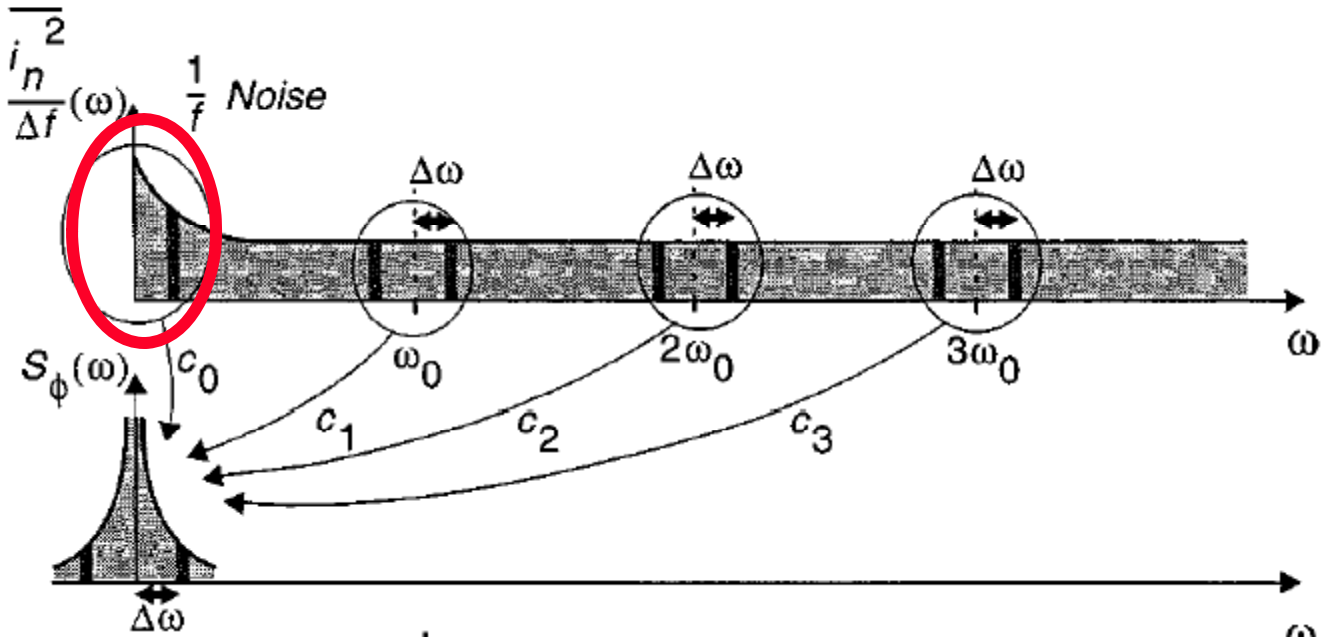
Thermal Noise Contribution

- Sum of noise power ≈ $\sum c_i^2 = 2 \cdot \Gamma_{rms}^2$
- $\mathcal{L}(\Delta\omega) = 10 \cdot \log(i_n^2/\Delta f \cdot \Gamma_{rms}^2 / (2q_{max}^2 \Delta\omega^2))$
- Minimize Γ_{rms} for low $1/f^2$ phase noise



Flicker Noise Contribution

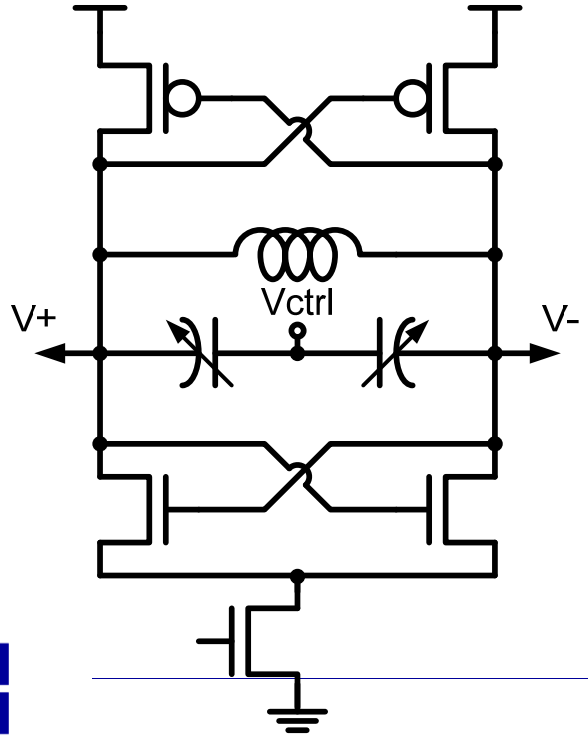
- Flicker noise: $i_{n,1/f}^2 = i_n^2 \cdot \omega_{1/f}/\Delta\omega$
- Only c_0 term counts: $c_0 = \Gamma_{dc}$
- $\mathcal{L}(\Delta\omega) = 10 \cdot \log(i_n^2/\Delta f \cdot \omega_{1/f} \cdot \Gamma_{dc}^2 / (8 q_{max}^2 \Delta\omega^3))$
- Minimize Γ_{dc} for low $1/f^3$ phase noise

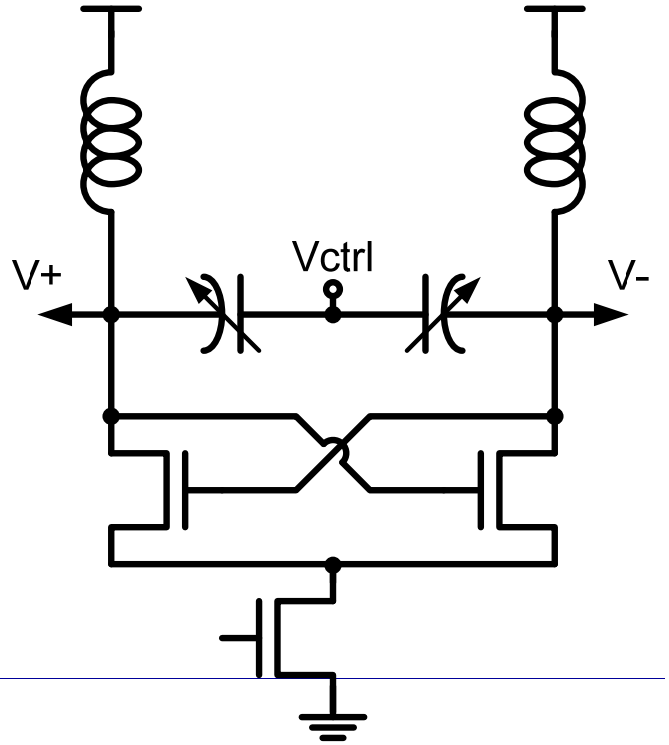


CMOS vs. NMOS/PMOS-only

- Better $1/f^3$: symmetric ISF lowers Γ_{dc} [Hajimiri99]
- Better $1/f^2$: twice G_m and V_{swing} for same I_{bias}

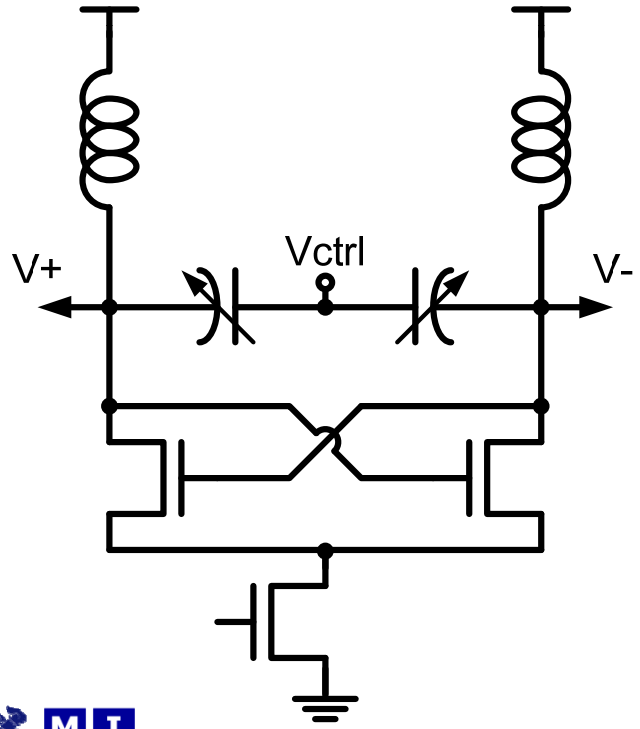
  $\Rightarrow$ 6-dB less phase noise [Andreani06]

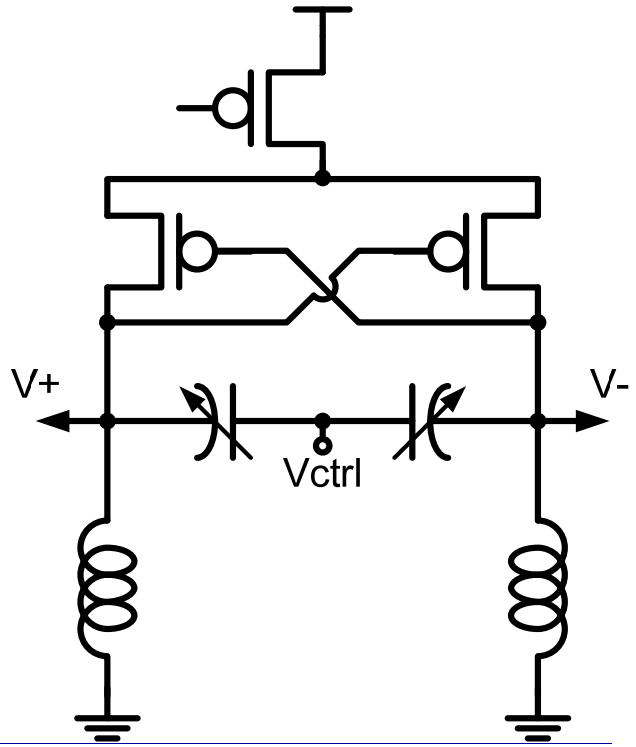




NMOS vs. PMOS

- [Jerng05]: PMOS has less thermal noise than NMOS, because it's less velocity-saturated
- PMOS also has lower flicker noise



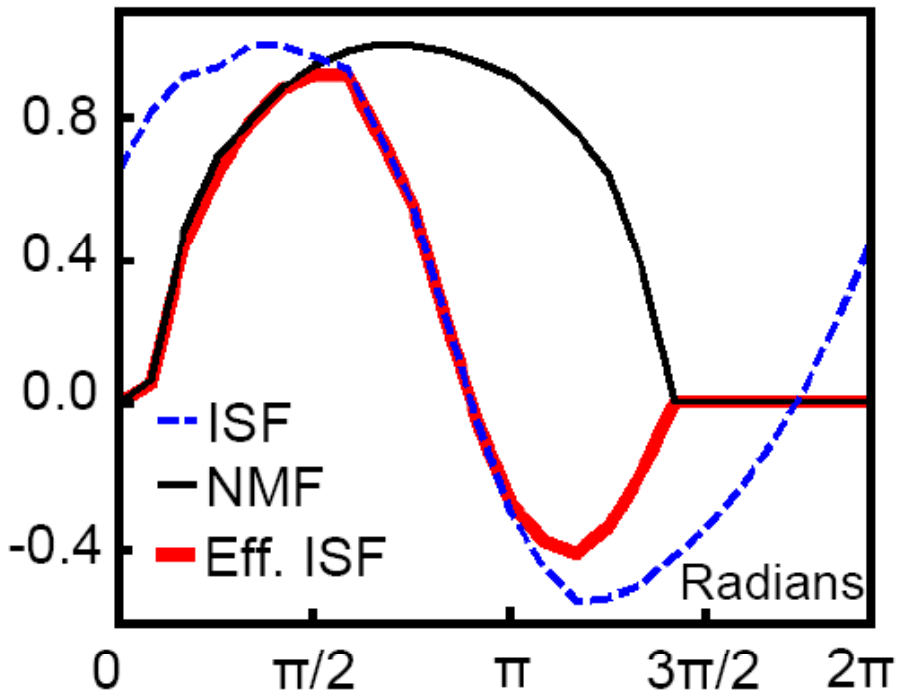


NMF: Cyclostationary Noise

- Noise profile changes with the circuit state
  - Changes periodically; cyclostationary noise
- Use $\Gamma_{eff} = \Gamma \cdot NMF$
- Minimize

  $\Gamma_{eff,rms}$ and

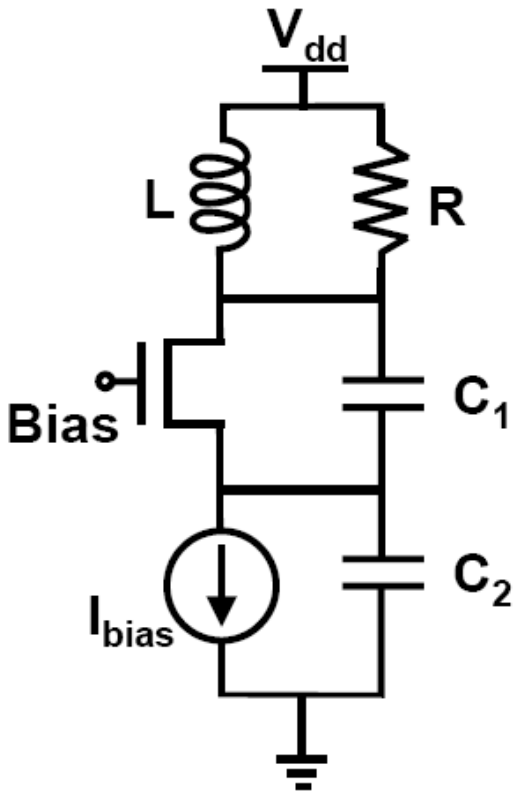
  $\Gamma_{eff,dc}$

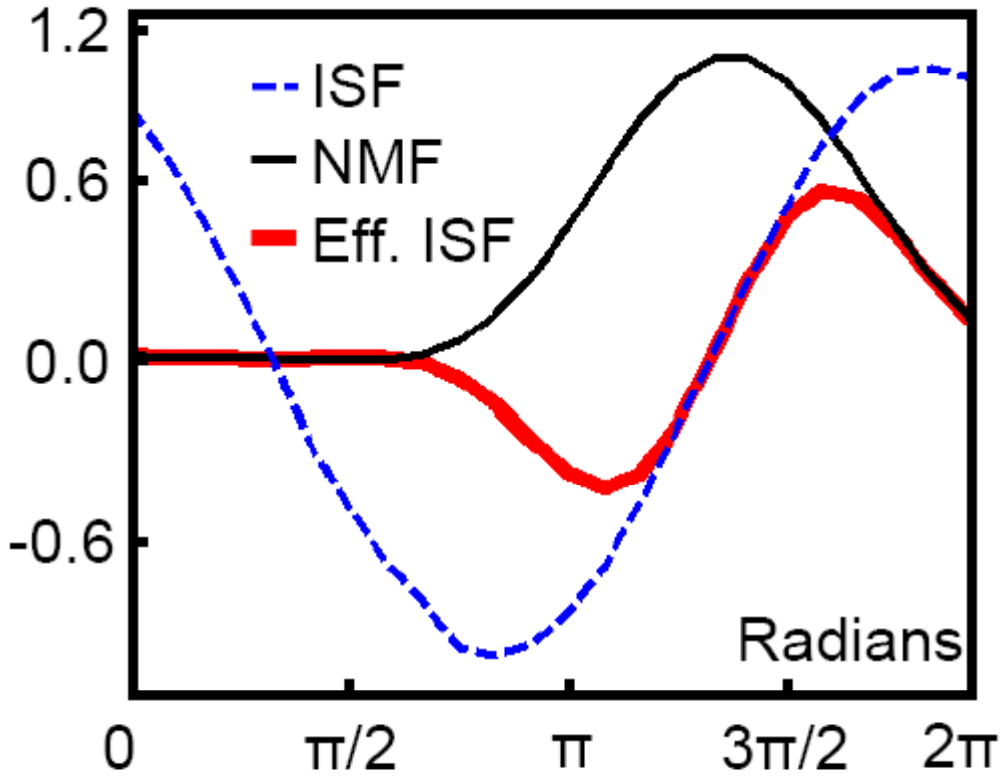


<CMOS LC>

Colpitts Oscillator

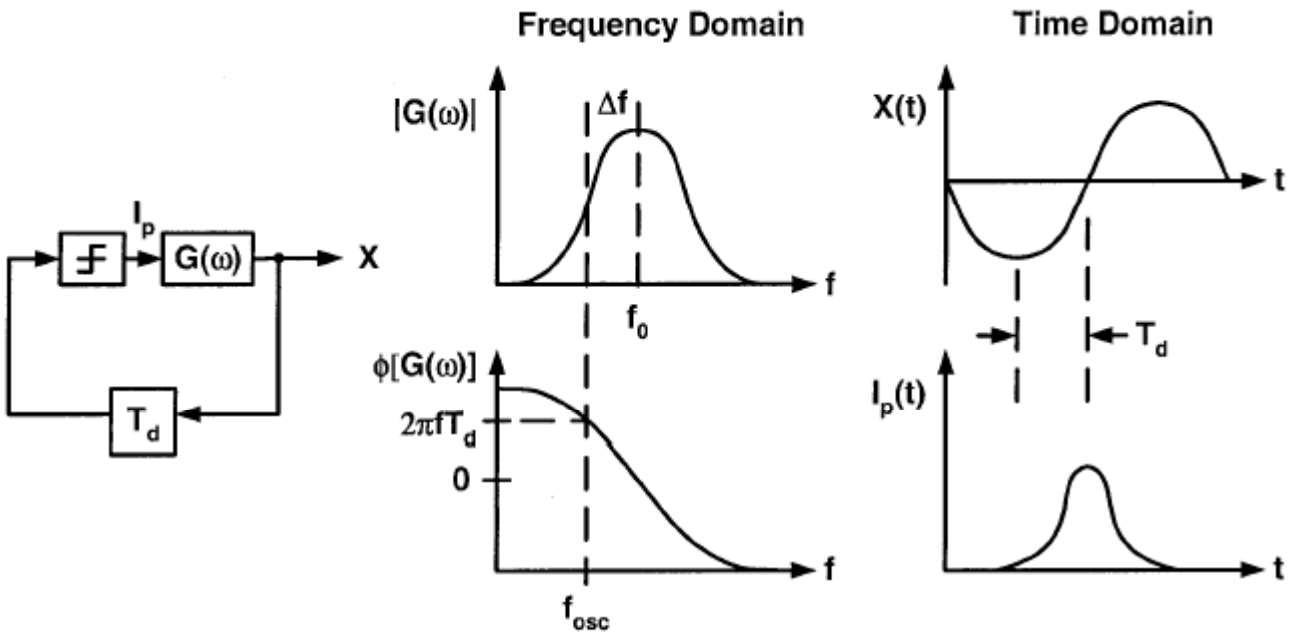
- Colpitts adds noise when osc is least sensitive
- But Colpitts generates more noise [Andreani05]





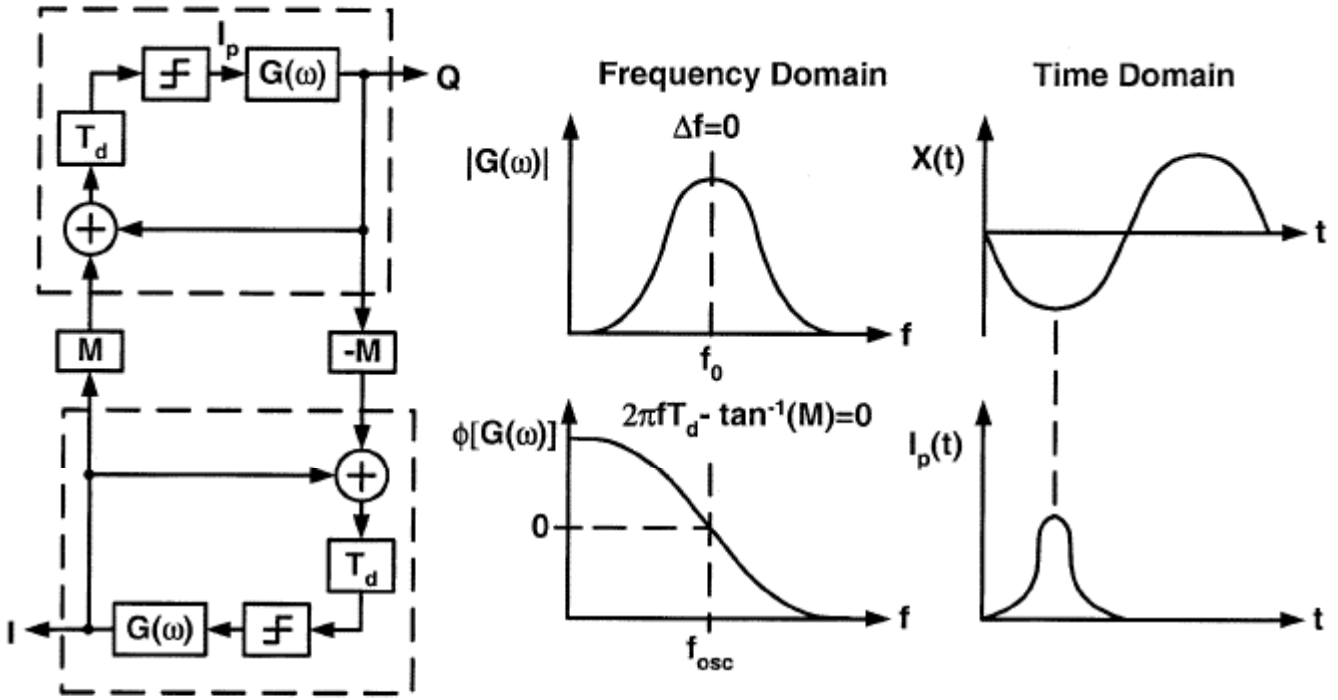
Loop Delay

- Loop delay adds to phase shift causing Δf
- Effective Q and ISF degrade [Shaeffer03]



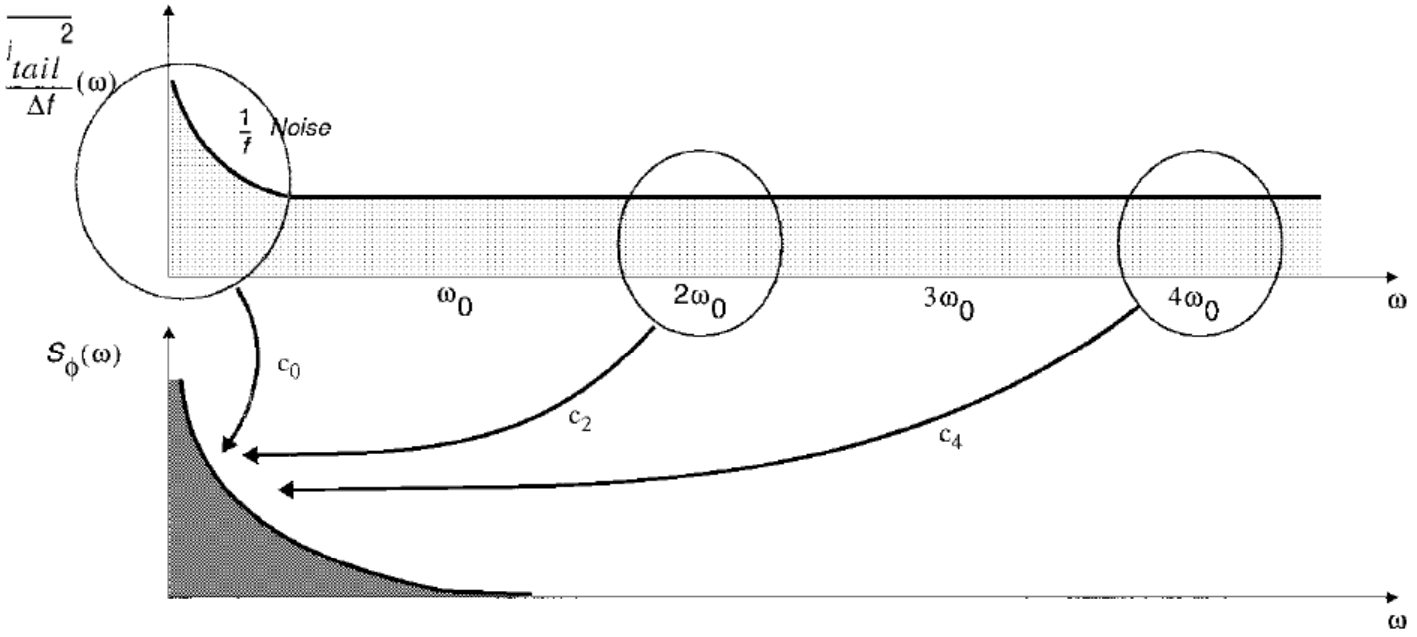
Delay Compensation via Coupling

- VCOs coupled in quadrature pull each other
- Pulling cancels the delay



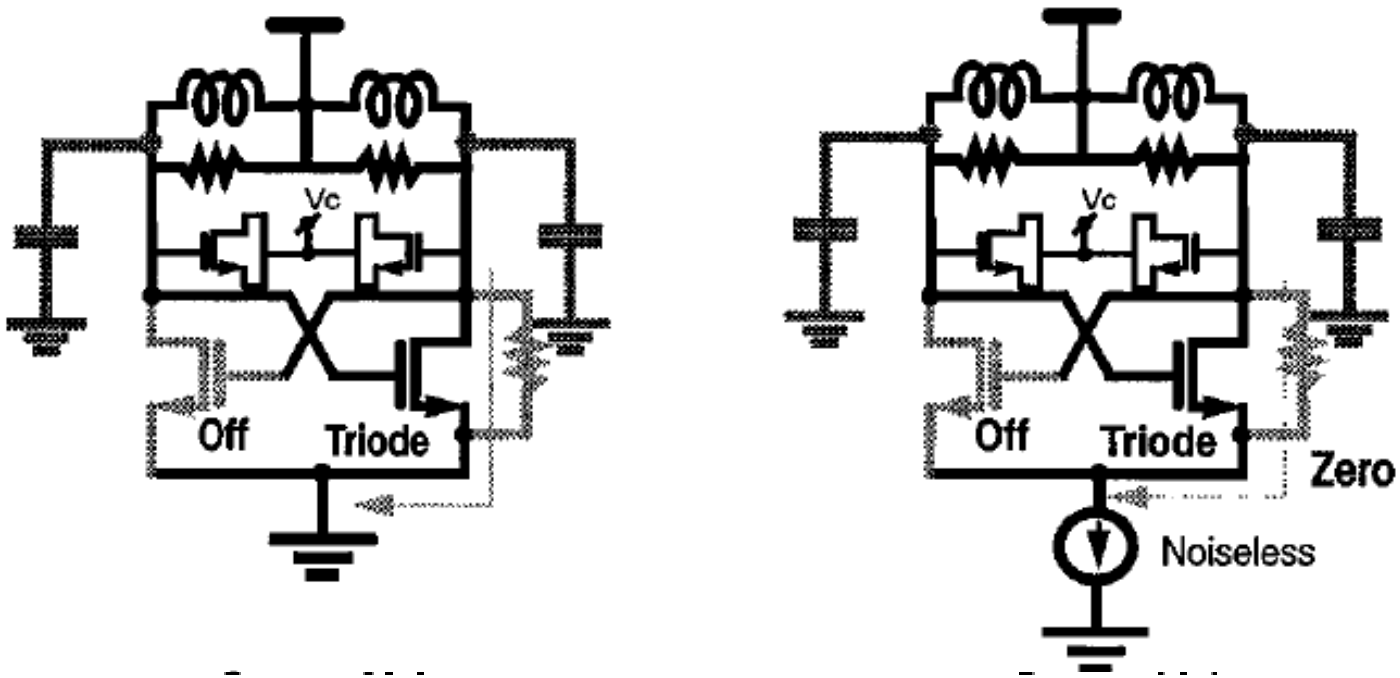
Tail Current 1/f Noise Up-Conversion

- Tail node fluctuates at $2\omega_o$; ISF periodic with $2\omega_o$
- DC-noise converts into AM only
- $2\omega_o$-noise converts into AM+PM [Hegazi01]



Tail Current Source

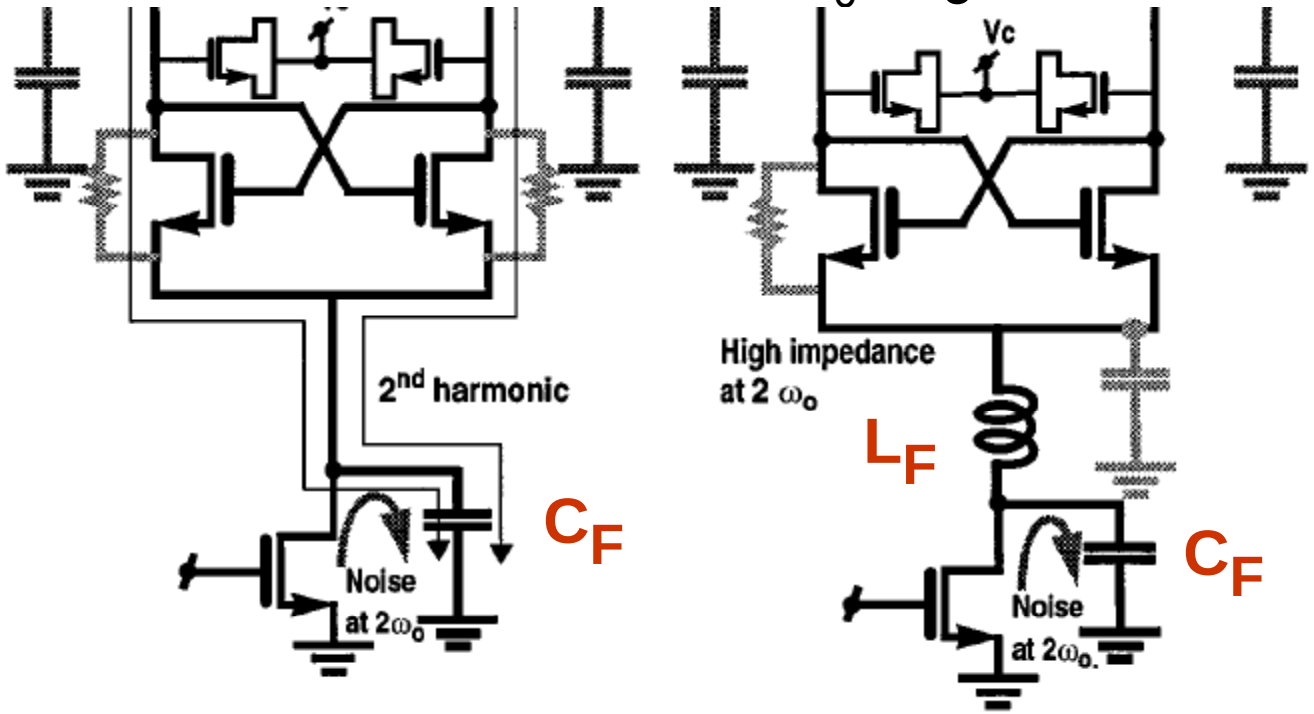
- Sets I_{bias} and provides high Z to diff pair
- Without CS, the device in triode adds noise



[Hegazi01]

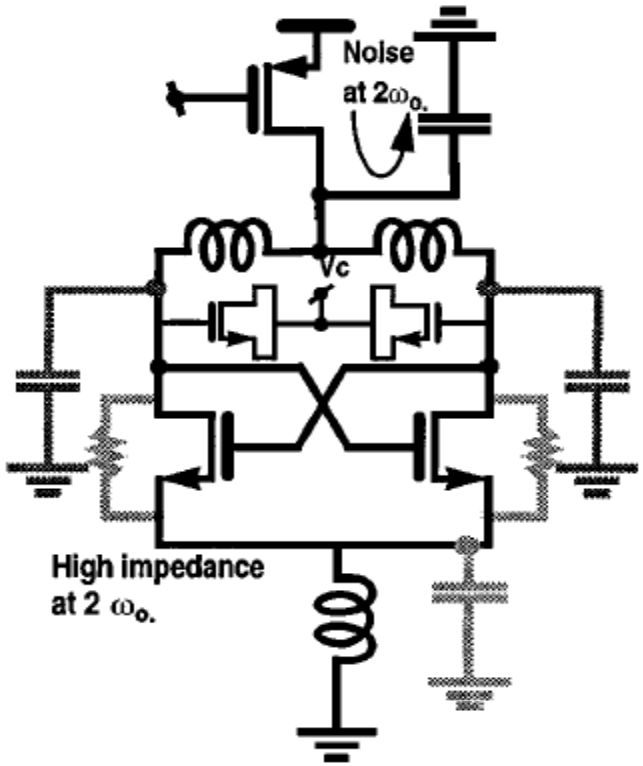
Noise Filter

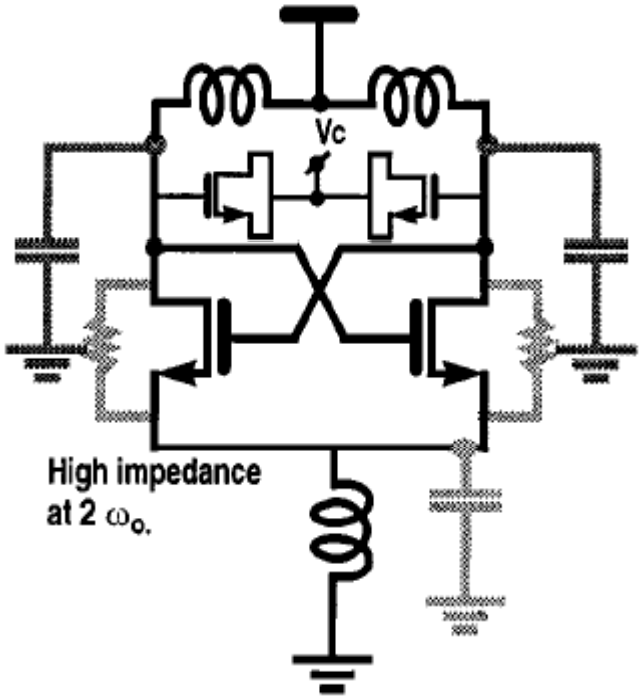
- High Z is required for even harmonics only
- L_F provides high Z at $2\omega_o$
- C_F shorts tail current noise at $2\omega_o$ to gnd



Inductor Tail

- Removes the current source device
- L_S provides high Z at $2\omega_o$





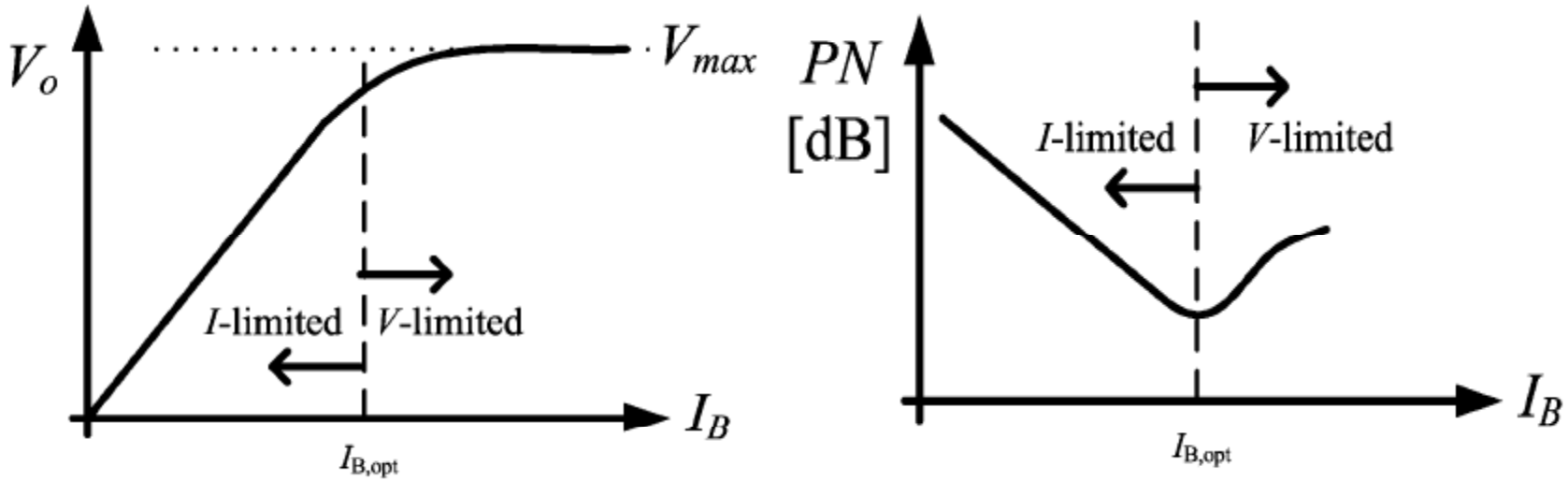
NTV Phase Noise Theory

NTV Phase Noise Theory

- In LTV, frequency translation occurs only due to the periodic ISF and NMF
- Nonlinearity in VCO can also cause frequency translation, thus noise folding
  - Nonlinear Gm of switches
  - Nonlinear C/V of varactors
- AM-noise gets converted to PM-noise
  - Tail bias 1/f noise
  - Vdd noise

Voltage Limiting

- Current-limited: $V_{swing} \approx I_{bias} \cdot R_{tank}$
- Voltage-limited: V_{swing} becomes limited by Vdd
- Phase noise may become worse!
  - Devices operate more in linear region (noisy)

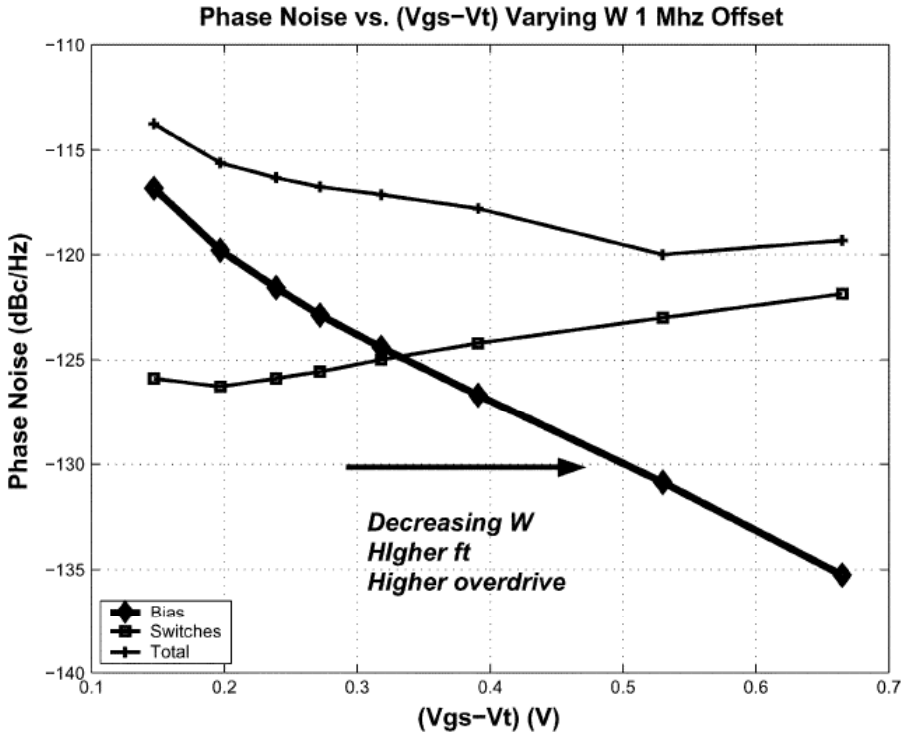


Switch Nonlinearity Adds Phase Noise

- Hard switching creates 2nd and 3rd harmonics of current in response to sine voltage
  - Nonlinear Gm; dependency on amplitude
- The harmonics flow into C causing imbalance
  - Imbalance will result in phase shift
- Thus, amplitude noise will turn into phase noise
  - Tail current noise including flicker
  - Vdd noise

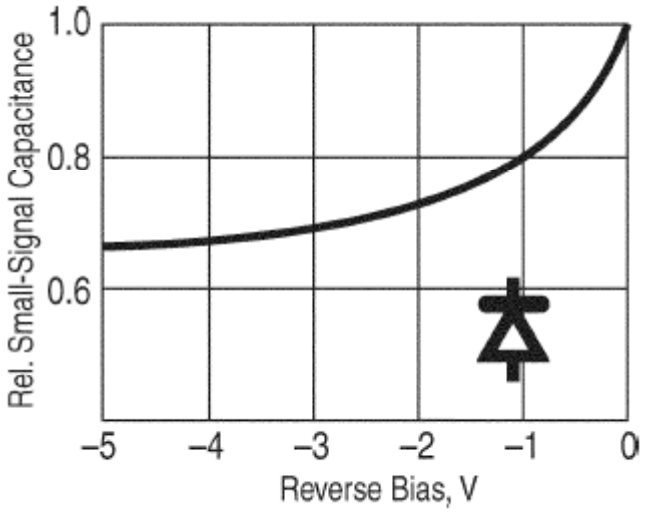
Switch Device Sizing

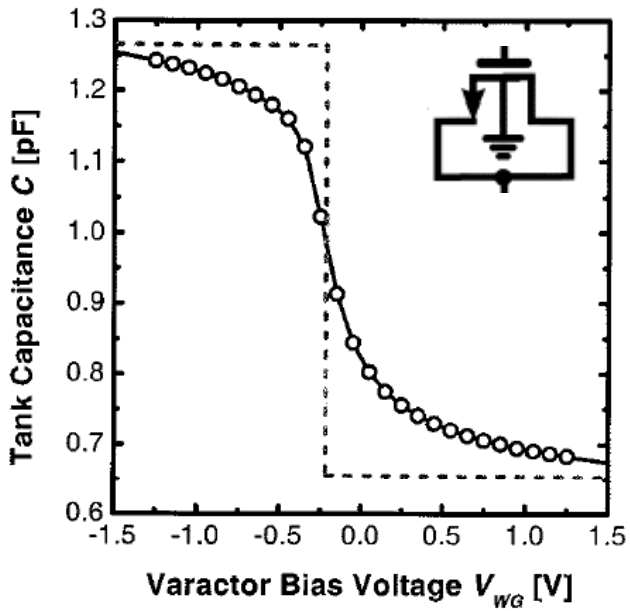
- In LTV, excess noise factor γ doesn't depend on switch device sizes [Rael00]
- But switch nonlinearity suggests that smaller device with higher Vgs-Vt yields lower phase noise [Jerng05]



AM-PM due to Varactor Nonlinearity

- Nonlinear C-V of varactor excites harmonics
  - Single-tone voltage in $\Rightarrow$ Multi-tone current out
- Another mechanism of noise folding
  - Up-conversion of tail bias 1/f noise
  - Vdd noise





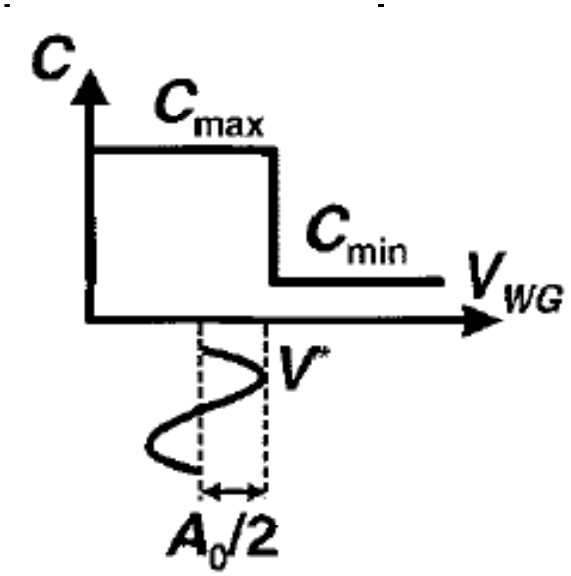
A_0-Dependency of f_{OSC}

- Due to large swing A_0, varactor C v
- Ceff = C_0-C_2/2

  C_0: time average of C
  C_2: second-order Fourier coeff
  [Hegazi03]

- f_{OSC} varies with A_0

  $\neq 1/2\pi\sqrt{LC_{nom}}$

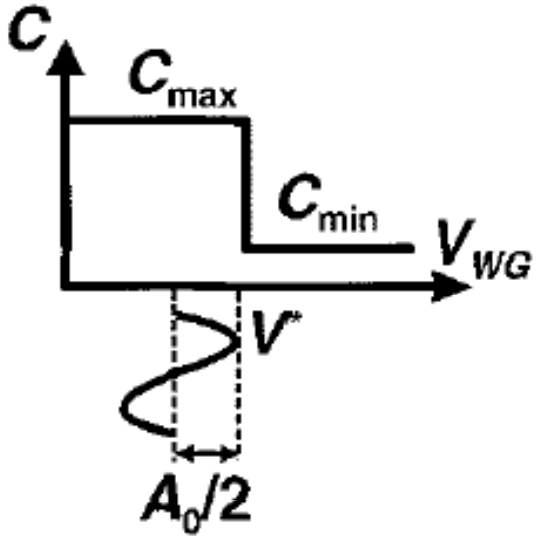


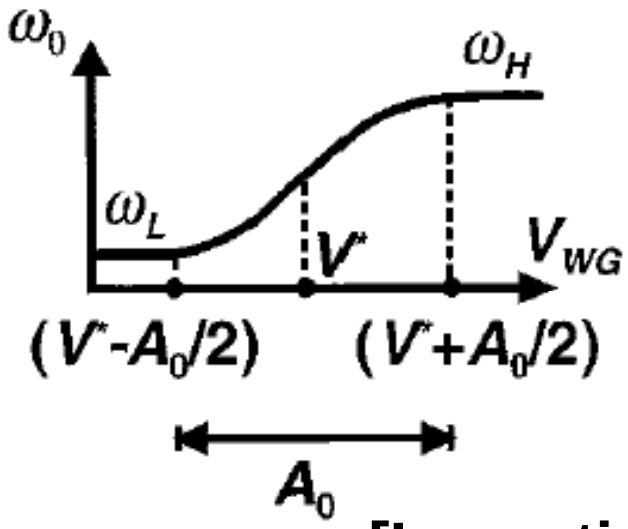
A_0-Dependency of Tuning Range

- 1st-order approximation of tuning range:

  $TR = Kvco \cdot \Delta V_{TUNE} = (\omega_H - \omega_L)/A_0 \cdot \Delta V_{TUNE}$

- TR also depends on A_0 and narrower than ω_H:ω_L

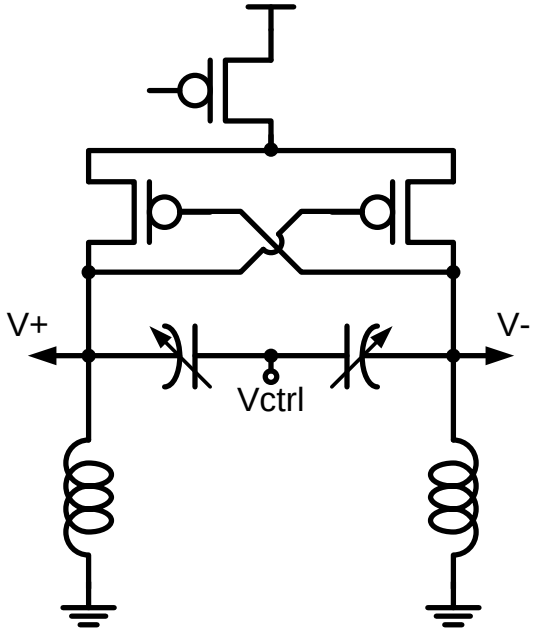




[Levantino02]

Vdd Noise Sensitivity

- CMOS: output V_{CM} varies with Vdd
  - V across varactor and switches also vary with Vdd
- PMOS: output V_{CM} is fixed at gnd
  - By 1st order, Vswing and Vgs-Vt are fixed by Ibias

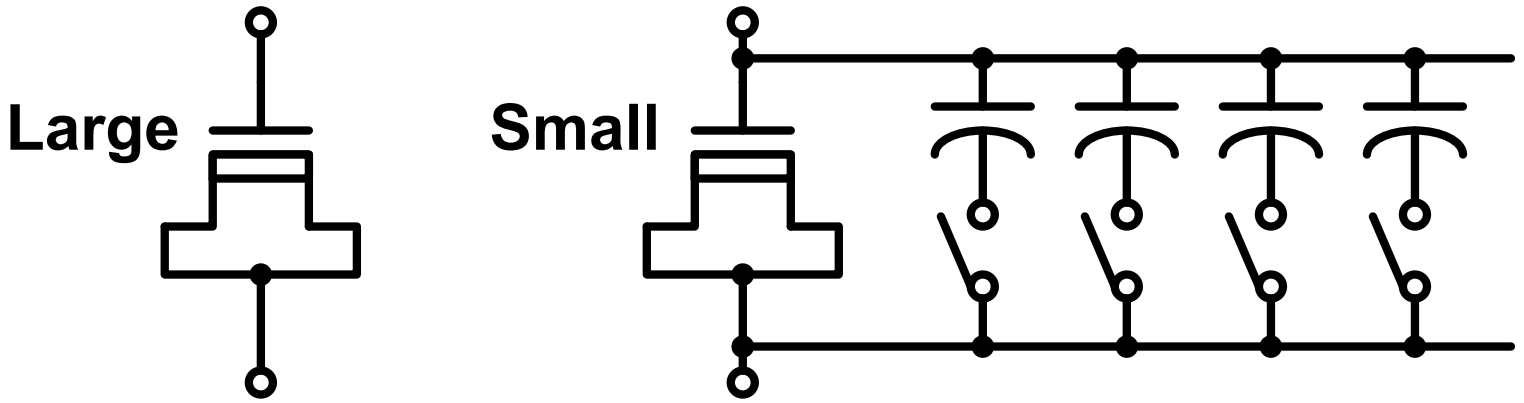


Selected Topics in LC Oscillator Design

- Design for Wide Tuning Range
- Multiphase Clock Generation
- VCO Design Optimization

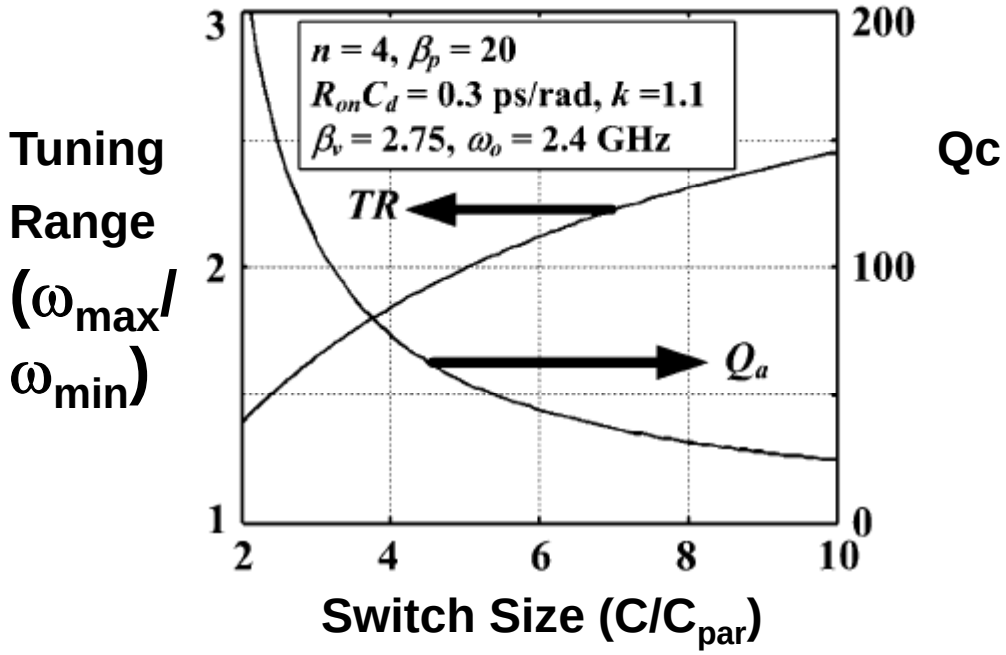
Issues for Wide Tuning Range

- MOS varactor is preferred for large dC/dV
- But nonlinear C/V of varactor degrades PN
- Use small varactor + switched array of fixed C



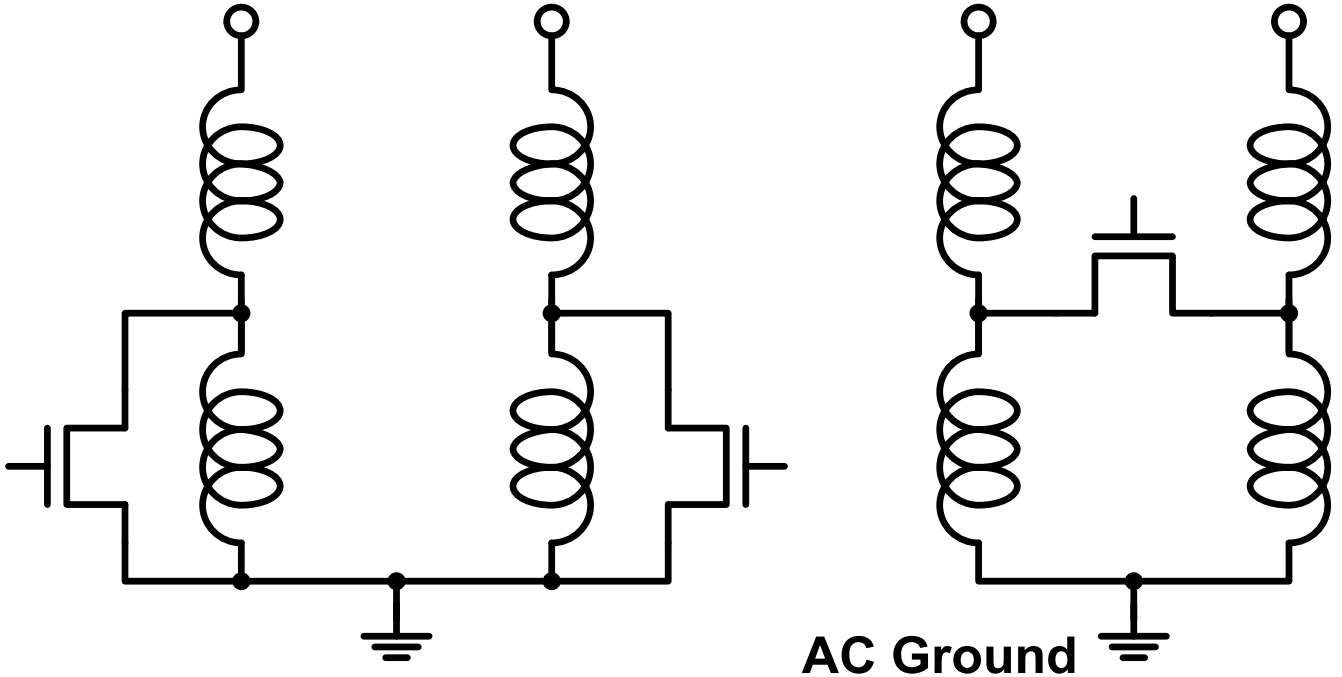
Switched Capacitor Array

- Switch size affects Q and tuning range
- ~2:1 range is feasible; but be aware of the broad-range design issues [Berny05]



Switched Inductor

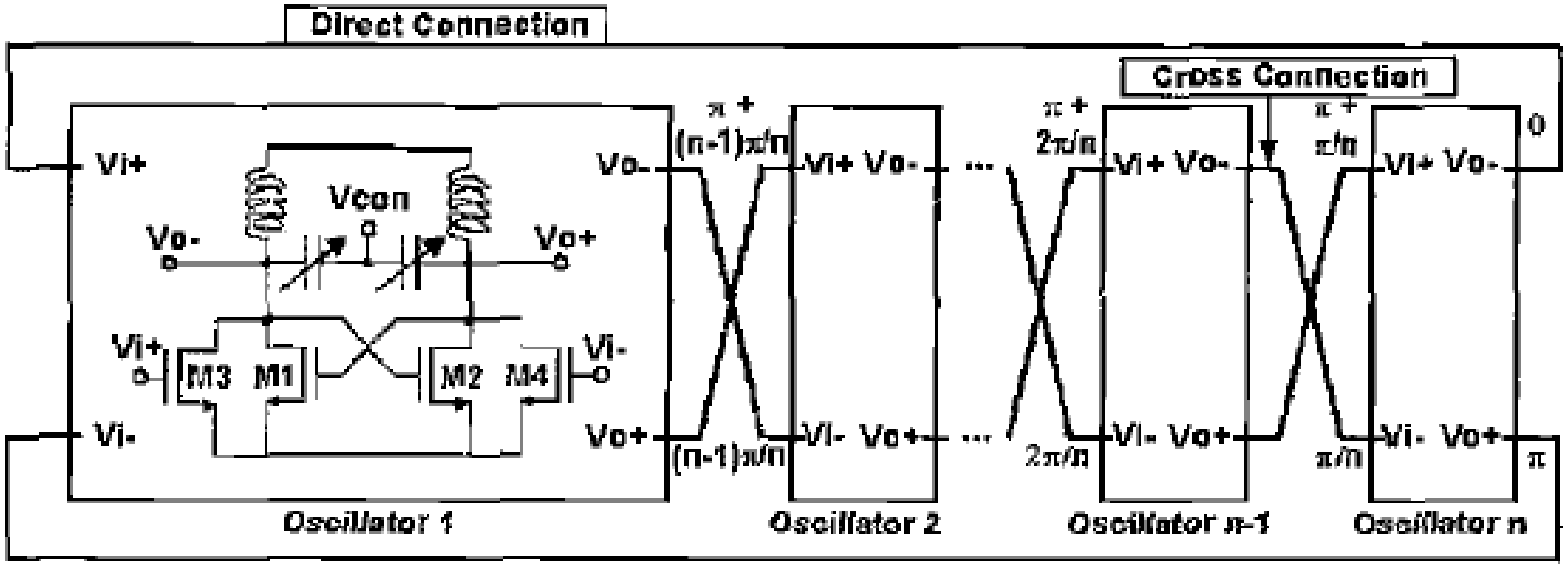
- Switch L to mitigate trade-offs in varying C only
  - If Q_L dominates, $R_{tank} \approx (\omega_o L_S)^2/R_S$
  - Waste of power occurs at high frequency



[ZLi05],[Yim01],[DaDalt05]

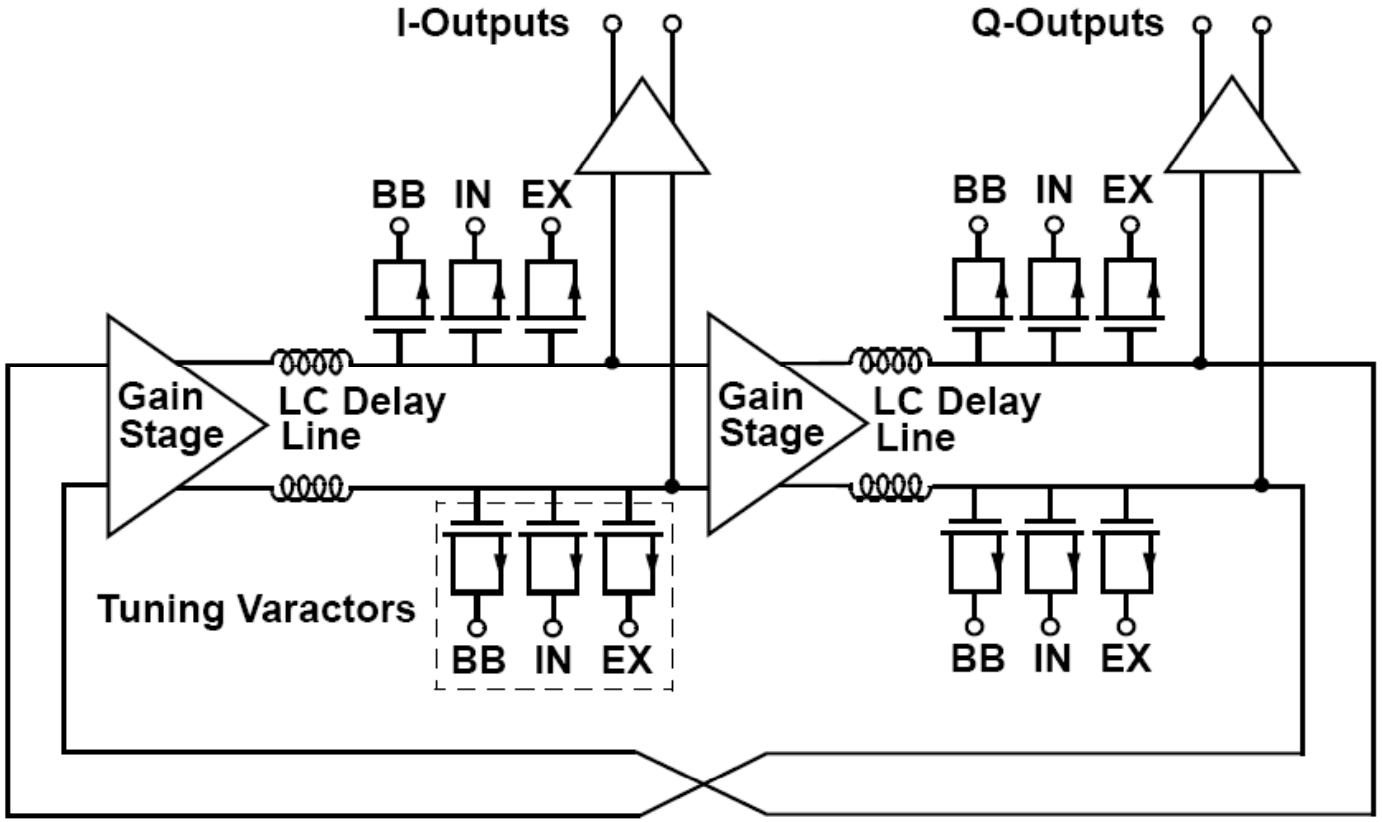
Multi-Phase Clock Generation (1)

- Coupled oscillators [JJKim00]



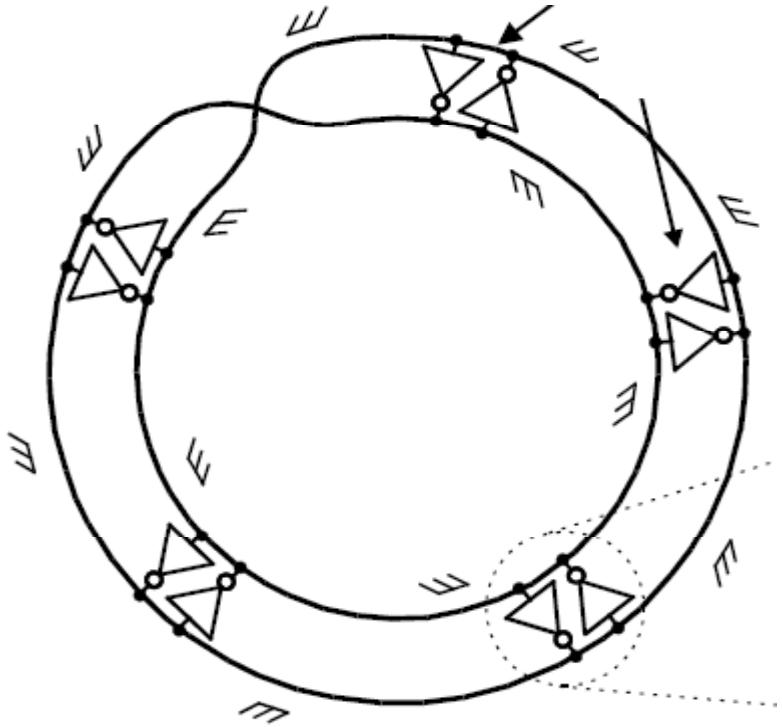
Multi-Phase Clock Generation (2)

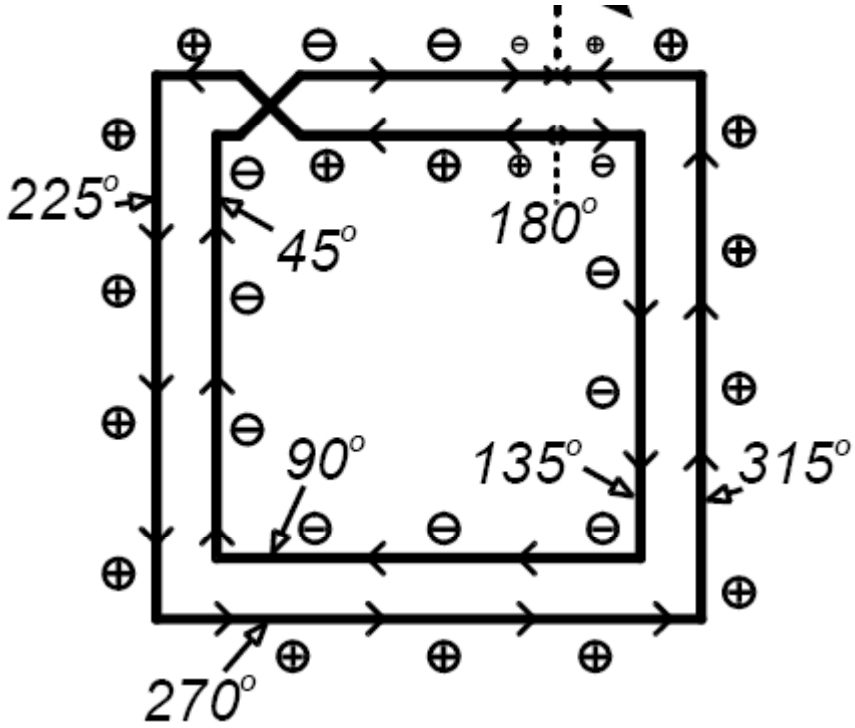
- LC-delay ring oscillators [Rogers02]



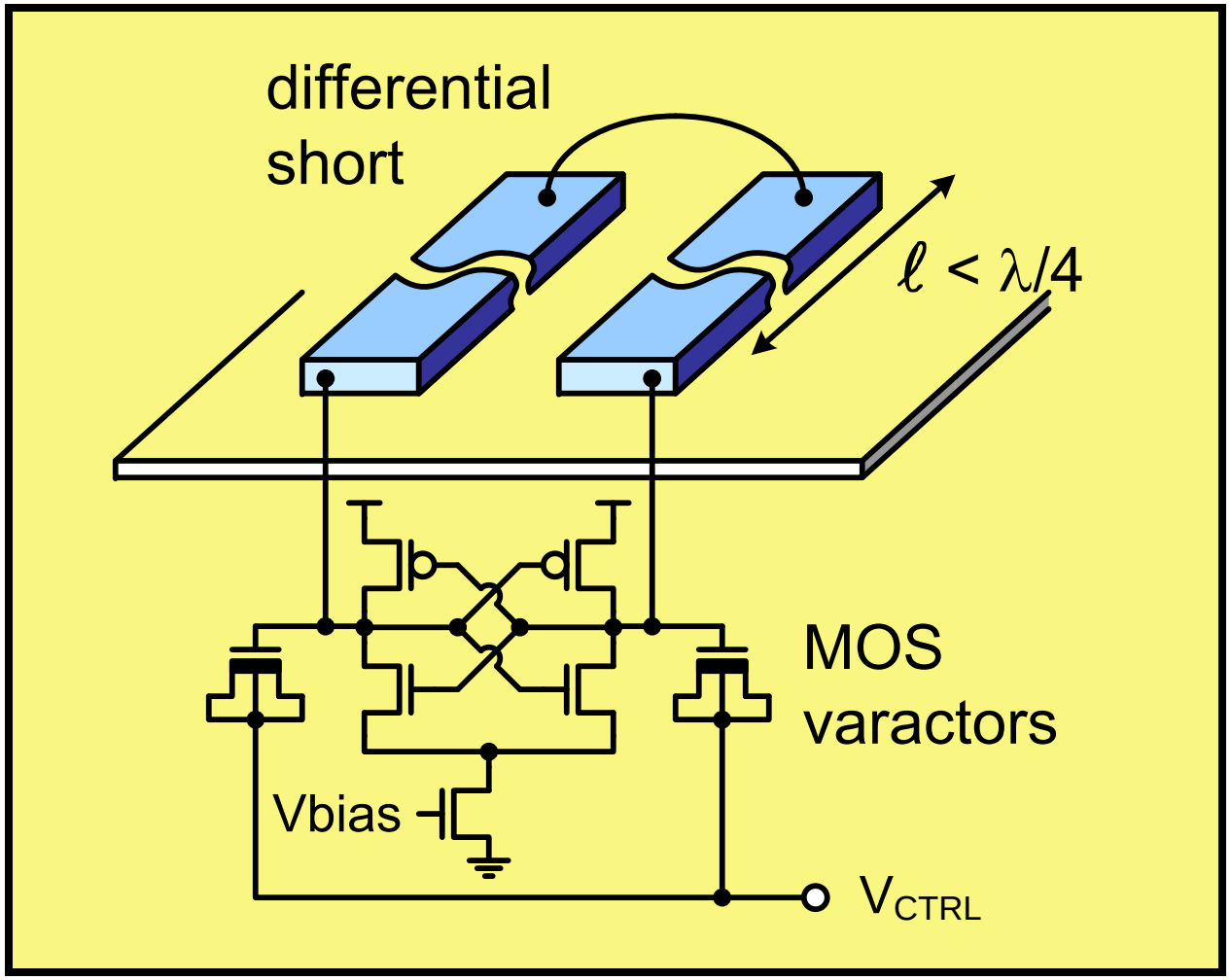
Multi-Phase Clock Generation (3)

- Rotary-wave oscillators [Wood01]





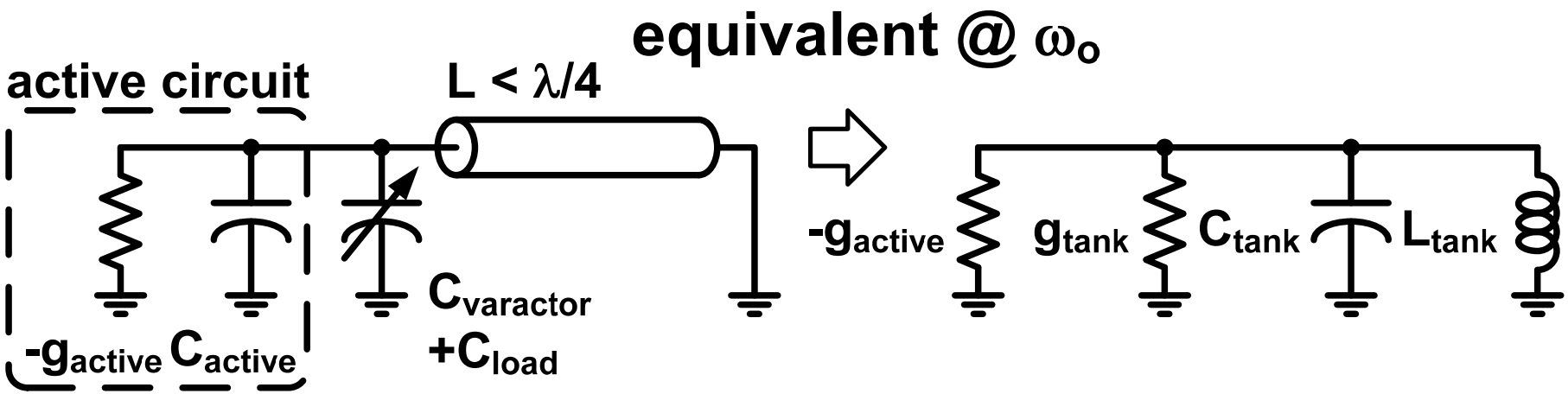
Optimization of LC Oscillator Design



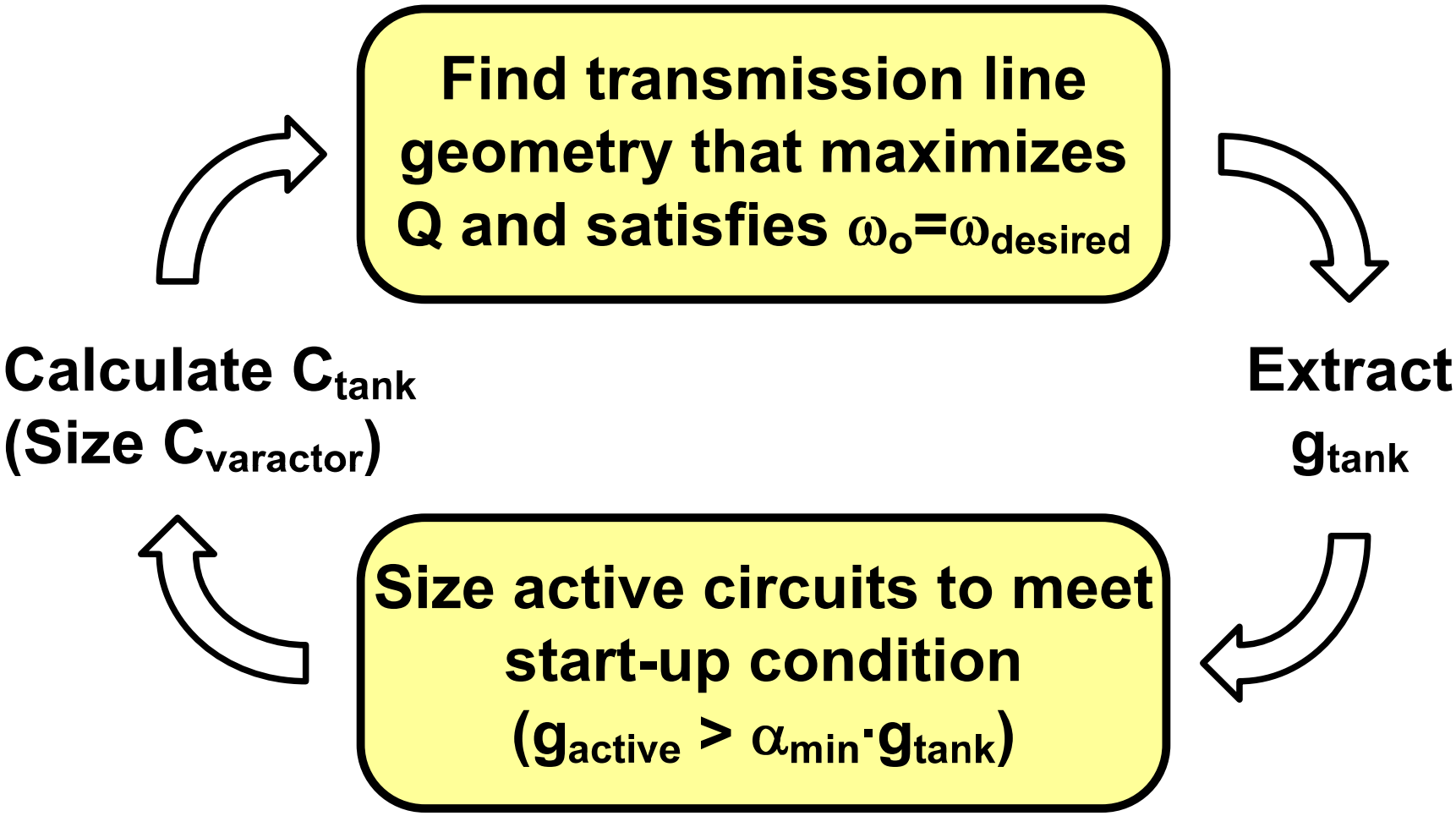
[JKim06]

VCO Design Constraints

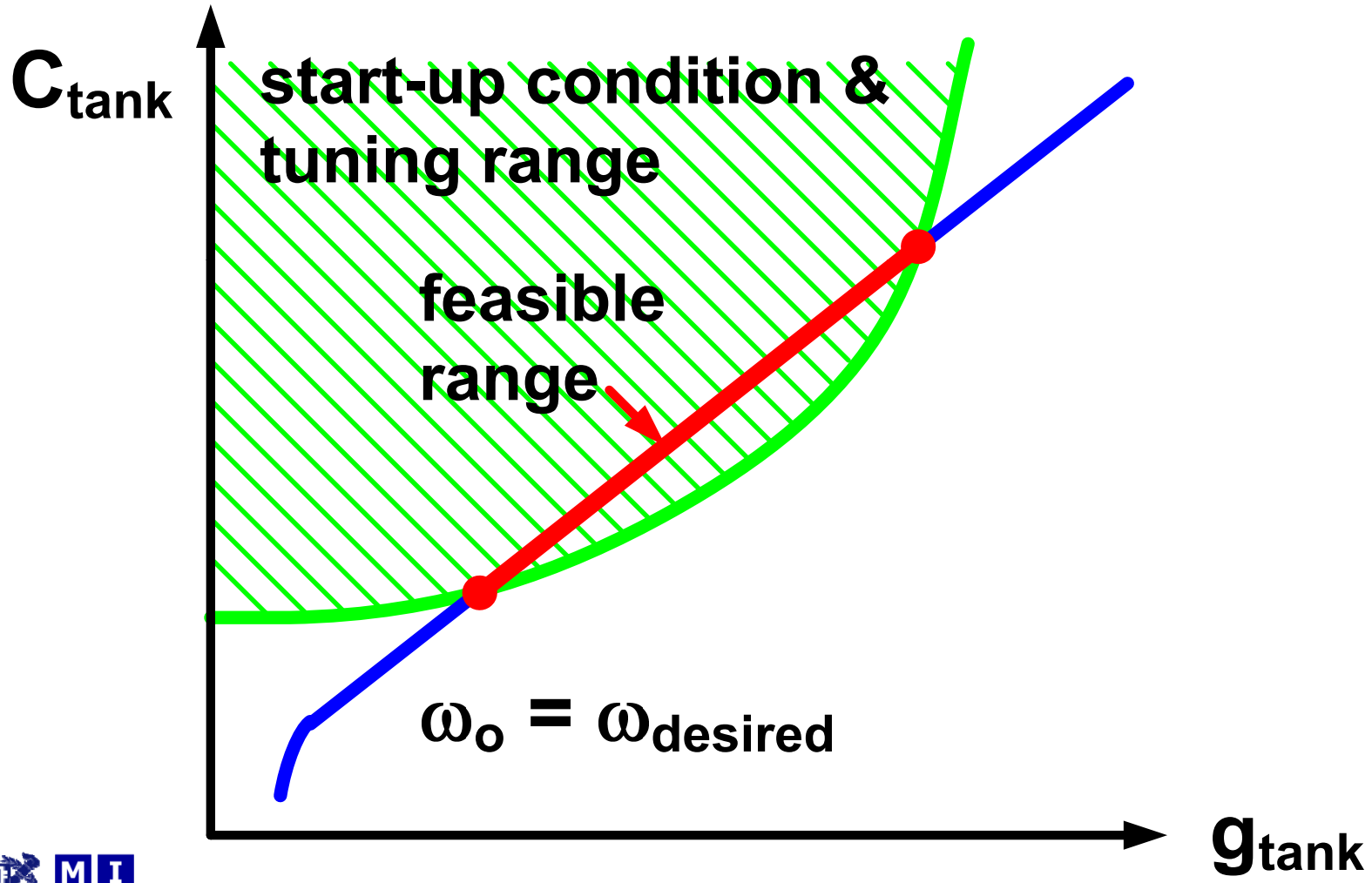
- Power : I_{bias}
- Start-up : $g_{active} \geq \alpha_{min} \cdot g_{tank}$ (α_{min} = 3~5)
- Osc freq : $\omega_o^2 = 1/L_{tank}C_{tank}$
- Tuning range : $C_{varactor}/C_{tank}$



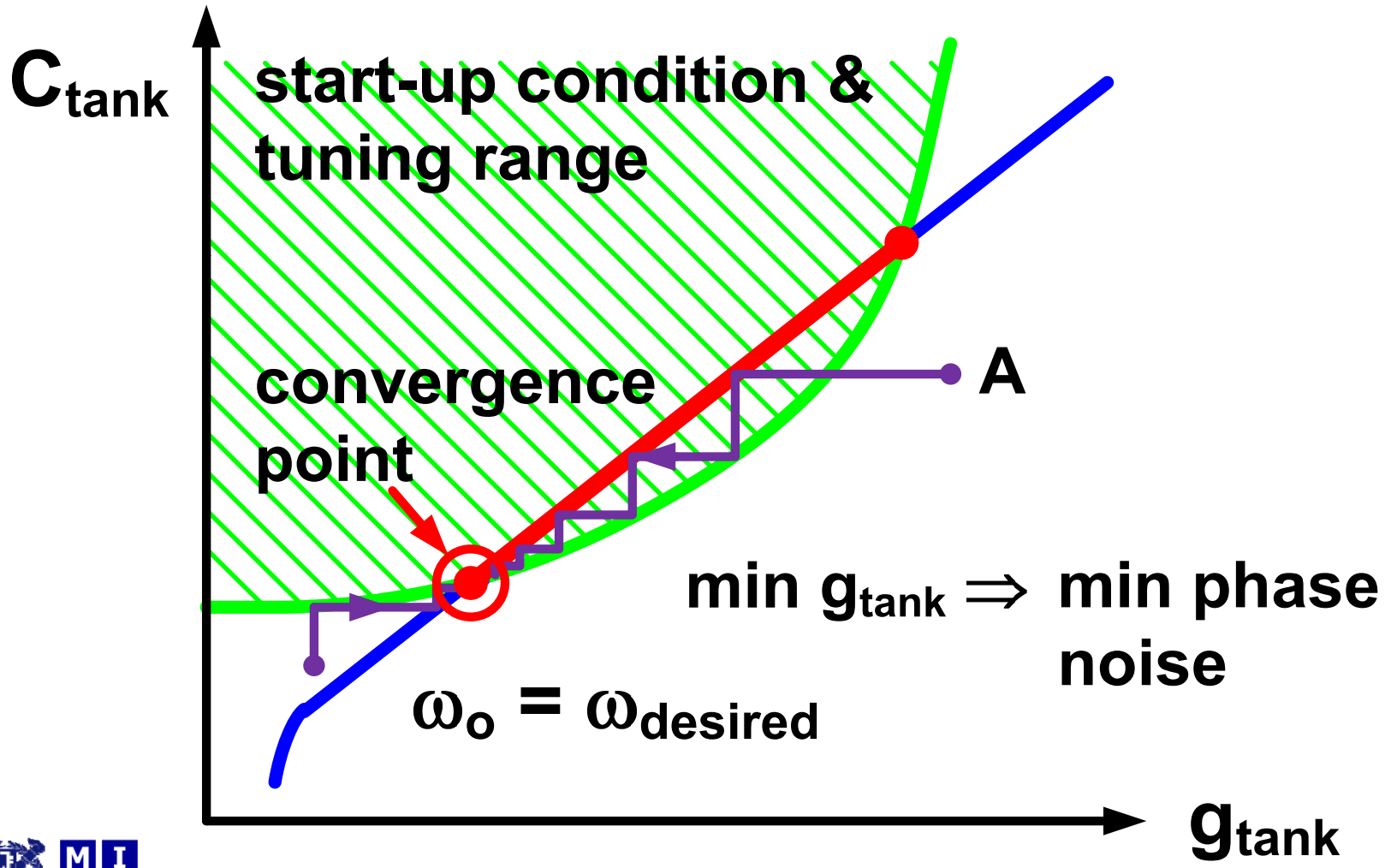
VCO Optimization via Iteration



Graphical Interpretation



Iteration Minimizes Phase Noise



Summary

- LTI theory gives the main guideline:
  - Maximize Q of the tank
  - Fundamental limit of γ : γ_{MOS}
- LTV/NTV theory explains noise mechanisms that determine excess noise factor γ
  - Major factor is still Q and γ_{MOS}
  - Not everyone agrees what the next dominant one is

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