Lecture 11. Mismatch Simulation using PNOISE

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Overview

- Readings
  - J. Kim, K. D. Jones, M. A. Horowitz, “Fast, Non-Monte-Carlo Estimation of Transient Performance Variation Due to Device Mismatch,” IEEE Trans. Circuits and Systems I, July 2010.
- Background
  - In this lecture, we will find another use of periodic analyses in RF simulators. First, we can approximate mismatch-induced offsets as low-frequency AC noise and hence substitute time-consuming Monte-Carlo simulations with small-signal noise analysis. The periodic noise (PNOISE) analysis lets you extend this approach to those that involve time-domain simulations.

Design for Yield

- CMOS device mismatch nearly doubles for every process generation < 100nm
  - 3σ-variation of I_{DS} reached beyond 30%
- Worst-case analysis is too pessimistic
  - Sacrifices speed, power, and area
- Must use statistical methods to estimate variation due to mismatch
  - And optimize circuits for highest yield

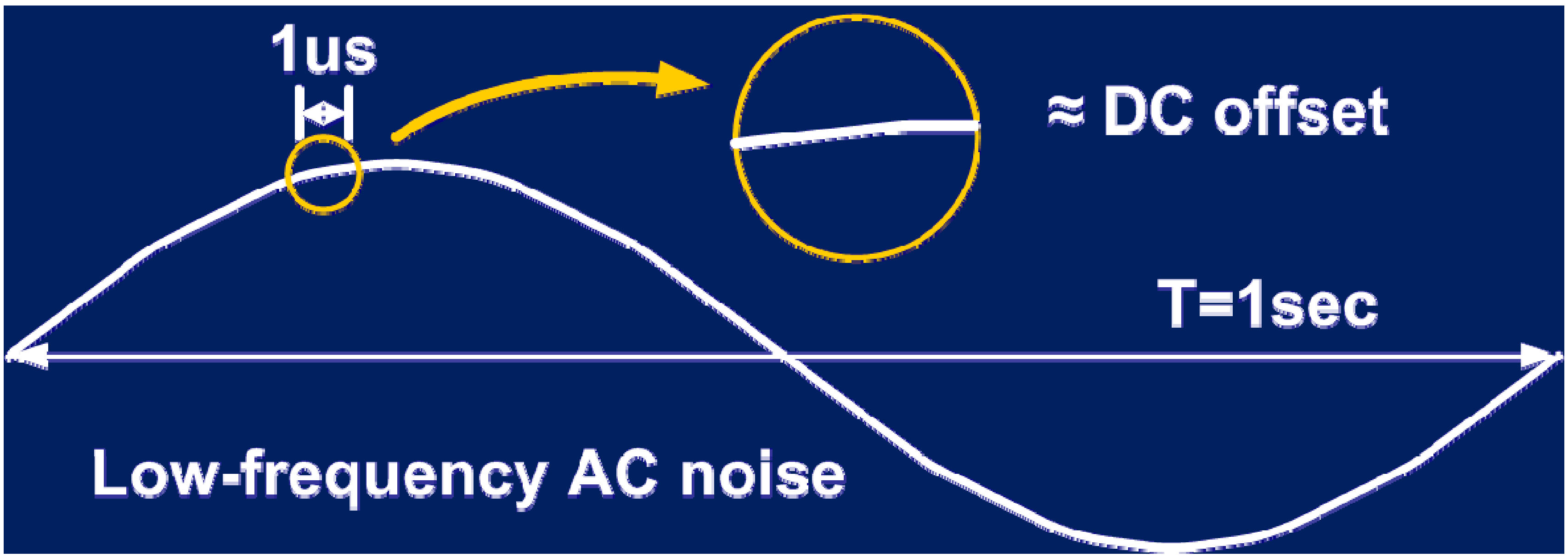
Previous Work

- Monte-Carlo Simulation
  - Repeated simulation with random samples
  - Often prohibitively time-consuming
- Yield optimization is even more costly
  - Iteration over Monte-Carlo simulations
  - Sensitivity requires additional sims
- Prior arts: variance reduction, response surface modeling, design centering, robust convex optimization, etc.

This Work

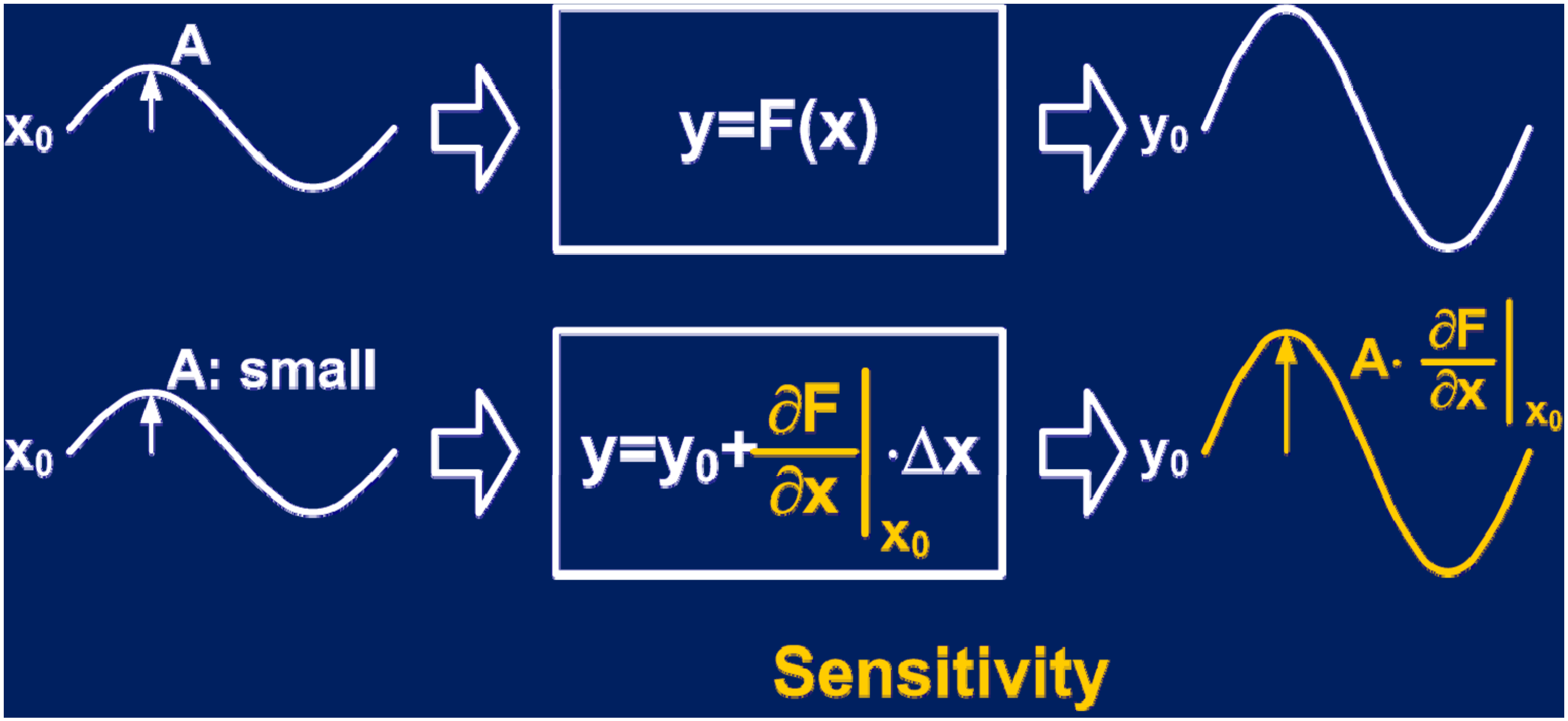
- Extends DCMATCH to estimate variation in transient measurements
  - Delay of logic path, frequency of VCO, input offset of comparator
  - Applies to small, Gaussian mismatches
- Achieves 100~1000× speed up compared to Monte-Carlo analysis
- Exploits currently available RF simulators (SpectreRF) and Verilog-A

Idea 1: DC offset ≈ low-freq AC noise



- If simulation time is bounded, low-freq AC noise appears the same as DC offset

Idea 2: Sensitivity-based Analysis



- If input variation is small enough,
  Δoutput $\approx$ Sensitivity $\times$ Δinput

Noise-Based Mismatch Analysis

- Sensitivity-based analysis (DCMATCH):

$$\sigma_{out}^2 = \sum S_i^2 \cdot \sigma_i^2$$

σ_i: variation in input parameter p_i

S_i: DC sensitivity of the output to p_i

Assuming mismatches are indep. Gaussian

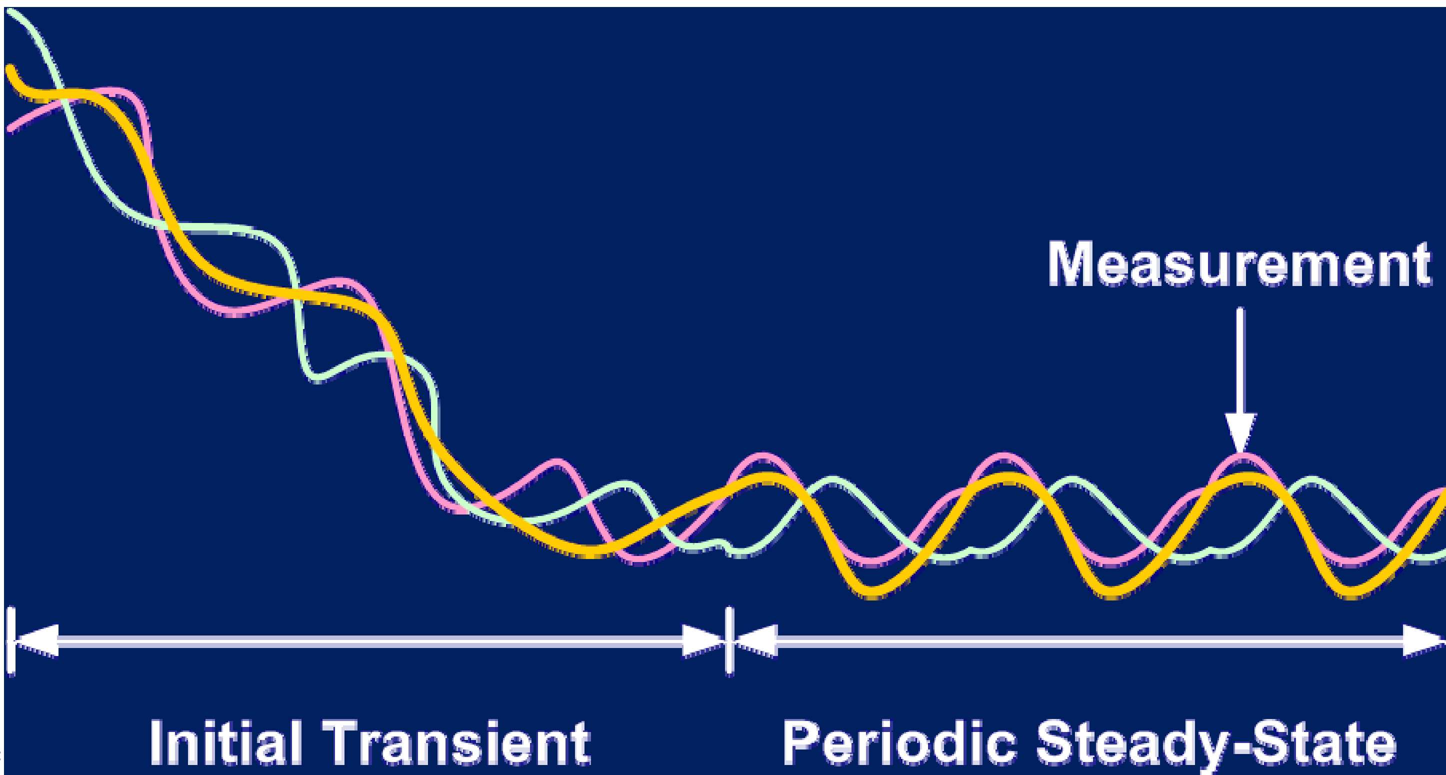
- Noise analysis:

$$Output\ PSD(f) = \sum |TF_i(f)|^2 \cdot Input\ PSD_i(f)$$

  - TF(f) ≈ DC sensitivity if f is low (e.g. 1Hz)
  - If $PSD_i(f) = \sigma_i^2$, then Output PSD (f) = σ_{out}^2

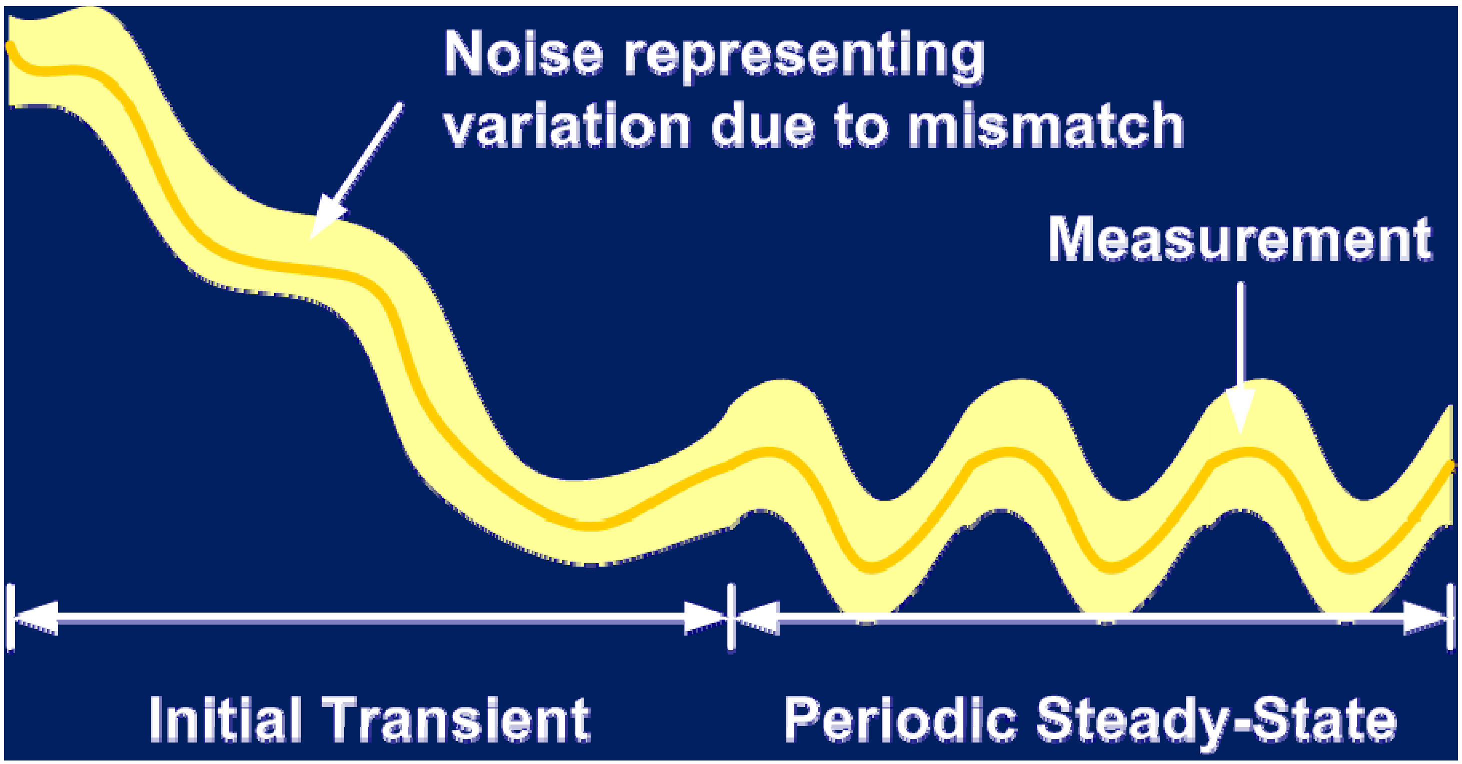
Monte-Carlo on Transient Measures

- Ex: VCO frequency, PLL static offset, …
- Measurement takes place only after a circuit settles to a steady-state



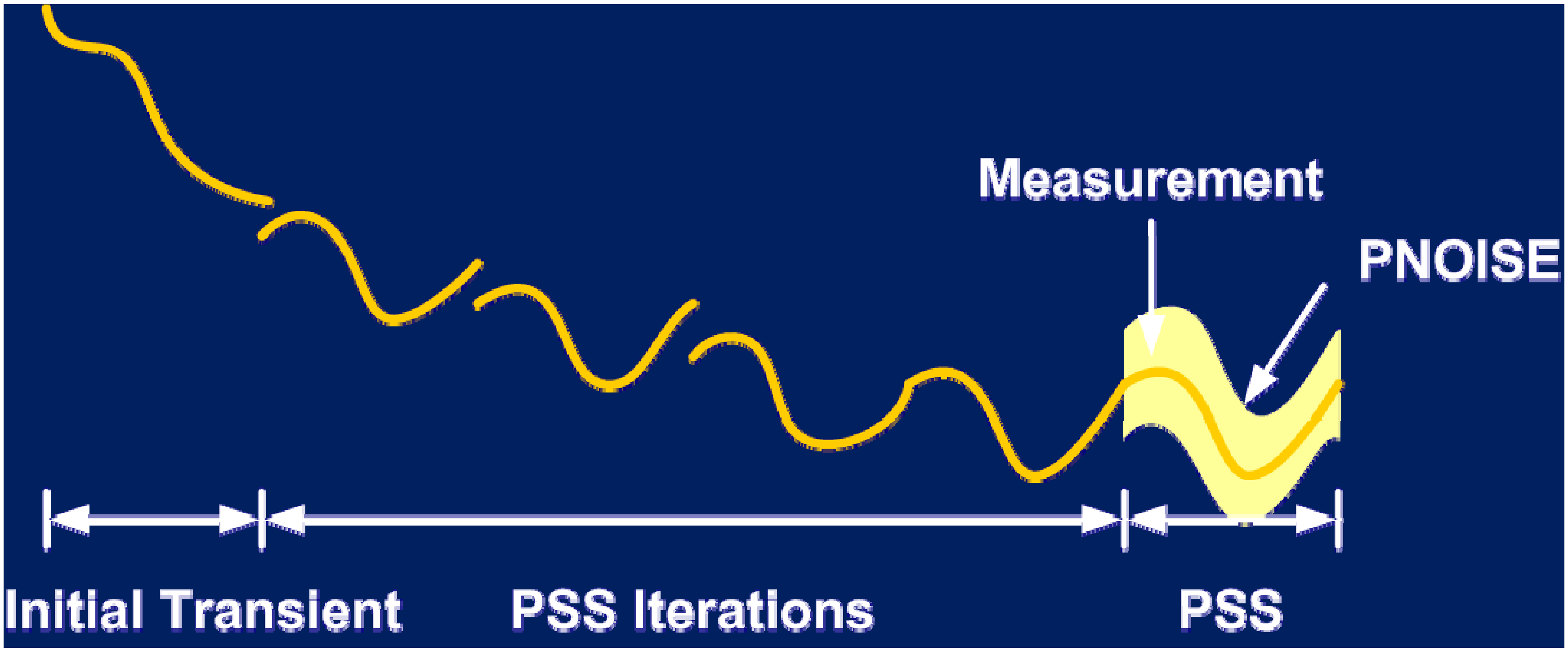
Extend Noise Analysis to Transient (1)

- Transient noise analysis wastes computation during initial transient

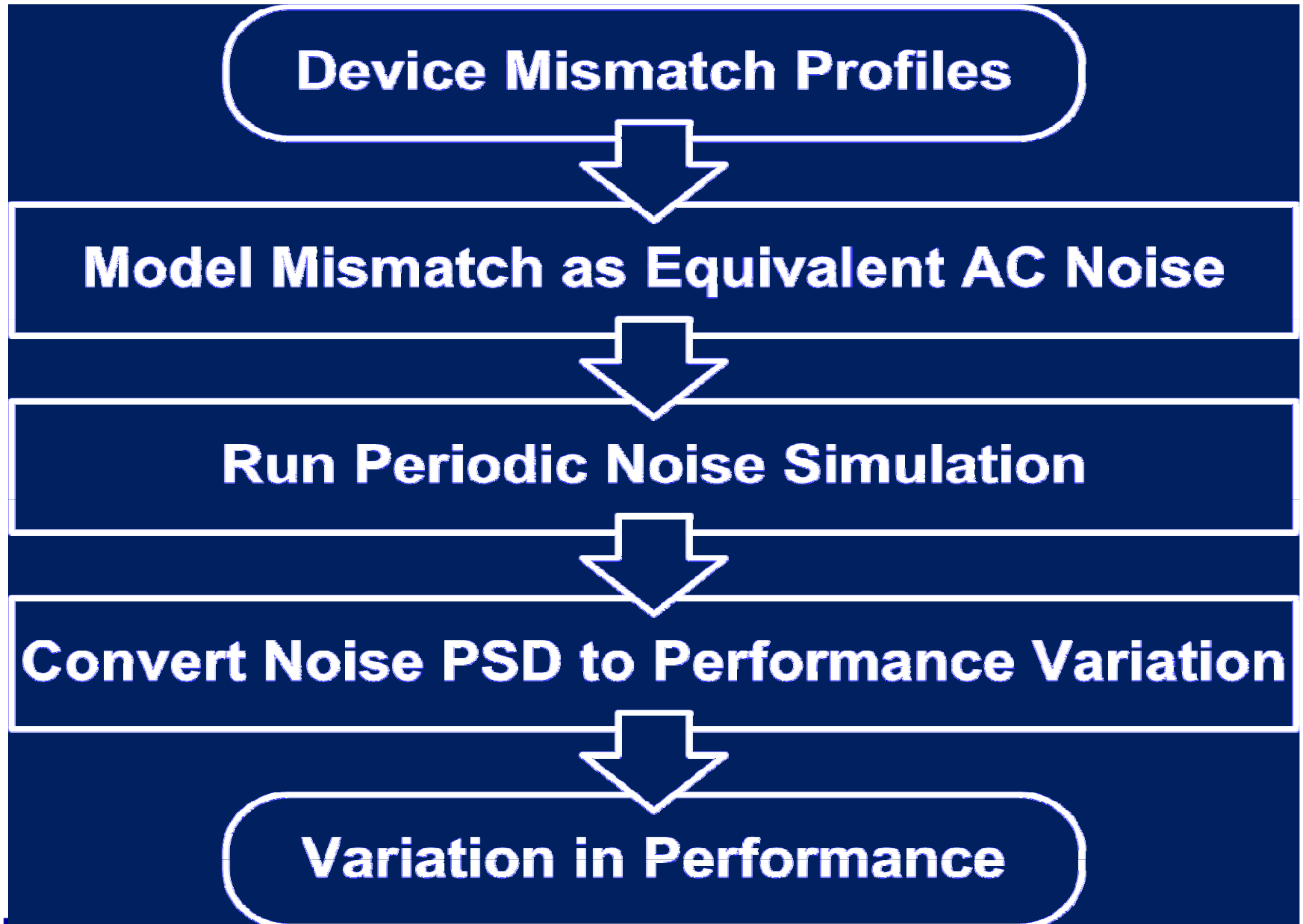


Extend Noise Analysis to Transient (2)

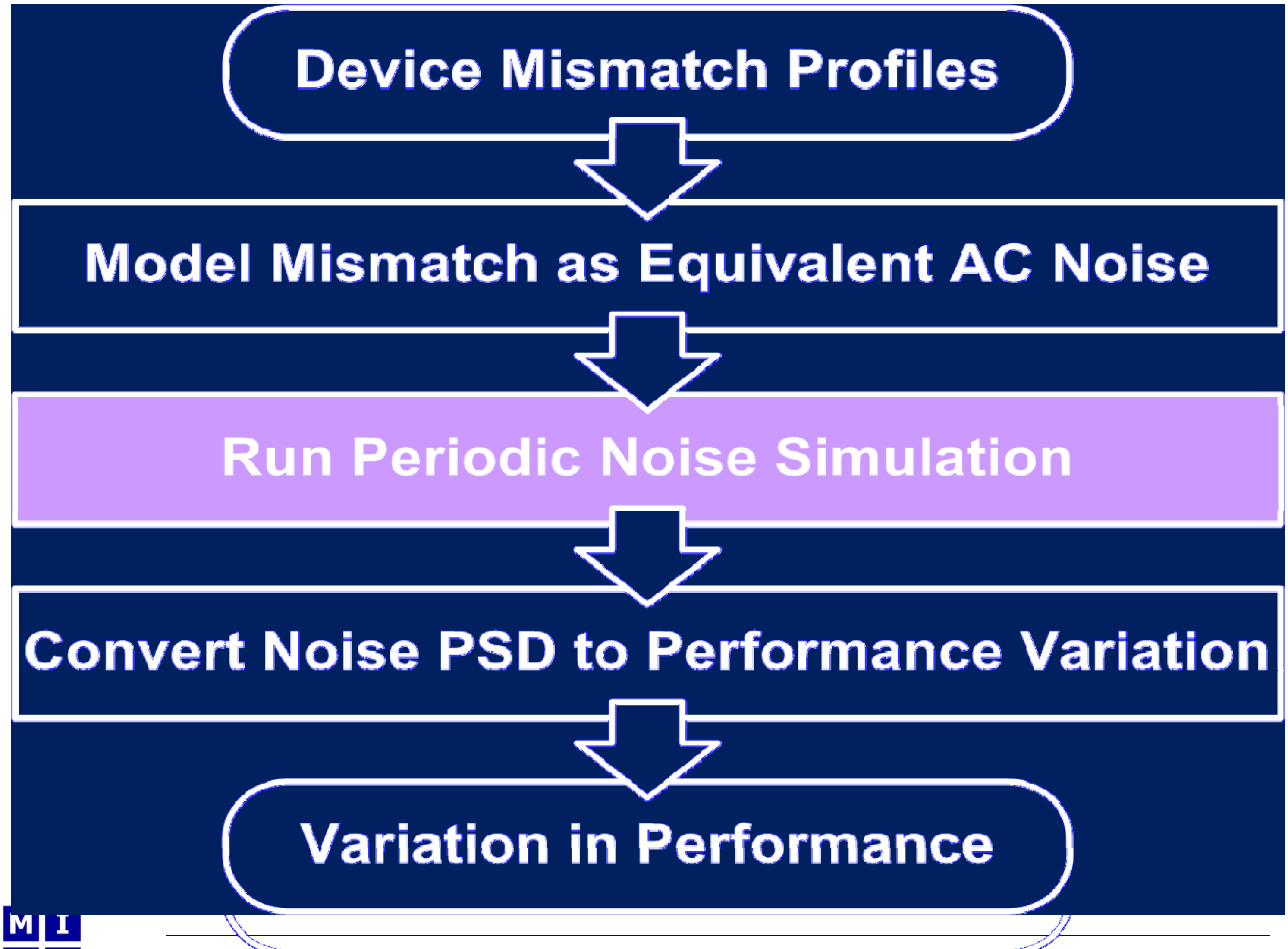
- PSS + PNOISE analysis:
  - PSS: expedites initial transient
  - PNOISE: freq-domain analysis only on PSS



Noise-Based Mismatch Analysis



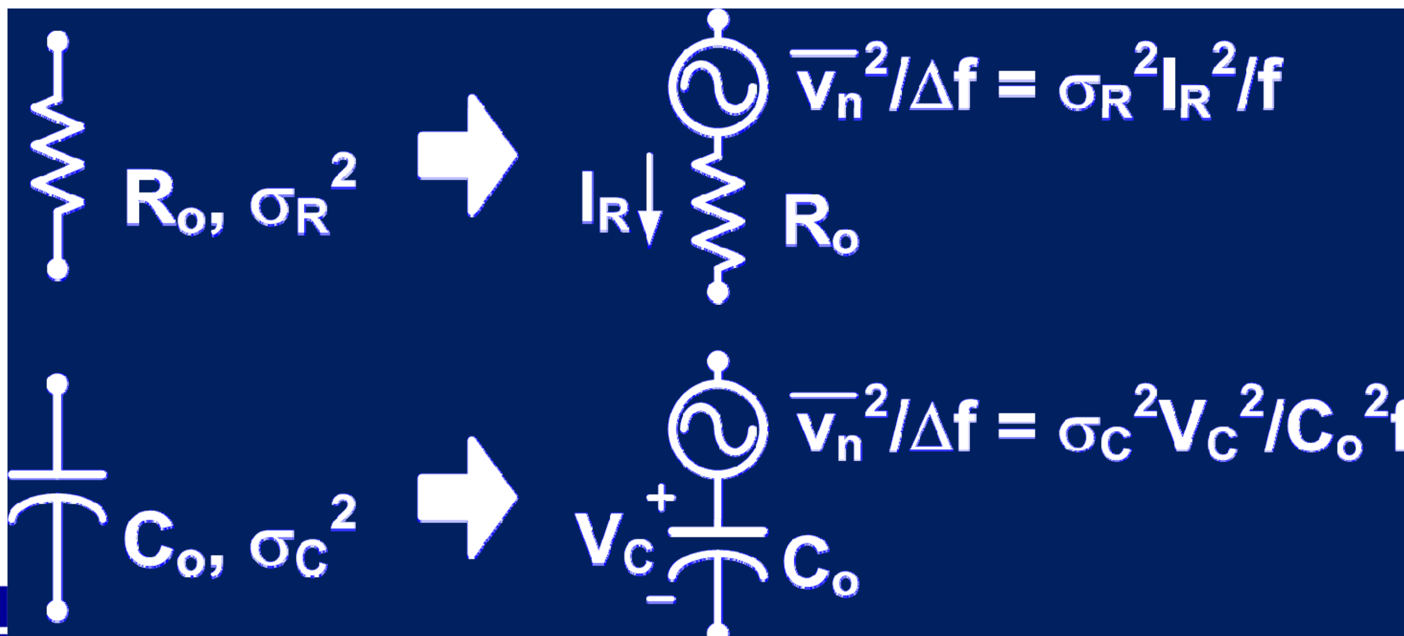
Noise-Based Mismatch Analysis



Modeling Mismatch as Noise

- Variation in passive elements (R, L, C)
  - Model as equivalent pseudo-noise in V or I

- Pseudo-noise has 1/f PSD profile
  - Mismatch with $\sigma^2 \longrightarrow \mathrm{PSD}(f) = \sigma^2/f$



Why Model Mismatch as 1/f Noise?

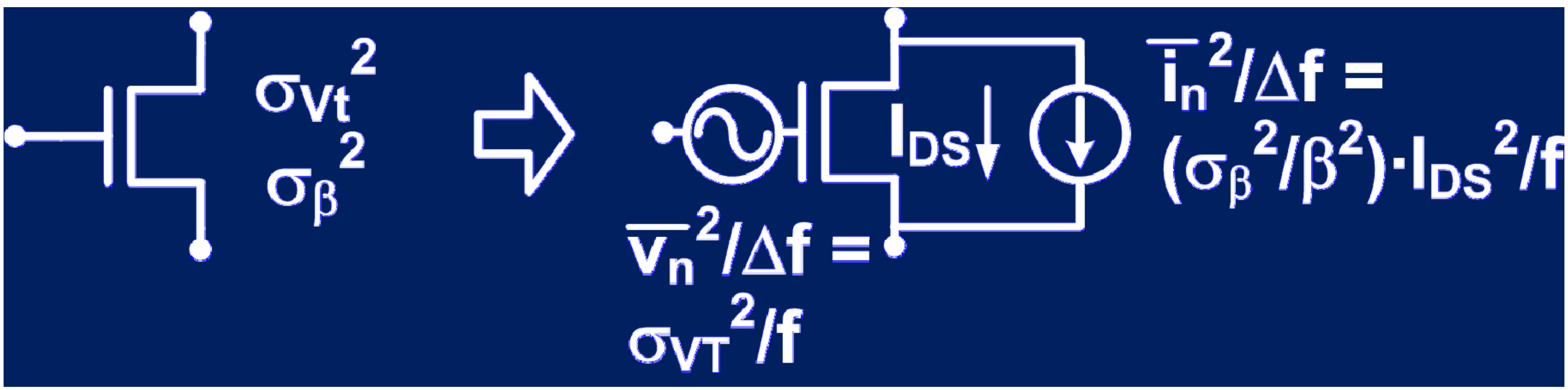
- In LTI frequency-domain analysis, each frequency point is independent
  - Only PSD at 1Hz matters
- In LPTV analysis, noise may up-convert or down-convert by $N \cdot f_c$ (noise folding)
  - f_c: fundamental frequency of PSS
- 1/f-noise ensures negligible contamination due to noise-folding
  - if $1\text{Hz} \ll f_c$

MOS Transistor Mismatch

- Pelgrom Model (JSSC, 1989):

  $\sigma_{VT}^2 = A_{VT}^2/WL$

  $\sigma_\beta^2/\beta^2 = A_\beta^2/WL$



Verilog-A Modeling of Pseudo-Noise

```
module mos_MC (d, di, g, gi, s);
inout d, di, g, gi, s;
parameter real var_VT=0.0, var_REL_BETA = 0.0;
analog begin
        I(d,s) <+ flicker_noise(var_REL_BETA*I(d,di)*I(d,di), 1, “beta”);
        V(g,gi) <+ flicker_noise(var_VT, 1, “vt”);
end
endmodule
```

```
subckt NMOS_MC ( d g s b )
parameters W=1.0u L=0.13u
transistor ( di gi s b )    nmos W=W L=L
mismatch ( d di g gi s )  mos_MC
+       var_VT=A_VT**2/(W*L) var_REL_BETA = A_rel_beta**2/(W*L)
ends NMOS_MC
```

Model Correlations

- Mismatches may be correlated
  - Ex: spatial correlation
  - Noise sources are assumed independent
- Model correlation among mismatches by combining independent noise sources
  - Assume N_1, N_2 are indep. Gaussian with $\sigma=1$
  - $X = x_1 \cdot N_1 + x_2 \cdot N_2 \rightarrow Var(X) = x_1^2 + x_2^2$

    $Y = y_1 \cdot N_1 + y_2 \cdot N_2 \rightarrow Var(Y) = y_1^2 + y_2^2$

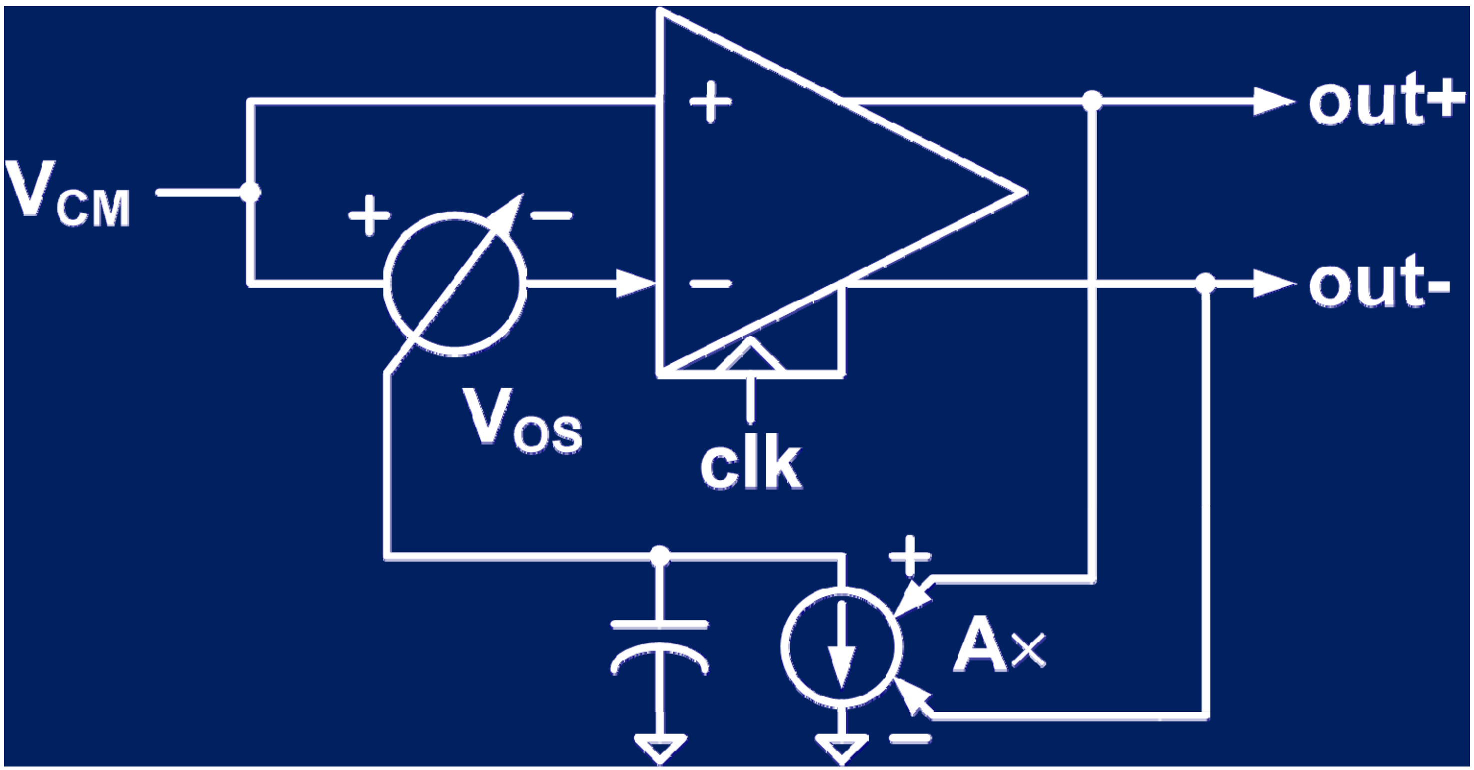
    $Cov(X,Y) = x_1 \cdot y_1 + x_2 \cdot y_2$

PNOISE Analysis

- LPTV small-signal noise analysis
  - Linearizes the circuit around its periodic steady-state (PSS)
  - Thus the circuit must have PSS
- Many transient sims can be made periodic
  - VCO frequency: already periodic
  - Logic path delay: apply periodic inputs
- SpectreRF, HSPICE-RF, ADS, …

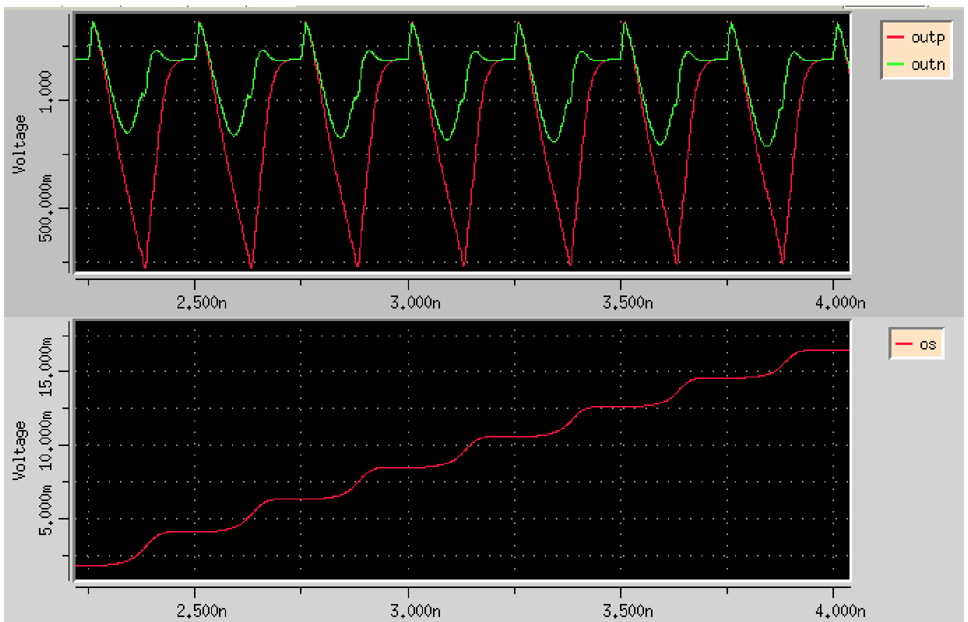
Periodic Setup for Comparator

- Feedback servos V_{OS} for V(out+)=V(out-)
- V_{OS} settles to input offset voltage at PSS

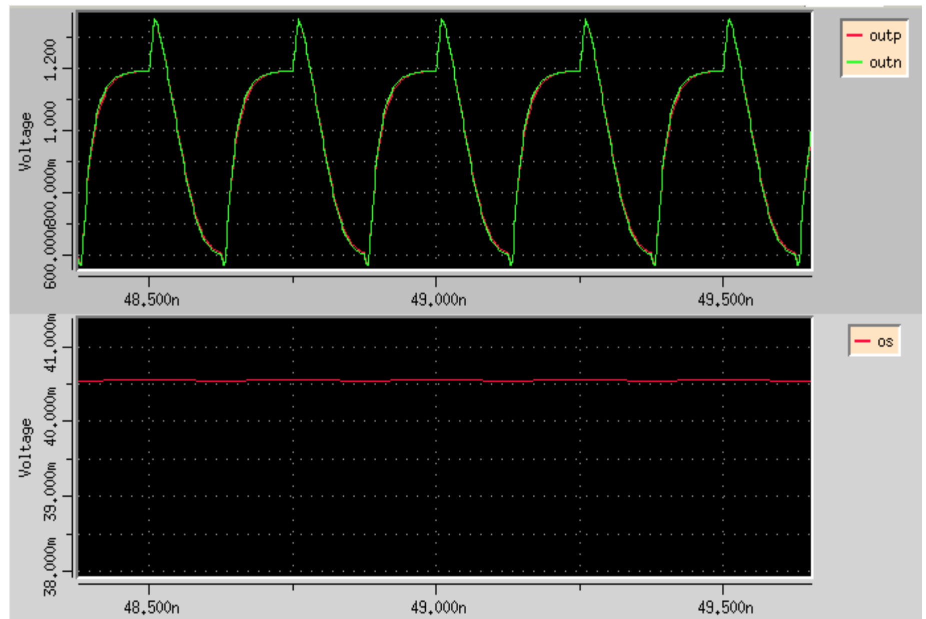


Comparator Offset Simulation

- V_{OS} settles to input offset voltage at PSS



Before Settling



After Settling

Interpreting Output Noise as Variation

- PNOISE output is cyclostationary noise
  - Described by a collection of PSDs at various sidebands: 0, $\pm f_c$, $\pm 2f_c$, $\pm 3f_c$, …
- Baseband noise PSD corresponds to variation in DC response
  - E.g. variation in offset voltage
  - PSD of P_1 at 1Hz $\rightarrow$ variation $\sigma^2 = P_1$

Variation in Delay and Frequency

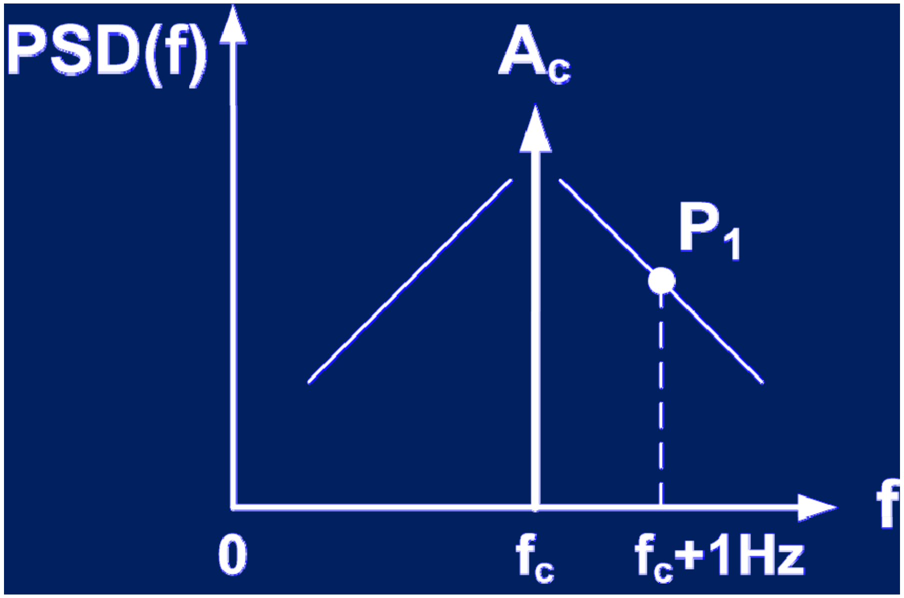
- Passband noise PSD corresponds to variation in AC response
  - E.g. time shifts in PSS: phase, delay, freq.

- From narrowband FM approximation:

$\sigma_{\Phi}^2 = \pi^2 \cdot P_1/A_c^2$

$\sigma_D^2 = 1/4f_c^2 \cdot P_1/A_c^2$

$\sigma_f^2 = 4f_1^2 \cdot P_1/A_c^2$



Breakdown of Noise Contributions

- Simulator also reports breakdown of contributions to total output noise
  - List of $(S_i \cdot \sigma_i)^2$ in $\sigma_{out}^2 = \sum S_i^2 \cdot \sigma_i^2$
- Use this breakdown to estimate:
  - Sensitivities
  - Correlations
  - At no additional simulation cost!

Sensitivity Analysis

- Sensitivity of output variation (σ_{out}) w.r.t. design parameters (e.g. device W)

$$\partial \sigma_{out}^2 / \partial W_i = \sum S_i^2 \cdot \partial \sigma_i^2 / \partial W_i$$

σ_i is either σ_{VT} or σ_β/β

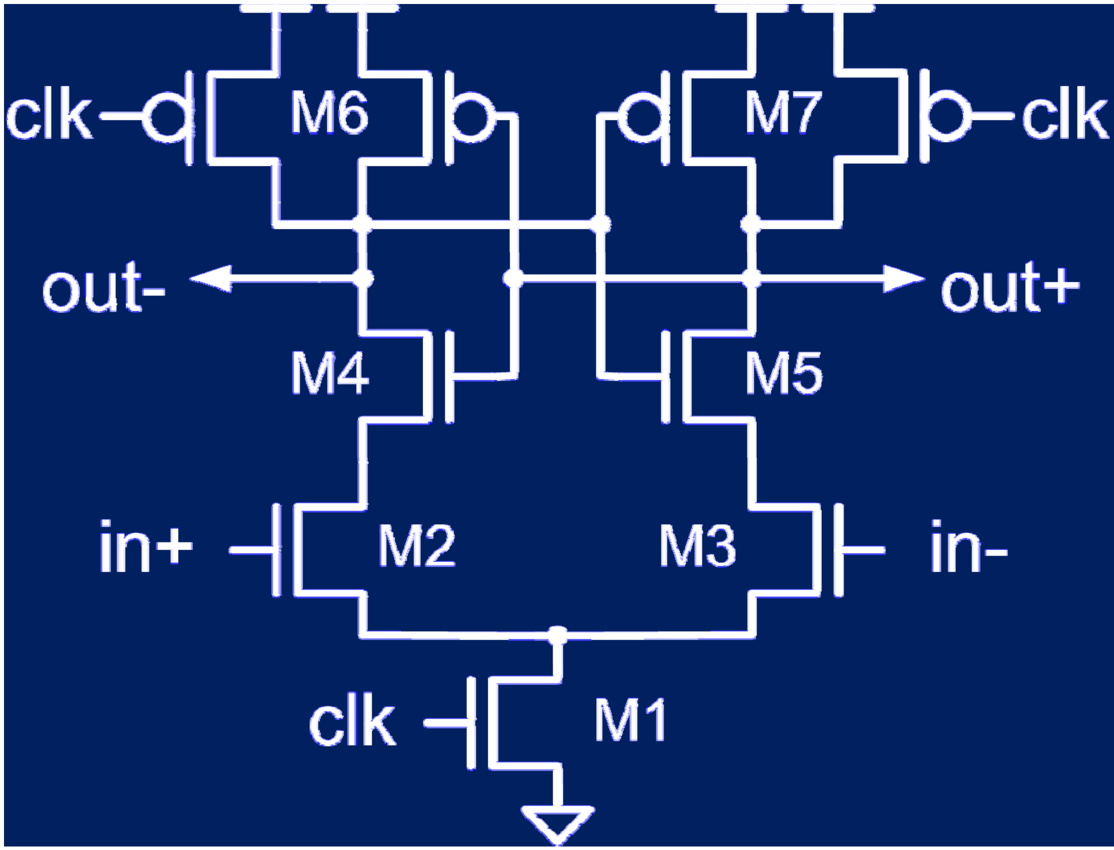
- According to Pelgrom model:

$\partial\sigma_i^2/\partial W = -A^2/W^2L = -\sigma_i^2/W$

- Therefore:

$$\partial \sigma_{out}^2 / \partial W_i = -\sum S_i^2 \cdot \sigma_i^2 / W_i$$

Comparator Mismatch Sensitivity



Parameter	Sensitivity
M1 width	5.017e-30
M2 width	5.851e-3
M3 width	5.851e-3
M4 width	3.028e-5
M5 width	3.028e-5
M6 width	1.366e-4
M7 width	1.366e-4

(in $V^2/\mu m$)

Correlation Analysis

- For Z = X+Y, $\sigma_Z^2 = \sigma_X^2 + \sigma_Y^2 + \sigma_{XY}$
  - But we often forget σ_{XY} term
  - Without σ_{XY} (covariance), RMS sum can either under-estimate or over-estimate

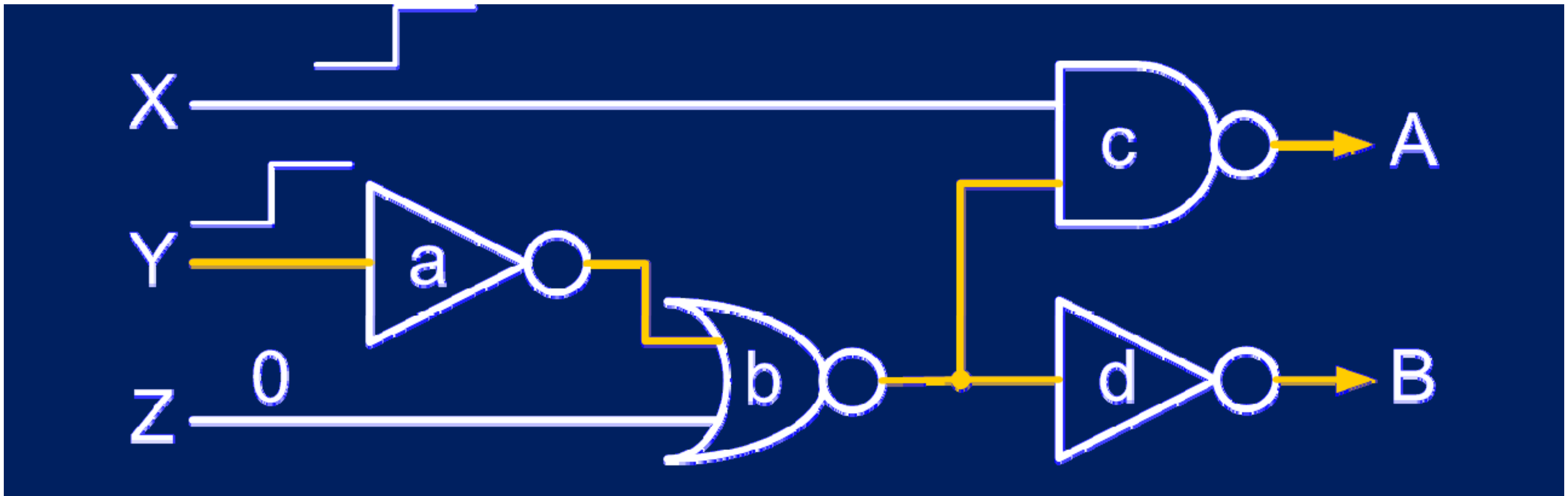
- If two measurements A, B vary as:

$$\sigma_A^2 = \sum \left(S_{A,i}^2 \cdot \sigma_i\right)^2 \text{ and } \sigma_B^2 = \sum \left(S_{B,i}^2 \cdot \sigma_i\right)^2$$

then covariance σ_{AB} is given by:

$$\sigma_{AB} = \sum \left(S_{A,i}^2 \cdot \sigma_i\right) \cdot \left(S_{B,i}^2 \cdot \sigma_i\right)$$

Correlation Analysis Example



Mismatch source	X rises first		Y rises first	
	Delay at A	Delay at B	Delay at A	Delay at B
Gate a (inv)	1.168e-23	1.145e-23	2.545e-33	1.147e-23
Gate b (nor)	2.060e-23	1.543e-23	1.094e-30	1.549e-23
Gate c (nand)	6.934e-24	5.662e-26	3.704e-24	6.133e-26
Gate d (inv)	1.068e-25	3.401e-24	5.443e-36	3.417e-24
Correlation (ρ)	0.885		0.010	

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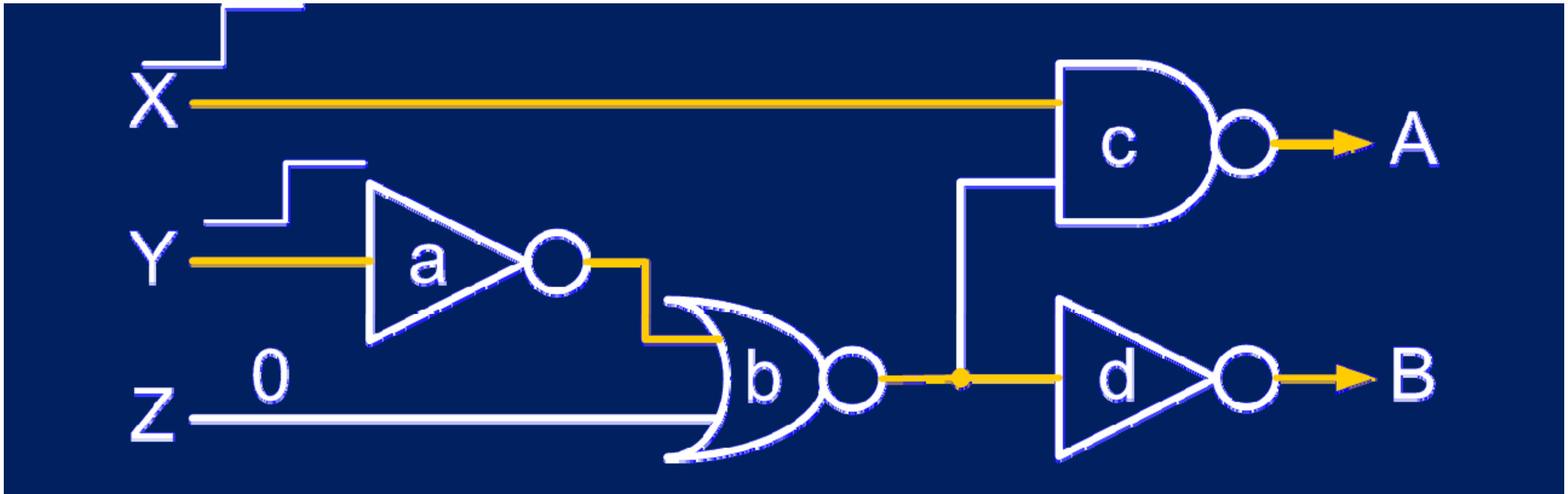

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Benchmark Results

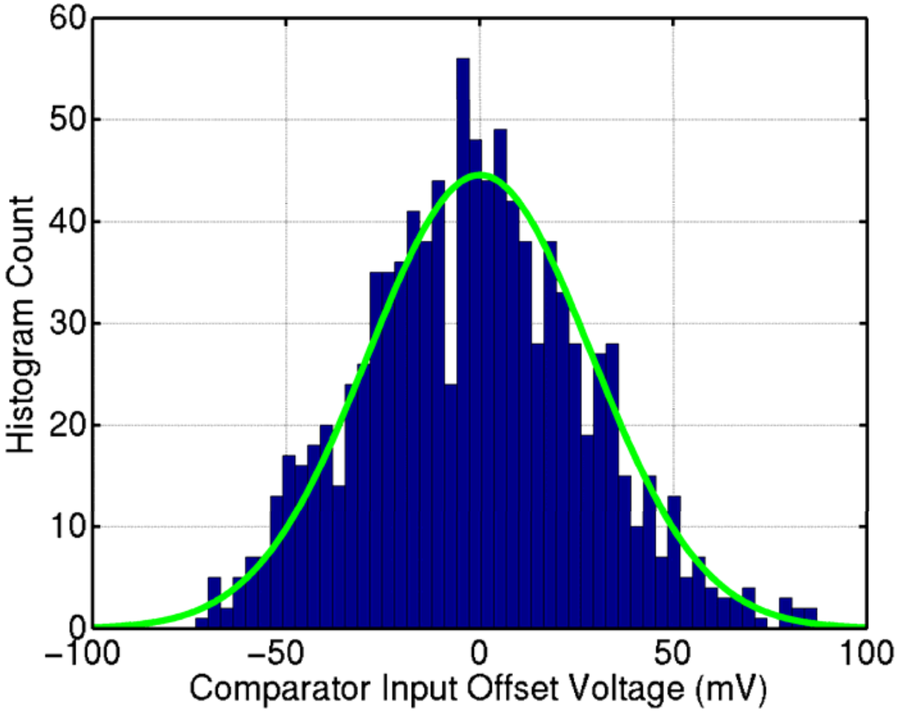
Test Case	CPU Time		Results (σ)	
	Proposed	1000-pt Monte-Carlo	Proposed	1000-pt Monte-Carlo
Comparator Input Offset	21.6 sec	24373 sec	28.741 mV	28.775 mV
Logic Path Delay	5.52 sec	1990 sec	A: 1.925 ps B: 5.518 ps	A: 2.004 ps B: 5.174 ps
5-stage Ring Oscillator	6.09 sec	652 sec	69.34 MHz	69.96 MHz

- 0.13μm CMOS, 3σ for $I_{DS} \approx 14\%$
- 3.6GHz Intel Xeon with 4GB memory

MI
CS

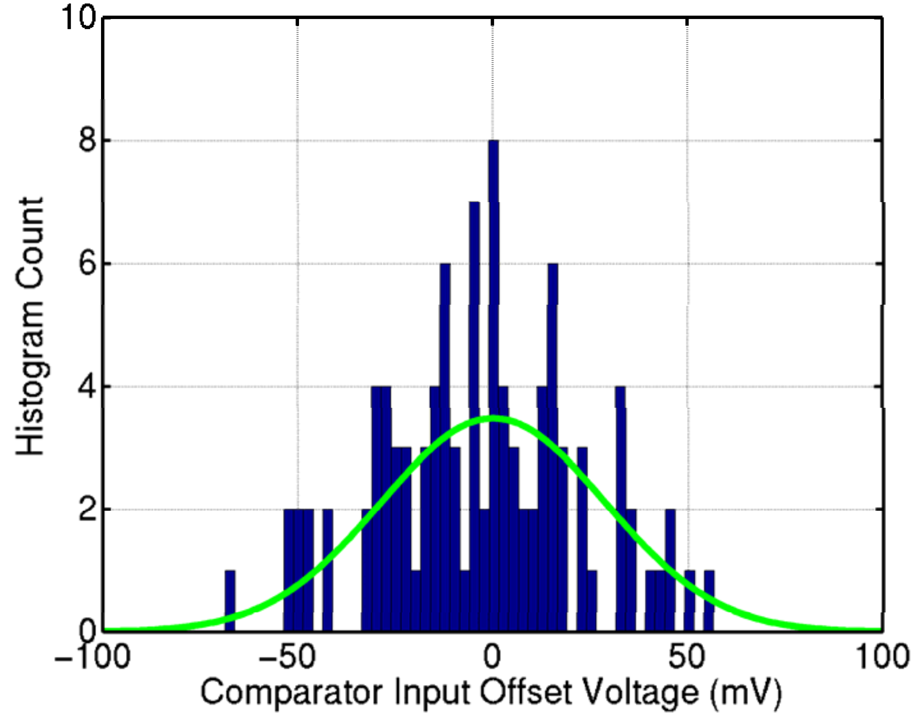
Histogram Comparison

1000-point Monte-Carlo



σ = 28.8mV

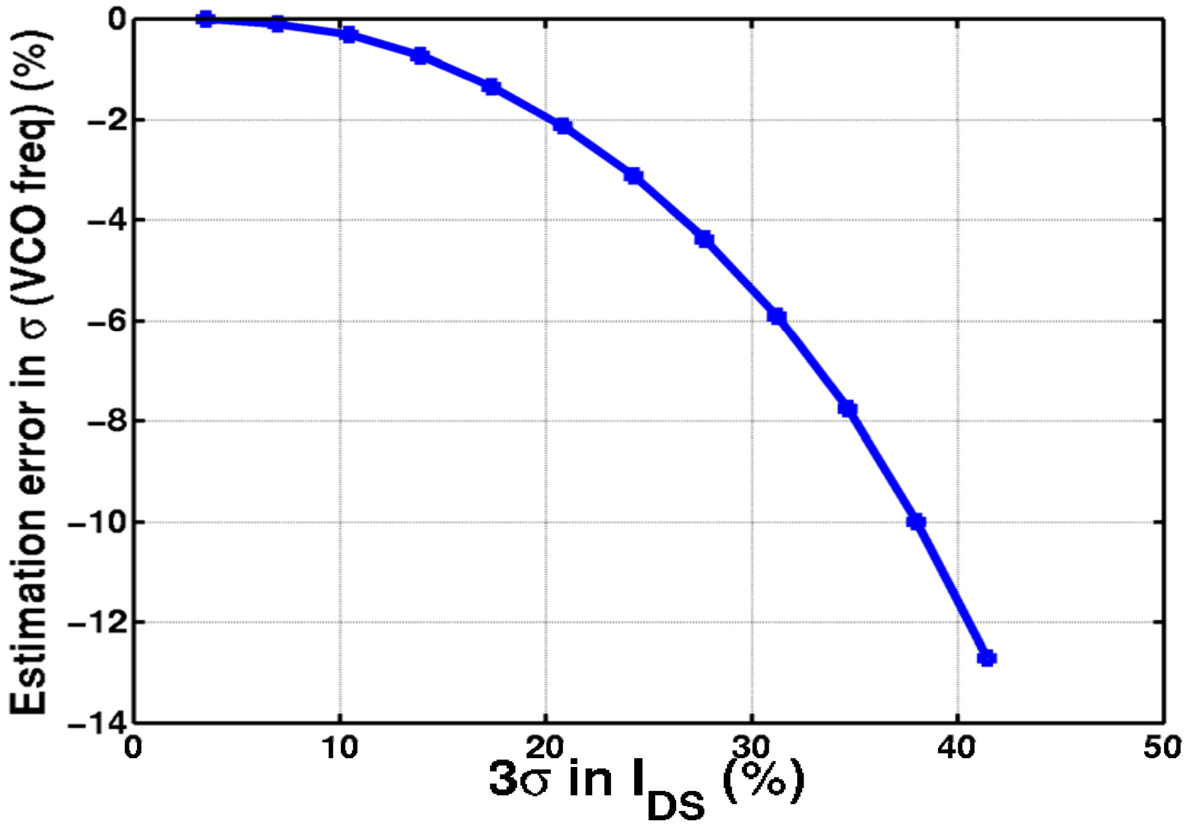
100-point Monte-Carlo



σ = 25.3mV

Limitations

- Small, Gaussian mismatches only
  - 10% error when 3σ in I_{DS} becomes 38%



Conclusions

- This work extends DCMATCH analysis to estimation of transient performance
  - Assumes small, Gaussian mismatch PDFs
- Noise-based analysis exploits efficient PSS and PNOISE algorithms
  - Compared to transient noise analysis
- Yield optimization becomes tractable