Computer Architecture

Multi-cycle Implementation

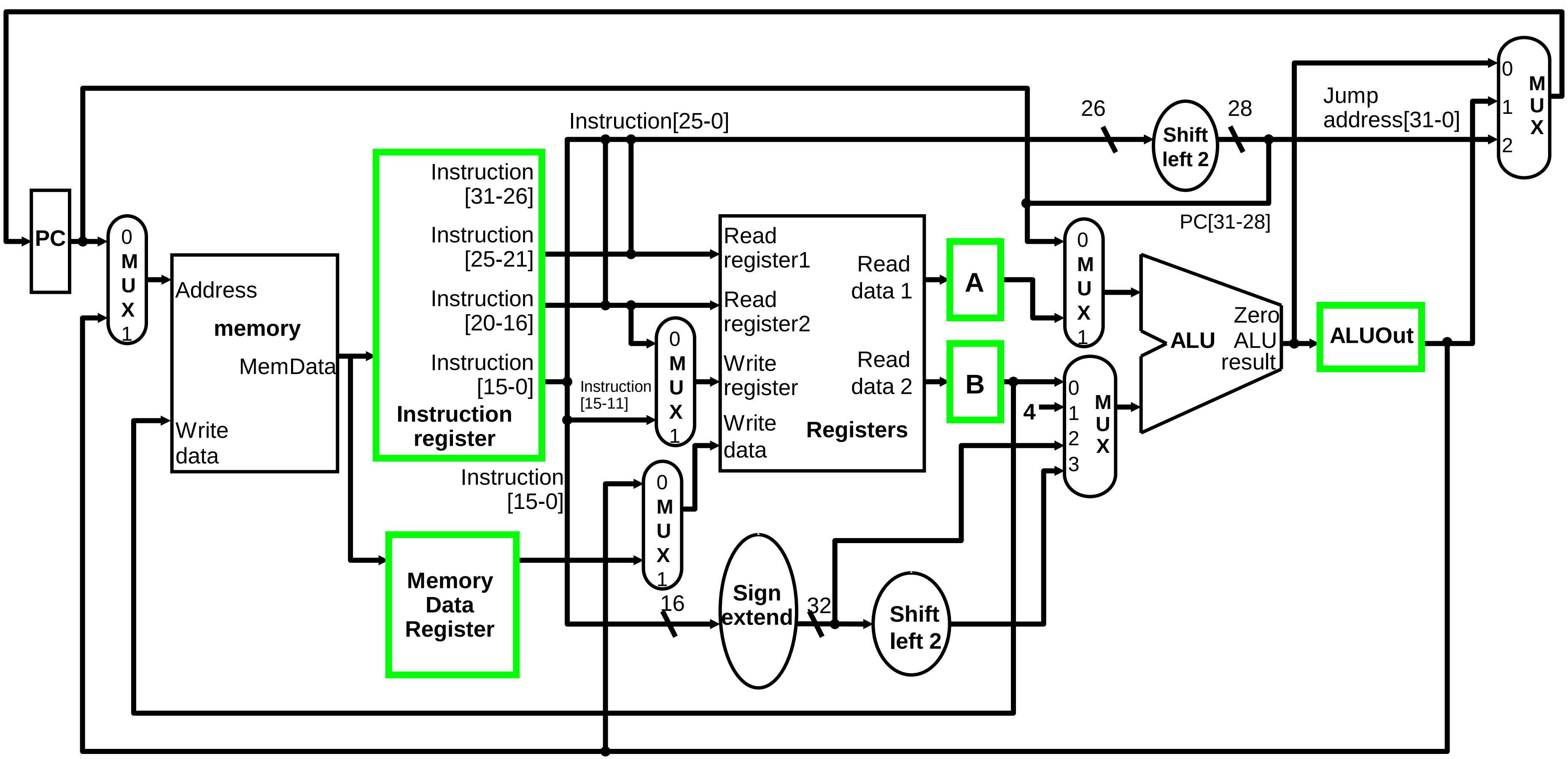
Outline

- Disadvantages of the Single-cycle implementation
  - Long cycle time, too long for all instructions except for the slowest (lw instruction)
  - Inefficient hardware utilization with unnecessarily duplicated resources
- Multi-cycle implementation
  - Partition execution into small steps
  - Process each step in one cycle
  - Different numbers of cycles for different instructions
    - Example
      - R-format instruction (4 cycles): (1) Instruction fetch (2) Instruction decode/register fetch (3) ALU operation (4) Register write
      - Load instruction (5 cycles): (1) Instruction fetch (2) Instruction decode/register fetch (3) address computation (4) memory read (5) Register write

Multiple-cycle Concept

- Reduce resource requirements by using the same resource for different purposes during different cycles
  - Single memory unit for instructions and data
  - Single ALU
- Use temporary registers to store intermediate results during execution
  - Instruction register (IR), A register, B register, ALUOut register, Memory data register (MDR)
- Partition criteria: at most one of the following operations
  - Memory access
  - Register file access
  - ALU operation

Multiple-cycle Datapath



Overview of Multi-cycle Execution

Step name	Action for R-type instructions	Action for memory-reference instructions	Action for branches	Action for jumps
Instruction fetch	IR = Memory[PC] PC = PC + 4			
Instruction decode/register fetch	A = Reg [IR[25-21]] B = Reg [IR[20-16]] ALUOut = PC + (sign-extend (IR[15-0]) << 2)			
Execution, address computation, branch/ jump completion	ALUOut = A op B	ALUOut = A + sign-extend (IR[15-0])	if (A ==B) then PC = ALUOut	PC = PC [31-28] II (IR[25-0]<<2)
Memory access or R-type completion	Reg [IR[15-11]] = ALUOut	Load: MDR = Memory[ALUOut] or Store: Memory [ALUOut] = B		
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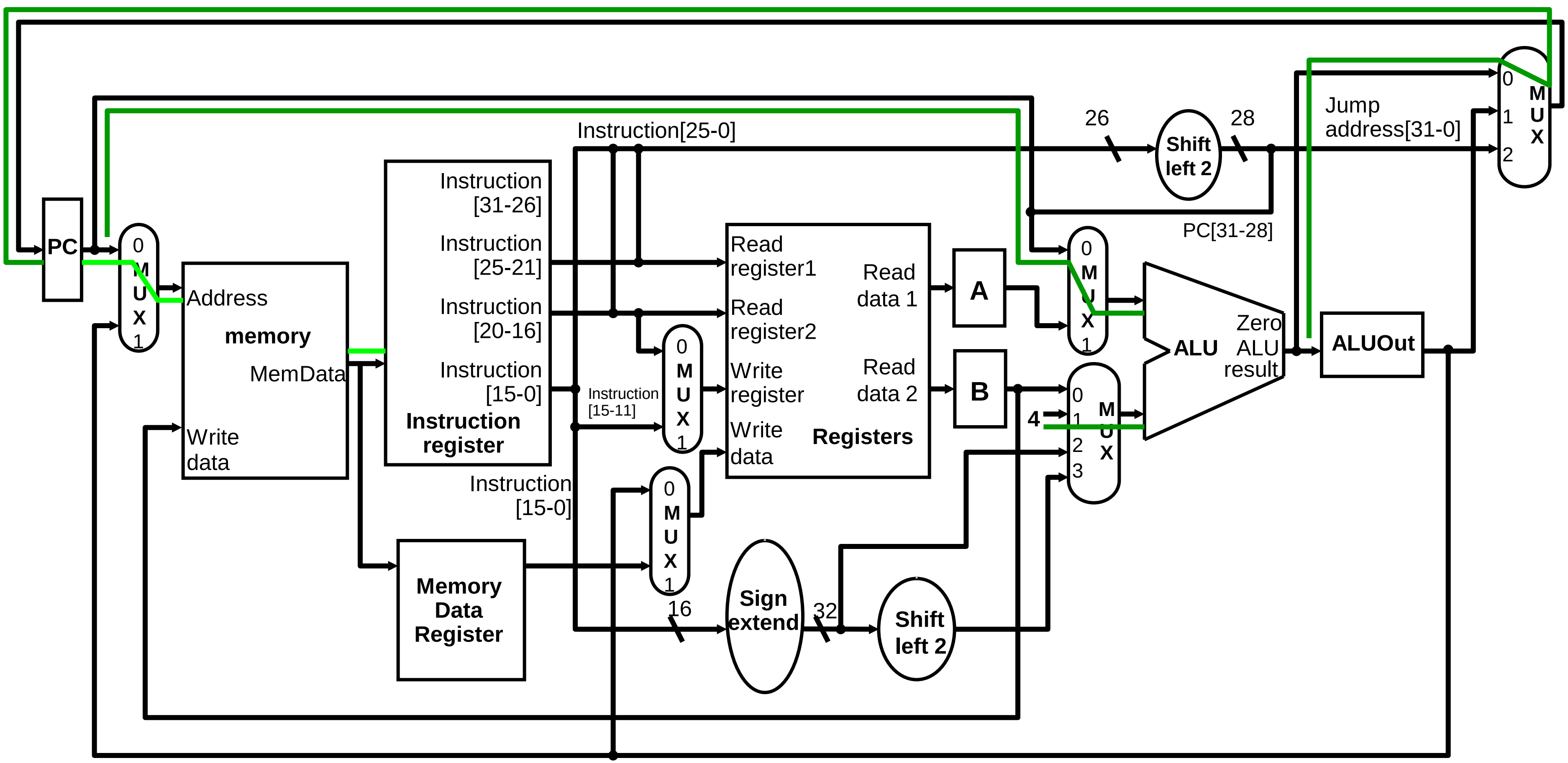

Instruction Decode/Register Fetch Step

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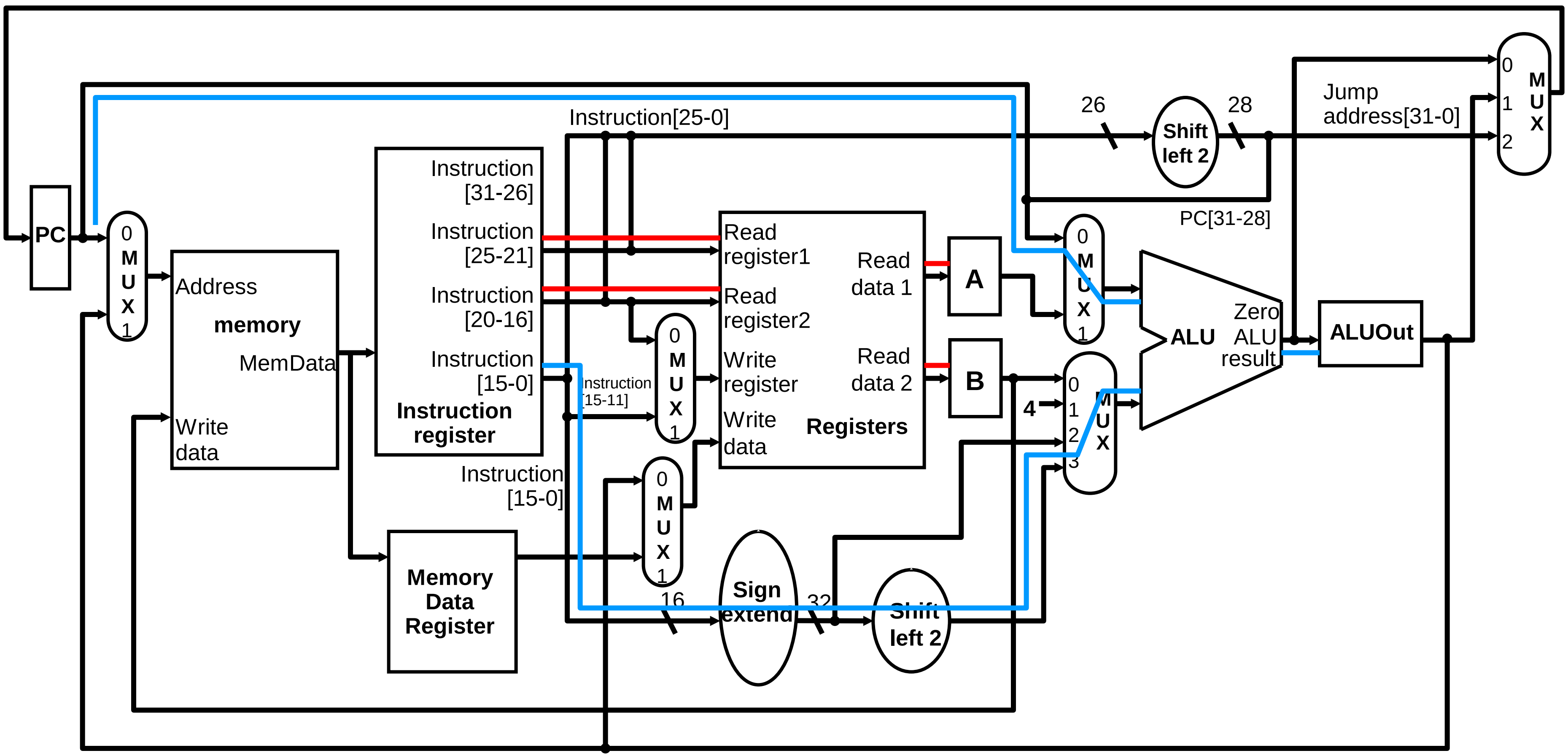

R-format Execution Step

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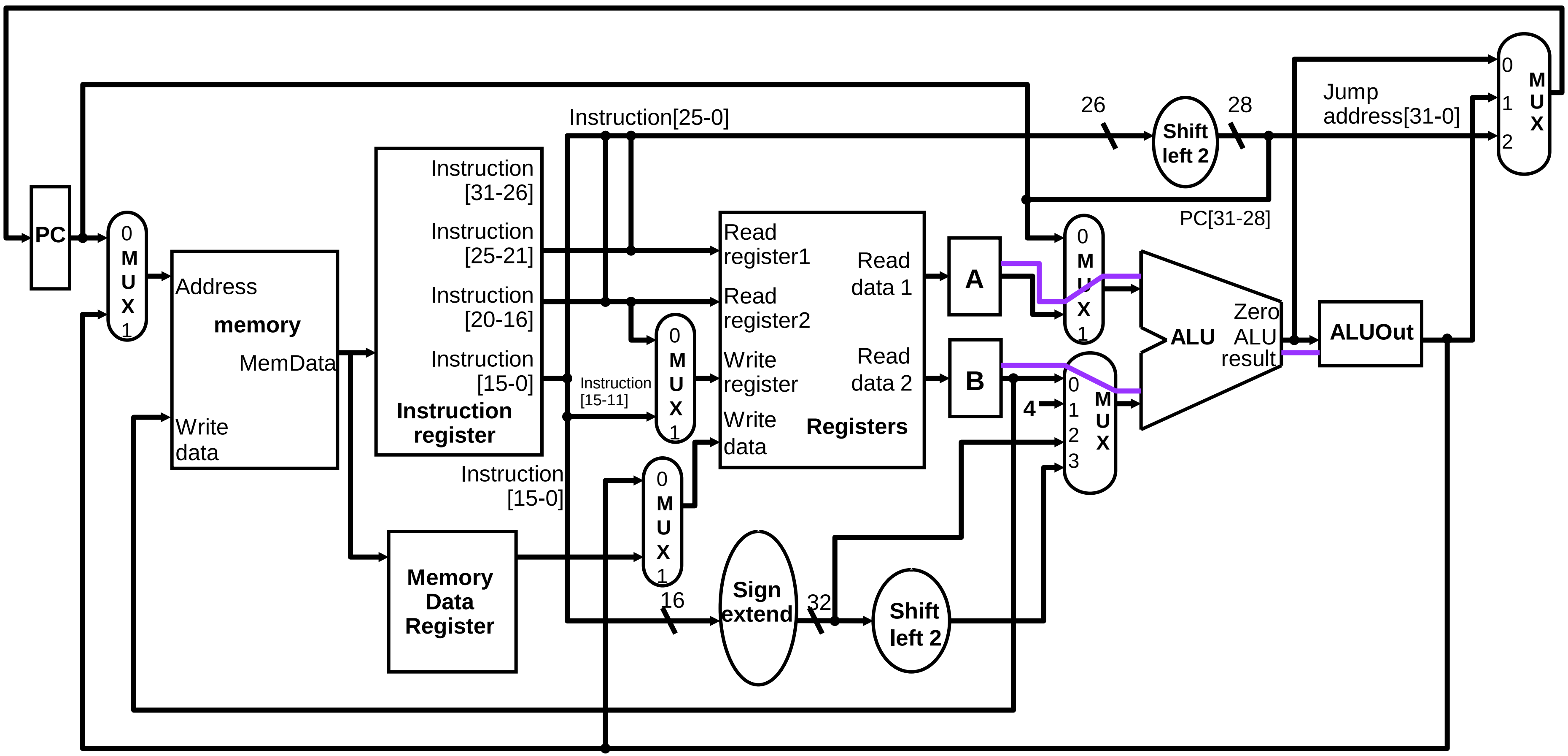

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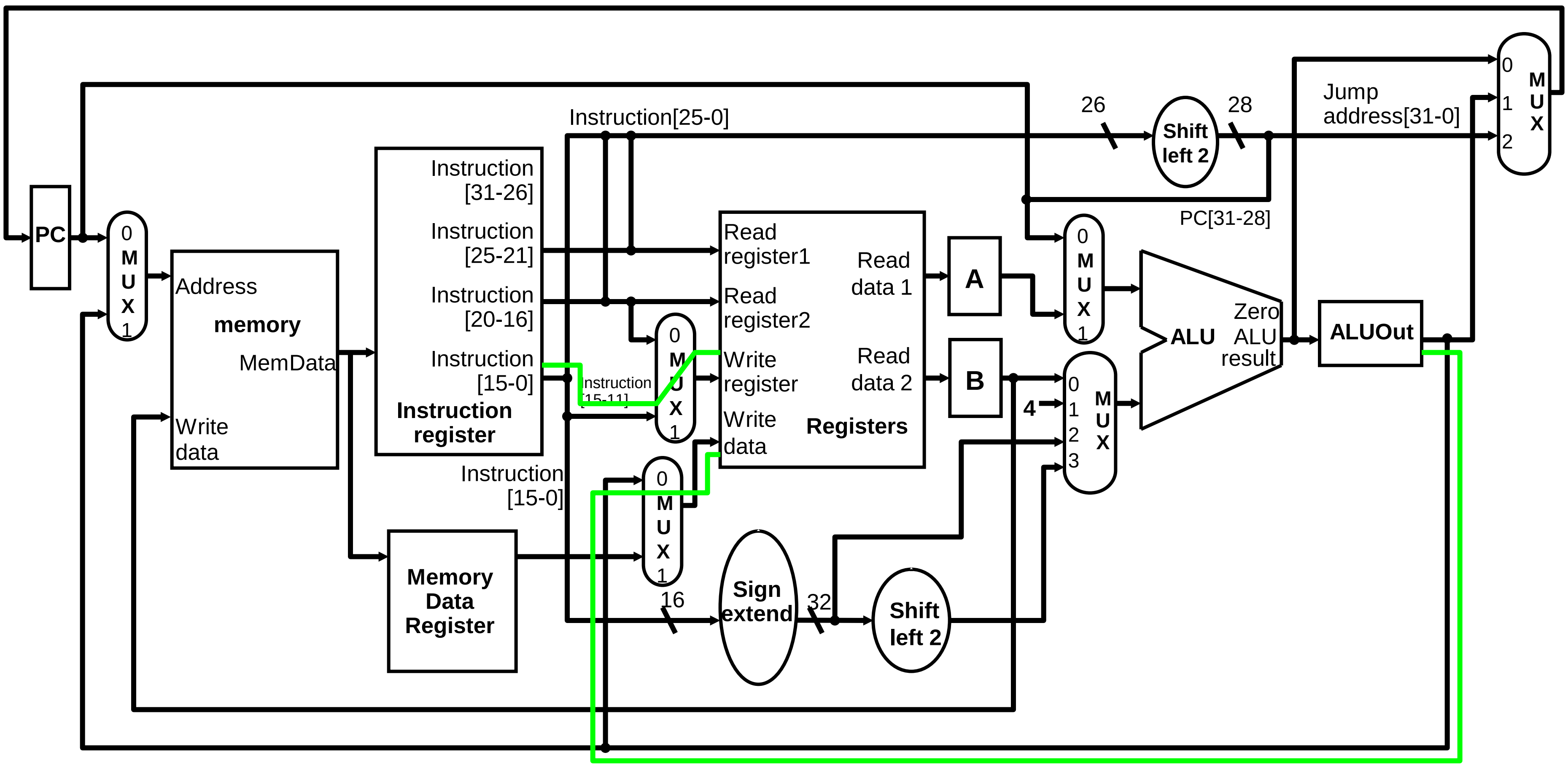

Load/Store Address Computation Step

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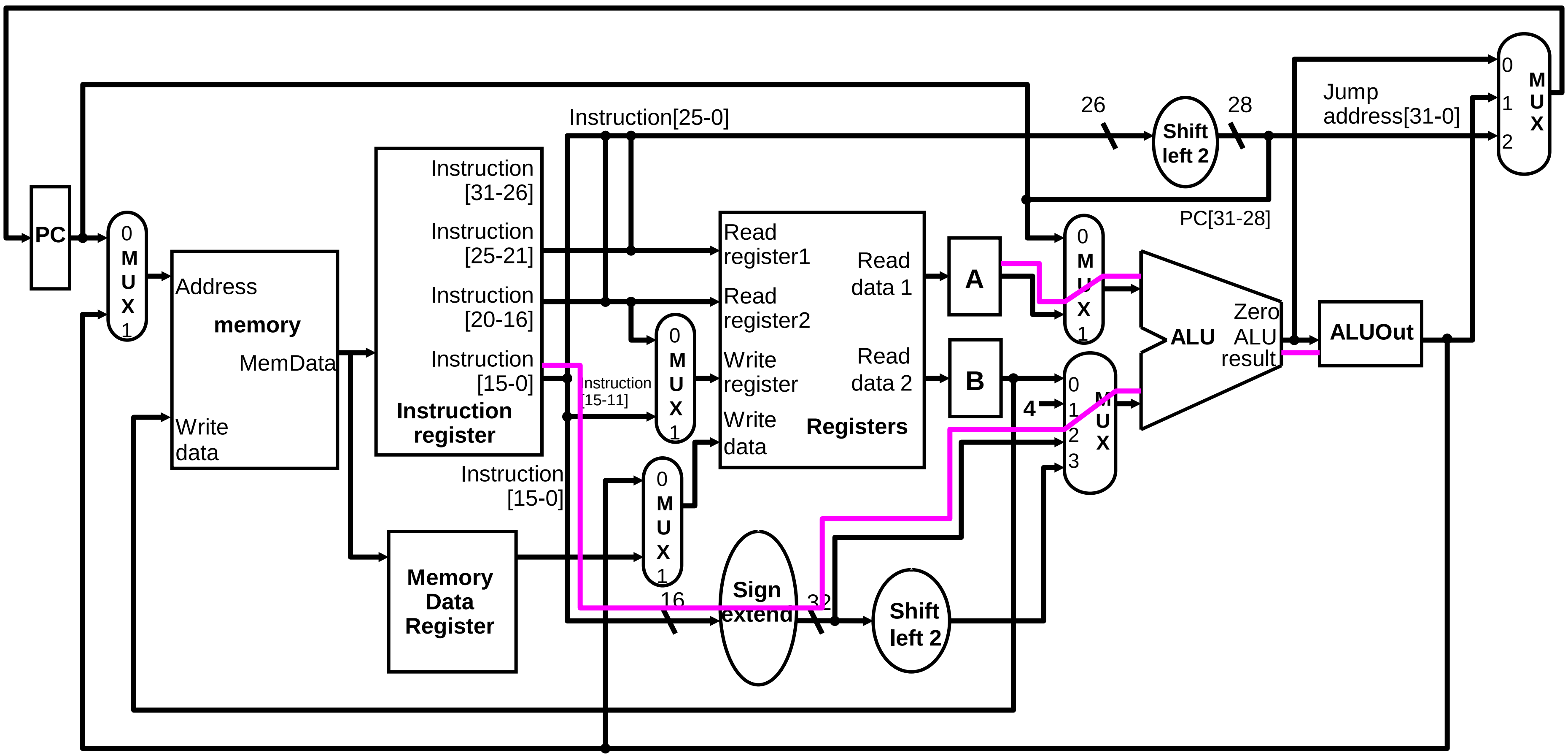

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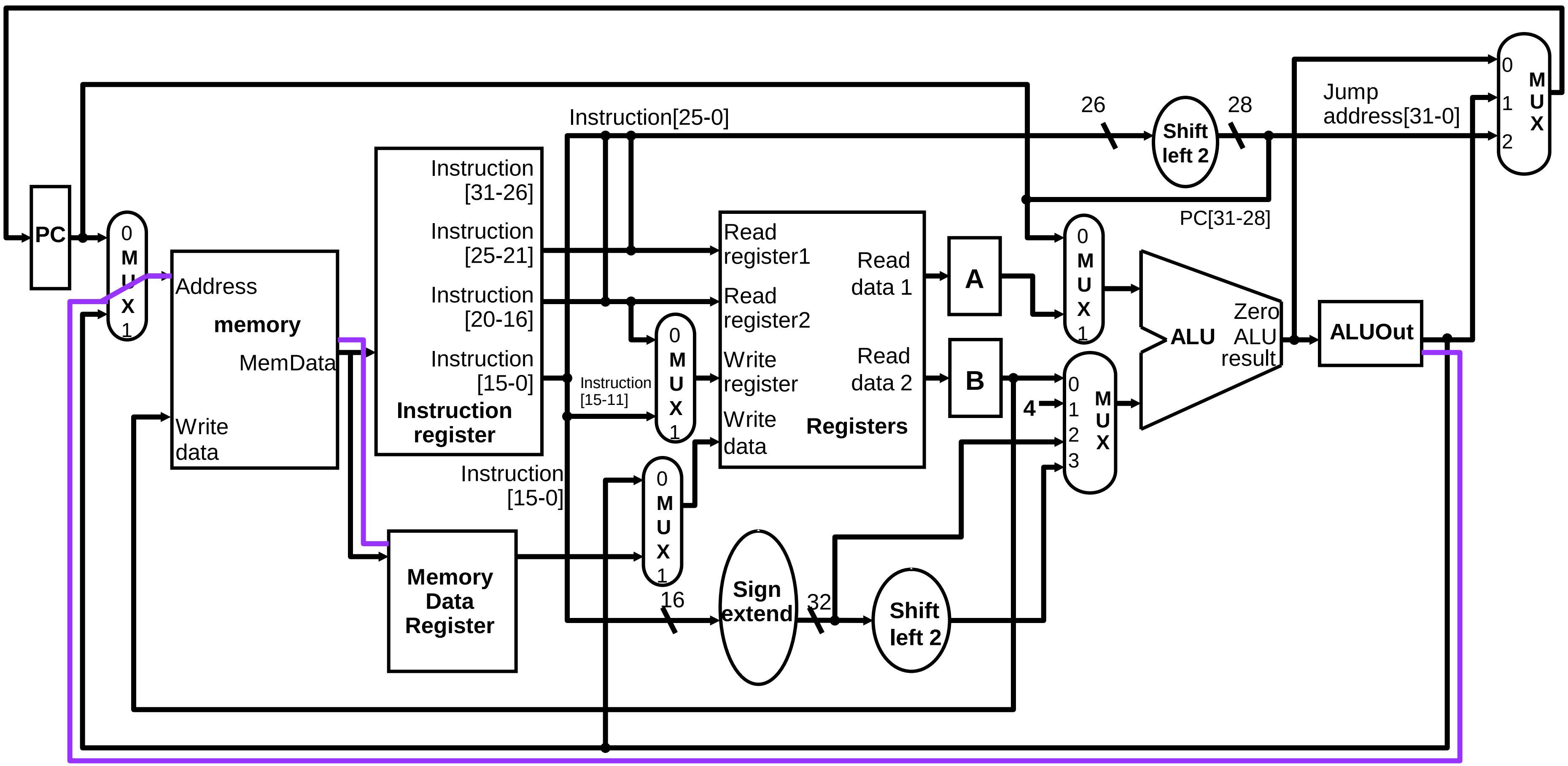

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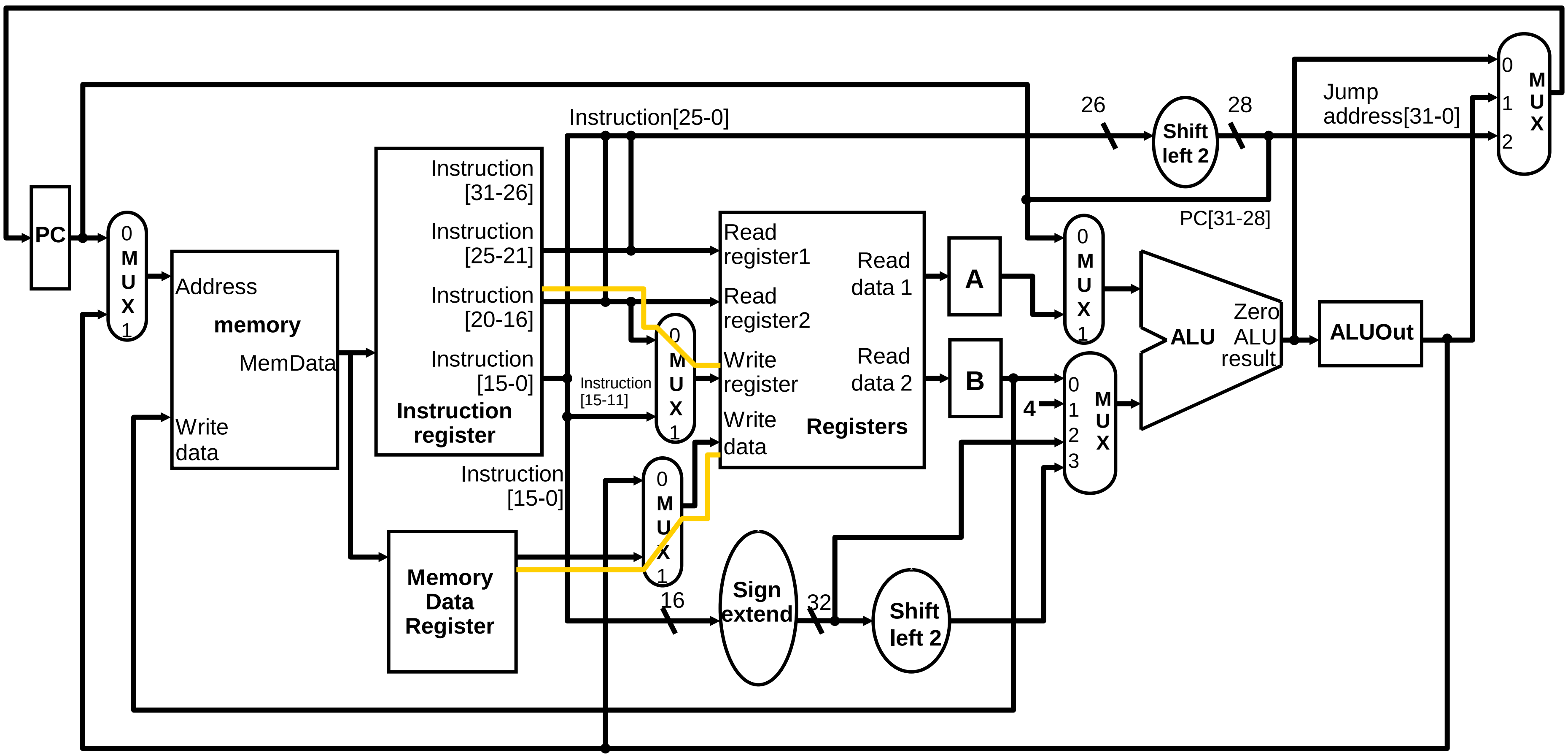
Load Completion Step



Store Memory Access Step

Step name	Action for R-type instructions	Action for memory-reference instructions	Action for branches	Action for jumps
Instruction fetch	IR = Memory[PC] PC = PC + 4			
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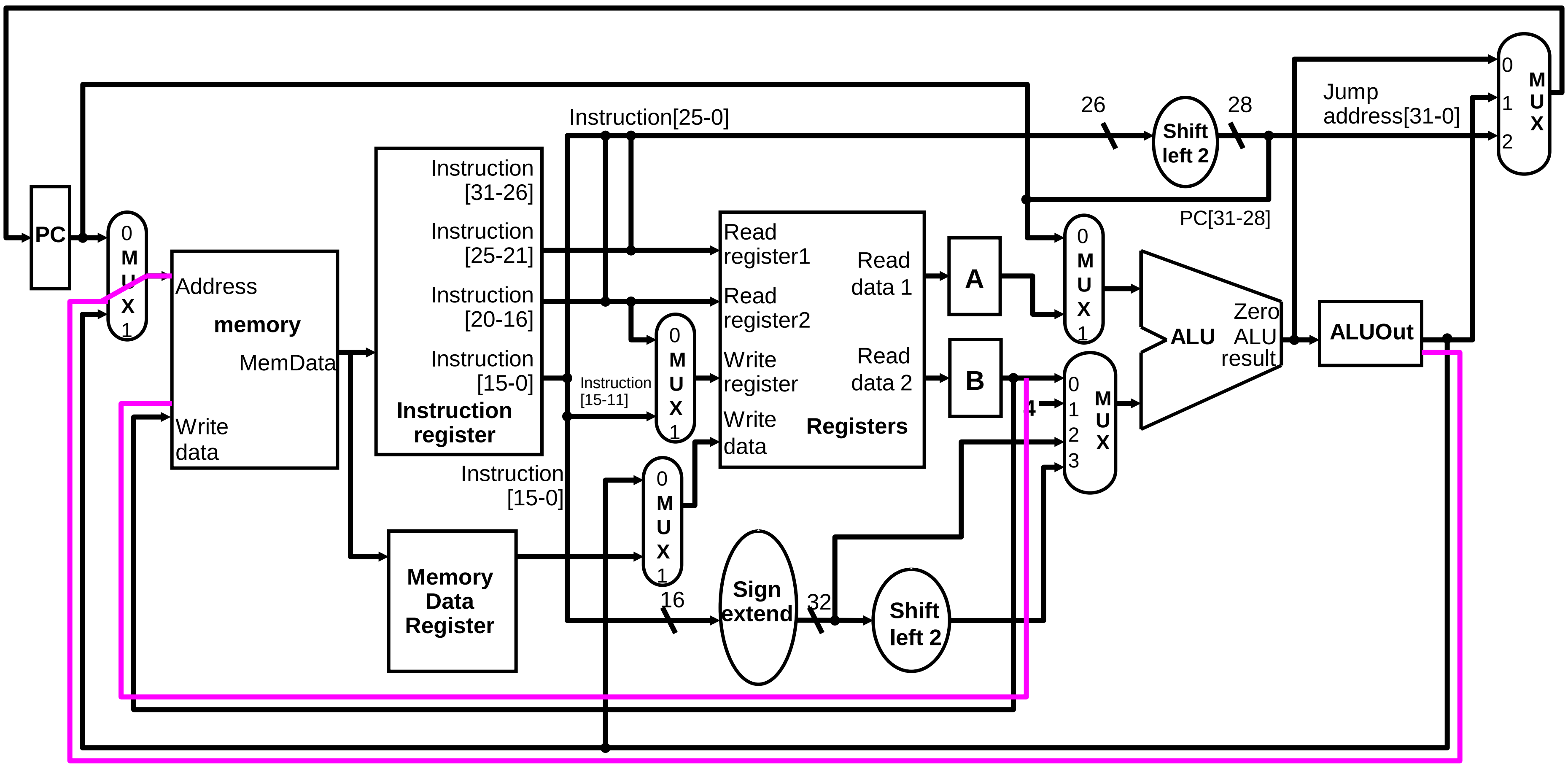
Store Memory Access Step



Branch Completion Step

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Execution, address computation, branch/ jump completion	ALUOut = A op B	ALUOut = A + sign-extend (IR[15-0])	if (A ==B) then PC = ALUOut	PC = PC [31-28] II (IR[25-0]<<2)
Memory access or R-type completion	Reg [IR[15-11]] = ALUOut	Load: MDR = Memory[ALUOut] or Store: Memory [ALUOut] = B		
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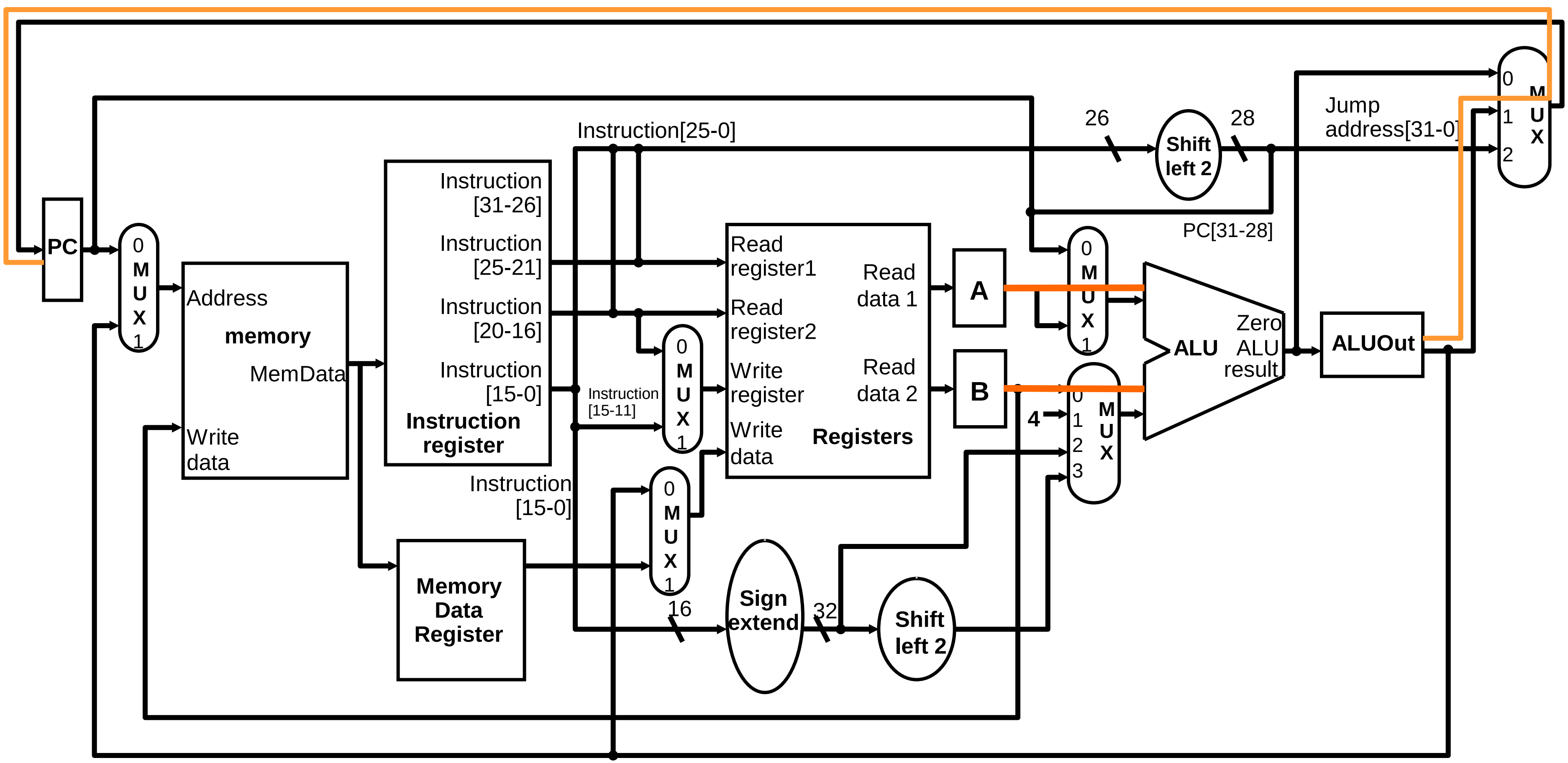
Branch Completion Step



Jump Completion Step

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Memory access or R-type completion	Reg [IR[15-11]] = ALUOut	Load: MDR = Memory[ALUOut] or Store: Memory [ALUOut] = B		
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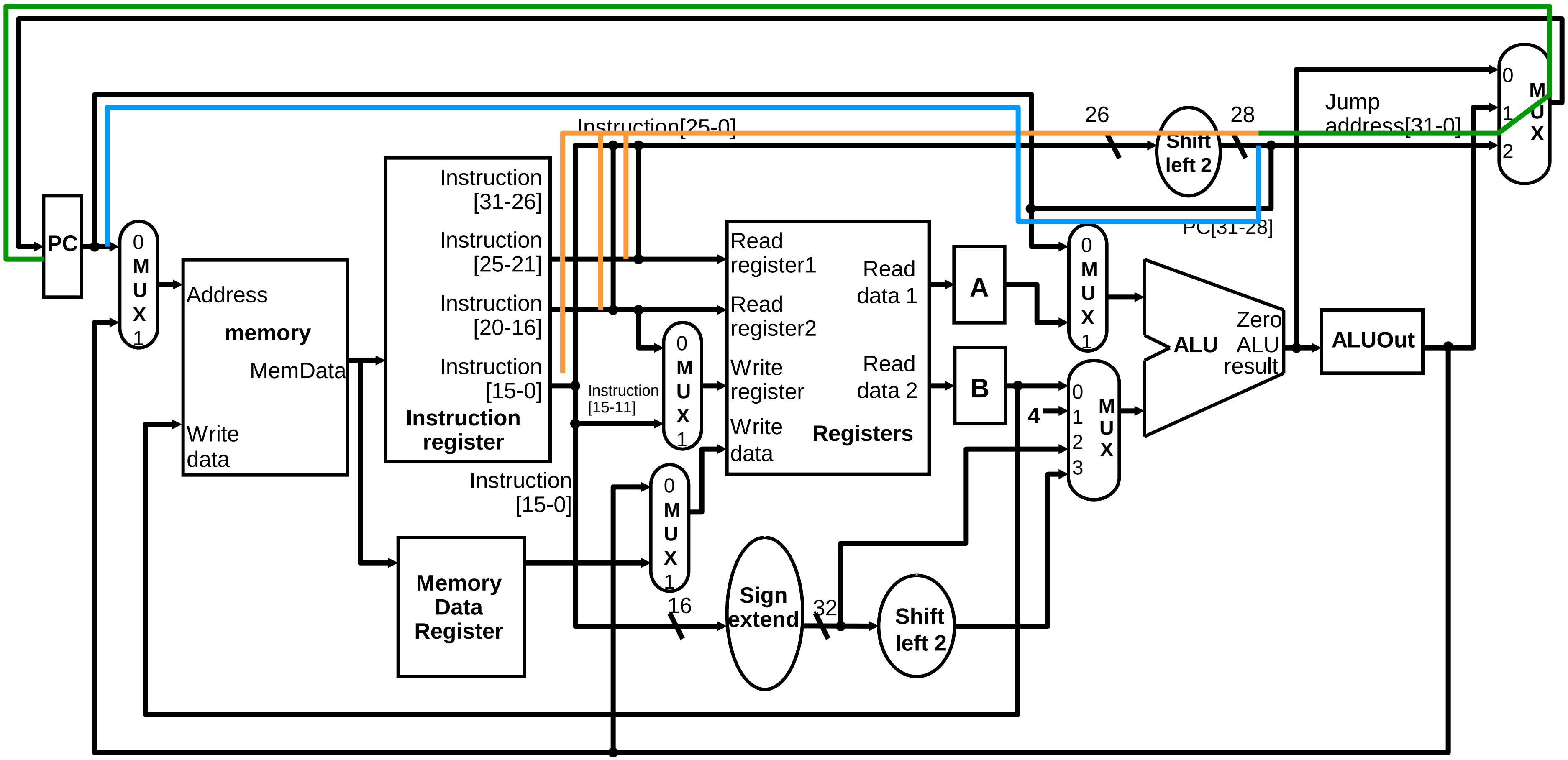
Jump Completion Step



Summary of Multi-cycle Steps

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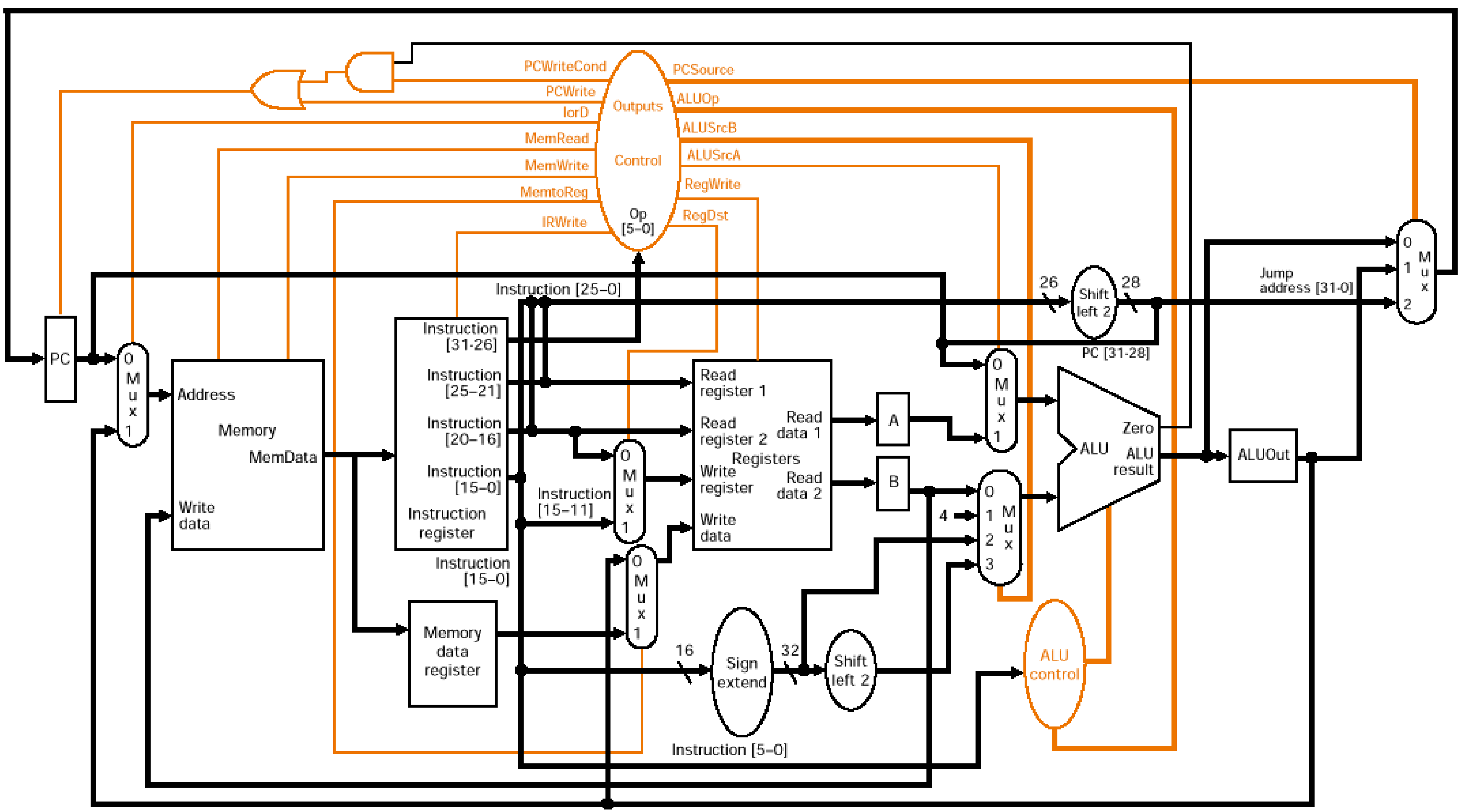
Memory read completion		Load: Reg[IR[20-16]] = MDR		

CPI of the Multi-cycle Implementation

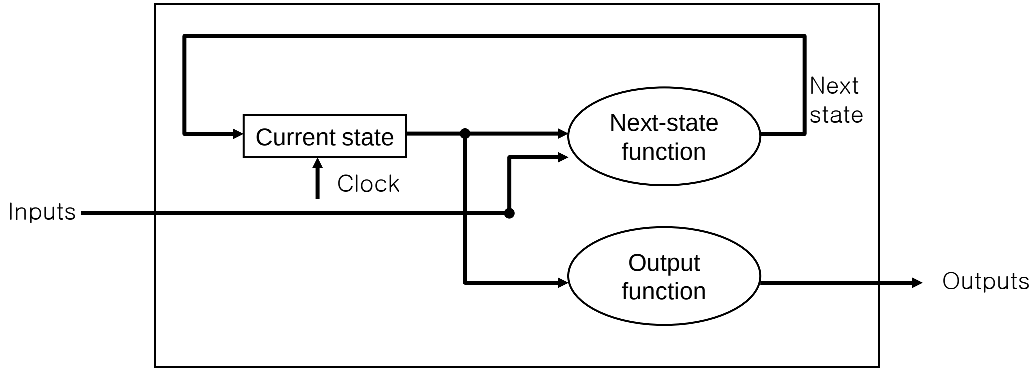
- Number of clock cycles
  - Loads : 5
  - Stores : 4
  - R-format instructions : 4
  - Branches : 3
  - Jumps : 3
- Instruction mix
  - 22% loads, 11% stores, 49% R-format instructions, 16% branches, and 2% jumps
- **CPI = 0.22 x 5 + 0.11 x 4 + 0.49 x 4 + 0.16 x 3 + 0.02 x 3 = 4.04**

Multiple-cycle Implementation (with control signals added)

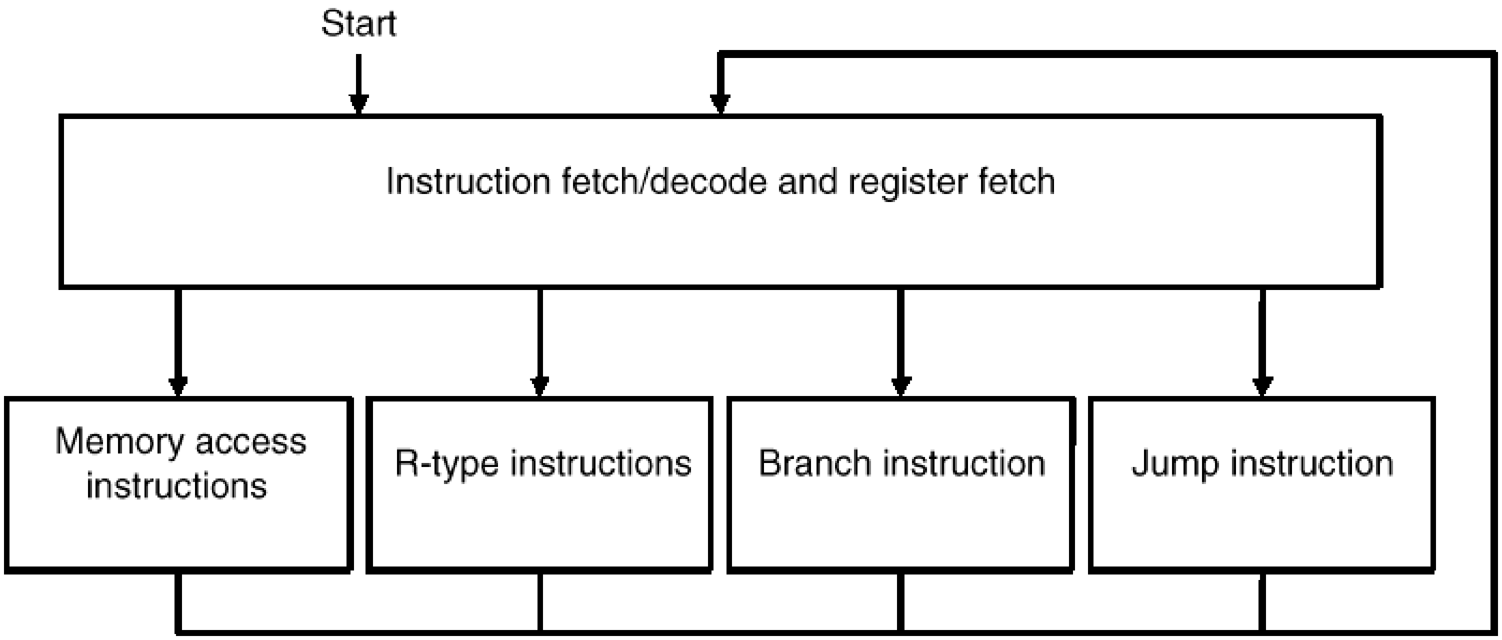


Finite State Machine

- Finite state machine
  - There are a finite set of possible machine states
  - The machine has two functions
    - next state function dependent on current state and input values
    - output function dependent on current state and input values
  - Two kinds of state machines
    - Moore machine has output based only on current state
    - Mealy machine has output based on current state and input values
    - We use a Moore machine

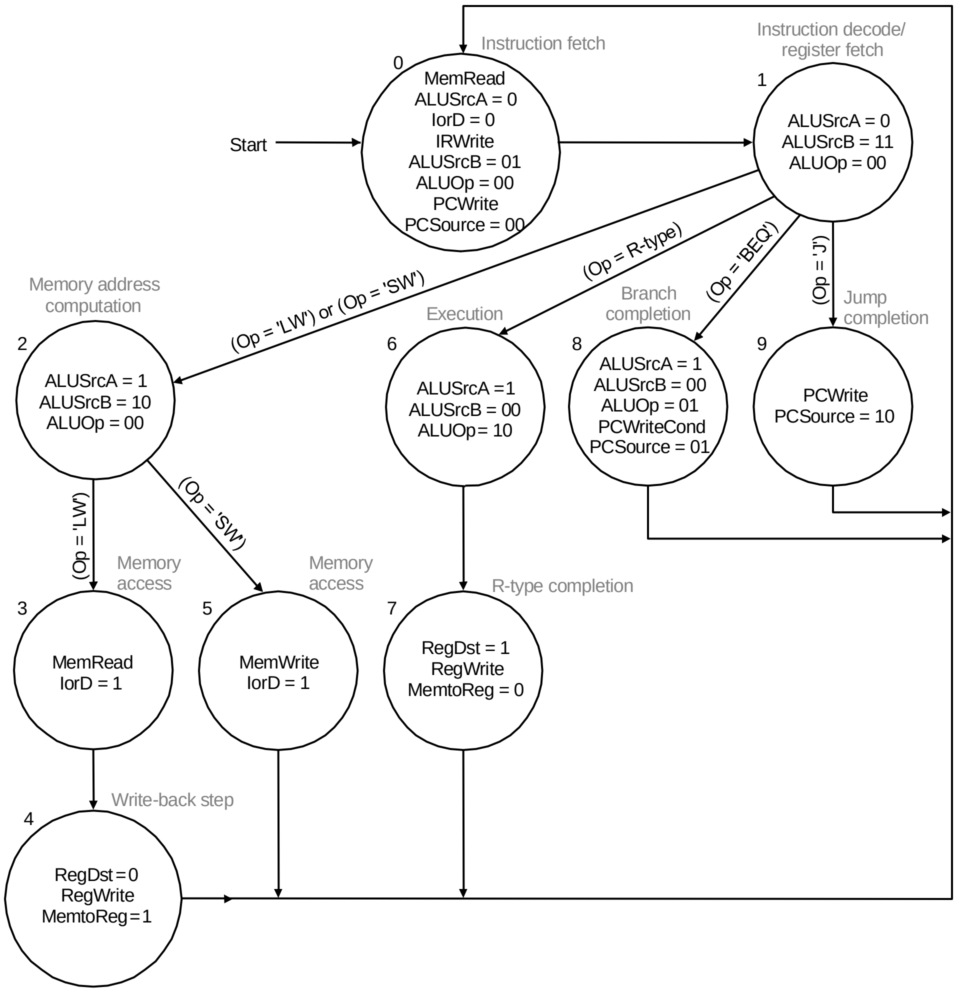


High-Level Control Flow

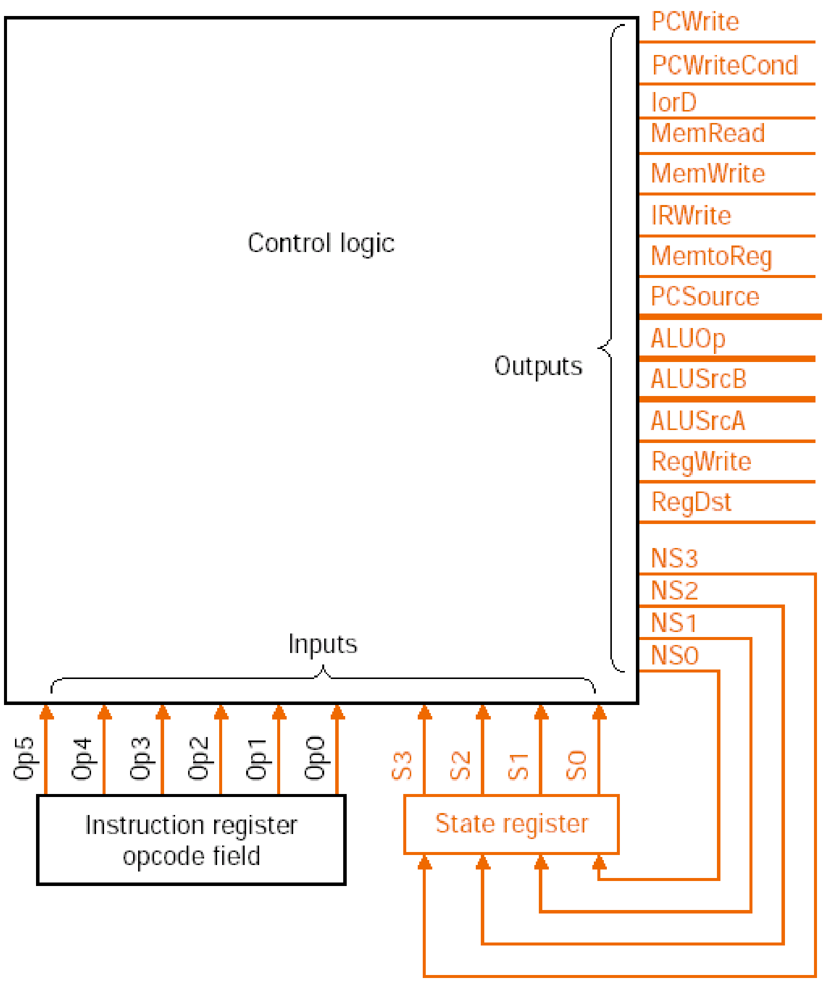


- Common 2-clock sequence to fetch/decode any instruction
- Separate sequence of 1 to 3 clocks to execute specific types of instruction

Finite State Machine Diagram

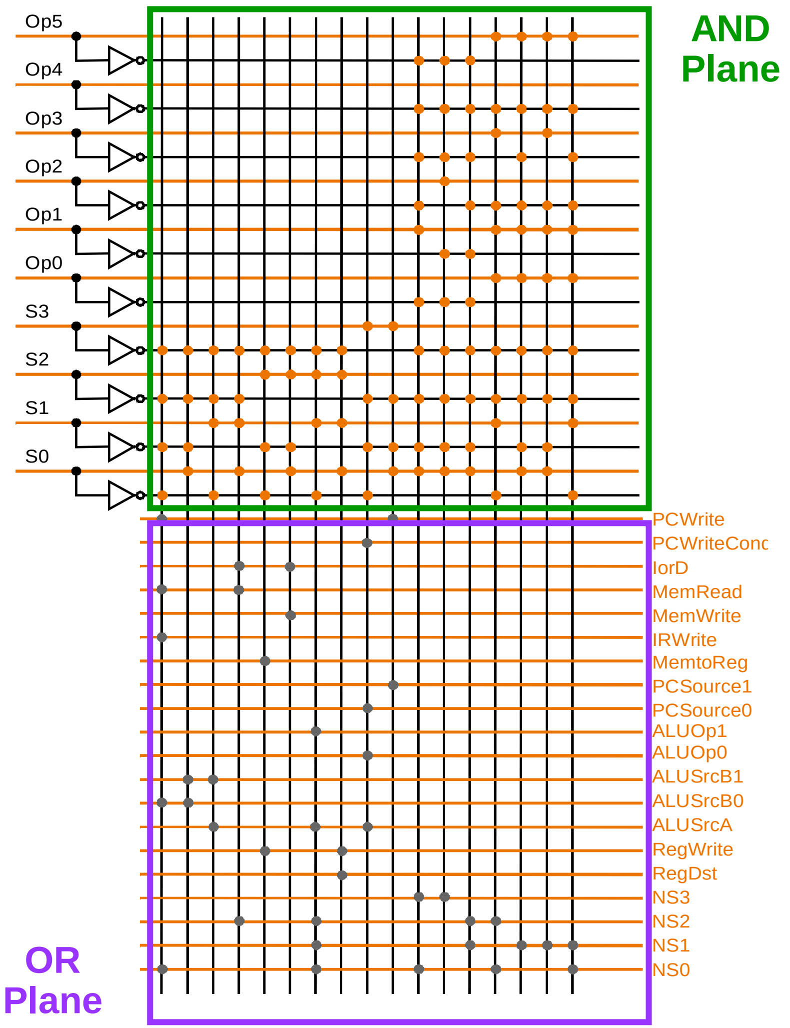


Finite State Machine Controller



PLA Implementation

- Outputs and next state are calculated by sum of products of inputs and current state
- Columns in AND plane form products
  - one column per unique product term
- Rows in OR plane form sum
- Programmed by placing transistors at intersection of row and column according to logic function
- When the inputs are fully decoded (2^N columns), a PLA is logically equivalent to a ROM
- Optimization can be automated



Exceptions and Interrupts

- Exception: an unexpected event from within the processor that traps into an operating system service routine
  - Arithmetic overflow
  - Undefined instruction
  - System call
- Interrupt: an event that comes from outside of the processor that also traps into an operating system service routine
  - I/O device request (I/O completion)
- Handling of exceptions and interrupts in MIPS
  - Saves PC (the address of the offending instruction) in EPC (exception program counter)
  - Records the reason for the exception or interrupt in the CAUSE register
  - Jumps to the operating system service routine
  - rfe (return from exception) instruction restores the PC from EPC

Summary

- Disadvantages of the Single-cycle implementation
  - Long cycle time, too long for all instructions except for the slowest
  - Inefficient hardware utilization with unnecessarily duplicated resources
- Multiple-cycle implementation
  - Partition execution into small steps of comparable duration
  - Process each step in one cycle
- Three general forms of control implementation
  - Random logic
  - PLA
  - Microcode