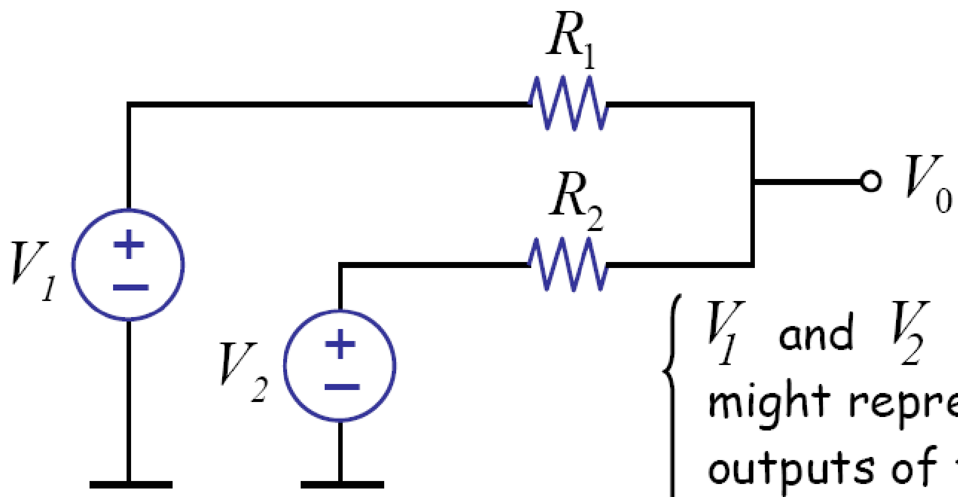
Chap. 5 The Digital Abstraction

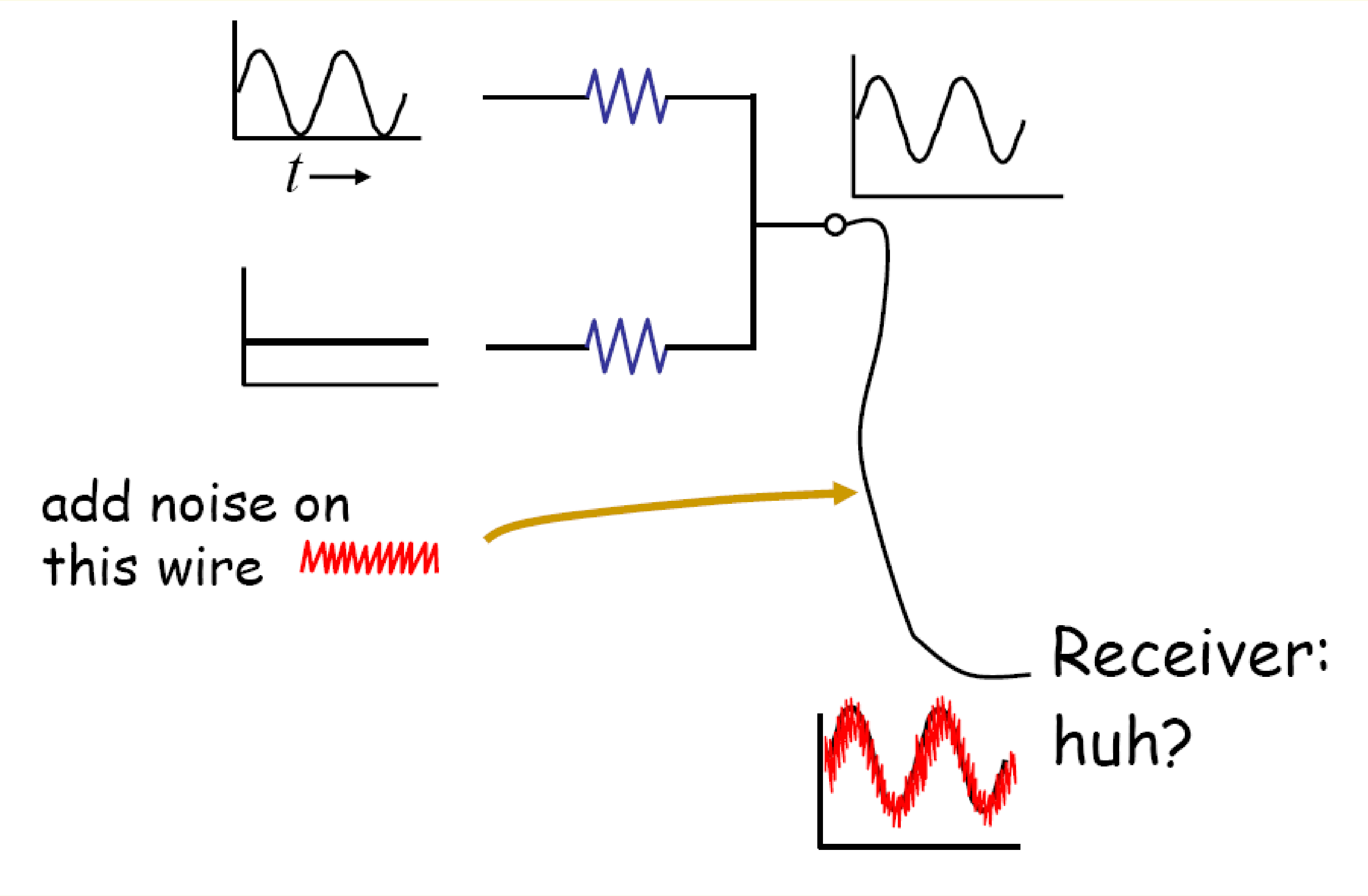
Voltage Levels and the Static Discipline

Analog Signal Processing

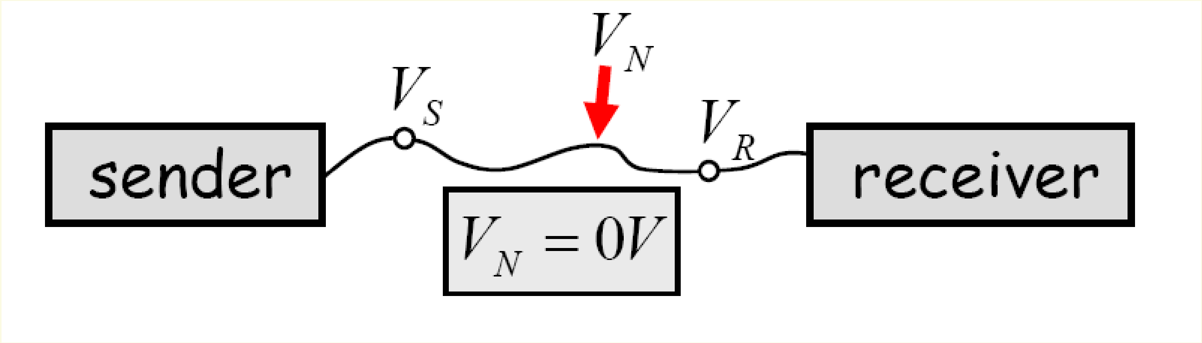


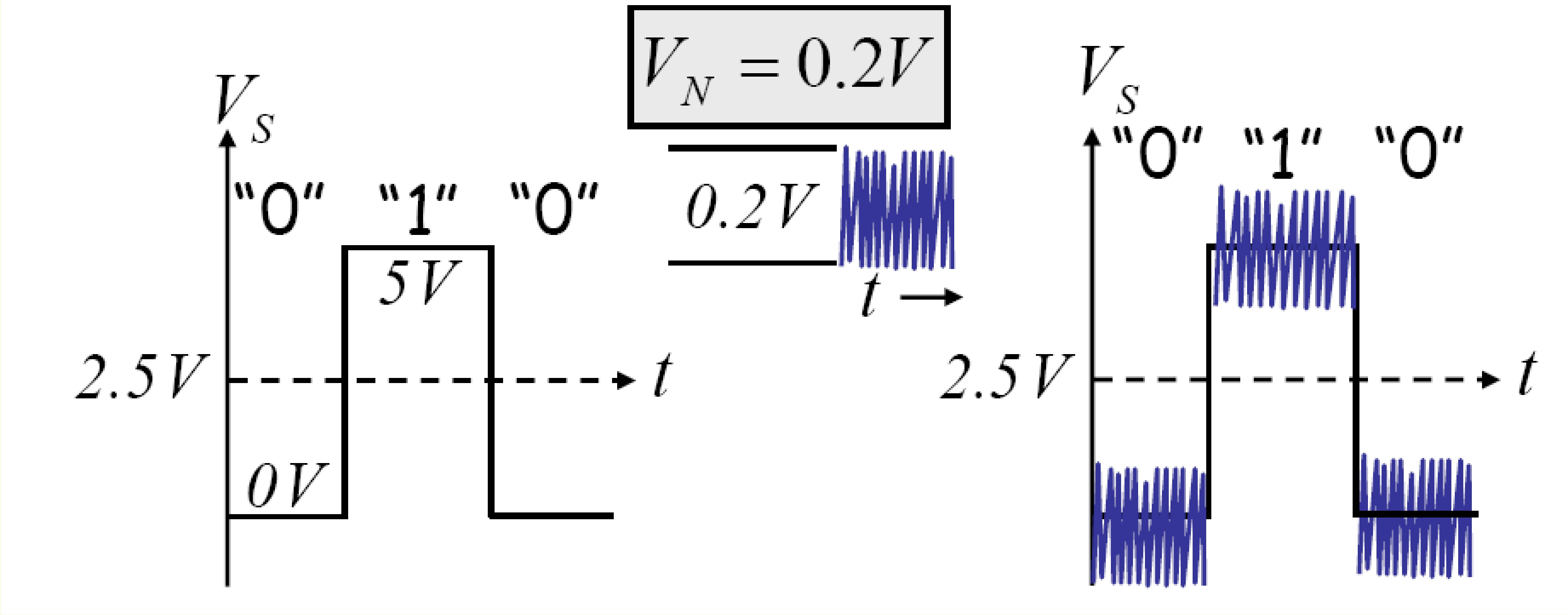
V_1 and V_2 might represent the outputs of two sensors, for example.

Noise Problem

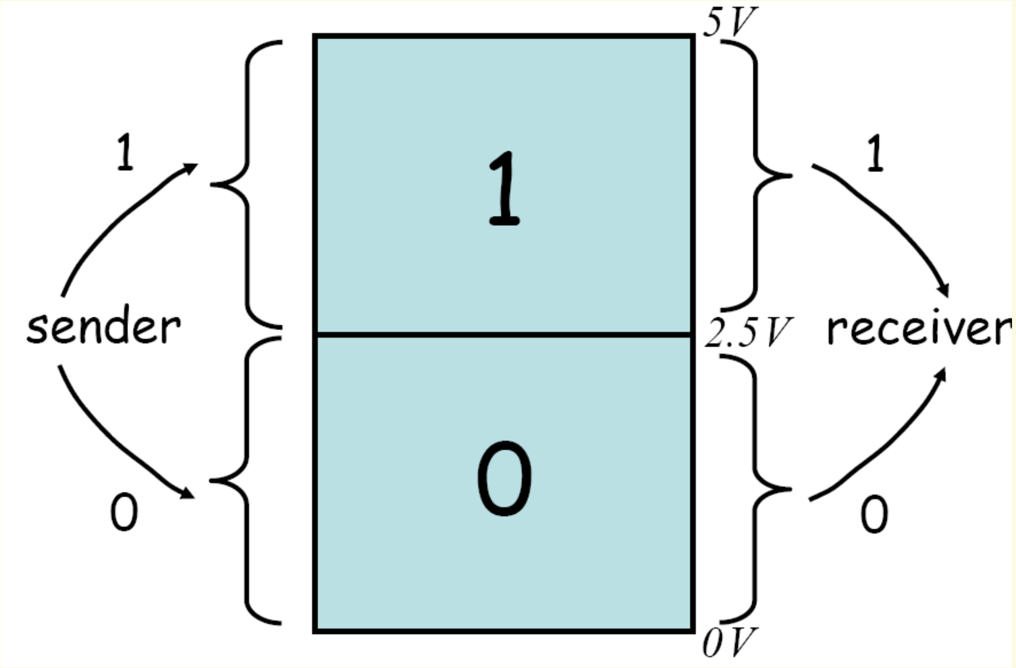


Digital System: Noise immunity !!



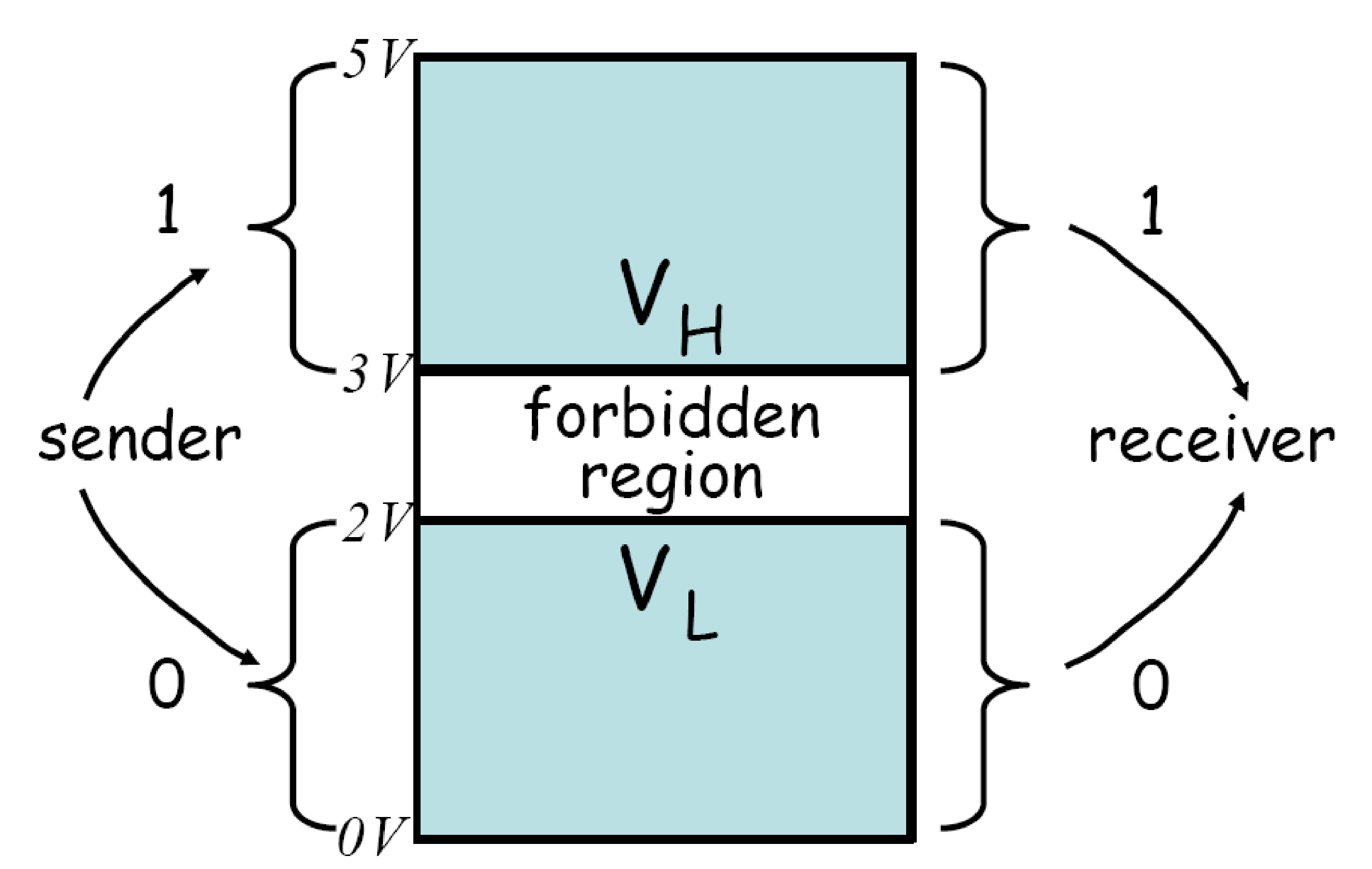


Value Discretization



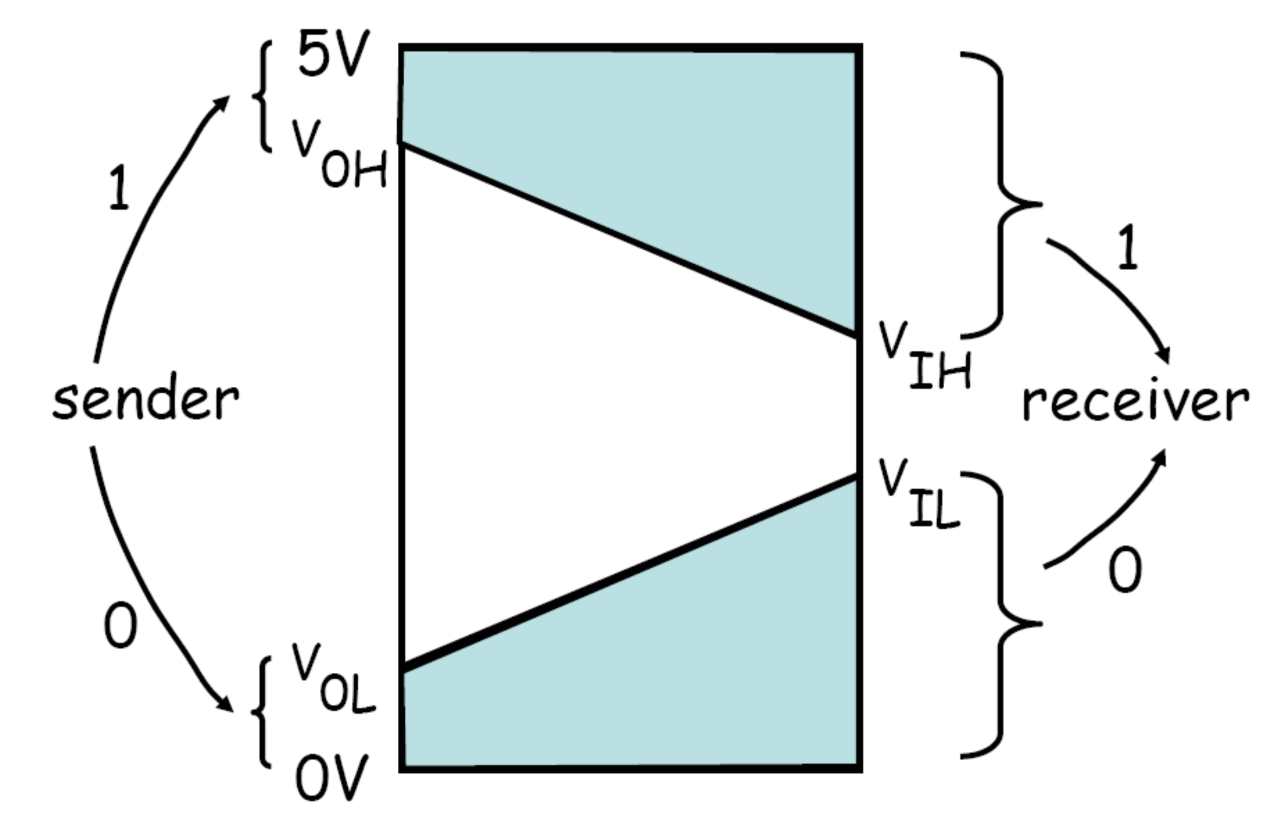
- What about 2.5 V ?

Forbidden Region



- Where is the noise margin?

Actual Value Discretization



- Noise margin

$$NM_0 = V_{IL} - V_{OL}$$

$$NM_1 = V_{OH} - V_{IH}$$

Static Discipline

- If inputs to a digital system meet valid input thresholds, the system guarantees that its outputs will meet valid output thresholds.

Conclusion

- Value discretization
- Noise margin
- Static discipline

Chap. 6 The MOSFET Switches

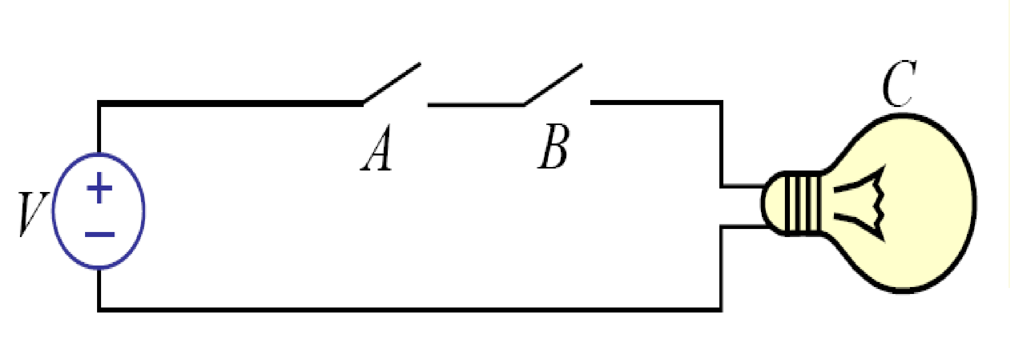
MOSFET and Switch(S) Model

Static Analysis Using S Model

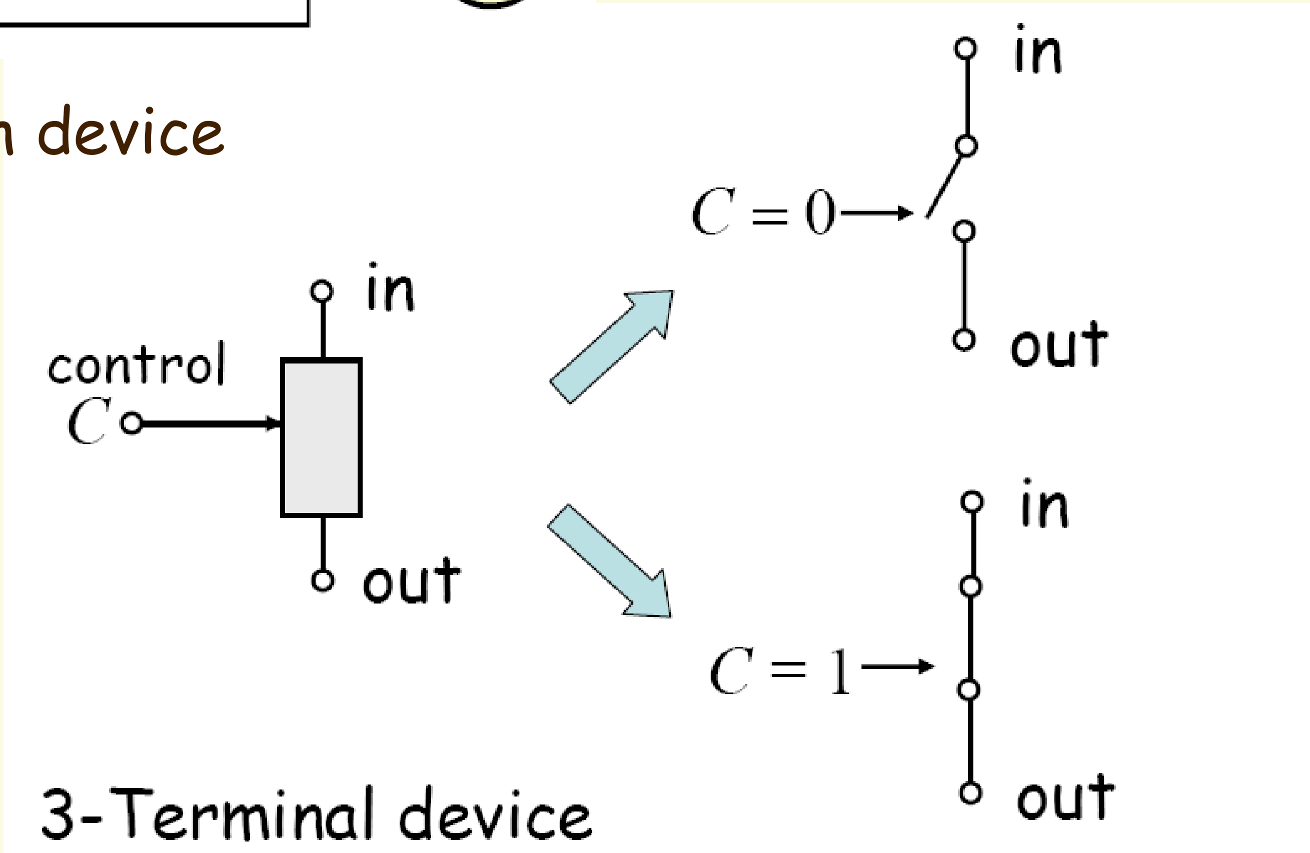
SR Model of MOSFET

Static Analysis

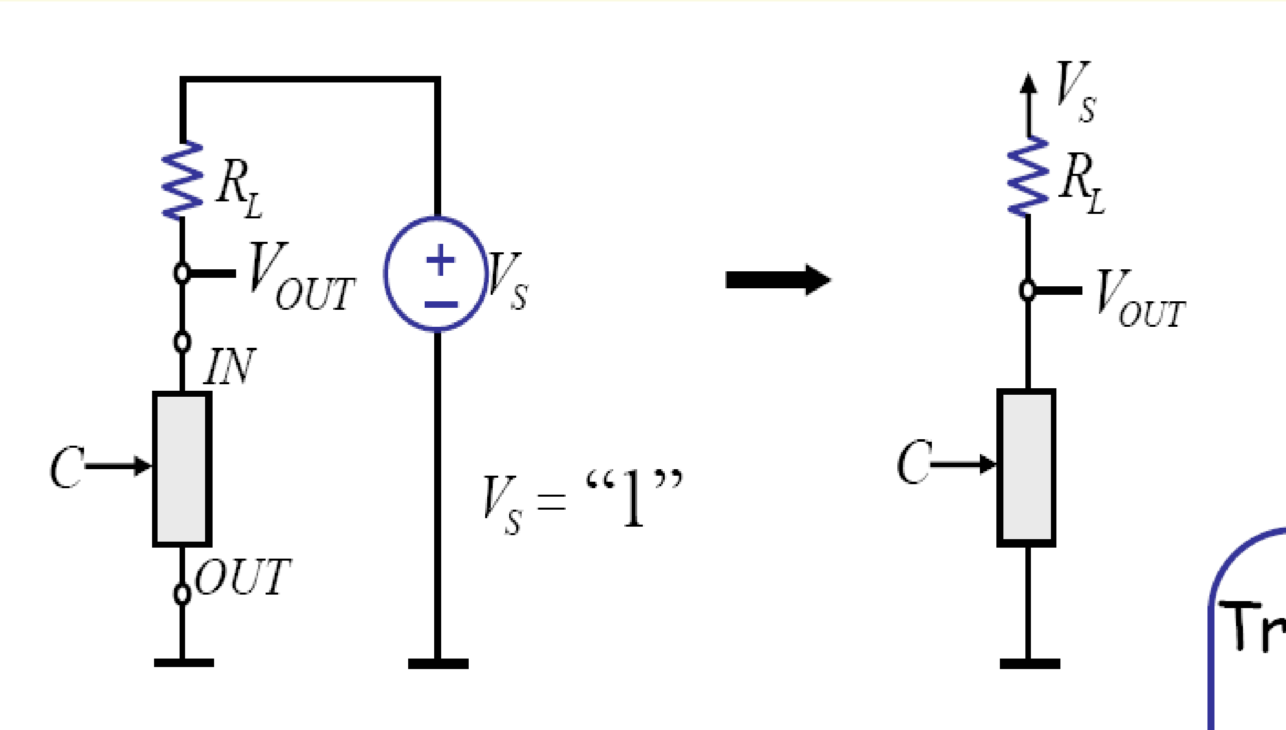
Switch Logic



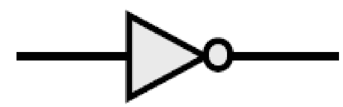
- Key: switch device



Logic Inverter



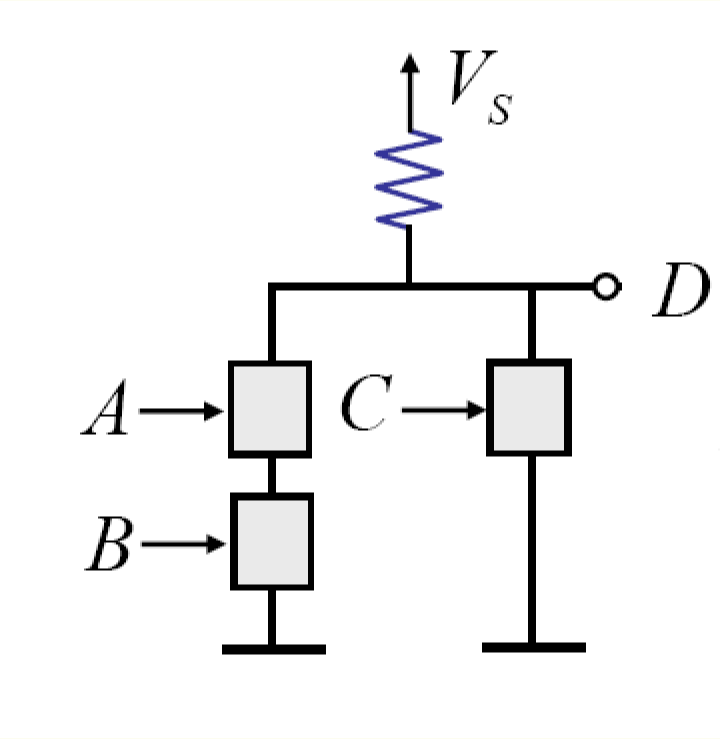
Truth table for



C	V_{OUT}
0	1
1	0

Example

- 1. Find the logic of this circuit.

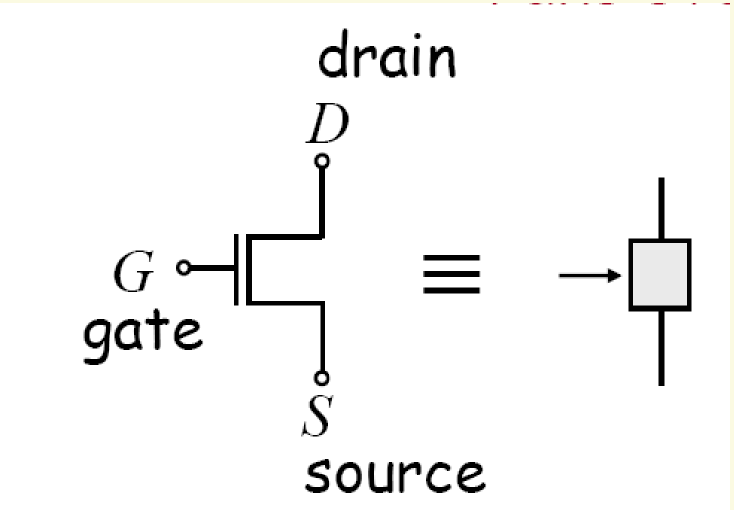


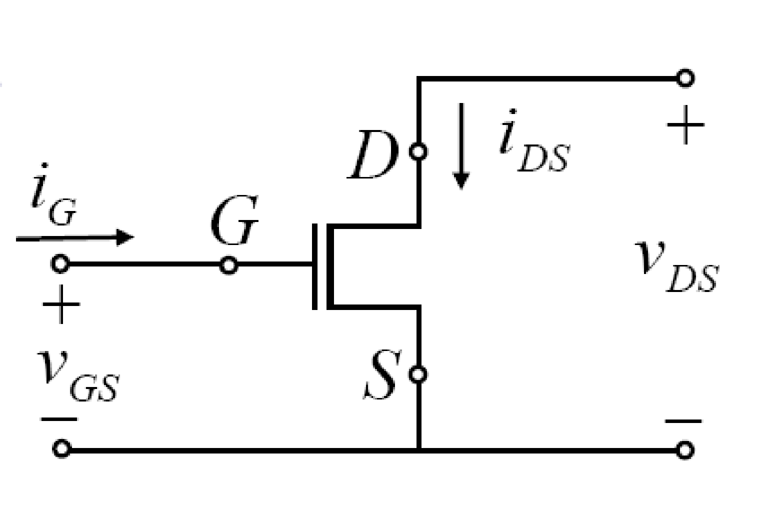
- 2. Draw the following logic circuit:

$$Y = \overline{A(B+C)}$$

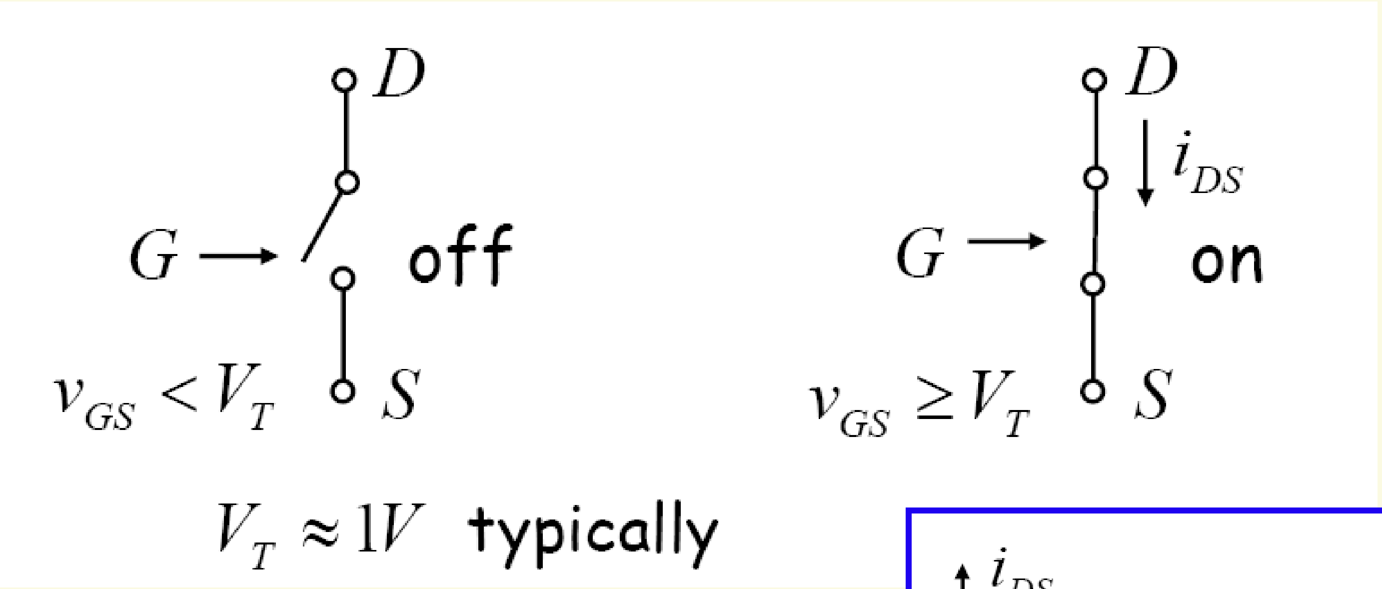
MOSFET

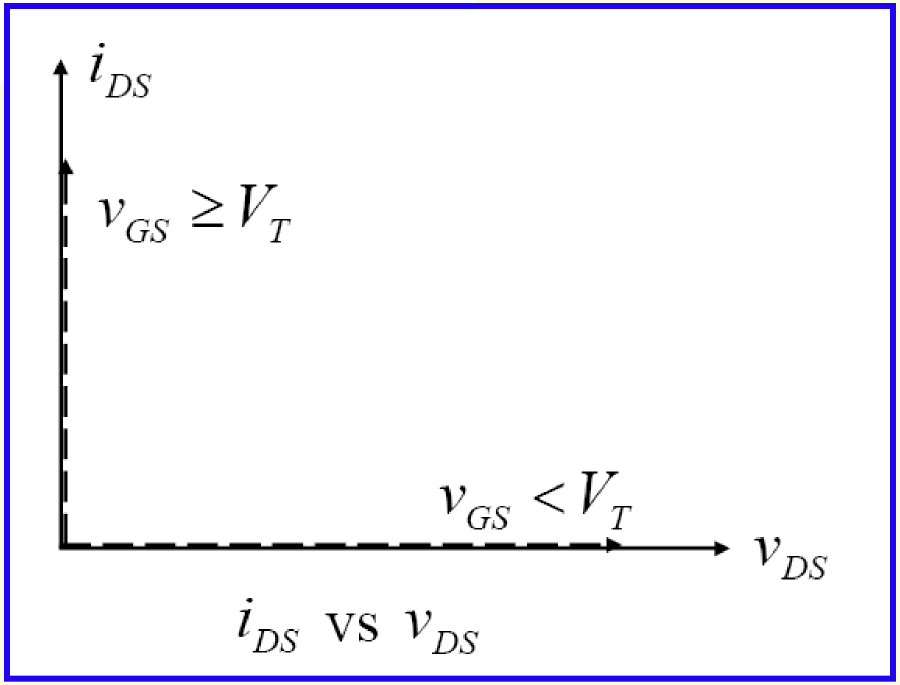
- Metal Oxide Semiconductor Field-Effect Transistor



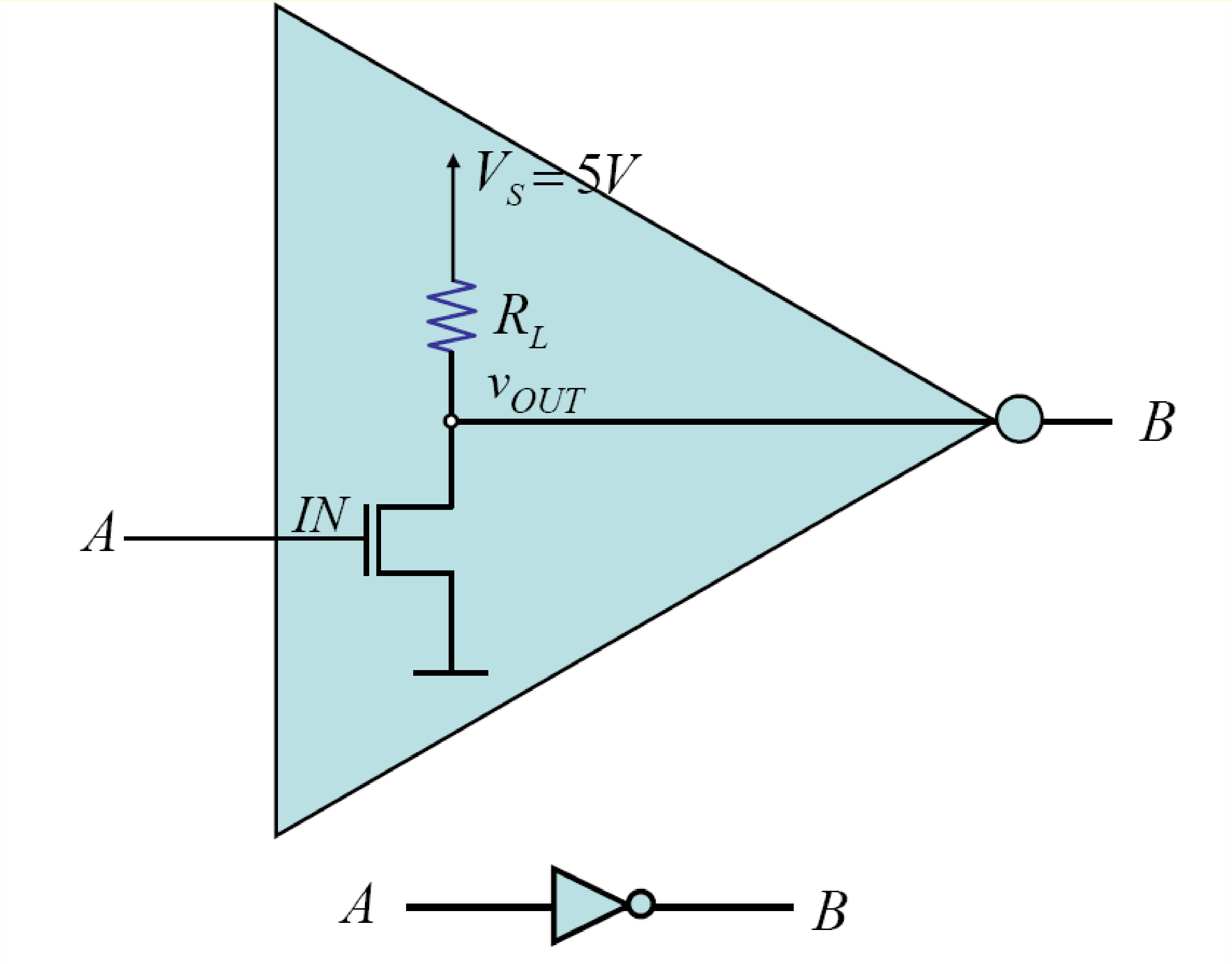


Switch (S) Model of MOSFET

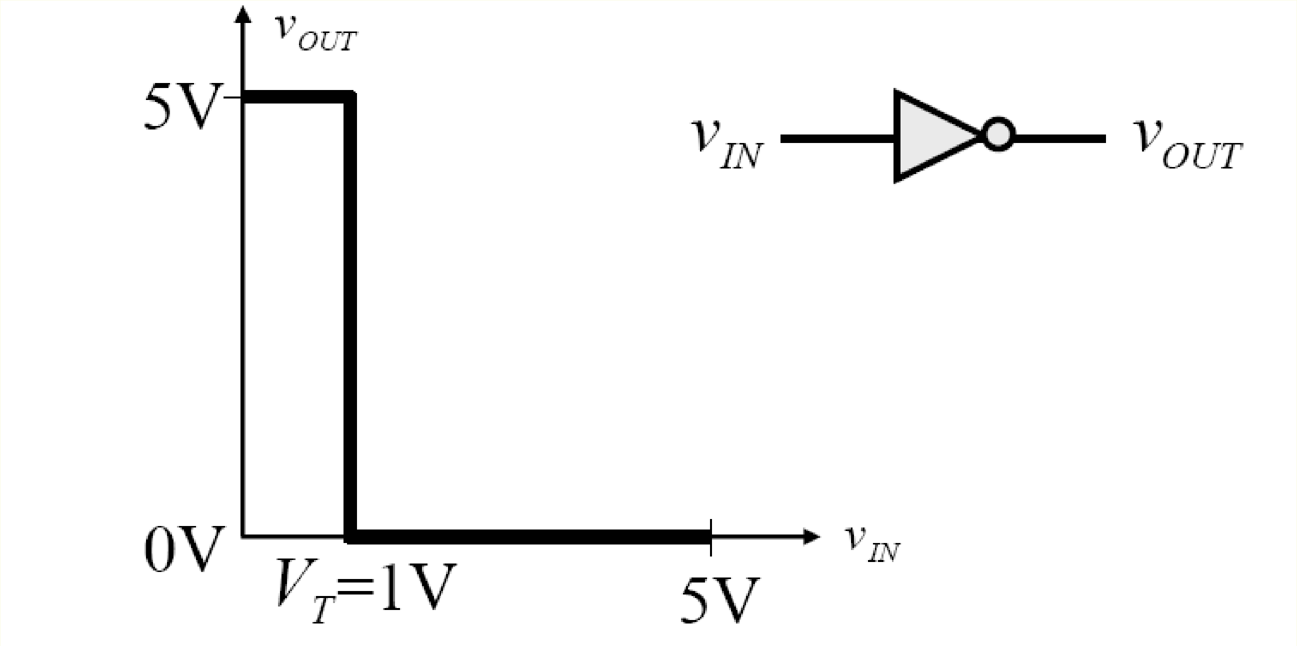




MOS Inverter



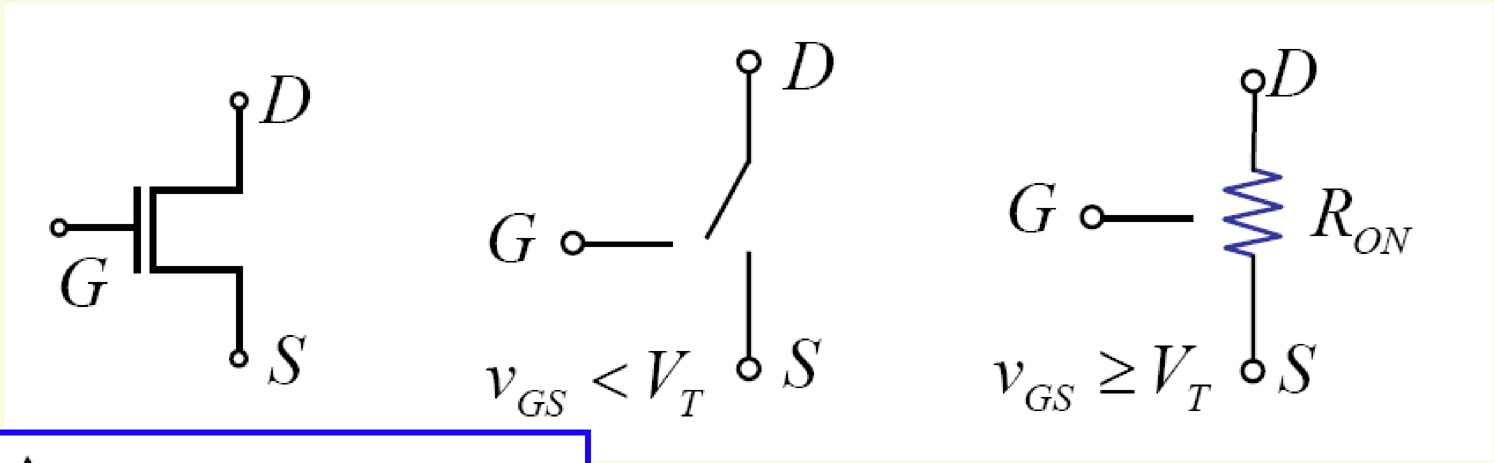
Voltage Transfer Characteristics

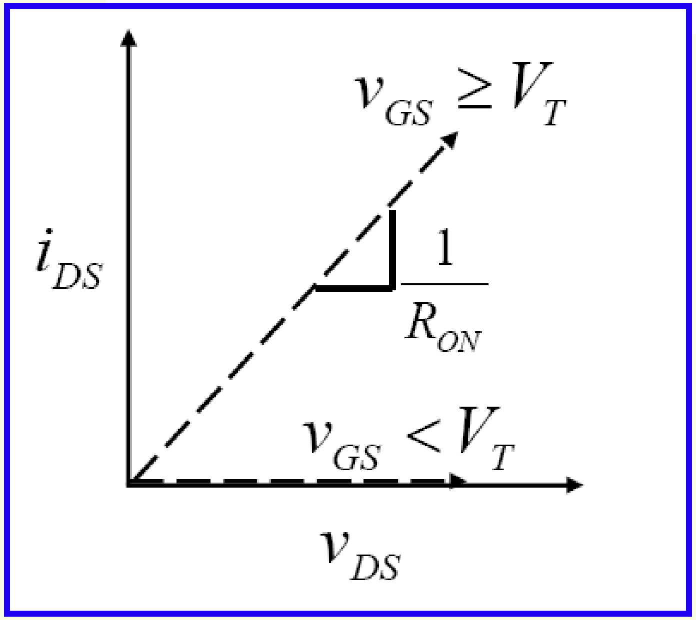


- Does it satisfy the following static discipline?
  - (1) $V_{OH} = 4.5V, \quad V_{OL} = 0.5V, \quad V_{IH} = 4V, \quad V_{IL} = 0.9V$
  - (2) $V_{OH} = 4V, \quad V_{OL} = 1V, \quad V_{IH} = 3.5V, \quad V_{IL} = 1.5V$

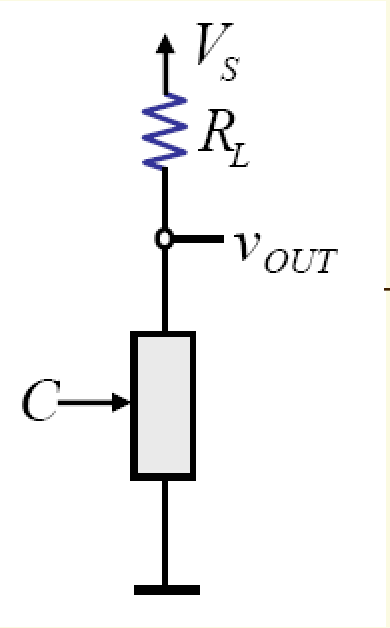
Switch Resistor (SR) Model of MOSFET

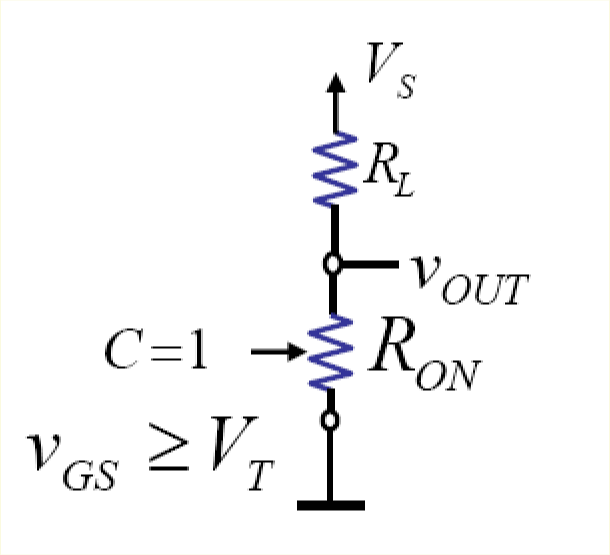
- Better approximation





MOSFET Inverter: Revisted

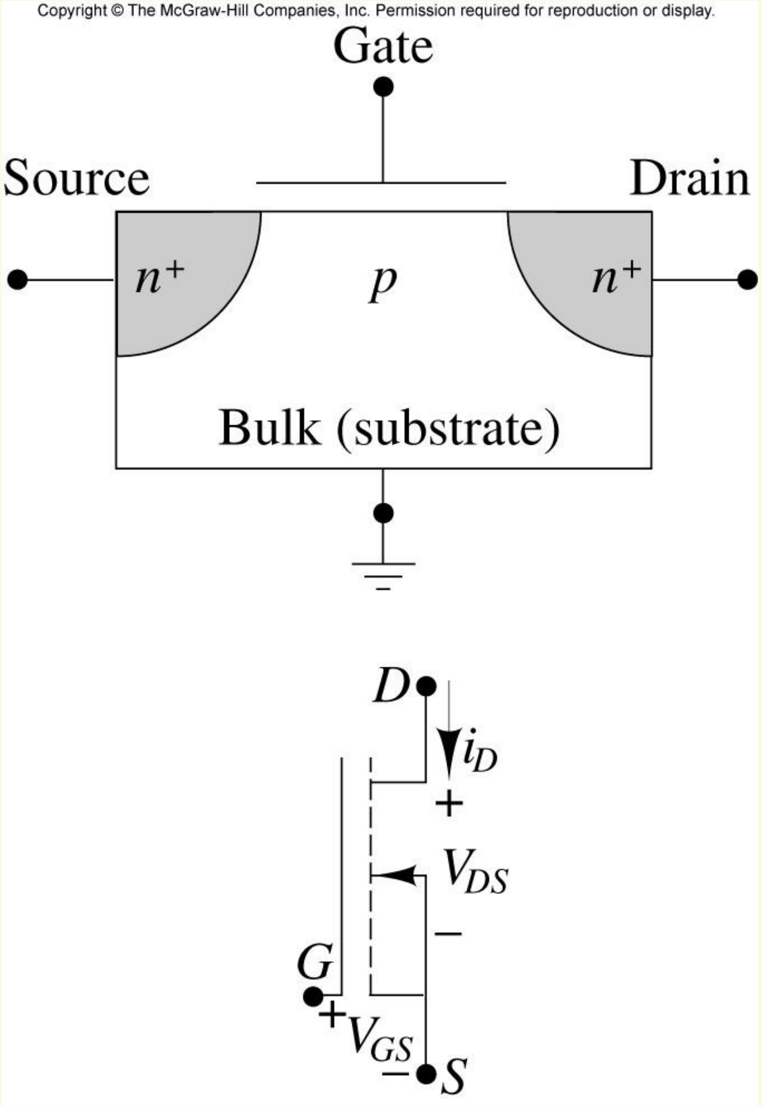




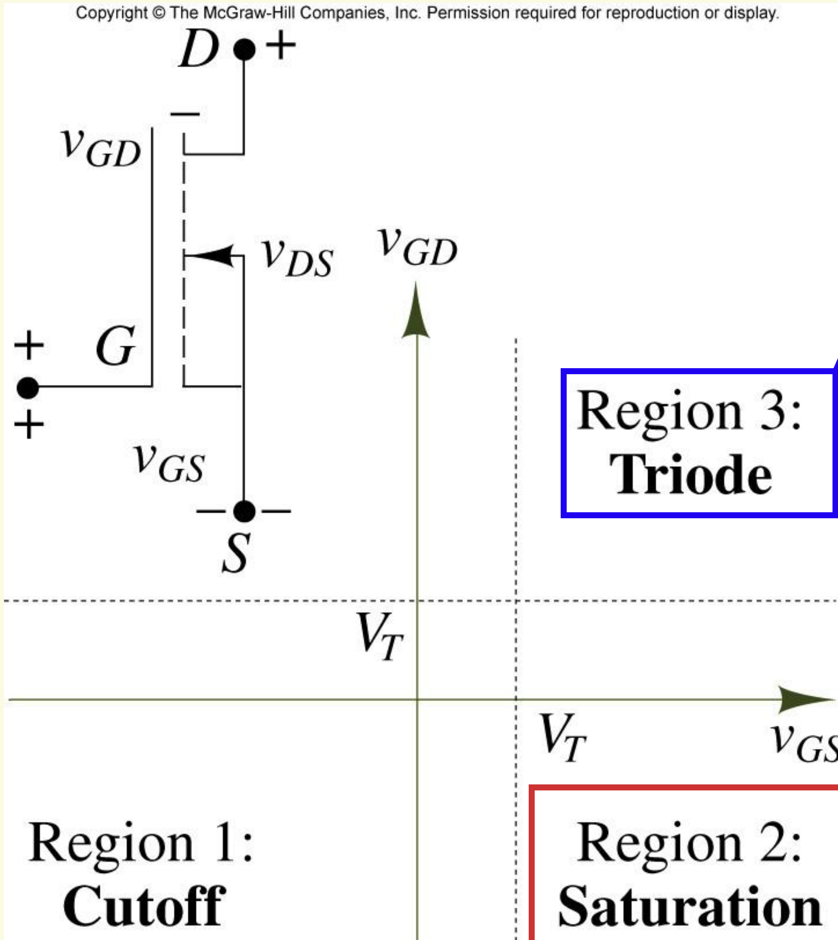
Choose R_L, R_{ON}, V_S such that:

$$v_{OUT} = \frac{V_S R_{ON}}{R_{ON} + R_L} \leq V_{OL}$$

Physical Structure of MOSFET



Regions of operation of NMOS transistor



Region 3 (Triode):

$$V_{GS} \geq V_T, \quad V_{GD} \geq V_T$$

$$i_D = K[2(V_{GS} - V_T)V_{DS} - V_{DS}{}^2]$$

Region 2 (Saturation):

$$V_{GS} \geq V_T, \quad V_{GD} < V_T$$

$$i_D = K(V_{GS} - V_T)^2 (1 + \frac{V_{DS}}{V_A})$$

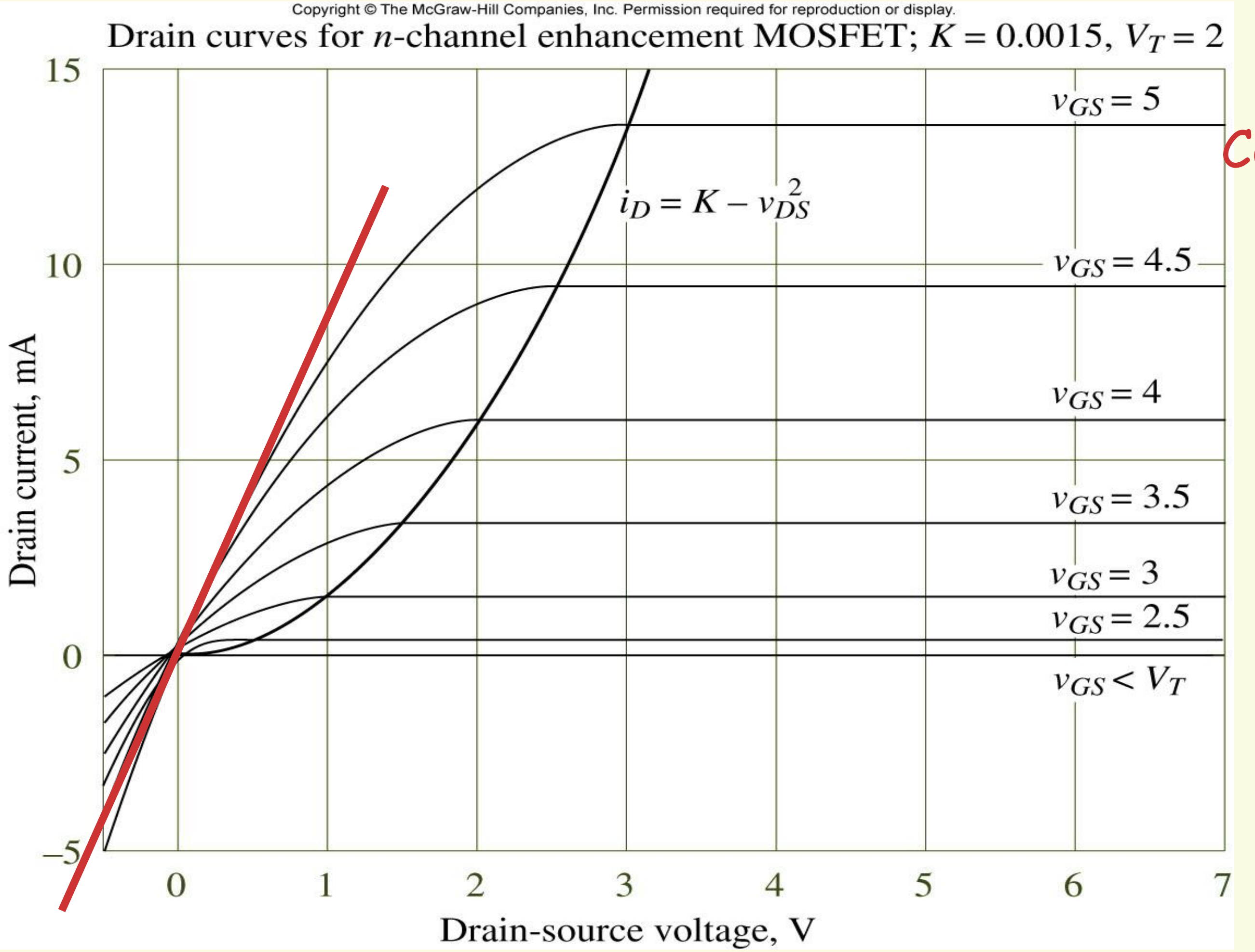
$$\approx K(V_{GS} - V_T)^2$$

Region 1 (Cutoff):

$$V_{GS} < V_T, \quad V_{GD} < V_T$$

$$i_D = 0$$

I-V Characteristic of NMOS

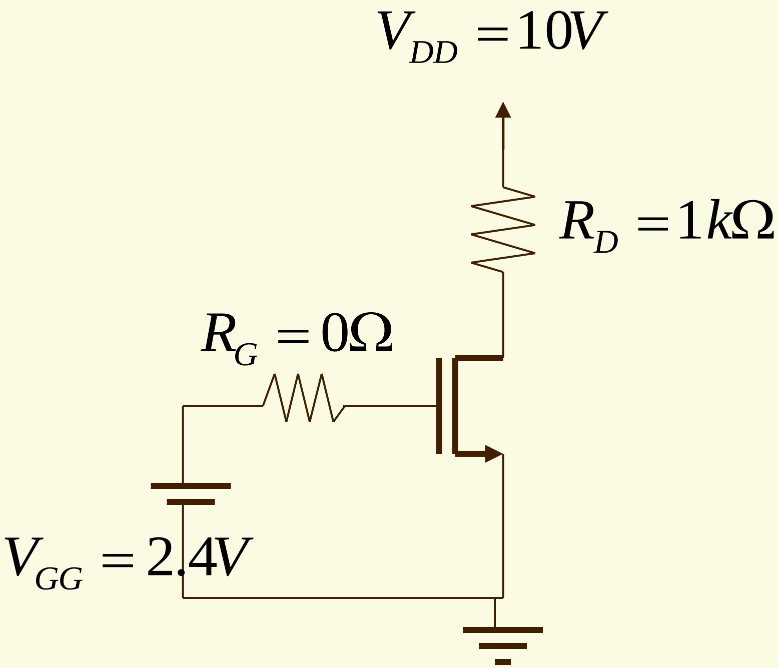


Conductance parameter

$$K = \frac{1}{2}\mu C_{OX}(\frac{W}{L})$$

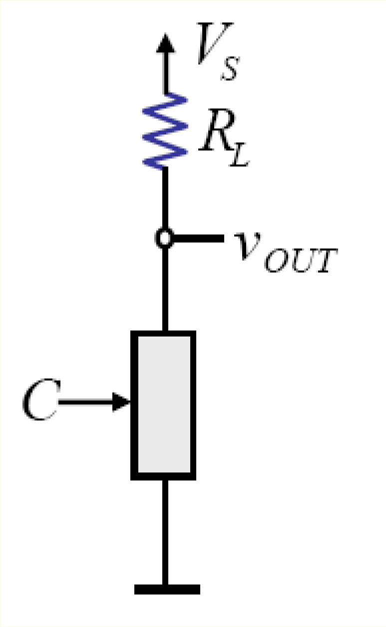
$$R_{ON} = R_n \frac{L}{W}$$

MOS Circuit Analysis

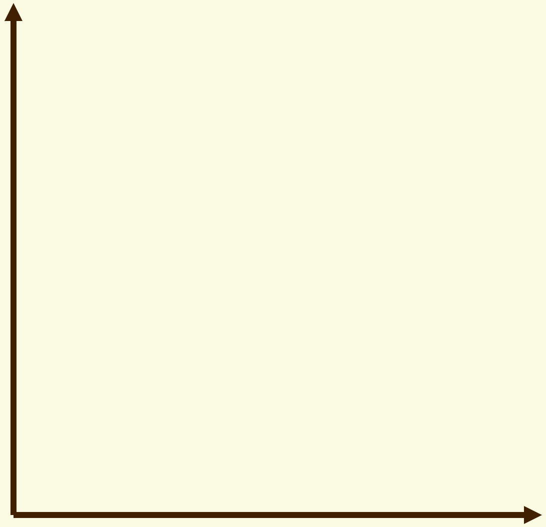


$V_T = 1.4V,\ K = 10mA/V$

Inverter Characteristics: SR Model



$$V_S = 5V, \quad V_T = 1V, \quad R_L = 14k\Omega, \quad R_{ON} = 1k\Omega$$



Example 6.5

- Determine W/L for correct inverter operation

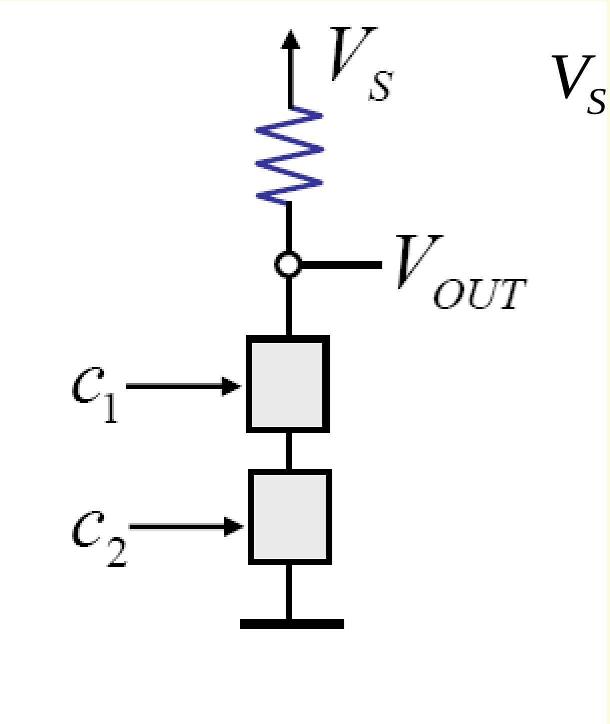
$$V_S = 5V, \quad V_T = 1V, \quad R_L = 10k\Omega, \quad R_n = 5k\Omega$$

Example 6.6

- To satisfy the following static discipline redesign the inverter.

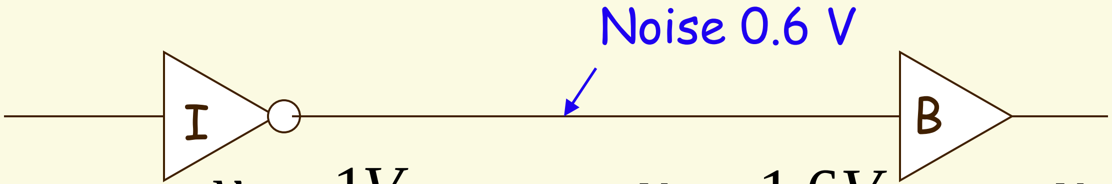
$$V_S = 5V, \quad V_T = 1V, \quad R_L = 10k\Omega, \quad R_n = 5k\Omega$$

Static Analysis of NAND Gate: SR Model



$$V_S = 5V, \quad V_T = 1V, \quad R_L = 14k\Omega, \quad R_{ON} = 1k\Omega$$

Signal Restoration and Gain



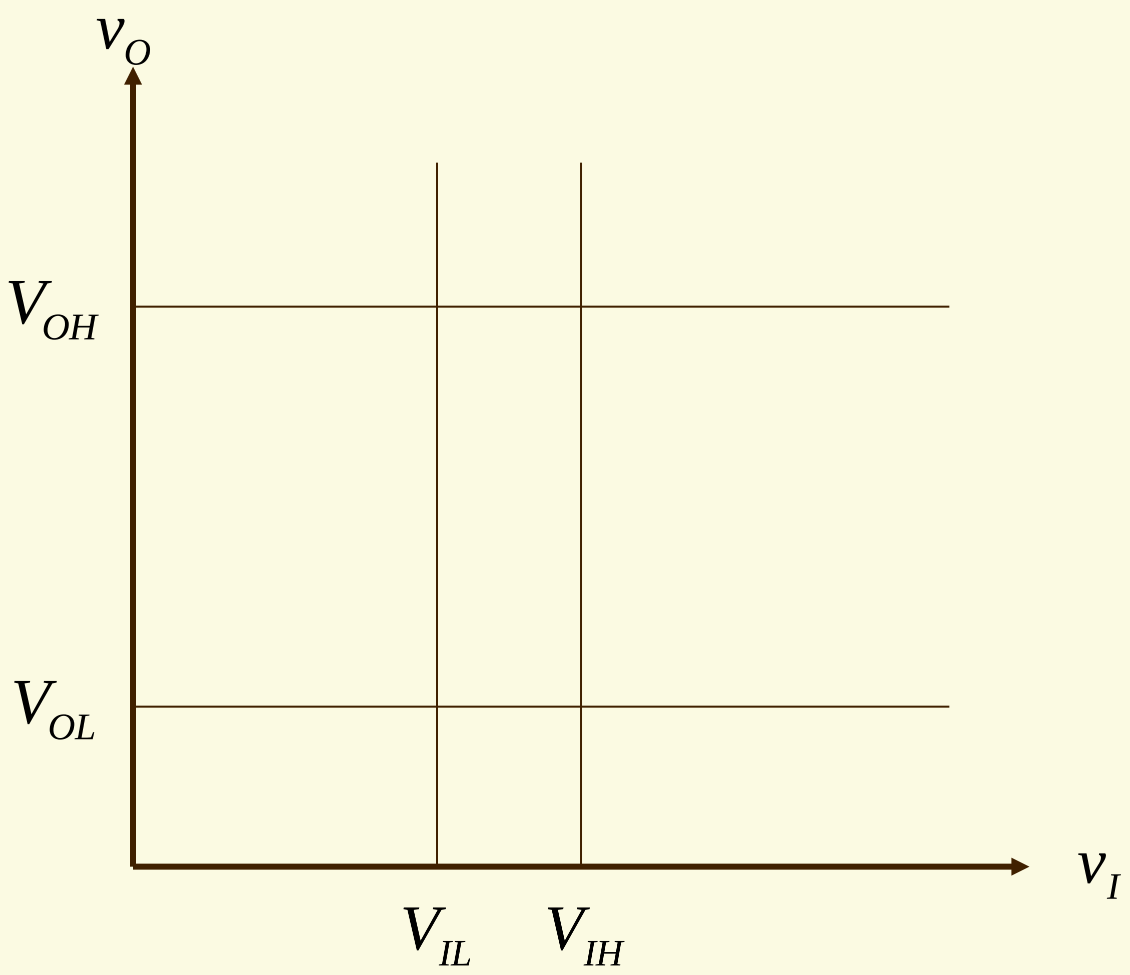
$v_O = 1V$ $\quad v_O = 1.6V$ $\quad v_O = 1V$

- Buffer restores the signal level (example)

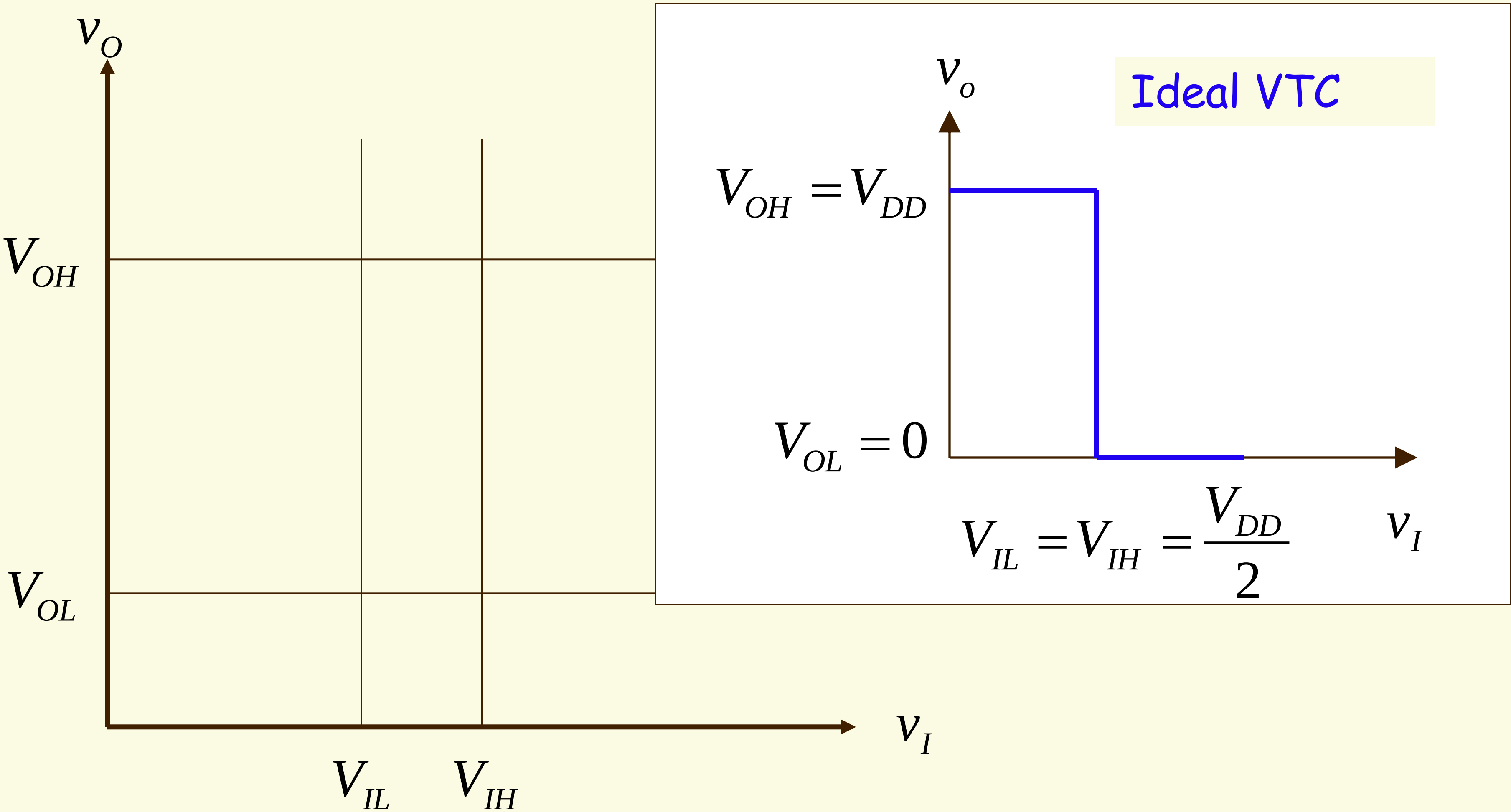
$$V_{IL} = 2V, \quad V_{IH} = 3V, \quad V_{OL} = 1V, \quad V_{OH} = 4V$$

Gain = $\dfrac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$

Buffer Voltage Transfer Characteristics (VTC)



Inverter VTC



Conclusion

- MOSFET and S Model
- MOSFET and SR Model
- MOSFET Analysis
- Signal Restoration and Gain