2007 Fall: Electronic Circuits 2

CHAPTER 9
Operational-Amplifier and Data-Converter Circuits

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Introduction

- In this chapter, we will be covering…
  - The Two-Stage CMOS Op Amp
  - The Folded-Cascode CMOS Op Amp
  - The 741 Op-Amp Circuit
  - D/A Converter
  - A/D Converter

9.1 The Two-Stage CMOS OP AMP

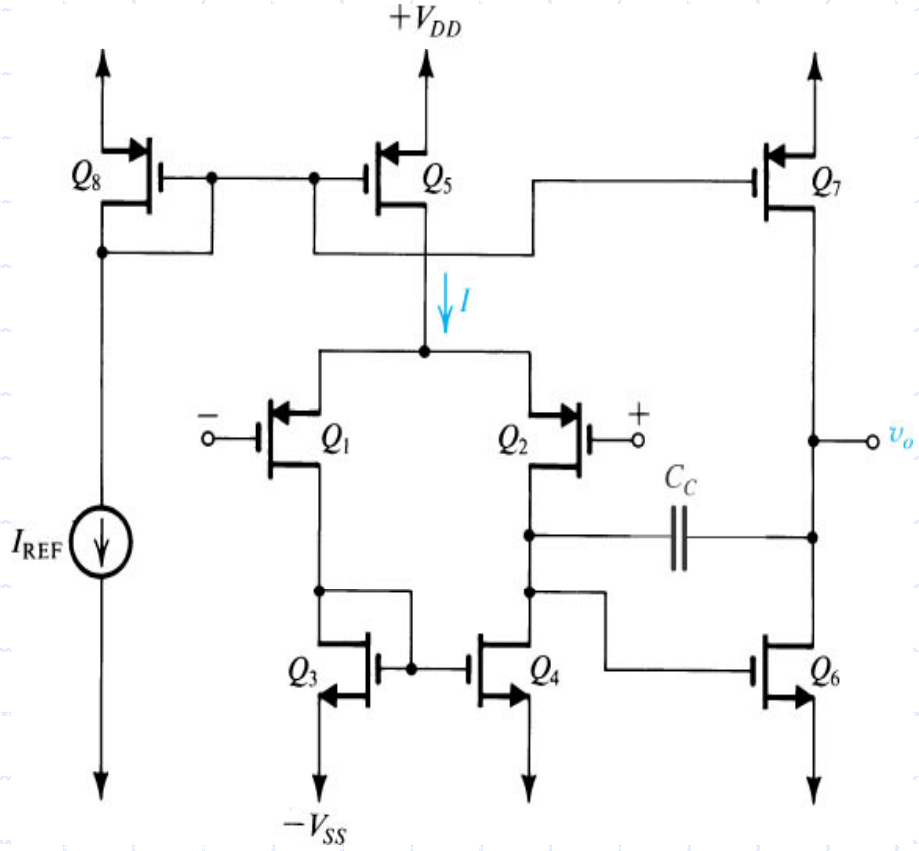


Figure 9.1 The basic two-stage CMOS op-amp configuration.

- Compensation capacitance C_c (together with C_{gd6}) is Miller-multiplied by the gain of the second stage

- Systematic output dc offset

→ can be eliminated by keeping

$$\frac{(W/L)_6}{(W/L)_4} = 2 \cdot \frac{(W/L)_7}{(W/L)_5}$$

9.1 The Two-Stage CMOS OP AMP

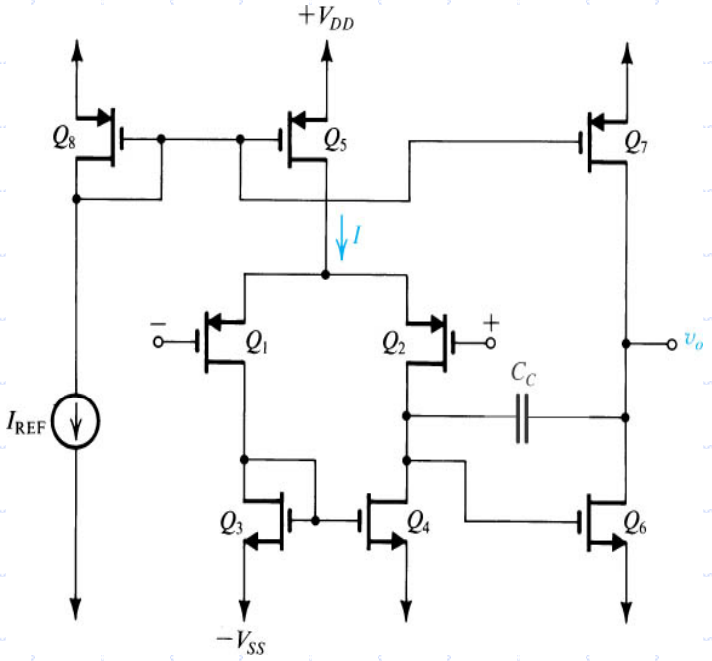
Input Common-Mode Range

- To Keep Q_1 & Q_2 in saturation

$$V_{ICM} \geq -V_{SS} + V_{tn} + V_{OV3} - |V_{tp}|$$

- To Keep Q5 in saturation

$$V_{ICM} \leq V_{DD} - |V_{OV5}| - V_{SG1}$$
$$= V_{DD} - |V_{OV5}| - |V_{tp}| - |V_{OV1}|$$



- Input common-mode range

$$-V_{SS} + V_{OV3} + V_{tn} - |V_{tp}| \leq V_{ICM} \leq V_{DD} - |V_{tp}| - |V_{OV1}| - |V_{OV5}|$$

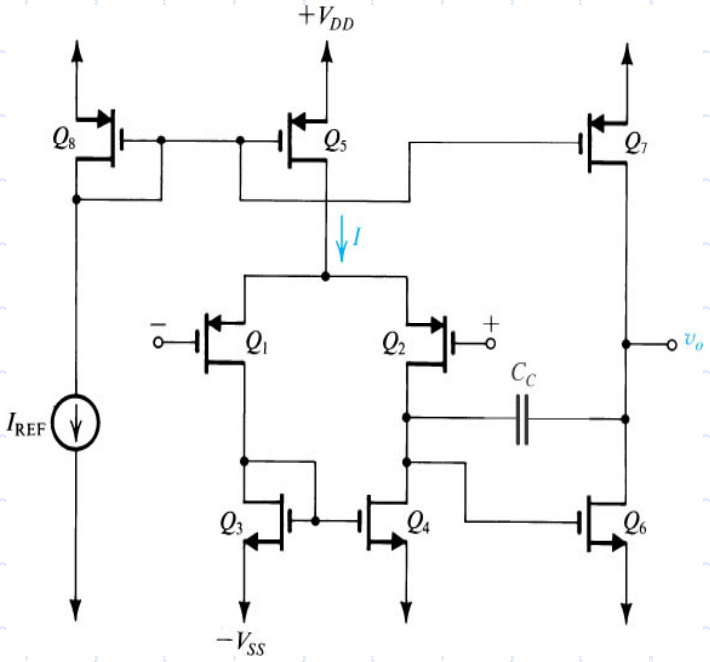
9.1 The Two-Stage CMOS OP AMP

Output Swing

- To keep Q_6 & Q_7 saturated,

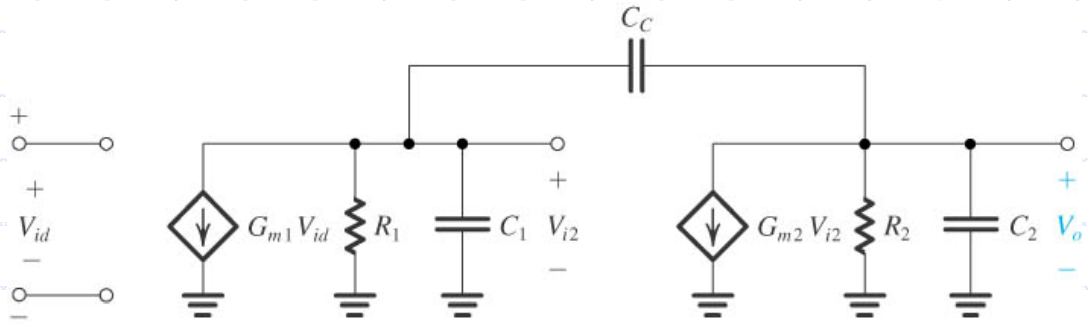
$$-V_{SS} + V_{OV6} \le V_O \le V_{DD} - |V_{OV7}|$$

- We need to keep the magnitude of V_{ov} as low as possible
- However, counteracted by the need to have high f_T for Q_6
- f_T is proportional to V_{ov} (in Section 6.2.3)



9.1 The Two-Stage CMOS OP AMP

Voltage Gain



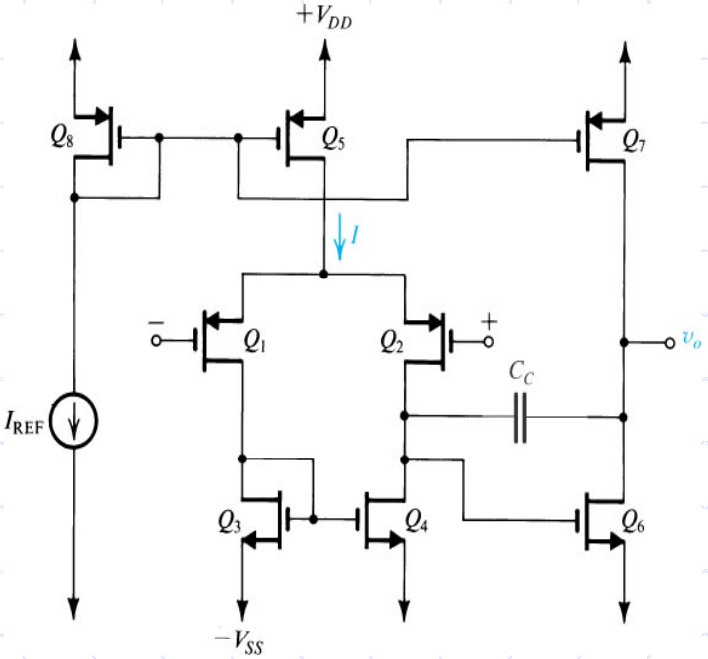


Figure 9.2 Small-signal equivalent circuit for the op amp in Fig. 9.1.

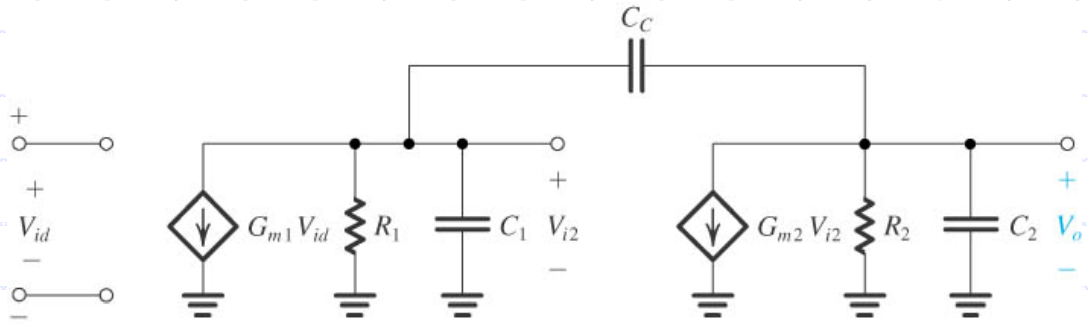
$$R_{in} = \infty$$

$$G_{m1} = g_{m1} = g_{m2} = \frac{2 \cdot (I/2)}{V_{OV1}} = \frac{I}{V_{OV1}}$$

$$R_1 = r_{o2} \| r_{o4}, \text{ where } r_{o2} = \frac{|V_{A2}|}{I/2} \text{ and } r_{o4} = \frac{V_{A4}}{I/2}$$

9.1 The Two-Stage CMOS OP AMP

Voltage Gain (cont)



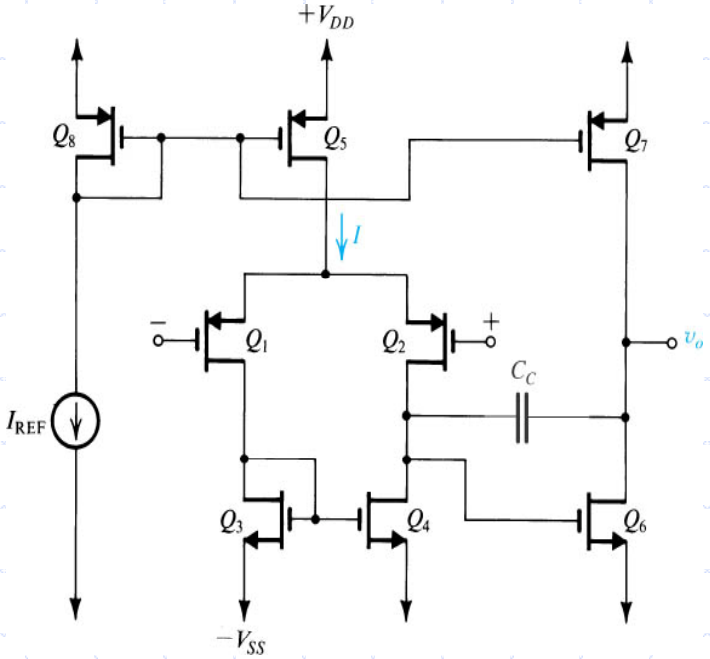


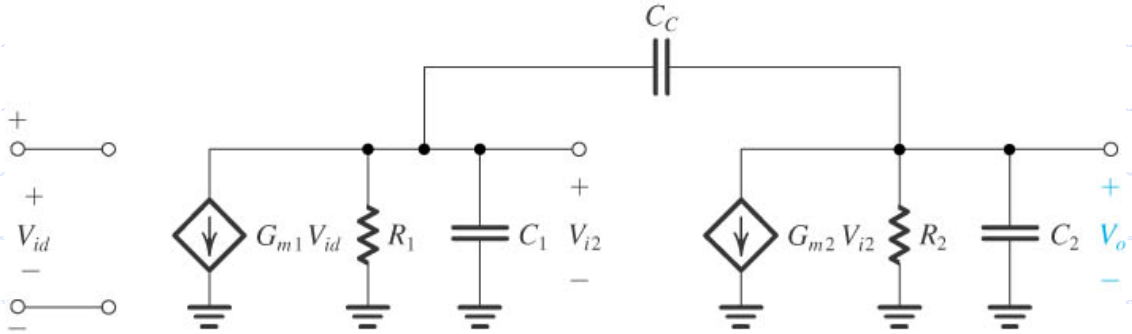
Figure 9.2 Small-signal equivalent circuit for the op amp in Fig. 9.1.

$$G_{m2} = g_{m6} = \frac{2 \cdot I_{D6}}{V_{OV6}}$$

$$R_2 = r_{o6} \parallel r_{o7}, \text{ where } r_{o6} = \frac{V_{A6}}{I_{D6}} \text{ and } r_{o7} = \frac{|V_{A7}|}{I_{D7}} = \frac{|V_{A7}|}{I_{D6}}$$

9.1 The Two-Stage CMOS OP AMP

Voltage Gain (Cont.)

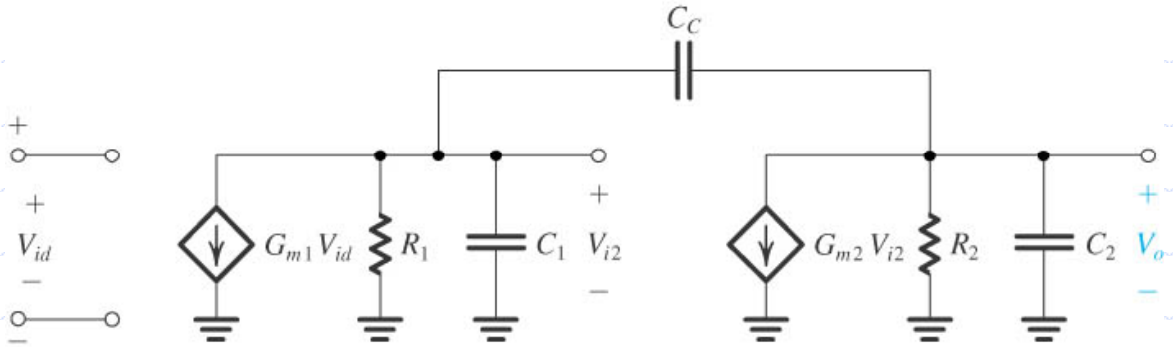


$$A_1 = -G_{m1}R_1$$
$$= -g_{m1}(r_{o2} \parallel r_{o4})$$
$$= -\frac{\frac{2}{V_{OV1}}}{\frac{1}{|V_{A2}|} + \frac{1}{V_{A4}}}$$

$$A_2 = -G_{m2}R_2$$
$$= -g_{m6}(r_{o6} \parallel r_{o7})$$
$$= -\frac{\frac{2}{V_{OV6}}}{\frac{1}{V_{A6}} + \frac{1}{|V_{A7}|}}$$

9.1 The Two-Stage CMOS OP AMP

Voltage Gain (Cont.)



- The overall dc voltage gain

$$\begin{aligned} A_v &= A_1 A_2 \\ &= G_{m1} R_1 G_{m2} R_2 \\ &= g_{m1}(r_{o2} \| r_{o4}) g_{m6}(r_{o6} \| r_{o7}) \end{aligned}$$

- Output resistance of the op amp

$$R_o = r_{o6} \| r_{o7}$$

9.1 The Two-Stage CMOS OP AMP

Frequency Response

- Capacitance C_1, C_2

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$

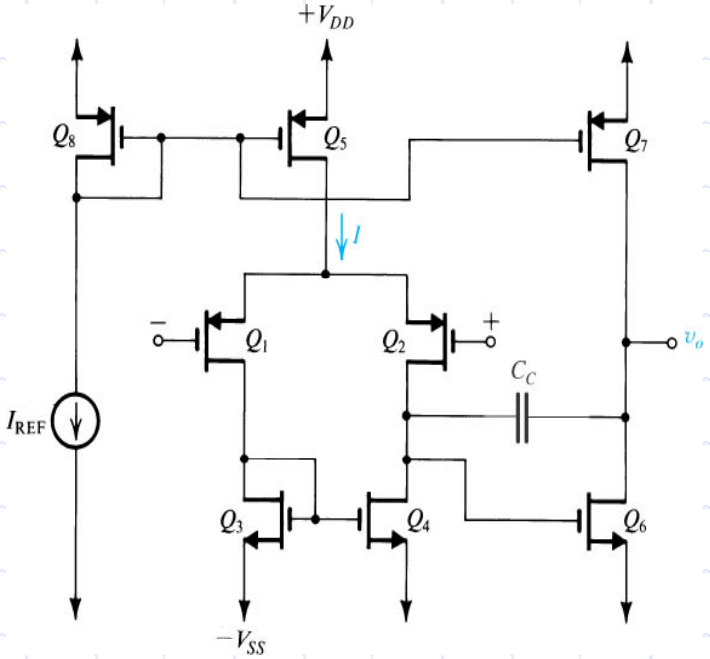
$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

- Pole & Zero (in Section 7.7.1)

$$f_{P1} \cong \frac{1}{2\pi R_1 G_{m2} R_2 C_C}$$ *: dominant pole*

$$f_{P2} \cong \frac{G_{m2}}{2\pi C_2}$$

$$f_Z \cong \frac{G_{m2}}{2\pi C_C}$$



9.1 The Two-Stage CMOS OP AMP

Frequency Response

- To guarantee stability, unity-gain frequency f_t must be lower than f_{p2} & f_z, so that $20\log|A_v|$ crosses 0 db at its -20db/dec decaying section

$$f_t = |A_v| f_{P1} = \frac{G_{m1}}{2\pi C_C} < f_{P2}, f_Z$$

$$\frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2}$$

$$G_{m1} < G_{m2}$$

9.1 The Two-Stage CMOS OP AMP

- Simplified Equivalent Circuit

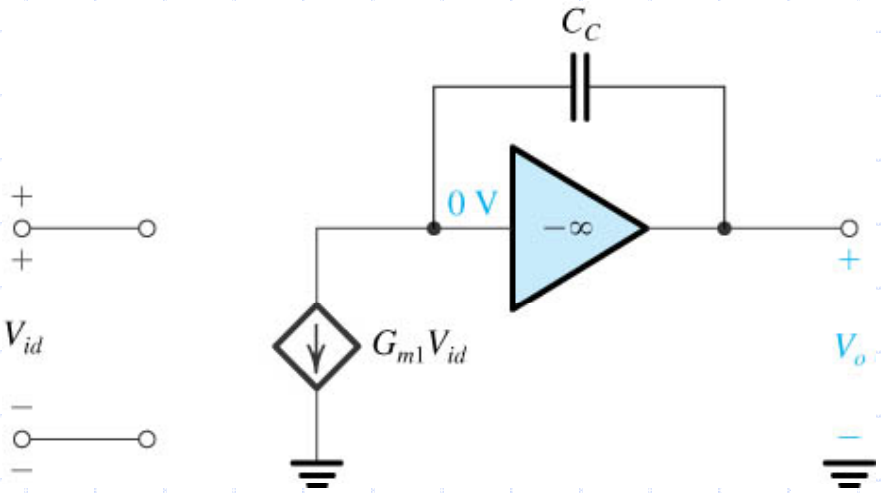


Figure 9.3 An approximate high-frequency equivalent circuit of the two-stage op amp. This circuit applies for frequencies $f >> f_{P1}$.

Based on the assumption that $|A_2|$ is large and a virtual ground appears at the input terminal

The second stage effectively acts as an integrator that is fed with the output current signal of the first stage : $G_{m1}V_{id}$

9.1 The Two-Stage CMOS OP AMP

Phase Margin

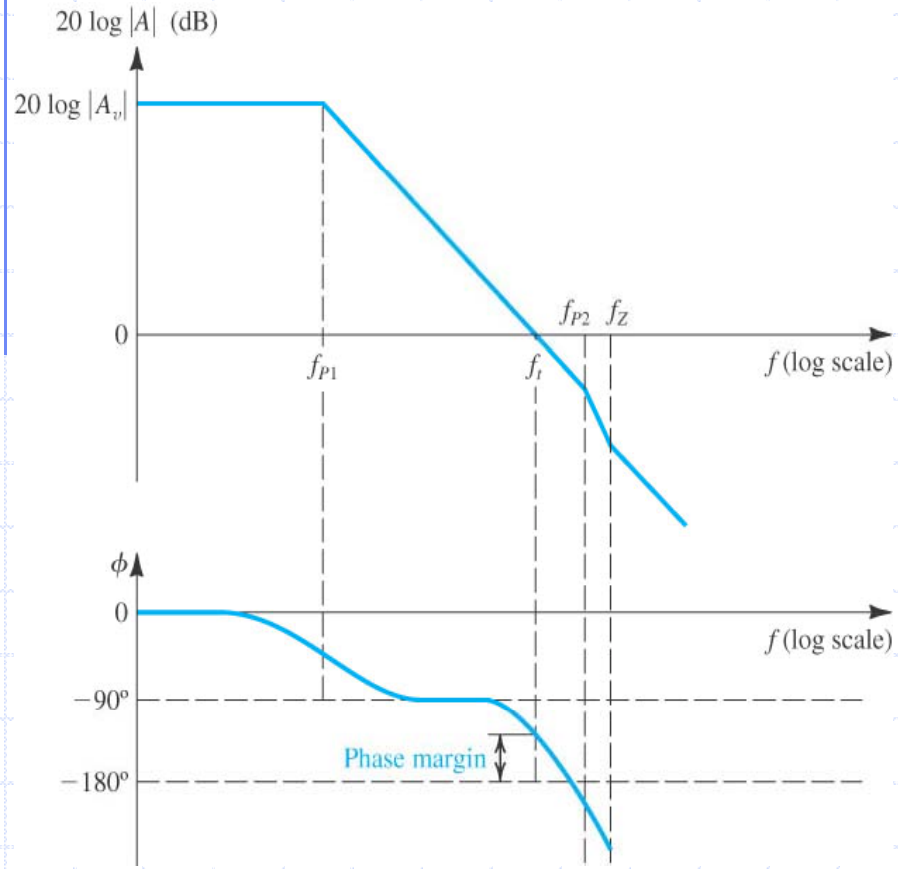


Figure 9.4 Typical frequency response of the two-stage op amp.

Excess Phase Shift

$$\phi_{P2} = -\tan^{-1}\left(\frac{f_t}{f_{P2}}\right)$$

$$\phi_z = -\tan^{-1}\left(\frac{f_t}{f_z}\right) \text{ : right half plane zero}$$

$$\phi_{total} = 90° + \tan^{-1}\left(\frac{f_t}{f_{P2}}\right) + \tan^{-1}\left(\frac{f_t}{f_z}\right)$$

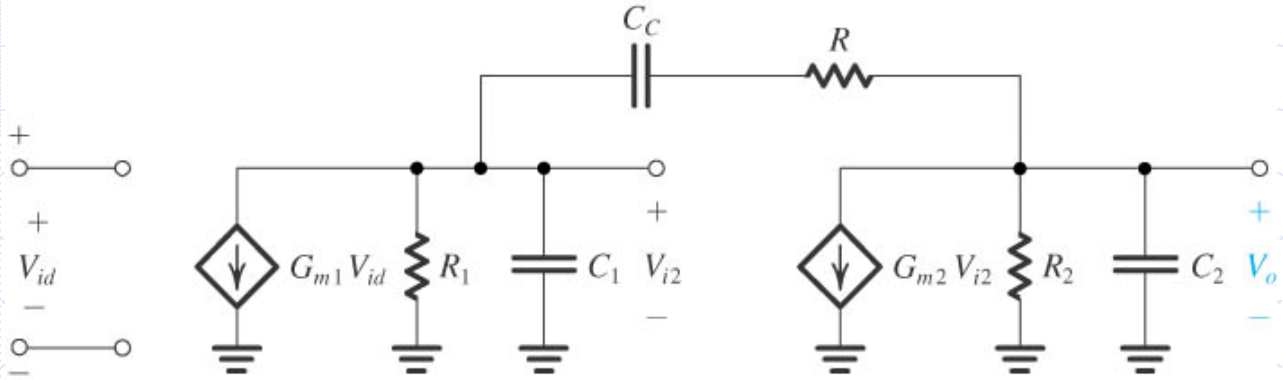
Phase Margin

$$\text{PM} = 180° - \phi_{total}$$

$$= 90° - \tan^{-1}\left(\frac{f_t}{f_{P2}}\right) - \tan^{-1}\left(\frac{f_t}{f_z}\right)$$

9.1 The Two-Stage CMOS OP AMP

- Phase Margin

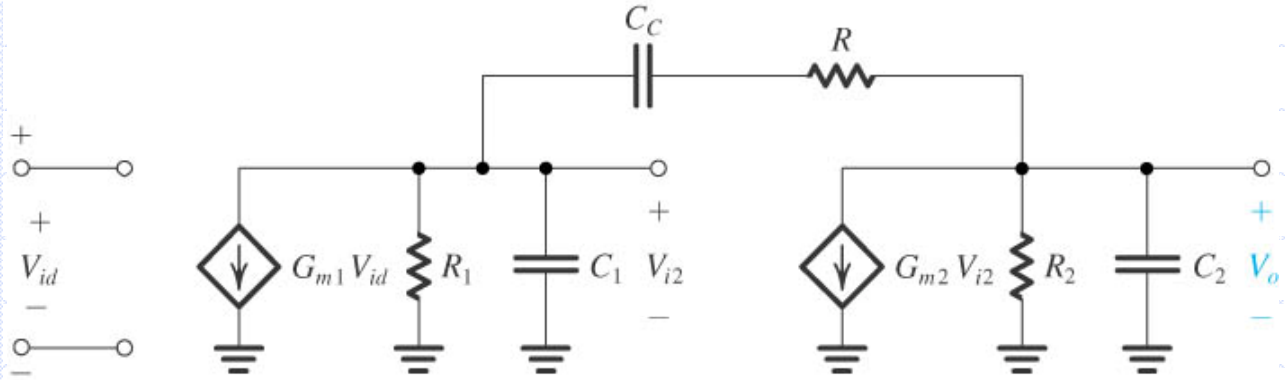


Problem: Additional phase lag by zero

Solution: Include R in series with C_C. The transmission zero can be moved to other less-harmful locations

9.1 The Two-Stage CMOS OP AMP

- Phase Margin



$$V_o = 0$$

$$\frac{V_{i2}}{R + \frac{1}{sC_C}} = G_{m2}V_{i2}$$

$$s = \frac{1}{C_C\left(\frac{1}{G_{m2}} - R\right)}$$

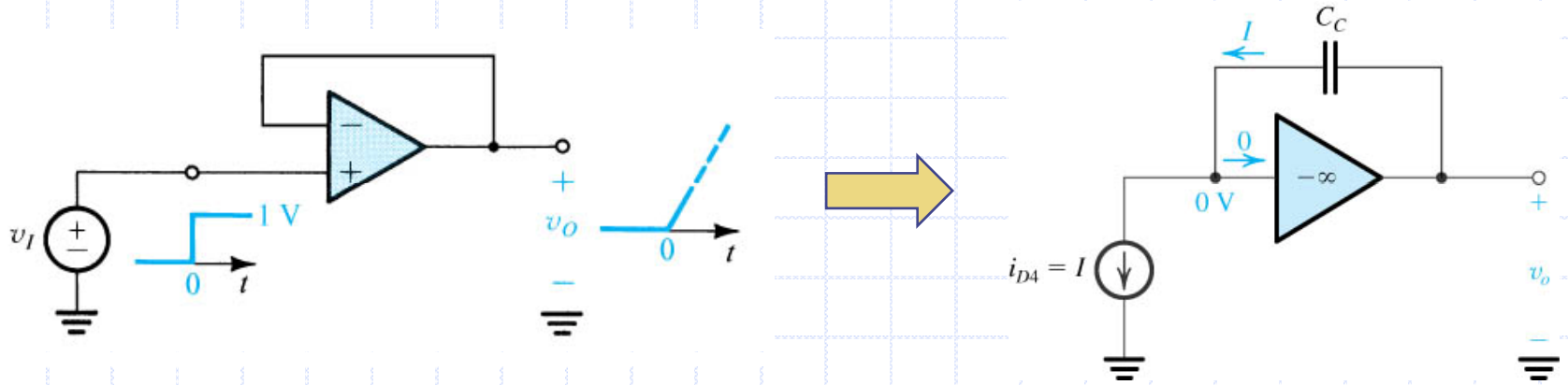
By selecting $R = \frac{1}{G_{m2}}, \; f_Z = \infty.$

By selecting $R > \frac{1}{G_{m2}}$

f_z is at a negative real-axis: the extra phase adds to the phase margin

9.1 The Two-Stage CMOS OP AMP

Slew Rate



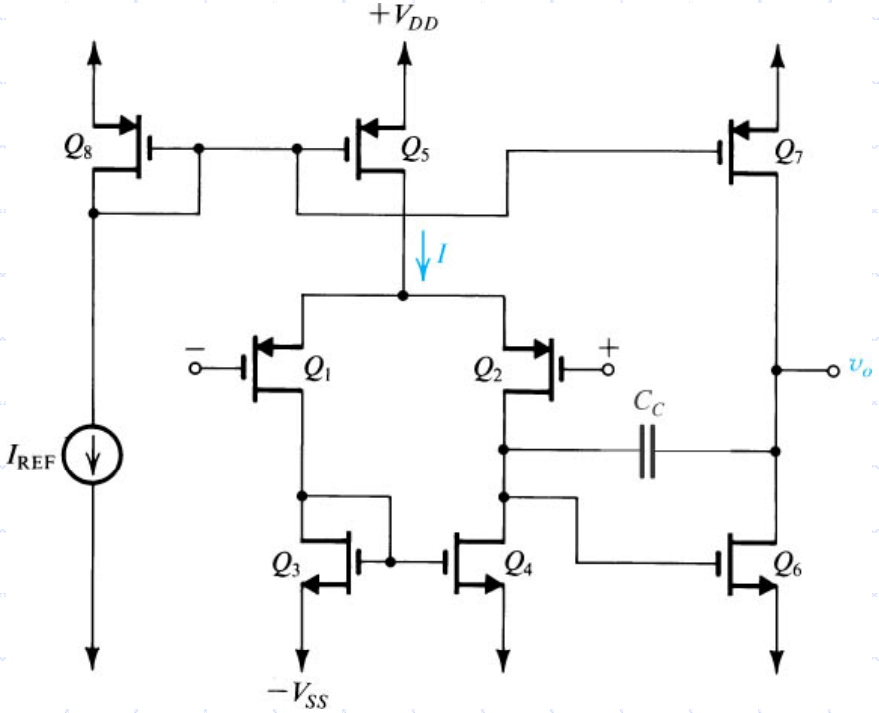
- 1V applied at the input
- A large signal will exceed the voltage required to turn off one side of the pair and switch the entire bias current I to the other side

$$v_o(t) = \frac{I}{C_C}t$$

$$SR = \frac{I}{C_C} = 2\pi f_t V_{OV} = V_{OV}\omega_t, \text{ since } G_{m1} = g_{m1} = \frac{I}{V_{OV1}}, \quad f_t = \frac{G_{m1}}{2\pi C_C}$$

9.1 The Two-Stage CMOS OP AMP

Example 9.1



$$A_v = g_{m1}\left(r_{o2}\|r_{o4}\right)g_{m6}\left(r_{o6}\|r_{o7}\right)$$

$$= \frac{2(I/2)}{V_{OV}} \times \frac{1}{2} \times \frac{V_A}{(I/2)} \times \frac{2I_{D6}}{V_{OV}} \times \frac{1}{2} \times \frac{V_A}{I_{D6}}$$

$$= \left(\frac{V_A}{V_{OV}}\right)^2$$

To obtain A_v=4000, given V_A=20V,

$$4000 = \frac{400}{V_{OV}^2} \Rightarrow V_{OV} = 0.316\text{V}$$

To obtain the required (W/L) ratios of Q_1 and Q_2,

$$I_{D1} = \frac{1}{2}k_p'\left(\frac{W}{L}\right)_1 V_{OV}^2 \Rightarrow 100 = \frac{1}{2}\times 80\left(\frac{W}{L}\right)_1 \times 0.316^2$$

$$\therefore \left(\frac{W}{L}\right)_1 = \frac{25\mu m}{1\mu m} \quad \text{and} \quad \left(\frac{W}{L}\right)_2 = \frac{25\mu m}{1\mu m}$$

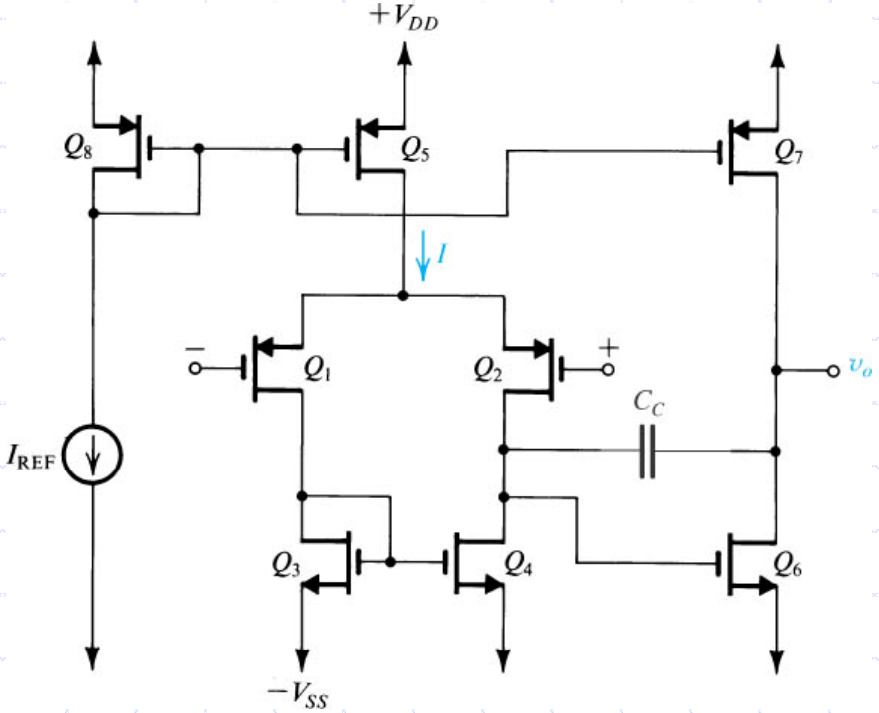
For Q3 and Q4

$$100 = \frac{1}{2}\times 200\left(\frac{W}{L}\right)_3 \times 0.316^2 \Rightarrow \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{10\mu m}{1\mu m}$$

For Q_5, $200 = \frac{1}{2}\times 80\left(\frac{W}{L}\right)_5 \times 0.316^2 \Rightarrow \left(\frac{W}{L}\right)_5 = \frac{50\mu m}{1\mu m}$

9.1 The Two-Stage CMOS OP AMP

Example 9.1



Since Q_7 is required to conduct $500\mu A$,

$$\left(\frac{W}{L}\right)_7 = 2.5\left(\frac{W}{L}\right)_5 = \frac{125\mu m}{1\mu m}$$

For Q_6, $500 = \frac{1}{2}\times 200\left(\frac{W}{L}\right)_6 \times 0.316^2$

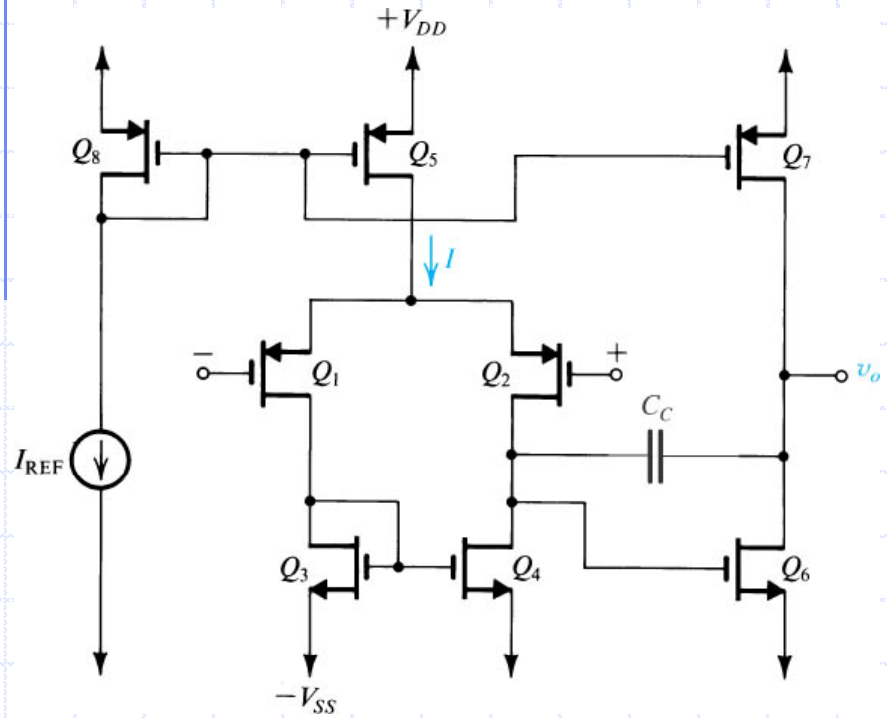
$$\Rightarrow \left(\frac{W}{L}\right)_6 = \frac{50\mu m}{1\mu m}$$

Finally, let's select I_{REF}=$20\mu A$, thus

$$\left(\frac{W}{L}\right)_8 = 0.1\left(\frac{W}{L}\right)_5 = \frac{5\mu m}{1\mu m}$$

9.1 The Two-Stage CMOS OP AMP

Example 9.1



$$-V_{SS} + V_{tn} + V_{OV3} - |V_{tp}| \le V_{ICM} \le V_{DD} - |V_{OV5}| - |V_{tp}| - |V_{OV1}|$$

$$=> -1.33V \le V_{ICM} \le 0.52V$$

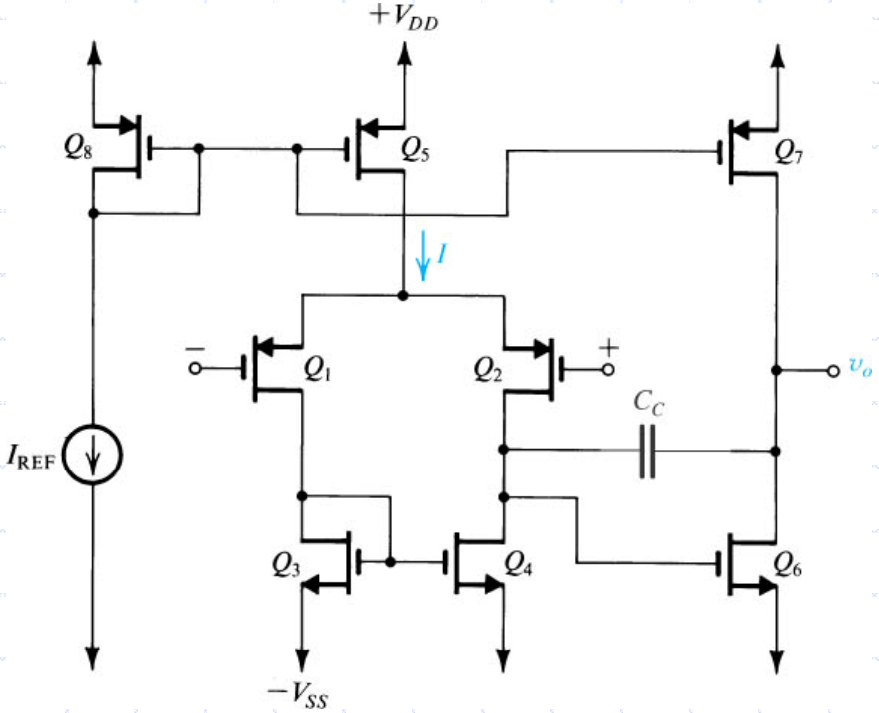
$$-V_{SS} + V_{OV6} \le v_o \le V_{DD} - |V_{OV7}|$$

The input resistance is practically infinite, and the output resistance is

$$R_O = r_{o6} \| r_{o7} = \frac{1}{2} \times \frac{20}{0.5} = 20k\Omega$$

9.1 The Two-Stage CMOS OP AMP

Example 9.1



To determine f_{P2}

$$G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{OV}} = \frac{2\times 0.5}{0.316} = 3.2mA/V$$

$$\Rightarrow f_{P2} \cong \frac{G_{m2}}{2\pi C_2} = \frac{3.2\times 10^{-3}}{2\pi\times 0.8\times 10^{-12}} = 637MHz$$

To move the transmission zero to s=∞

$$R = \frac{1}{G_{m2}} = \frac{1}{3.2\times 10^{-3}} = 316\Omega$$

For a phase margin of 75°, the phase shift due to the second pole at f=f_t, must be 15°, that is,

$$\tan^{-1}\frac{f_t}{f_{P2}} = 15^o \Rightarrow f_t = 637\times\tan 15^o = 171MHz$$

$$C_C = \frac{G_{m1}}{2\pi f_t} \quad \text{where } G_{m1} = g_{m1} = \frac{2\times 100\mu A}{0.316\text{V}} = 0.63mA/V$$

$$\Rightarrow C_C = \frac{0.63\times 10^{-3}}{2\pi\times 171\times 10^6} = 0.6\,pF$$

$$SR = 2\pi f_t V_{OV} = 2\pi\times 171\times 10^6\times 0.316 = 340V/\mu s$$

9.2 The Folded-Cascode CMOS OP AMP

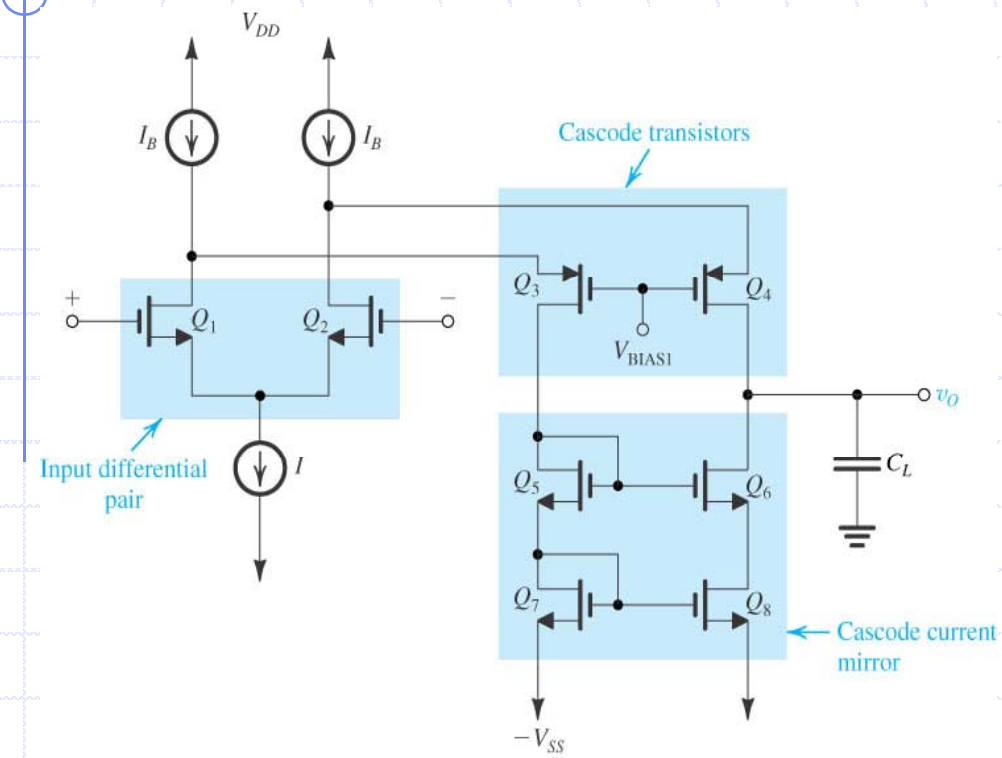


Figure 9.8 Structure of the folded-cascode CMOS op amp.

- Q_1, Q_2: input differential pair
- Q_3, Q_4: cascode transistors
- Each of Q_1, Q_2 is operating at a bias current ($I/2$)
- The bias current of each of Q_3, Q_4 is ($I_B - I/2$)
- The cascode current mirror Q_5 to Q_8: for high output resistance

- C_L: the total capacitance at the output node
- The load capacitance contributes to frequency compensation

9.2 The Folded-Cascode CMOS OP AMP

- Input common-mode range and the output voltage

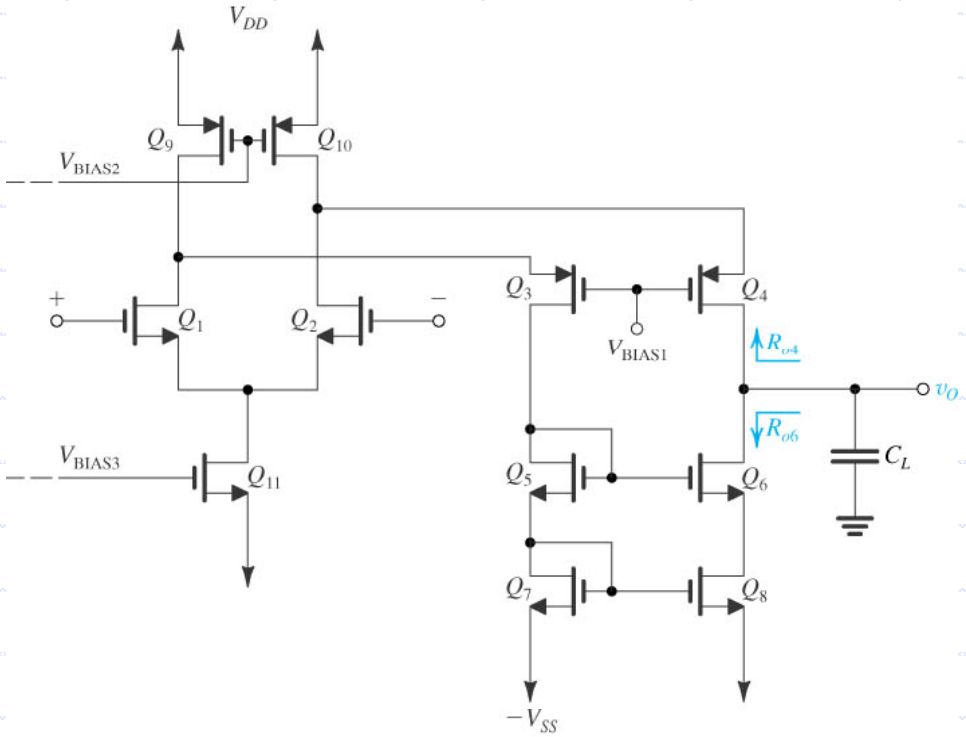


Figure 9.9 A more complete circuit for the folded-cascode CMOS amplifier of Fig. 9.8.

Assuming that Q_9 and Q_{10} are operated at the edge of saturation

$$V_{ICM\max} = V_{DD} - |V_{OV9}| + V_{tn}$$

$$V_{ICM\min} = -V_{SS} + V_{OV11} + V_{OV1} + V_{tn}$$

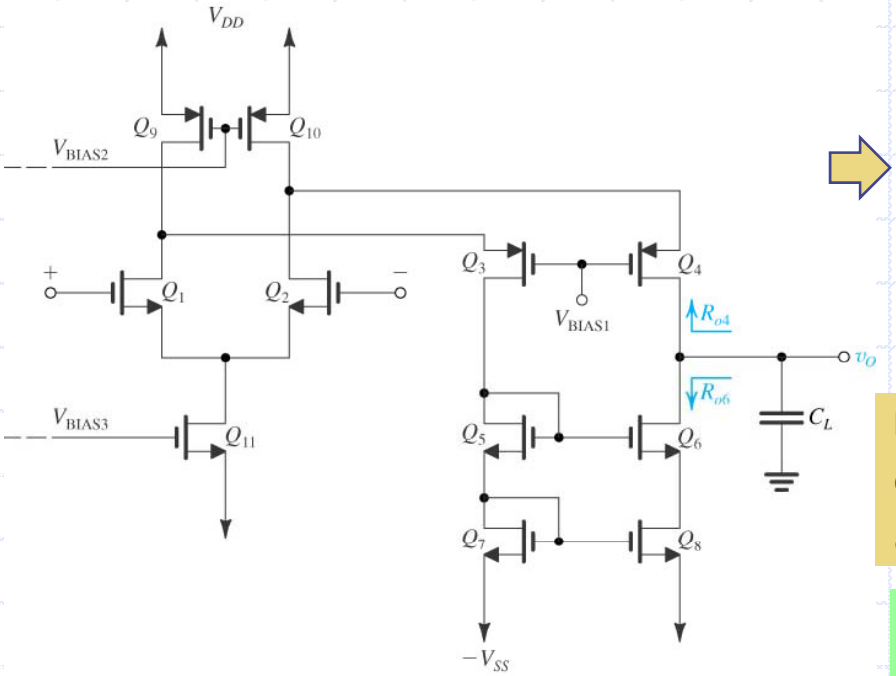
$$V_{BIAS1} = V_{DD} - |V_{OV10}| - V_{SG4}$$

$$v_{o\max} = V_{DD} - |V_{OV10}| - |V_{OV4}|$$

$$v_{o\min} = -V_{SS} + V_{OV7} + V_{OV5} + V_{tn}$$

9.2 The Folded-Cascode CMOS OP AMP

- Input common-mode range and the output voltage



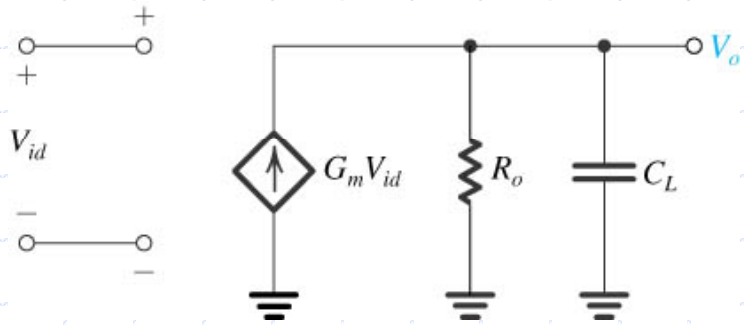


Figure 9.10 Small-signal equivalent circuit of the folded-cascode CMOS amplifier. Note that this circuit is in effect an operational transconductance amplifier (OTA).

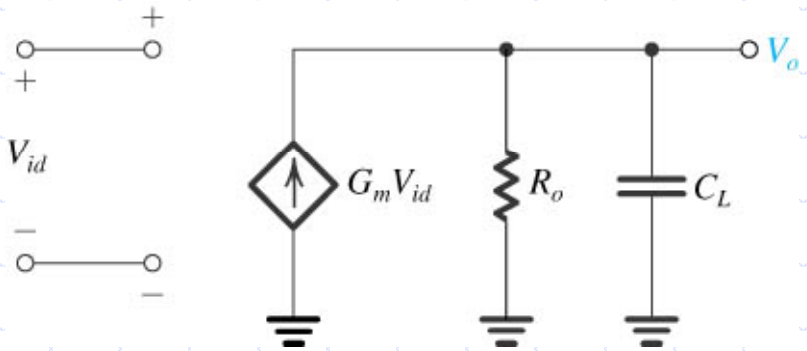
$$G_m = g_{m1} = g_{m2} = \frac{2(I/2)}{V_{OV1}} = \frac{I}{V_{OV1}}$$

$$R_O = R_{O4} \,||\, R_{O6} = [(g_{m4} r_{o4})(r_{o2} \,||\, r_{o10})] \,||\, (g_{m6} r_{o6} r_{o8})$$

$$A_V = G_m R_O = g_{m1} \cdot \{[(g_{m4} r_{o4})(r_{o2} \,||\, r_{o10})] \,||\, (g_{m6} r_{o6} r_{o8})\}$$

9.2 The Folded-Cascode CMOS OP AMP

Frequency response



$$\frac{V_O}{V_{id}} = \frac{G_m R_O}{1 + sC_L R_O}$$

The dominant pole has a frequency f_P

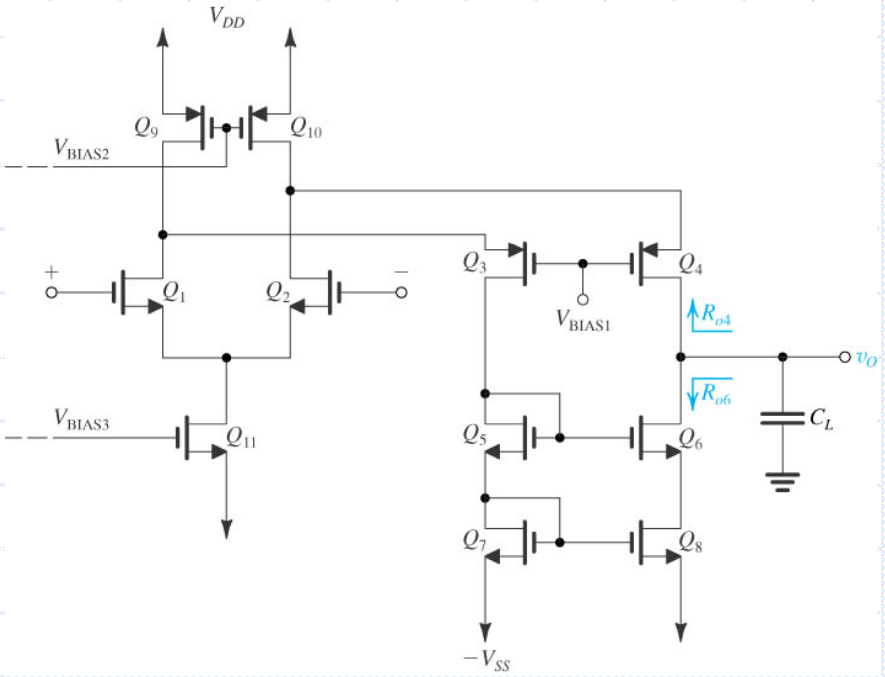
$$f_P = \frac{1}{2\pi C_L R_O}$$

The unity-gain frequency f_t

$$f_t = G_m R_O f_P = \frac{G_m}{2\pi C_L}$$

9.2 The Folded-Cascode CMOS OP AMP

- Slew rate



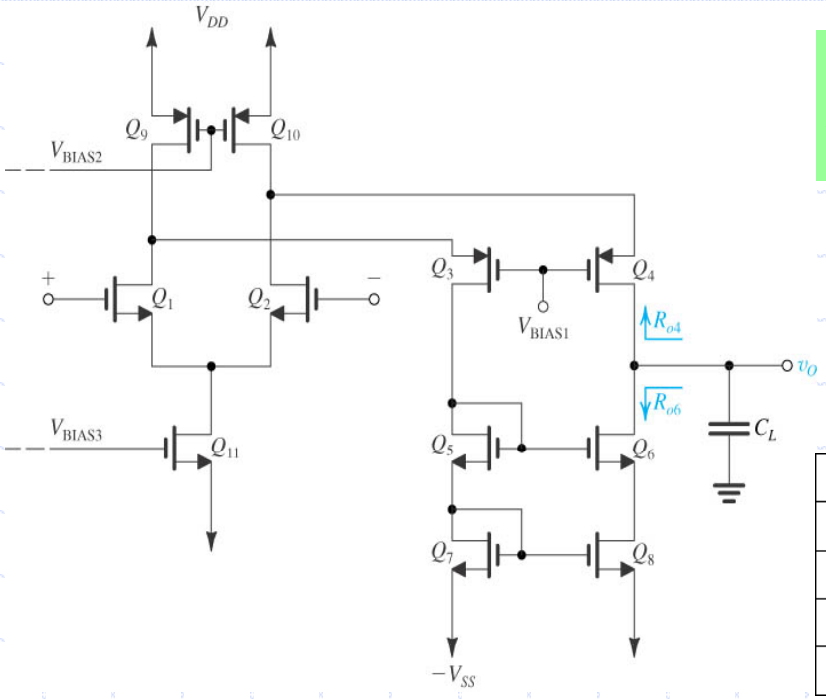
When $I_B > I$, the current that will flow into C_L will be

$I_4 - I_6 = I_B - (I_B - I) = I$

$$SR = \frac{I}{C_L} = 2\pi f_t V_{OV\,1}$$

9.2 The Folded-Cascode CMOS OP AMP

- Example 9.2



$$g_m = \frac{2I_D}{V_{OV}} = \frac{2I_D}{0.25}, \quad r_o = \frac{|V_A|}{I_D} = \frac{20}{I_D}, \quad \left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{k'V_{OV}^2}$$

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}
$I_D(\mu A)$	100	100	150	150	150	150	150	150	250	250	200
$g_m(mA/V)$	0.8	0.8	1.2	1.2	1.2	1.2	1.2	1.2	2.0	2.0	1.6
$r_o(k\Omega)$	200	200	133	133	133	133	133	133	80	80	100
W/L	32	32	120	120	48	48	48	48	200	200	64

9.2 The Folded-Cascode CMOS OP AMP

Example 9.2

Note that for all transistors,

$$g_m r_o = 160\text{V/V}, \quad V_{GS} = 1.0\text{V}$$

$$-V_{SS} + V_{OV11} + V_{OV1} + V_{tn} \le V_{ICM} \le V_{DD} - |V_{OV9}| + V_{tn}$$

$$\Rightarrow -1.25\text{V} \le V_{ICM} \le 3\text{V}$$

$$-V_{SS} + V_{OV7} + V_{OV5} + V_{tn} \le v_o \le V_{DD} - |V_{OV10}| - |V_{OV4}|$$

$$\Rightarrow -1.25\text{V} \le v_o \le 2\text{V}$$

$$R_{o4} \cong (g_{m4} r_{o4})(r_{o2} \| r_{o10}) = 160(200 \| 80) = 9.14M\Omega$$

$$R_{o6} \cong g_{m6} r_{o6} r_{o8} = 21.28M\Omega$$

$$\therefore R_o = R_{o4} \| R_{o6} = 6.4M\Omega$$

$$\therefore A_v = G_m R_o = 0.8 \times 10^{-3} \times 6.4 \times 10^6 = 5120\text{V/V}$$

9.2 The Folded-Cascode CMOS OP AMP

- Example 9.2

$$f_t = G_m R_o f_P = \frac{G_m}{2\pi C_L} = \frac{0.8\times10^{-3}}{2\pi\times5\times10^{-12}} = 25.5MHz$$

$$f_p = \frac{f_t}{A_v} = \frac{25.5MHz}{5120} = 5kHz$$

$$SR = \frac{I}{C_L} = \frac{200\times10^{-6}}{5\times10^{-12}} = 40\,\mathrm{V/\mu s}$$

Finally, to determine the power dissipation we note that the total current is 500μA=0.5mA, and the total supply voltage is 5V, thus

$$P_D = 5\times0.5 = 2.5\mathrm{mW}$$

9.2 The Folded-Cascode CMOS OP AMP

- Increasing the input common-mode range: Rail-to-rail input operation

An NMOS and a PMOS differential pair placed in parallel would provide an input stage with a common-mode range that exceeds the power supply voltage in both directions.

⇨ Rail-to-rail input operation

Each of the current increments indicated is equal to $G_m(V_{id}/2)$.

$$V_O = 2G_m R_O V_{id}, \qquad A_V = 2G_m R_O$$

This assumes that both differential pairs will be operating simultaneously.

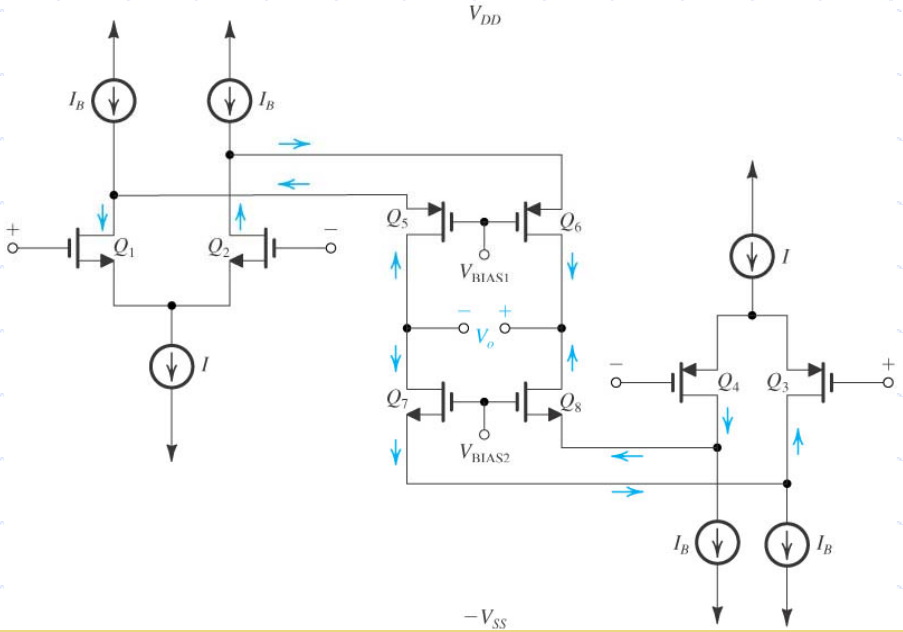


Figure 9.11 A folded-cascode op amp that employs two parallel complementary input stages to achieve rail-to-rail input common-mode operation. Note that the two "+" terminals are connected together and the two "–" terminals are connected together.

9.2 The Folded-Cascode CMOS OP AMP

- Increasing the output voltage range:
  The wide-swing current mirror

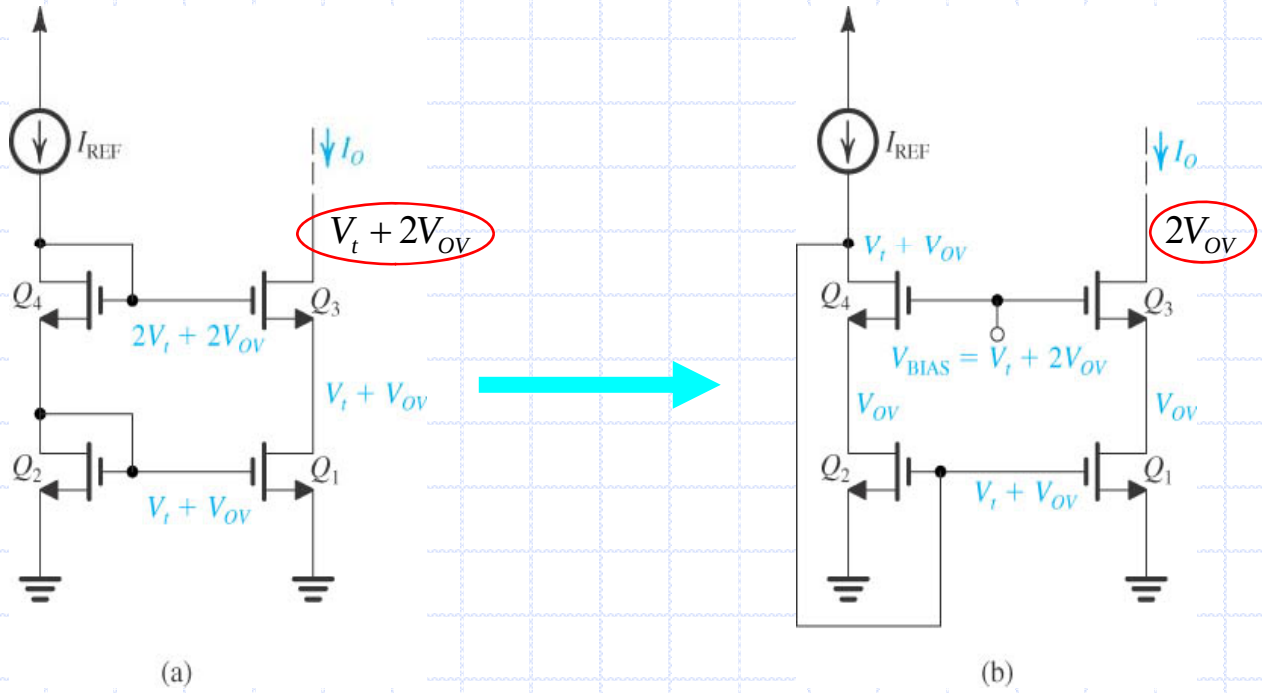


Figure 9.12 (a) Cascode current mirror with the voltages at all nodes indicated. Note that the minimum voltage allowed at the output is $V_t + V_{OV}$. (b) A modification of the cascode mirror that results in the reduction of the minimum output voltage to V_{OV}. This is the wide-swing current mirror.

9.3 The 741 OP-AMP Circuit

- The IC design philosophy
  - Mostly transistors
  - Relatively few resistors
  - Only one capacitor

  This philosophy is dictated by the economics (silicon area, ease of fabrication, quality of realizable components) of the fabrication of active and passive components in IC form.

- Two power supplies ($+V_{CC}$ and $-V_{EE}$)
  - Normally, $V_{CC}=V_{EE}=15V$
  - But the circuit also operates satisfactorily with $\pm 5V$.

- With a relatively large circuit, the first step in the analysis is the identification of its recognizable parts and their functions.

9.3 The 741 OP-AMP Circuit

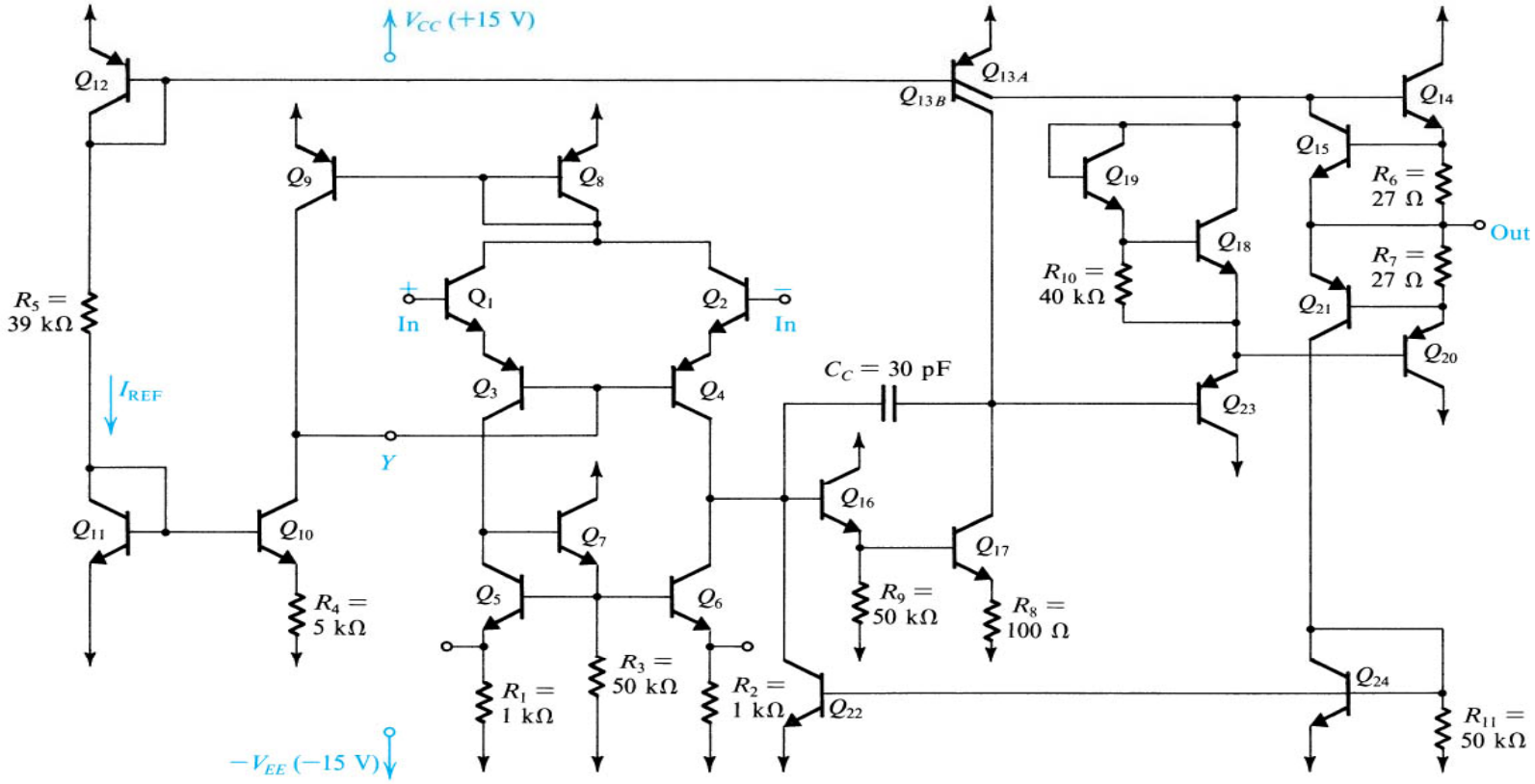
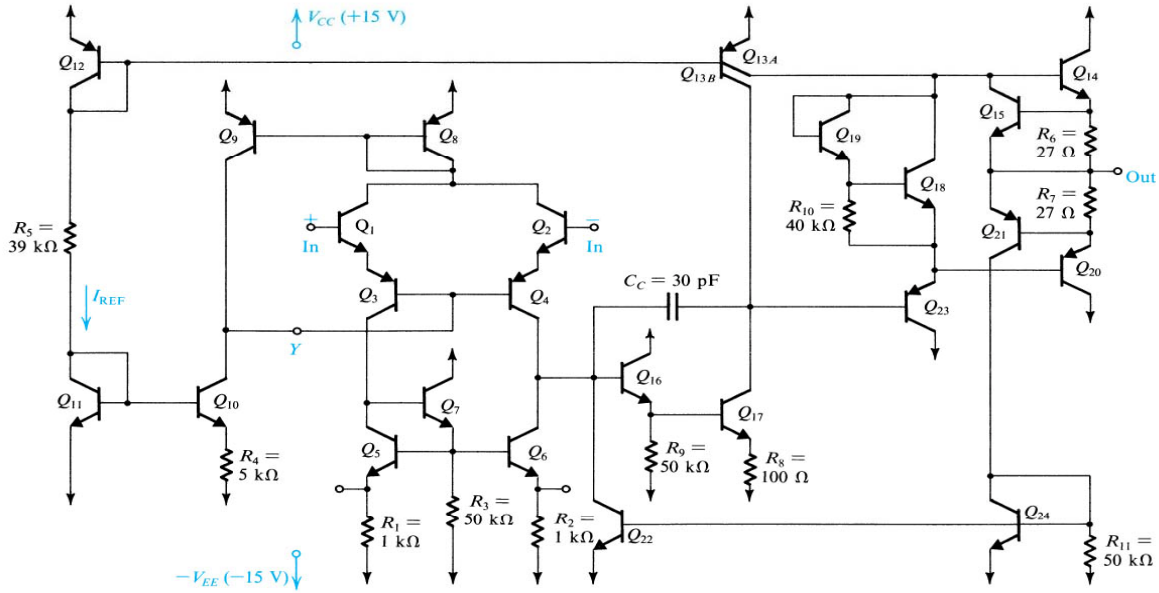


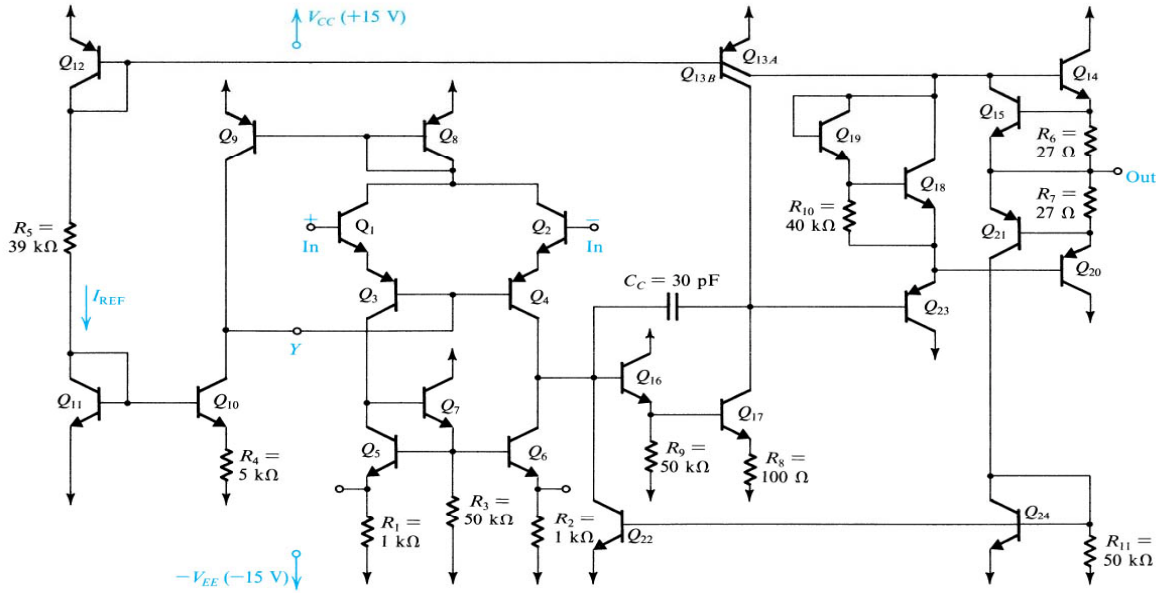
Figure 9.13 The 741 op-amp circuit. Q_{11}, Q_{12}, and R_5 generate a reference bias current, I_{REF}. Q_{10}, Q_9, and Q_8 bias the input stage, which is composed of Q_1 to Q_7. The second gain stage is composed of Q_{16} and Q_{17} with Q_{13B} acting as active load. The class AB output stage is formed by Q_{14} and Q_{20} with biasing devices Q_{13A}, Q_{18}, and Q_{19}, and an input buffer Q_{23}. Transistors Q_{15}, Q_{21}, Q_{24}, and Q_{22} serve to protect the amplifier against output short circuits and are normally cut off.

9.3 The 741 OP-AMP Circuit



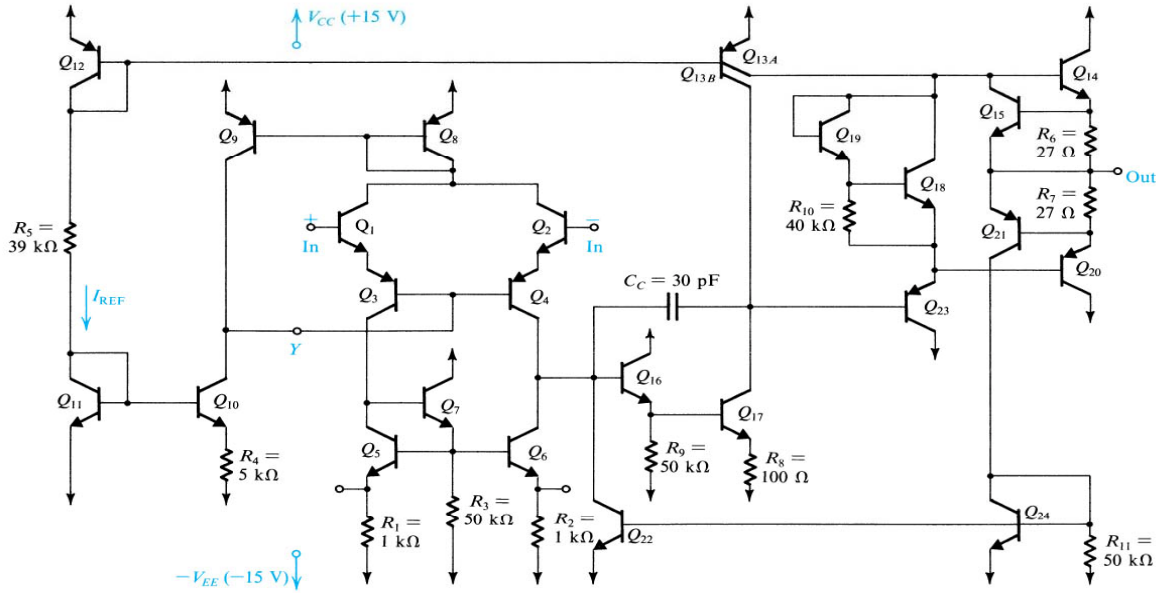
- **Bias Circuit**
  - Q_{11}, Q_{12}, R_5: I_{REF} (reference bias current)
  - Q_{11}, Q_{10}, R_4: Widlar current source
  - Q_8, Q_9: Current mirror, Q_{12},Q_{13A}, Q_{13B} : Current mirror
  - Q_{18}, Q_{19}: $2V_{BE}$ drops between Q_{14} and Q_{20}
- **Short-Circuit Protection Circuitry**
  - R_6, R_7, Q_{15}, Q_{21}, Q_{24}, R_{11}: normally off

9.3 The 741 OP-AMP Circuit



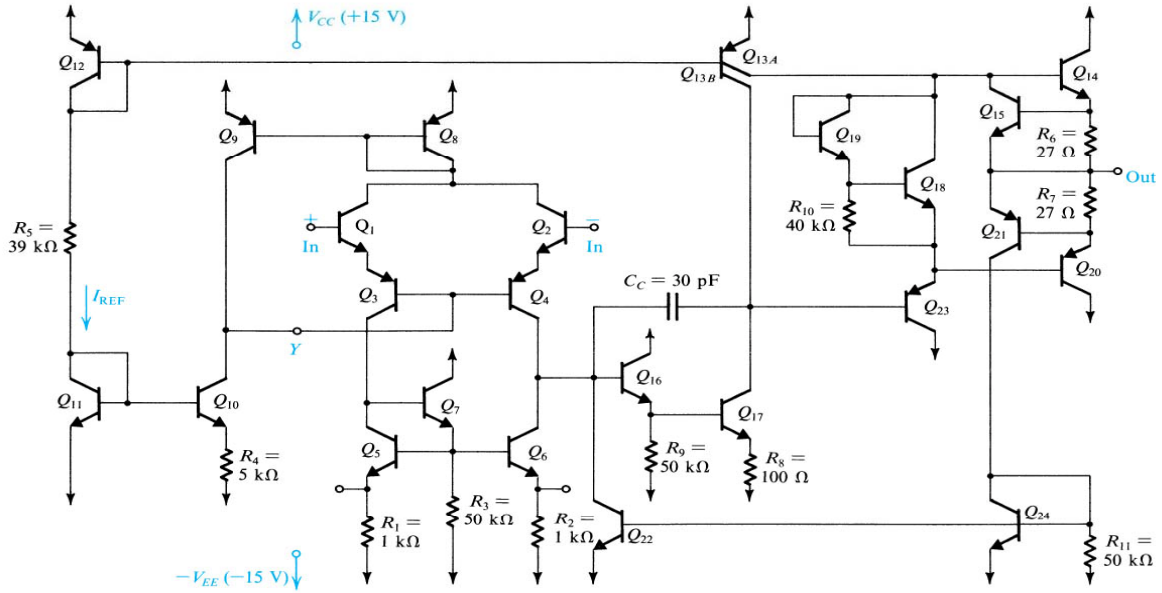
- **The input stage (Differential stage)**
  - Q_1~Q_7 with biasing performed by Q8~Q10
  - Q_1, Q_2 : Emitter follower, R_{in} high
  - Q_3, Q_4 : Common base amp, Level shifter, Q1,Q2 protection
    (npn: Breakdown 7V, pnp: Breakdown 50V)
  - Q_5, Q_6, Q_7, R_1, R_2, R_3 :
    Load circuit of input stage
    Current mirror (High resistance),
    Differential >> Single ended (Q_6 Collector)

9.3 The 741 OP-AMP Circuit



- **The second stage (Single ended high gain stage)**
  - Intermediate stage: Q_{16}, Q_{17}, Q_{13B}, R_8, R_9
  - Q_{16} : Emitter follower(High R_{in}), Q_{17} : Common emitter amp
  - Q_{13B} : Active load (High gain), C_C: Frequency compensation
  - Dominant pole : 4Hz, unity gain bandwidth : 1MHz

9.3 The 741 OP-AMP Circuit



- **The output stage (Buffering stage)**
  - Class AB output stage, Low R_{out}, Large load current
  - Q_{14}, Q_{20} : Complementary pair
  - Q_{18}, Q_{19} are fed by Q_{13A} and bias Q_{14}, Q_{20}
  - Q_{23} : Emitter follower (minimizing loading effect on second stage)

9.3 The 741 OP-AMP Circuit

- The output stage (buffering stage)
  - Class AB output stage is utilized in 741 Op-Amp

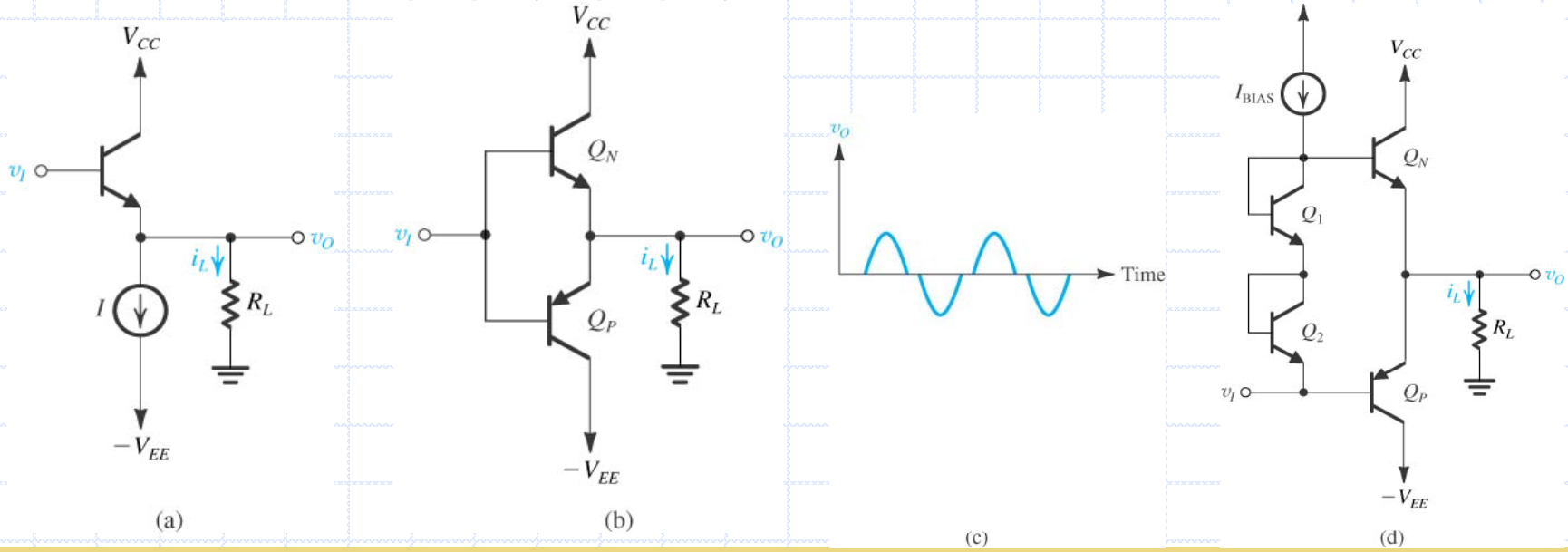
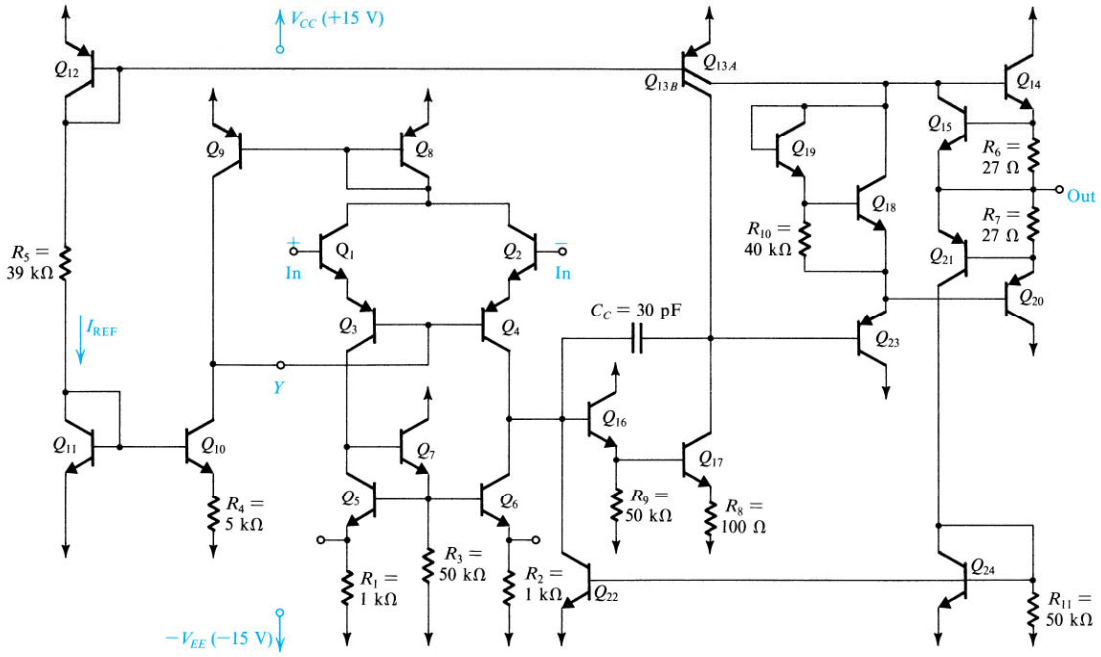


Figure 9.14 (a) The emitter follower is a class A output stage. (b) Class B output stage. (c) The output of a class B output stage fed with an input sinusoid. Observe the crossover distortion. (d) Class AB output stage.

9.3 The 741 OP-AMP Circuit

- Device parameters



For NPN $I_S = 10^{-14}$ A, $\beta = 200$, $V_A = 125$ V

For PNP $I_S = 10^{-14}$ A, $\beta = 50$, $V_A = 50$ V

For Multi-collector PNP $I_{SA} = 0.25 \times 10^{-14}$ A, $I_{SB} = 0.75 \times 10^{-14}$ A

9.4 DC Analysis of the 741

- Reference bias current

$$I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5} = 0.73mA \; (V_{CC} = V_{EE} = 15V, \; V_{BE11} = V_{EB12} \cong 0.7V)$$

- Input-stage bias

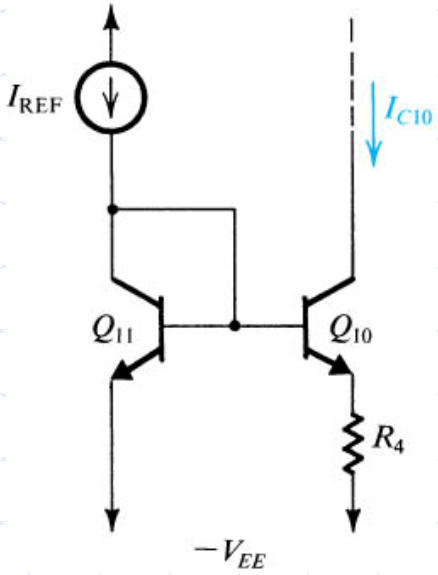


Figure 9.15 The Widlar current source.

- Widlar Current Source

$$V_{BE11} - V_{BE10} = I_{C10} R_4$$

$$V_T \ln \frac{I_{REF}}{I_{C10}} = I_{C10} R_4 \; (I_{S10} = I_{S11}) \Rightarrow I_{C10} = 19\mu A$$

9.4 DC Analysis of the 741

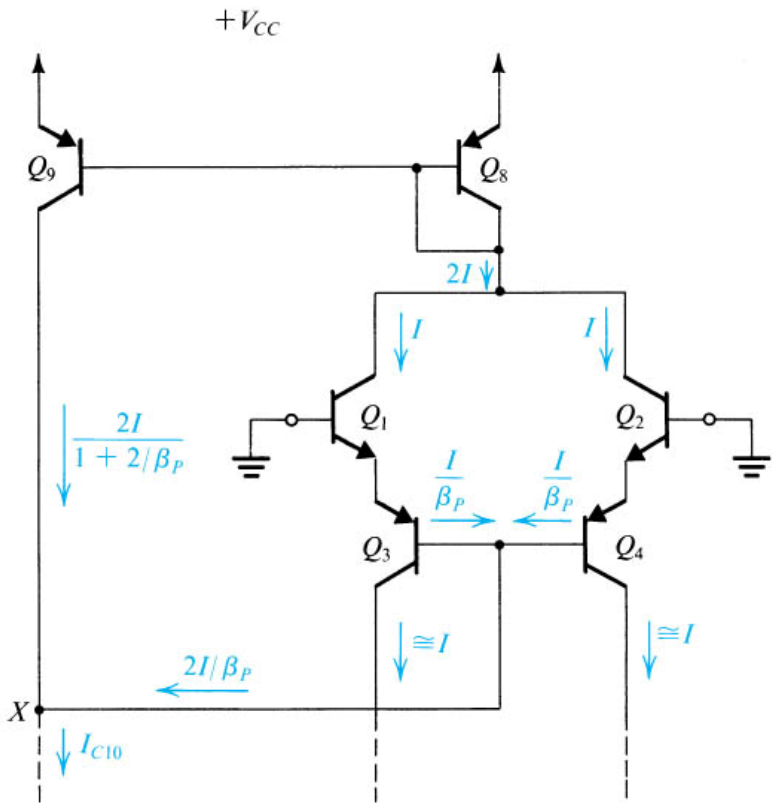


Figure 9.16 The dc analysis of the 741 input stage.

From symmetry $I_{C1} = I_{C2}$

If the npn β is high $I_{B3} = I_{B4} \cong I$

Q_3 and Q_4 base current : $\frac{I}{\beta_P + 1} \cong \frac{I}{\beta_P}$

Using the result in Eq.(6.21)

Q_8 and Q_9 current mirror : $I_{C9} = \frac{2I}{1 + 2/\beta_P}$

Node X : if $\beta_P >> 1, \quad 2I \cong I_{C10} = 19uA$

$$\therefore I = I_{C1} = I_{C2} \cong I_{C3} = I_{C4} = 9.5uA$$

Q_1 through Q_4,Q_8 and Q_9 : negative feedback loop

To stabilize $I \cong I_{C10}/2$

$$I \uparrow \Rightarrow I_{C8} \uparrow \Rightarrow I_{C9} \uparrow \Rightarrow$$

$$2I/\beta_P \downarrow (I_{C10}\ const) \Rightarrow I \downarrow$$

9.4 DC Analysis of the 741

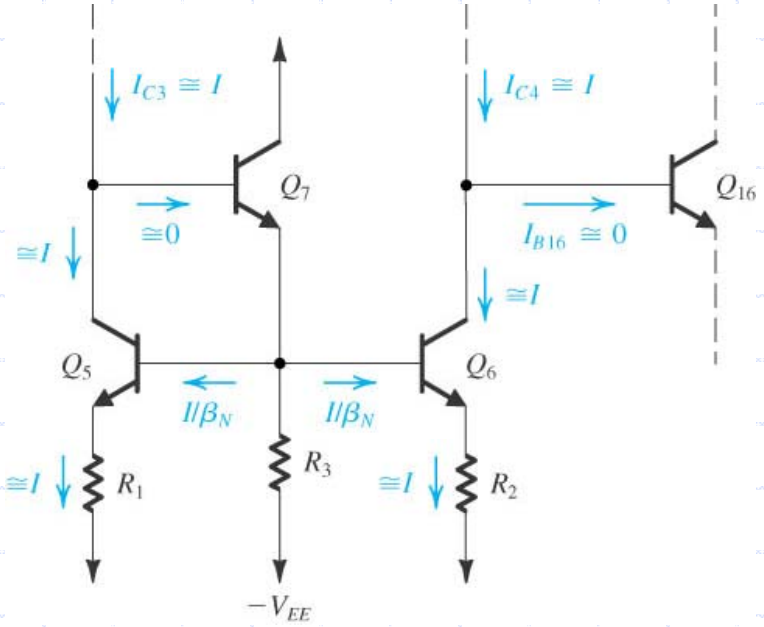


Figure 9.17 The dc analysis of the 741 input stage, continued.

If neglect the base current of Q_{16},Q_7

$$I_{C6} = I_{C5} \cong I$$

Q7 bias current

$$I_{C7} \cong I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3}$$

$$V_{BE6} = V_T \ln \frac{I}{I_S} = 25mV \ln \frac{9.5uA}{10^{-14} A} = 517m$$

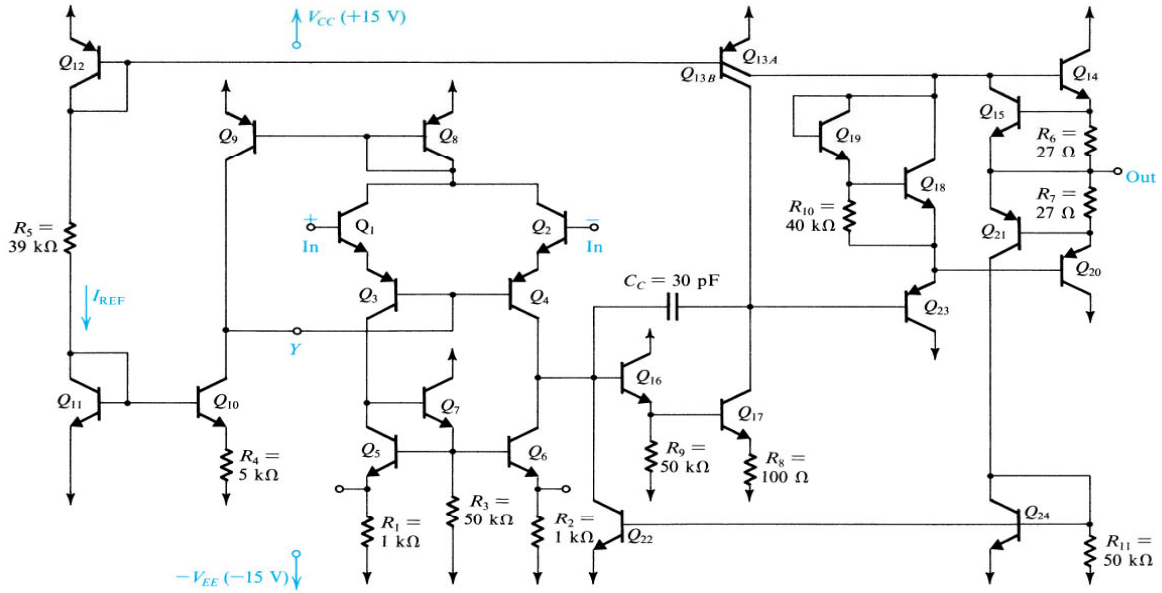
$$\Rightarrow I_{C7} = 10.5uA$$

Input Bias and Offset Currents

$$I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{I}{\beta_N} = 9.5/200 = 47.5nA$$

input offset current $I_{OS} = |I_{B1} - I_{B2}|$

9.4 DC Analysis of the 741



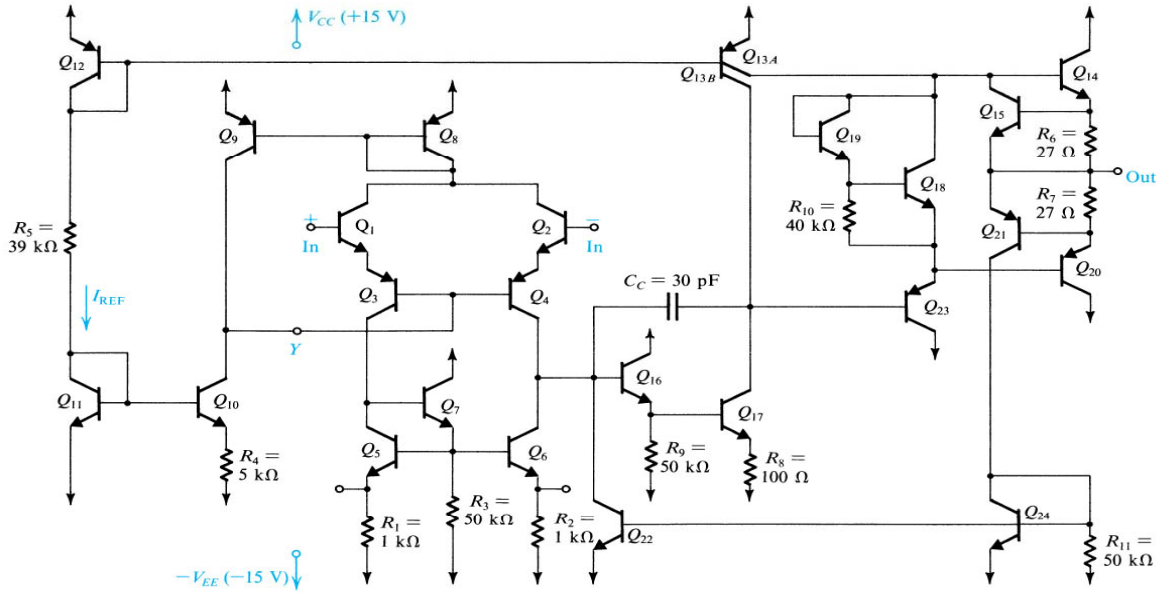
- **Input offset voltage**

  V_{OS} : differential input voltage to reduce the output current to zero

- **Input common-mode range**

  Input stage remains in the linear active mode
  The upper end by saturation of Q_1, Q_2
  The lower end by saturation of Q_3, Q_4

9.4 DC Analysis of the 741



- **Second-stage bias (Fig. 9.13)**

$$I_{C13B} = 0.75 I_{REF} \text{ (by Emitter Area Ratio)} = 550\mu\text{A} = I_{C17}$$

$$Q_{17} \Rightarrow V_{BE17} = V_T \ln \frac{I_{C17}}{I_S} = 618mV,\ V_{B17} = I_{E17} R_8 + V_{BE17}$$

$$Q_{16} \Rightarrow I_{C16} \cong I_{E16} = I_{B17} + \frac{V_{B17}}{R_9} = 16.2\mu A$$

9.4 DC Analysis of the 741

Output-stage bias

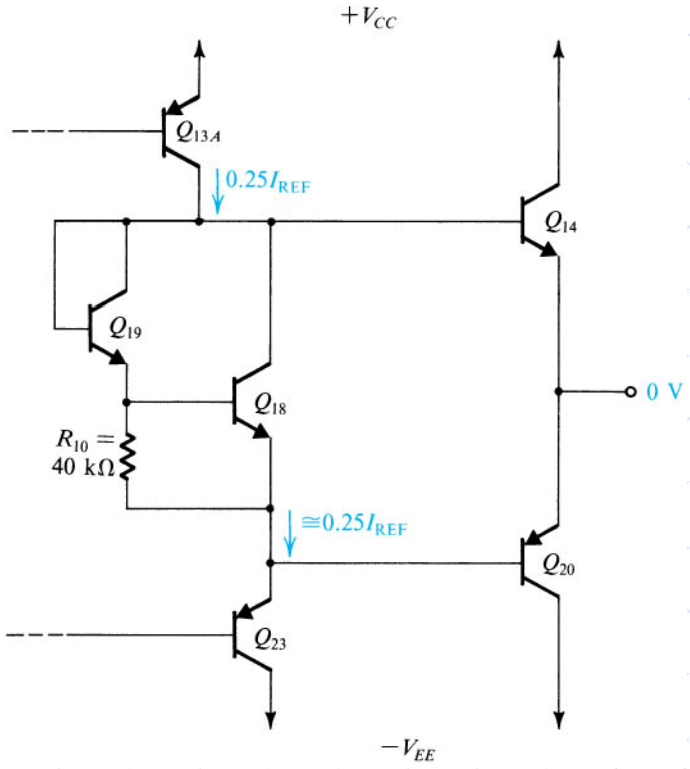


Figure 9.18 The 741 output stage without the short-circuit protection devices.

If neglect the base current of Q_{14},Q_{20}

$$I_{C23} \cong I_{E23} \cong 0.25 I_{REF} = 180uA$$

If V_{BE18} is 0.6V,

$$I_{R10} = \frac{0.6}{40k} = 15uA$$

$$I_{E18} = 180 - 15 = 165uA \cong I_{C18}$$

$$\Rightarrow V_{BE18} = V_T \ln \frac{I_{C18}}{I_S} \cong 588mV$$

$$in\ Q_{18}, I_{B18} = 165/200 = 0.8uA$$

$$\Rightarrow I_{C19} \cong I_{E19} = 15.8uA$$

$$in\ Q_{19}, V_{BE19} = V_T \ln \frac{I_{C19}}{I_S} = 530mV$$

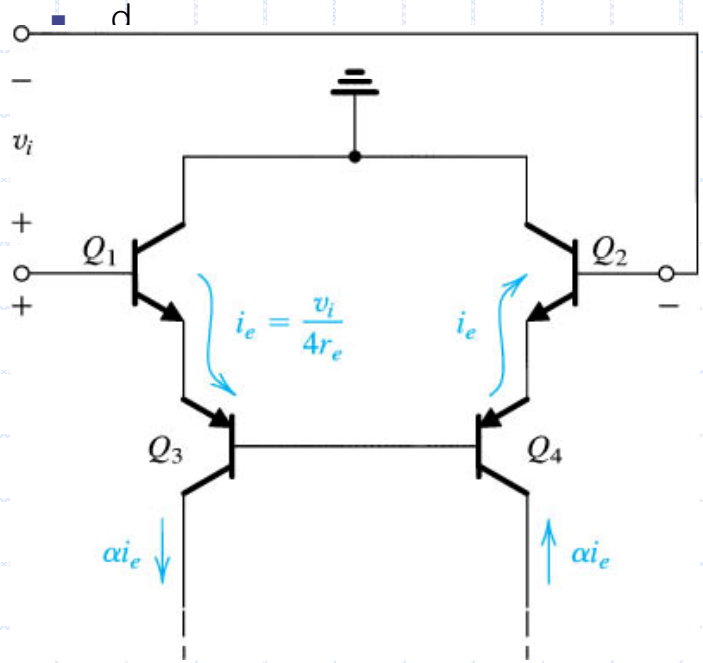
$$V_{BB} = V_{BE18} + V_{BE19} = 588 + 530 = 1.118V$$

$$Also,\ V_{BB} = V_T \ln \frac{I_{C14}}{I_{S14}} + V_T \ln \frac{I_{C20}}{I_{S20}}$$

$$\Rightarrow\ I_{C14} = I_{C20} = 154uA$$

9.5 Small-Signal Analysis of the 741 Input Stage

The Input Stage



- Differential signal v_i
- Four emitter resistances connected in series $4 \cdot r_e$

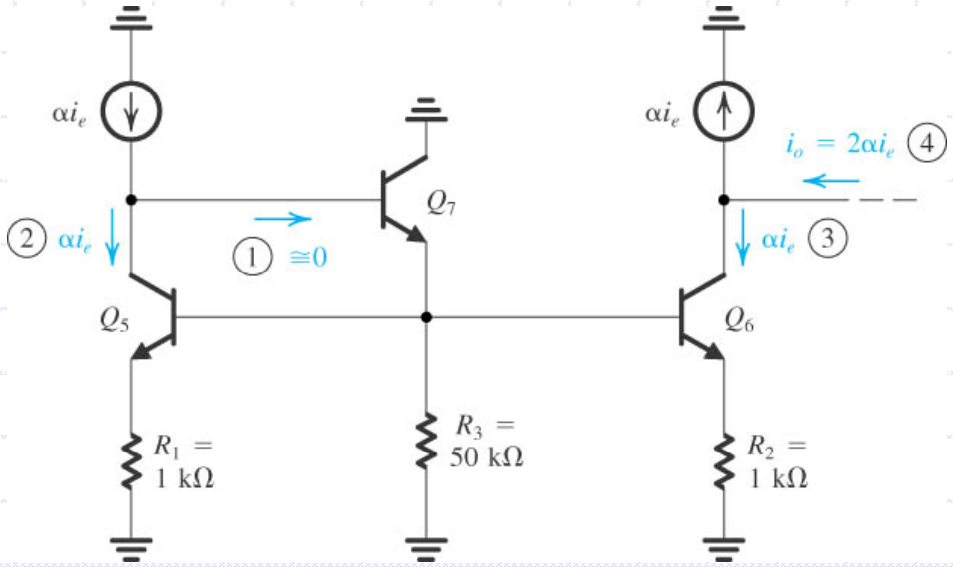
$$i_e = \frac{v_i}{4r_e},\ r_e = \frac{V_T}{I} = \frac{25mV}{9.5uA} = 2.63\ k\Omega$$

- Input resistance

$$R_{id} = 4 \cdot (\beta_N + 1) \cdot r_e = 2.1\ M\Omega$$

Figure 9.19 Small-signal analysis of the 741 input stage.

9.5 Small-Signal Analysis of the 741 Input Stage



i_{b7} : neglected

$i_{c5} = \alpha i_e$

Q_5, Q_6 identical : $i_{c5} = i_{c6}$

output node : $i_o = 2\alpha i_e$

Figure 9.20 The load circuit of the input stage fed by the two complementary current signals generated by Q_1 through Q_4 in Fig. 9.19. Circled numbers indicate the order of the analysis steps.

The transconductance of the input stage

$$G_{m1} \equiv \frac{i_o}{v_i} = \frac{2 \cdot \alpha \cdot i_e}{4 \cdot r_e \cdot i_e} = \frac{\alpha}{2r_e} \quad (r_e = 2.63\,\text{k}\Omega, \alpha \cong 1, G_{m1} = 1/5.26\,\text{mA/V})$$

9.5 Small-Signal Analysis of the 741 Input Stage

- Output resistance

  (current source of Q_4) || (output resistance of Q_6)

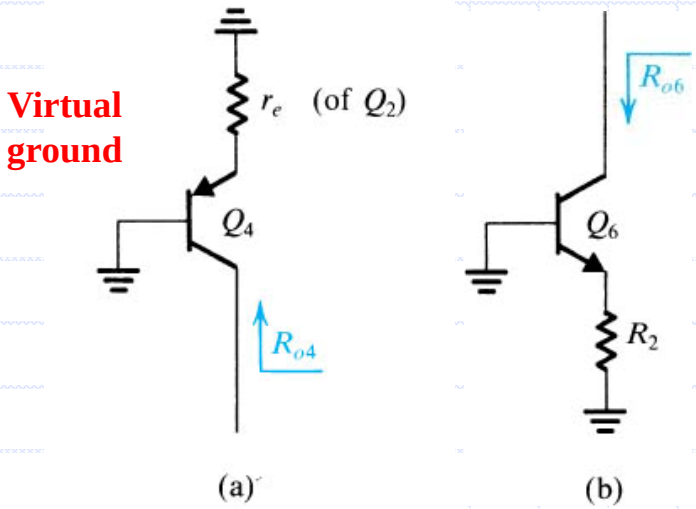


Figure 9.21 Simplified circuits for finding the two components of the output resistance R_{o1} of the first stage.

$$r_o = \frac{V_A}{I} = \frac{50V}{9.5\mu A} = 5.26M\Omega$$

$$R_{o4} = r_o[1 + g_m(r_e \,//\, r_\pi)] = 10.5M\Omega$$

$$i_b \cong 0$$

$$R_{o6} = r_o[1 + g_m(R_2 \,//\, r_\pi)] = 18.2M\Omega$$

$$\Rightarrow\ R_{o1} = R_{o4} \,//\, R_{o6} = 6.7M\Omega$$

9.5 Small-Signal Analysis of the 741 Input Stage

- Small signal equivalent circuit of input stage

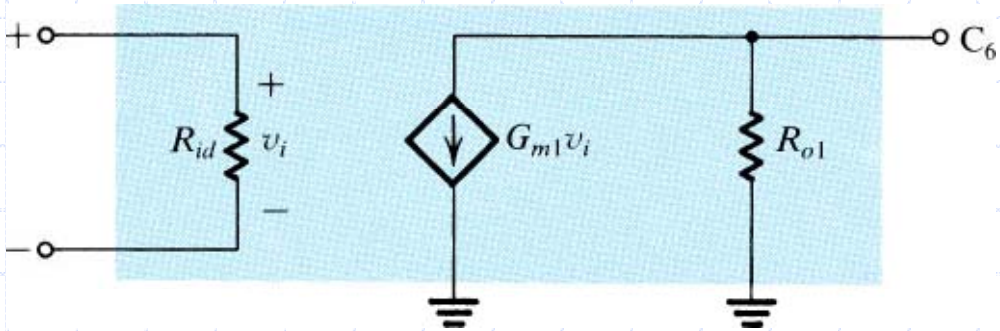


Figure 9.22 Small-signal equivalent circuit for the input stage of the 741 op amp.

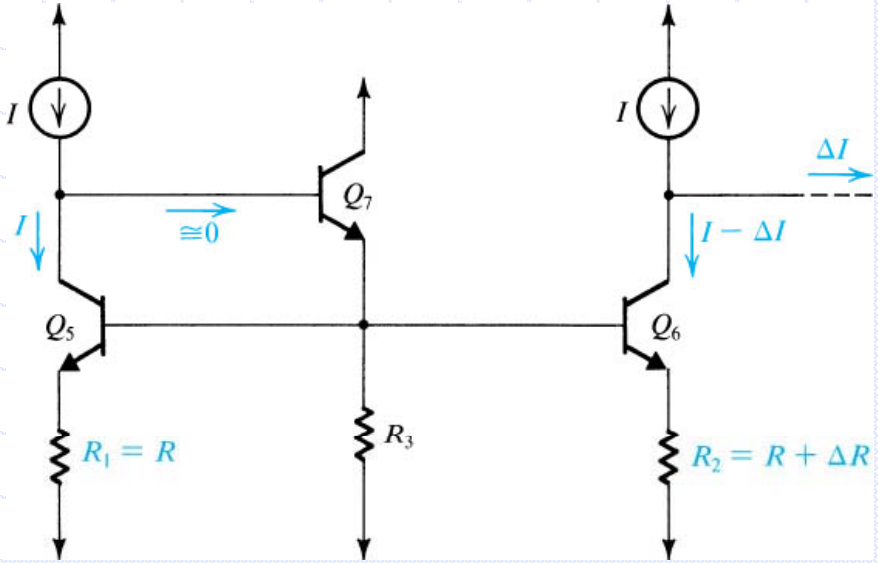
$$R_{id} = 2.1M\Omega$$

$$G_{m1} = 1/5.26\ mA/V$$

$$R_{o1} = 6.7M\Omega$$

9.5 Small-Signal Analysis of the 741 Input Stage

Example 9.3



$$R_1 = R,\ R_2 = R + \Delta R \text{ where } \frac{\Delta R}{R} = 0.02$$

current in $Q_6 \Rightarrow \Delta I$ decreasing

$$V_{BE5} + IR = V_{BE6} + (I - \Delta I)(R + \Delta R)$$

$$V_{BE5} - V_{BE6} = I\Delta R - \Delta I(R + \Delta R) \cong \Delta I r_e$$

$$\therefore \ \frac{\Delta I}{I} = \frac{\Delta R}{R + \Delta R + r_e} = 5.5 \times 10^{-3}$$

To reduce ΔI to zero, we have to apply an input voltage V_{OS}

$$V_{OS} = \frac{\Delta I}{G_{m1}} = \frac{5.5 \times 10^{-3} I}{G_{m1}} \cong 0.3mV$$

9.5 Small-Signal Analysis of the 741 Input Stage

The second stage

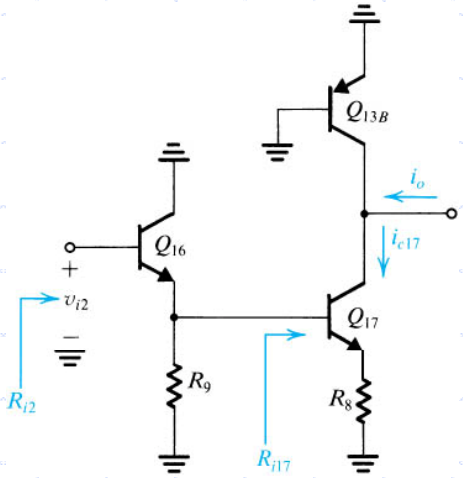


Figure 9.24 The 741 second stage prepared for small-signal analysis.

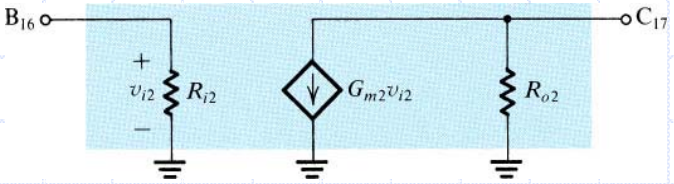


Figure 9.25 Small-signal equivalent circuit model of the second stage.

- Input resistance by inspection

$$R_{i2} = (\beta_{16}+1)[r_{e16} + R_9 \,||\, (\beta_{17}+1)(r_{e17}+R_8)]$$
$$R_{i2} \cong 4M\Omega$$

- Transconductance

$-G_{m2}$: short-circuit output current to input voltage($i_{c13B} = 0$)

$$\Rightarrow\ i_o = i_{c17} = G_{m2} v_{i2}$$

$$i_{c17} = \frac{\alpha v_{b17}}{r_{e17}+R_8},\quad v_{b17} = v_{i2}\frac{(R_9 \,//\, R_{i17})}{(R_9 \,//\, R_{i17}) + r_{e16}}$$

$$R_{i17} = (\beta_{17}+1)(r_{e17}+R_8)$$

$$\therefore G_{m2} \equiv \frac{i_{c17}}{v_{i2}} = 6.5mA/V$$

9.5 Small-Signal Analysis of the 741 Input Stage

The second stage

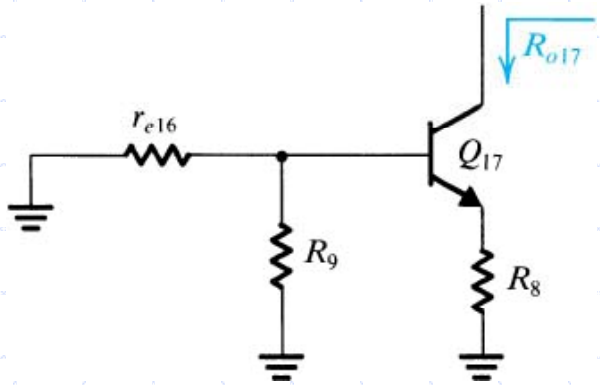


Figure 9.26 Definition of R_{o17}.

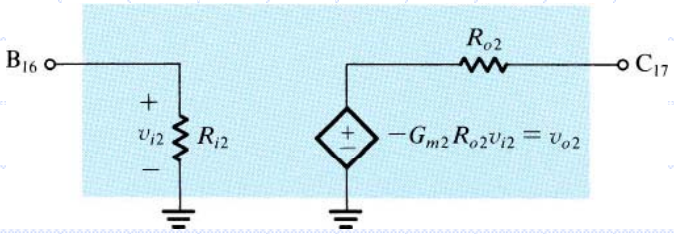


Figure 9.27 Thévenin form of the small-signal model of the second stage.

- Output resistance

  - R_{o2} : output resistance of second stage

  $R_{o2} = (R_{o13B} // R_{o17})$

  - Q_{13B} base and emitter grounded

  $R_{o13B} = r_{o13B} = 90.9\text{k}\Omega$

  - $R_{o17} = r_{o17}[1 + g_{m17}(R_8 // r_{\pi 17})] = 787k\Omega$

  $(r_{e16} // R_9 << r_{\pi 17})$

  $\Rightarrow \; R_{o2} = R_{o13B} // R_{o17} = 81k\Omega$

- Thévenin Equivalent circuit

  $Thevenin \text{ form} : v_{o2} = -G_{m2}R_{o2}v_{i2}$

  $open-circuit \; voltage \; gain : \; -G_{m2}R_{o2}$

9.5 Small-Signal Analysis of the 741 Input Stage

The output stage

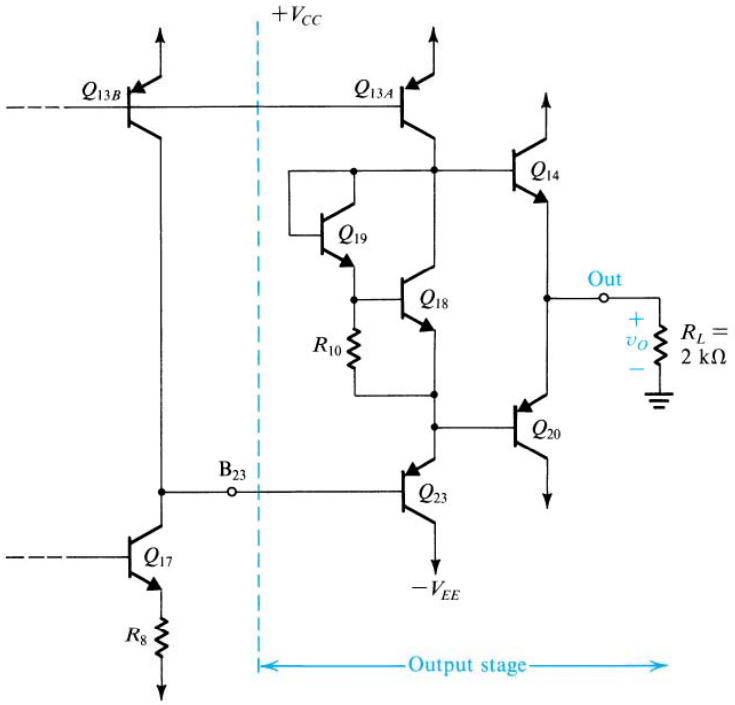


Figure 9.28 The 741 output stage.

- Output voltage limits
  - when Q_{13A} is saturated

$$v_{o\max} = V_{CC} - V_{CEsat} - V_{BE14}$$

$$(1V \text{ below } V_{CC})$$

  - when Q_{17} is saturated

$$v_{o\min} = -V_{EE} + V_{CEsat} + V_{EB23} + V_{EB20}$$

$$(1.5V \text{ above } -V_{EE})$$

9.5 Small-Signal Analysis of the 741 Input Stage

The output stage

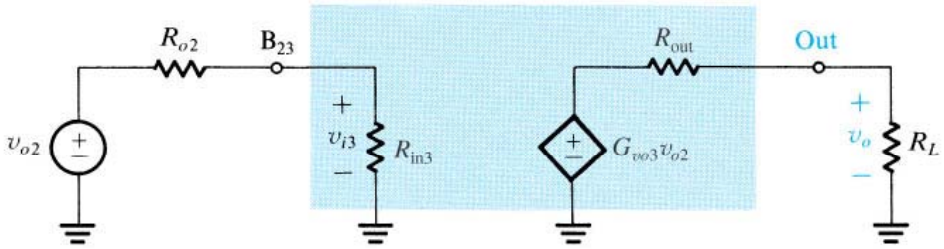


Figure 9.29 Model for the 741 output stage. This model is based on the amplifier equivalent circuit presented in Table 5.5 as "Equivalent Circuit C."

- Open-circuit output voltage of the second stage

$$v_{o2} = -G_{m2}R_{o2}v_{i2}$$

- Second stage voltage gain

$$A_2 \equiv \frac{v_{i3}}{v_{i2}} = -G_{m2}R_{o2}\frac{R_{in3}}{R_{in3}+R_{o2}}$$

- Input resistance

$$R_{in3} = f(R_L)$$

$$assume\ Q_{20}\ active,\ R_{b20} = r_{\pi 23} + \beta_{20}R_L \cong 100k\Omega,\ r_{o13A} \cong 280k\Omega,\ R\ of\ Q_{18} - Q_{19}\ negligible$$

$$\Rightarrow total\ resistance\ in\ the\ emitter\ of\ Q_{23}: r_{o13A} \| R_{b20} = 74k\Omega$$

$$\therefore R_{in3} \cong \beta_{23} \times 74k\Omega = 3.7M\Omega,\ \ A_2 = -515\ V/V$$

9.5 Small-Signal Analysis of the 741 Input Stage

The output stage

- Open-circuit overall voltage gain of the output stage

$$R_L = \infty \rightarrow G_{vo3} = \left.\frac{v_o}{v_{o2}}\right|_{R_L=\infty} \cong 1$$

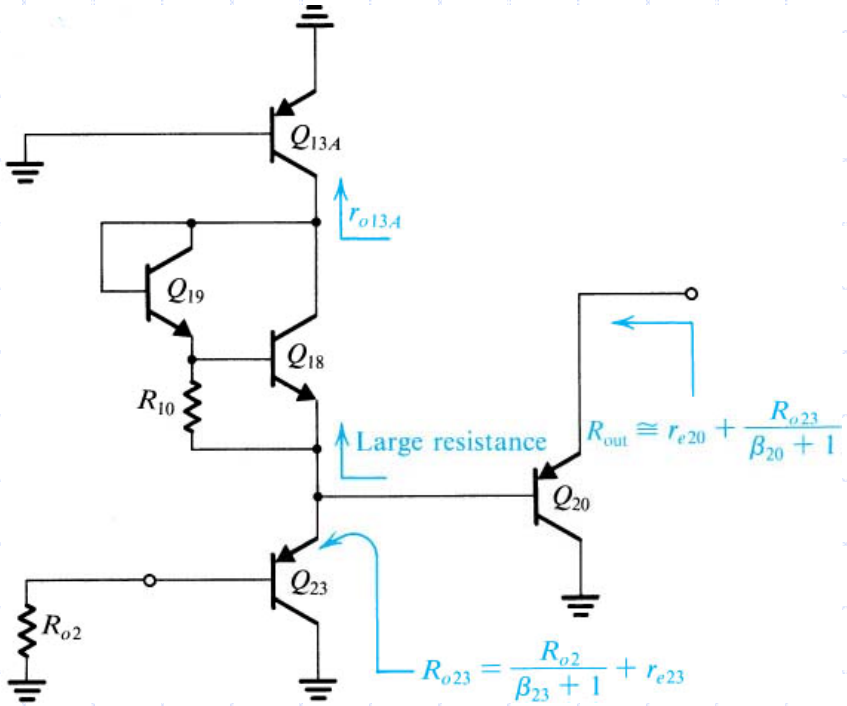


Figure 9.30 Circuit for finding the output resistance R_{out}.

- Output resistance

$$R_o = f(I_L, Q_{20}\text{on}/Q_{14}\text{off} \text{ or } Q_{20}\text{off}/Q_{14}\text{on})$$

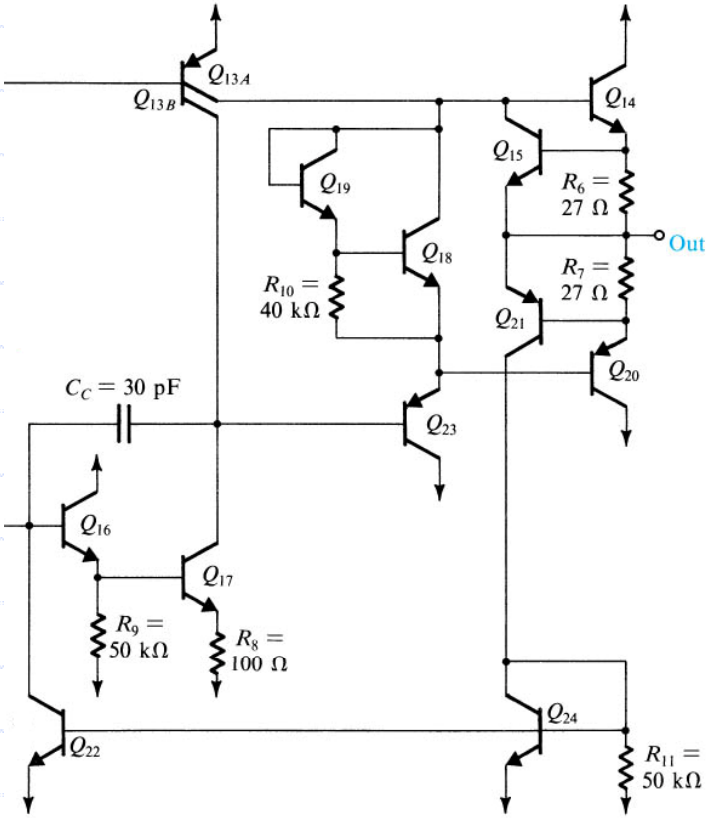
v_o : negative $\Rightarrow$ Q_{20} *active*

$$R_{o23} = \frac{R_{o2}}{\beta_{23}+1} + r_{e23} = 1.73k\Omega << r_{o13A}(0.28M\Omega)$$

$$\Rightarrow R_o \cong \frac{R_{o23}}{\beta_{20}+1} + r_{e20} = 39\Omega \ (if \ I_L = 5mA)$$

9.5 Small-Signal Analysis of the 741 Input Stage

The output stage



- Output short-circuit protection

  - Output terminal Short-circuited
    ⇒ Large current ⇒ Burnout of IC

  - Short-Circuit Protection
    ⇒ limit the current in the output TR
  - In Fig 9.13

    $\text{If } I_{E14} > 20\text{mA}(\text{Q}_{14}),\ V_{BE15} = R_6 I_{E14} > 540mV$

    $\Rightarrow$ Turn on Q_{15}, $I_{C15} \uparrow \Rightarrow I_{B14} \downarrow$

    limit the maximum current that OP Amp can source to about 20mA

9.6 Gain, frequency response, and slew rate of the 741

- Small-signal gain

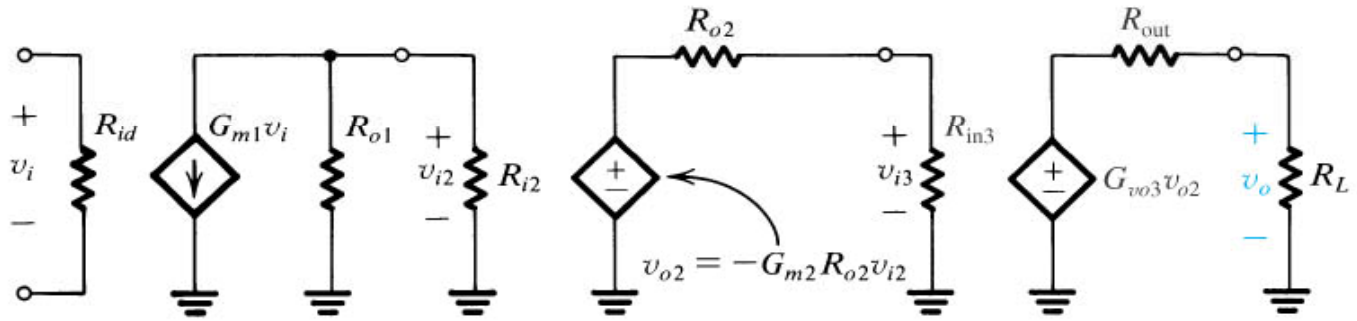


Figure 9.31 Cascading the small-signal equivalent circuits of the individual stages for the evaluation of the overall voltage gain.

$$\frac{v_o}{v_i} = \frac{v_{i2}}{v_i}\frac{v_{o2}}{v_{i2}}\frac{v_o}{v_{o2}}$$

$$= -G_{m1}(R_{o1} /\!/ R_{o2})(-G_{m2}R_{o2})G_{vo3}\frac{R_L}{R_L + R_o}$$

$$= -476.1 \times (-526.5) \times 0.97 = 243{,}147 \text{ V/V}$$

$$= 107.7 \; dB$$

9.6 Gain, frequency response, and slew rate of the 741

Frequency response

- Using Miller's theorem in second stage C_C, the effective capacitance

$$C_{in} = C_C(1+|A_2|) = 30p(1+515) = 15480pF$$

A_2 : the second-stage gain

- This capacitance is quite large, we neglect all other C between Q_{16} and signal ground
- The total R between this node and ground

$$R_t = (R_{O1} \| R_{i2}) = (6.7M\Omega \| 4M\Omega) = 2.5M\Omega$$

- The dominant pole

$$f_p = \frac{1}{2\pi C_{in} R_t} = 4.1Hz$$

9.6 Gain, frequency response, and slew rate of the 741

Frequency response

- The unity-gain bandwidth f_t

$$f_t = A_0 f_{3dB} = 243147 \times 4.1 \cong 1MHz$$

- The phase shift at f_t is -90°
- The phase margin is 90°
- This phase margin is sufficient to provide stable operation for closed loop amp with any value of β

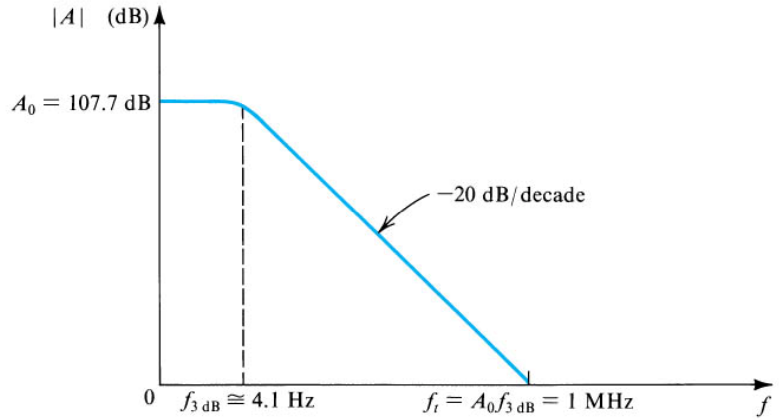


Figure 9.32 Bode plot for the 741 gain, neglecting nondominant poles.

9.6 Gain, frequency response, and slew rate of the 741

- The high-gain second stage (C_c)

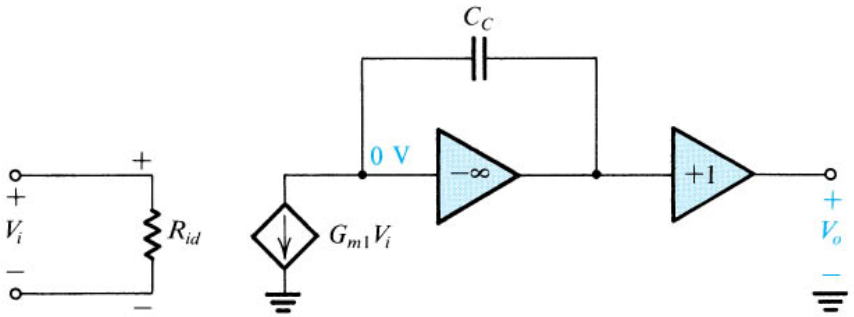


Figure 9.33 A simple model for the 741 based on modeling the second stage as an integrator.

- The second stage gain is large (The output R of the input stage and the input R of the second stage have been omitted)

$$A(s) \equiv \frac{V_o(s)}{V_i(s)} = \frac{G_{m1}}{sC_C} \Rightarrow A(jw) = \frac{G_{m1}}{j\omega C_C}$$

- The magnitude of gain becomes unity at $\omega=\omega_t$

$$\omega_t = \frac{G_{m1}}{C_C} \quad f_t = \frac{\omega_t}{2\pi} \cong 1MHz \quad (G_{m1} = 1/5.26mA/V \text{ and } C_C = 30pF)$$

9.6 Gain, frequency response, and slew rate of the 741

Slew rate

- The large input voltage causes the input stage to be overdriven, and its small-signal model no longer applies

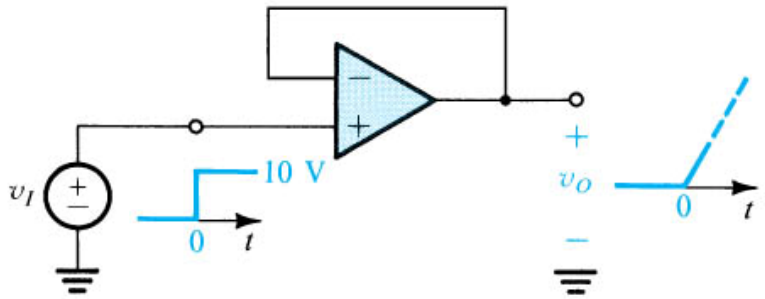


Figure 9.34 A unity-gain follower with a large step input. Since the output voltage cannot change instantaneously, a large differential voltage appears between the op-amp input terminals.

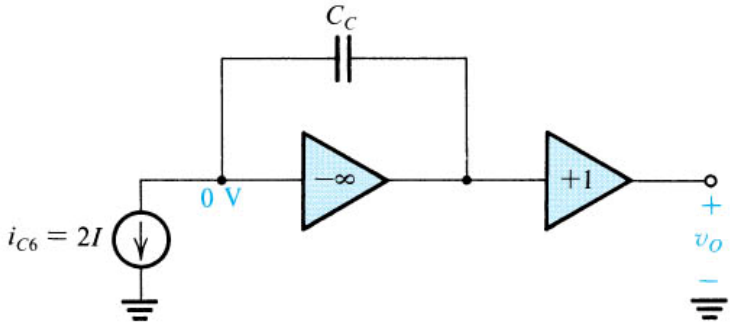


Figure 9.35 Model for the 741 op amp when a large positive differential signal is applied.

$$t > 0^+,\ V_+ - V_- = 10V$$
$$\Rightarrow Q_1, Q_3\ on\ and\ \ Q_2, Q_4\ off$$
$$\Rightarrow I_{c3} = I_{c6} = 2I$$

$$v_o(t) = v_c = \frac{\int i_C dt}{C_C} = \frac{2I}{C_C}t$$

$$\omega_t = \frac{G_{m1}}{C_C},$$

$$SR = \frac{2I}{C_C} = \frac{2(9.5\mu)}{30p} = 0.63V/\mu s$$

9.6 Gain, frequency response, and slew rate of the 741

- Relationship between f_t and SR

$$G_{m1} = 2\frac{1}{4r_e}$$

r_e: Emitter resistance of each of Q_1 through Q_4

$$r_e = \frac{V_T}{I}, \quad G_{m1} = \frac{I}{2V_T}$$

$$therefore \ \ \omega_t = \frac{I}{2C_C V_T} = \frac{SR}{4V_T}$$

$$SR = 4V_T\omega_t = 4\times 25\times 10^{-3}\times 2\pi\times 10^6 = 0.63V/\mu s \ (for\ 741)$$

9.7 Data Converters – An Introduction

Digital processing of signals

- Convert the signal from analog to digital form and then use digital ICs to perform digital signal processing
- The digital signal processor can perform a variety of arithmetic and logic operations that implement a filtering algorithm
- Analog to digital converter (ADC)

  Accept an analog sample and produce an N-bit digital word
- Digital to analog converter (DAC)

  Accept an N-bit digital word and produce an analog sample

9.7 Data Converters – An Introduction

- Sampling of analog signals
  - Sample-and-hold

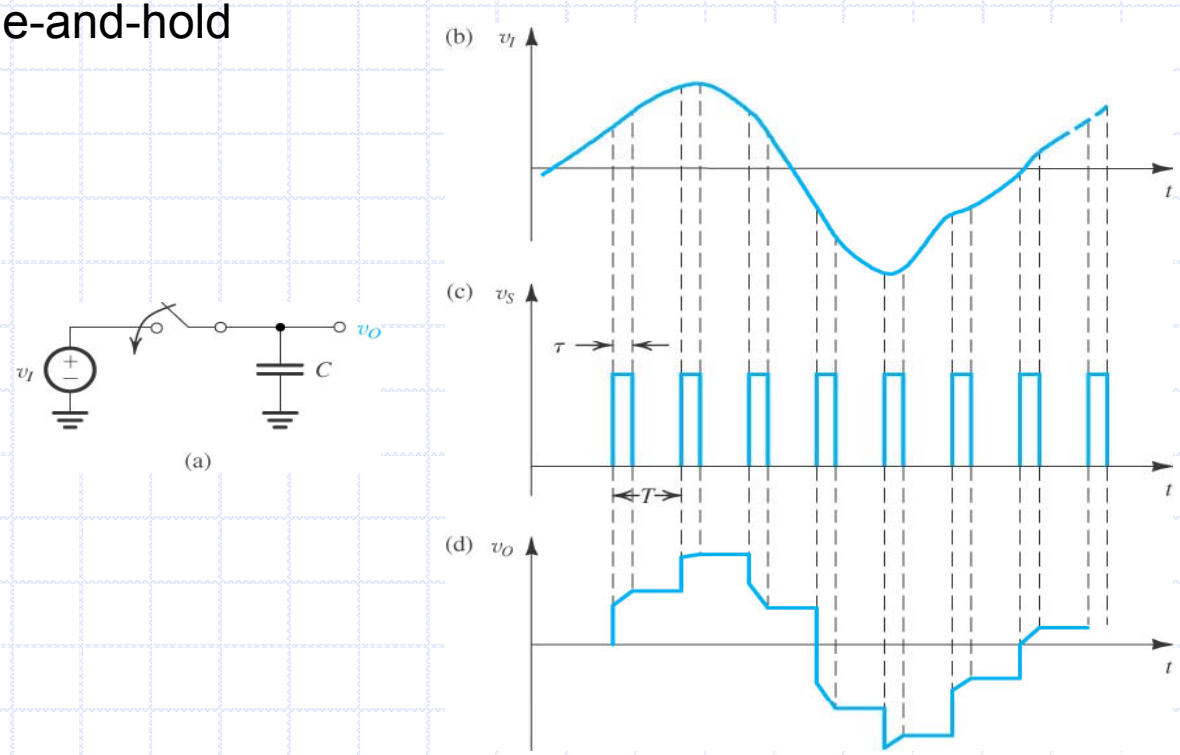


Figure 9.36 The process of periodically sampling an analog signal. (a) Sample-and-hold (S/H) circuit. The switch closes for a small part (*t* seconds) of every clock period (*T*). (b) Input signal waveform. (c) Sampling signal (control signal for the switch). (d) Output signal (to be fed to A/D converter).

9.7 Data Converters – An Introduction

Signal quantization

- Consider: 0~10V
- Assuming that we wish to convert this signal to digital form and that the required output is a 4-bit digital signal

0V → 0000
2/3V → 0001
6V → 1001
10V → 1111

$$resolution = \frac{10V}{15} = \frac{2}{3}V$$

- Example: the case of a 6.2V analog level (between 18/3 and 20/3) →18/3 (6V)
- Quantization error
- Use of more bits reduces quantization error

9.7 Data Converters – An Introduction

- The A/D and D/A converters as functional blocks

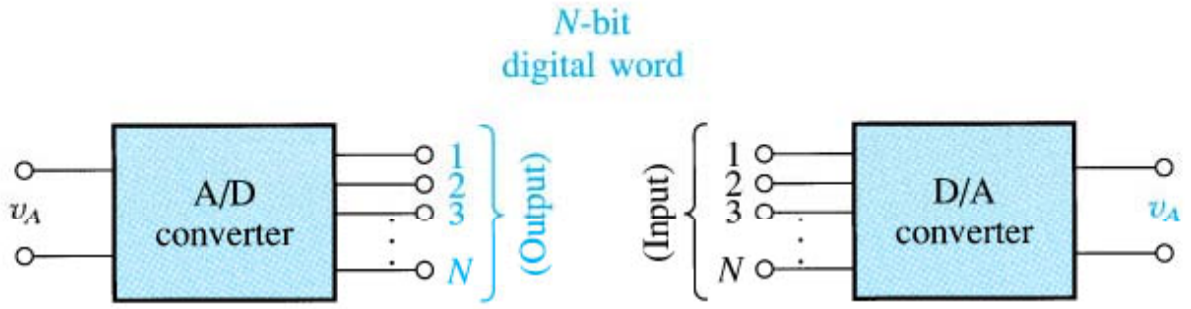


Figure 9.37 The A/D and D/A converters as circuit blocks.

9.7 Data Converters – An Introduction

- The A/D and D/A converters as functional blocks

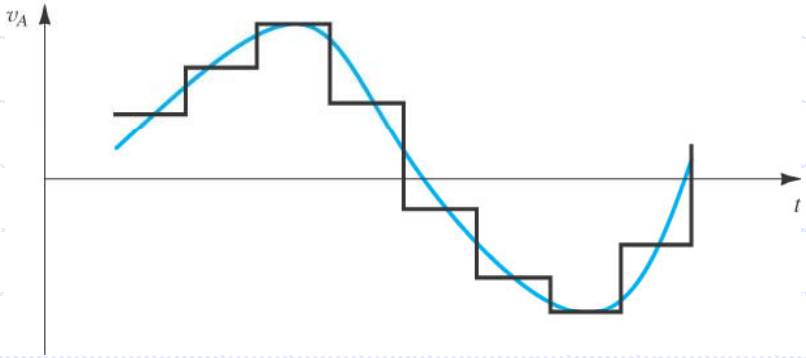


Figure 9.38 The analog samples at the output of a D/A converter are usually fed to a sample-and-hold circuit to obtain the staircase waveform shown. This waveform can then be filtered to obtain the smooth waveform, shown in color. The time delay usually introduced by the filter is not shown.

- The analog samples at the output of a D/A converter are usually fed to a sample-and-hold circuit to obtain the staircase waveform
- This waveform can then be smoothed by a low-pass filter, giving rise to the smooth curve in color in Fig.9.38

9.8 D/A Converter Circuits

- Basic circuit using binary-weighted resistors

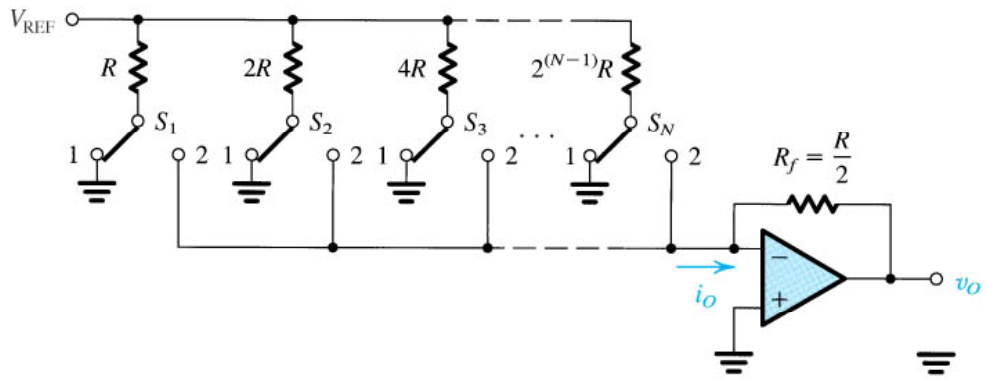


Figure 9.39 An *N*-bit D/A converter using a binary-weighted resistive ladder network.

$$N-bit\ digital\ word\ D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}$$

$$i_o = \frac{V_{REF}}{R} b_1 + \frac{V_{REF}}{2R} b_2 + \cdots + \frac{V_{REF}}{2^{N-1}R} b_N$$

$$= \frac{2V_{REF}}{R}\left(\frac{b_1}{2} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}\right) = \frac{2V_{REF}}{R} D$$

$$v_o = -i_o R_f = -V_{REF} D$$

9.8 D/A Converter Circuits

Basic circuit using binary-weighted resistors

- The accuracy of the DAC depends on
  - The accuracy of V_{ref}
  - The precision of the binary-weighted resistors
  - The perfection of the switches

- Disadvantages
  - For a large number of bits (N>4) the spread between the smallest and largest R becomes quite large.
  - This implies difficulties in maintaining accuracy in R values.

- A more convenient scheme exists utilizing a resistive network called the R-2R ladder

9.8 D/A Converter Circuits

R-2R Ladders

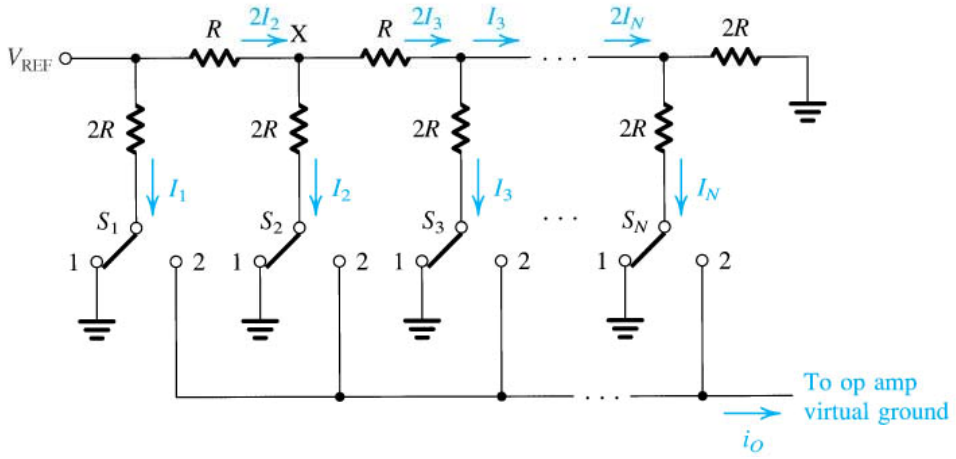


Figure 9.40 The basic circuit configuration of a DAC utilizing an *R*-2*R* ladder network.

$$I_1 = 2I_2 = 4I_3 = \cdots = 2^{N-1} I_N$$

$$\left(I_1 = \frac{V_{REF}}{2R}, I_2 = \frac{V_{REF}}{4R}, \cdots \right)$$

$$i_o = \frac{V_{REF}}{2R} b_1 + \frac{V_{REF}}{4R} b_2 + \cdots + \frac{V_{REF}}{2^N R} b_N$$

$$= \frac{V_{REF}}{R} \left(\frac{b_1}{2} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N} \right) = \frac{V_{REF}}{R} D$$

$$v_o = -i_o R_f = -V_{REF} D$$

- Because of the small spread in R values, this network is usually preferred to the binary-weighted scheme discussed earlier, especially for N>4

9.8 D/A Converter Circuits

- A practical circuit implementation

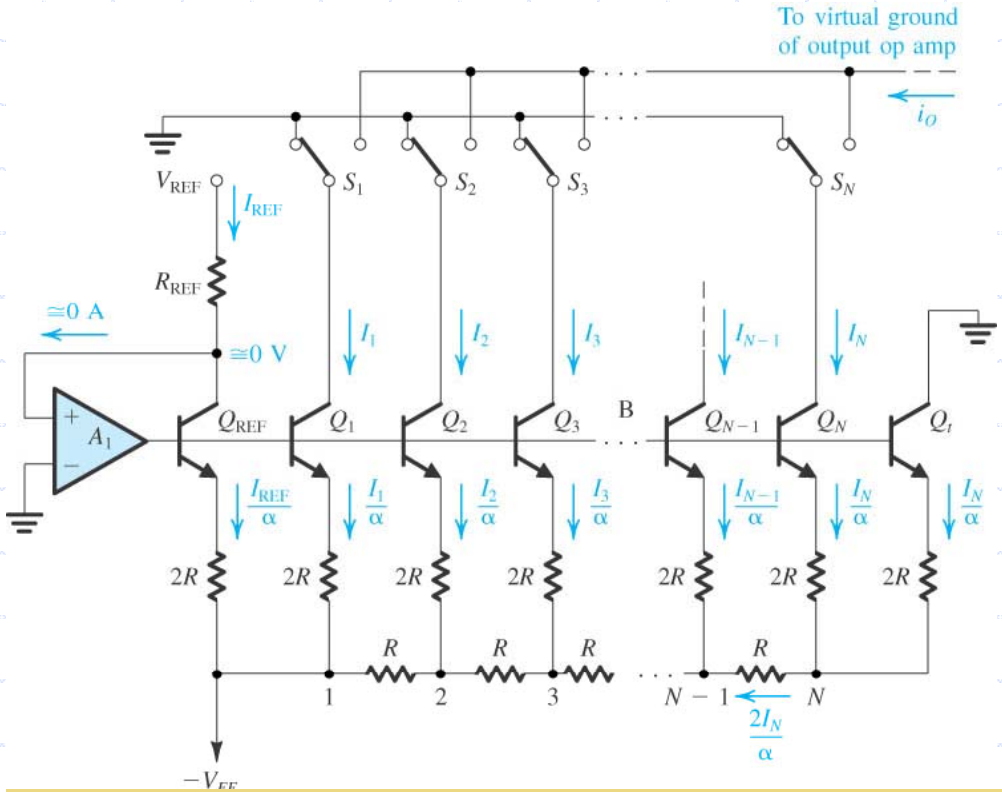


Figure 9.41 A practical circuit implementation of a DAC utilizing an *R*-2*R* ladder network.

$$V_N = V_{BE_N} + \left(\frac{I_N}{\alpha}\right)(2R)$$

$$V_{N-1} = V_N + \left(\frac{2I_N}{\alpha}\right)R$$

$$= V_{BE_N} + \frac{4I_N}{\alpha}R = V_{BE_{N-1}} + \left(\frac{I_{N-1}}{\alpha}\right)2R$$

$$if \quad V_{BE_{N-1}} = V_{BE_N} \Rightarrow I_{N-1} = 2I_N$$

$$\therefore I_1 = 2I_2 = 4I_3 = \cdots = 2^{N-1}I_N$$

9.8 D/A Converter Circuits

Current switches

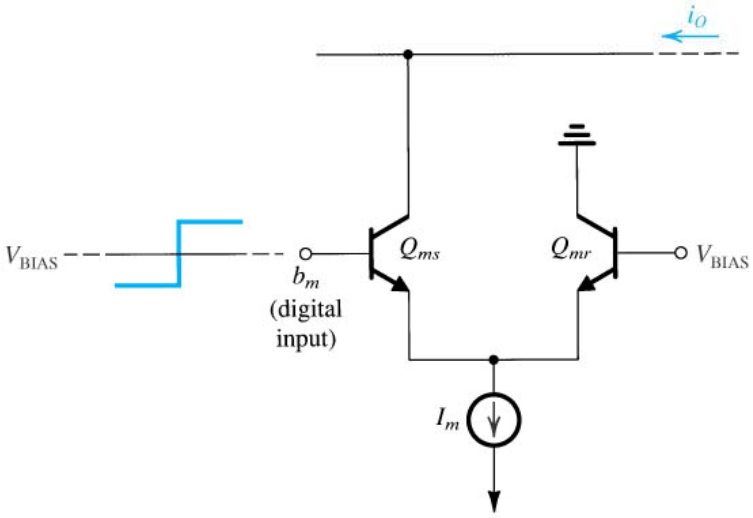


Figure 9.42 Circuit implementation of switch S_m in the DAC of Fig. 9.41. In a BiCMOS technology, Q_{ms} and Q_{mr} can be implemented using MOSFETs, thus avoiding the inaccuracy caused by the base current of BJTs.

- Each of the single-pole double-throw switches in the DAC circuit of Fig.9.41 can be implemented by a circuit as that shown in Fig.9.42 for switch S_m
- I_m: the current flowing in the collector of the m_{th}-bit transistor
- Q_{mr}: the reference transistor
- If $b_m > V_{BIAS}$ → Q_{ms} turn on, Q_{mr} turn off → I_m through Q_{ms}
- If $b_m < V_{BIAS}$ → Q_{ms} turn off, Q_{mr} turn on→ I_m through Q_{mr}

9.9 A/D Converter Circuits

The feedback-type converter

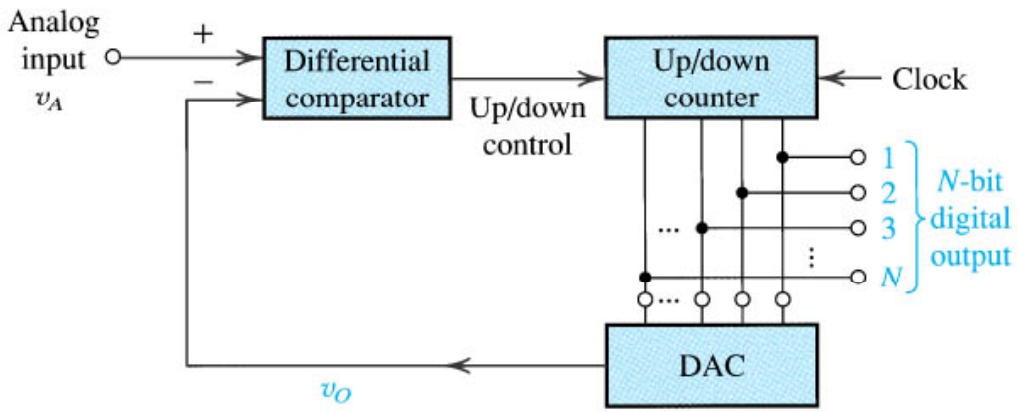


Figure 9.43 A simple feedback-type A/D converter.

- The comparator circuit provides an output that assumes one of two distinct values
- An up-down counter is simply a counter that can count either up or down depending on the binary level applied at its up-down control terminal

9.9 A/D Converter Circuits

- The dual-slope A/D converter

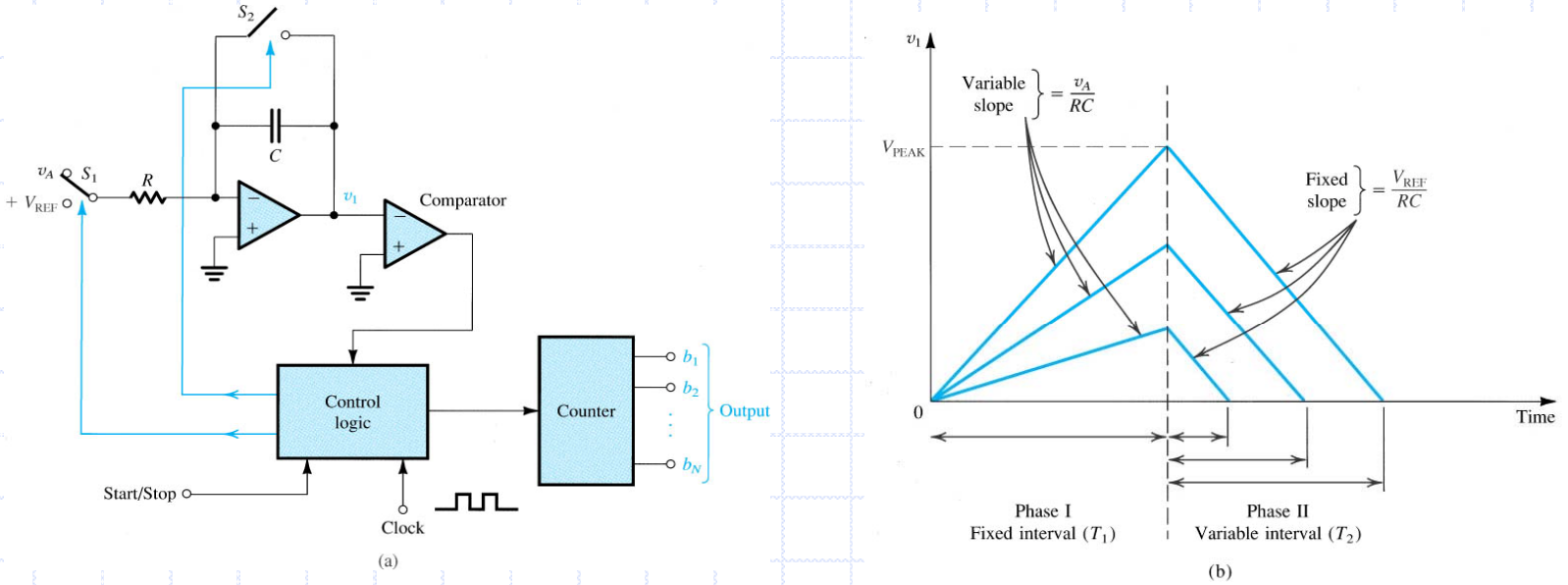
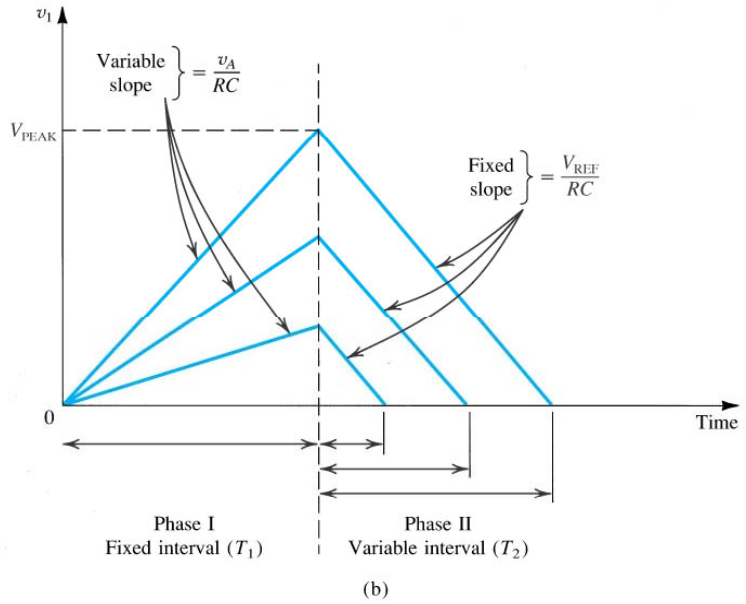


Figure 9.44 The dual-slope A/D conversion method. Note that v_A is assumed to be negative.

- Close S_2 (discharge C, v_1=0)
  → Open S_2 and switch S_1 to v_A ($I=v_A/R$ flow away from the integrator)
- V_1 rises linearly with a slope of $I/C=v_A/RC$, as indicated in Fig. (b)

9.9 A/D Converter Circuits

The dual-slope A/D converter



(b)

- Reference to Fig. 9.44(b)

$$\frac{V_{peak}}{T_1} = \frac{v_A}{RC}$$

- At the end of this phase, the counter is reset to zero
- In phase II, v_1 decreases linearly with a slope of (V_{ref}/RC)
- When v_1 reaches zero, the control logic stops the counter
- Thus the content of the counter, n, at the end of the conversion process is the digital equivalent of v_A

$$\frac{V_{peak}}{T_2} = \frac{V_{ref}}{RC} \qquad T_2 = T_1\left(\frac{v_A}{V_{ref}}\right)$$

$$n = n_{ref}\left(\frac{v_A}{V_{ref}}\right)$$

9.9 A/D Converter Circuits

- The parallel or flash converter

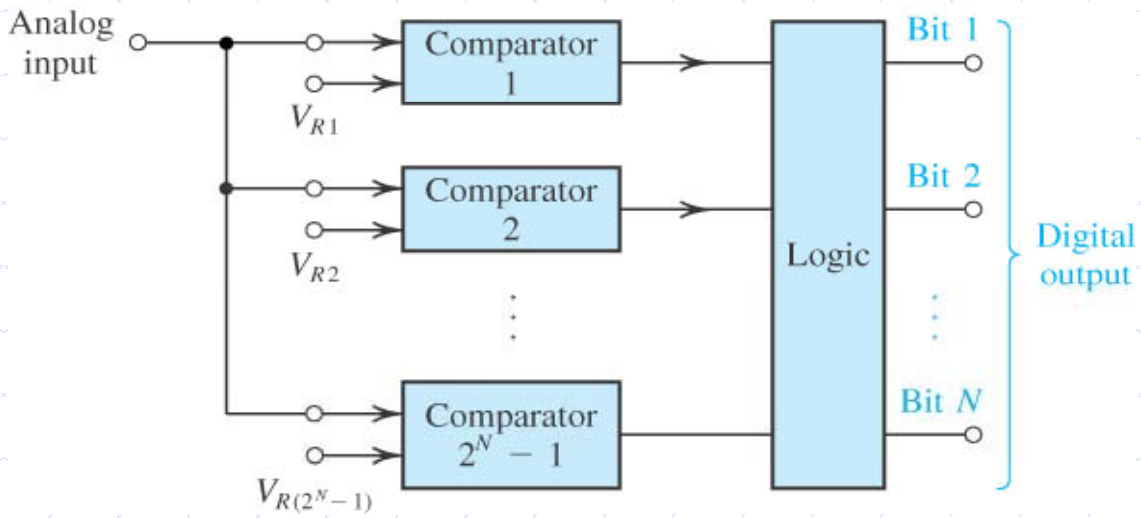


Figure 9.45 Parallel, simultaneous, or flash A/D conversion.

- Very fast
- A rather complex circuit

9.9 A/D Converter Circuits

The feedback-type converter

- Suitable for CMOS implementation

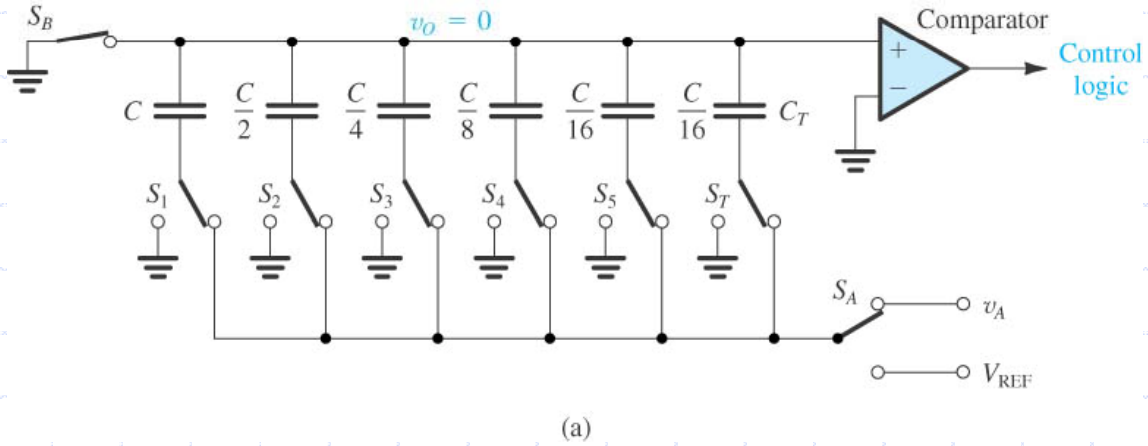
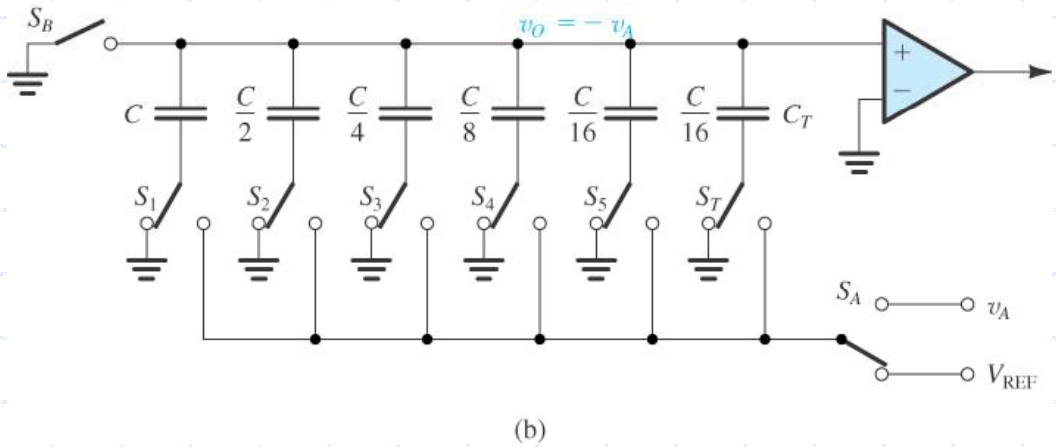


Figure 9.46 Charge-redistribution A/D converter suitable for CMOS implementation: (a) sample phase

- (a) sample phase: S_B closed, v_0=0, s_A=v_A, Q=-2Cv_A

9.9 A/D Converter Circuits

- The feedback-type converter

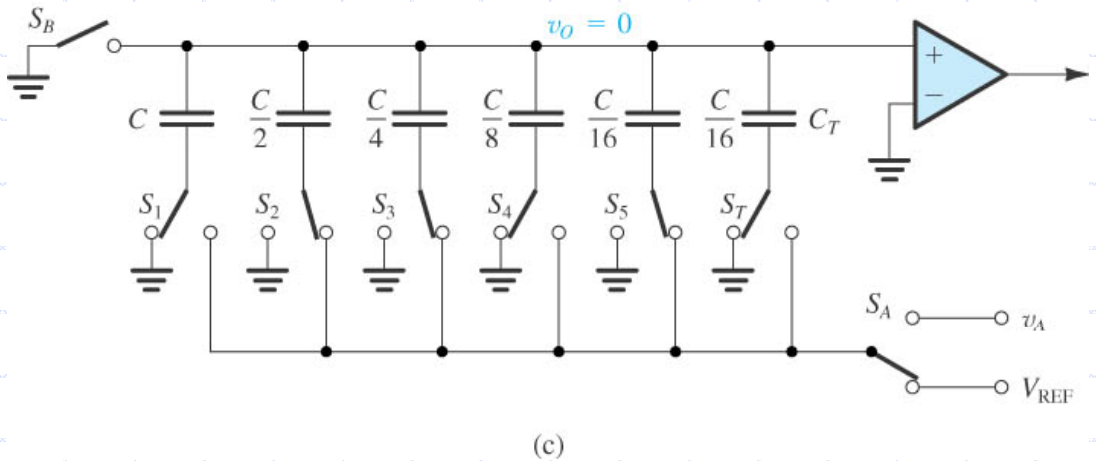


(b)

- (b) hold phase: S_B open, S_i to GND, S_A to V_{ref}, v_o=-v_A

9.9 A/D Converter Circuits

The feedback-type converter



- (c) charge-redistribution phase

S_1 to V_{ref} : $v_o=-v_A+V_{ref}/2$,
- If $v_A>V_{ref}/2$, $v_o<0$, S_1 to V_{ref} , $b_1=1$
- If $v_A<V_{ref}/2$, $v_o>0$, S_1 to GND , $b_1=0$

S_2 to V_{ref} : $v_o=-v_A+V_{ref}/2+V_{ref}/4$,
- If $v_A>V_{ref}/2+V_{ref}/4$, $v_o<0$, S_1 to V_{ref} , $b_2=1$
- If $v_A<V_{ref}/2+V_{ref}/4$, $v_o>0$, S_1 to GND, $b_2=0$

$$S_1 : \frac{v_{ref}}{2}, S_2 : \frac{v_{ref}}{4}, S_3 : \frac{v_{ref}}{8}, \cdots$$