2007 Fall: Electronic Circuits 2

CHAPTER 11

Memory and Advanced Digital Circuit

Deog-Kyoon Jeong
dkjeong@snu.ac.kr
School of Electrical Engineering
Seoul National University

Introduction

- In this chapter, we will be covering…
  - Latches and Flip-Flops
  - Multivibrator Circuits
- Sequential circuits
  - Memory included
  - Timing generator(clock) required

11.1.1 The Latch

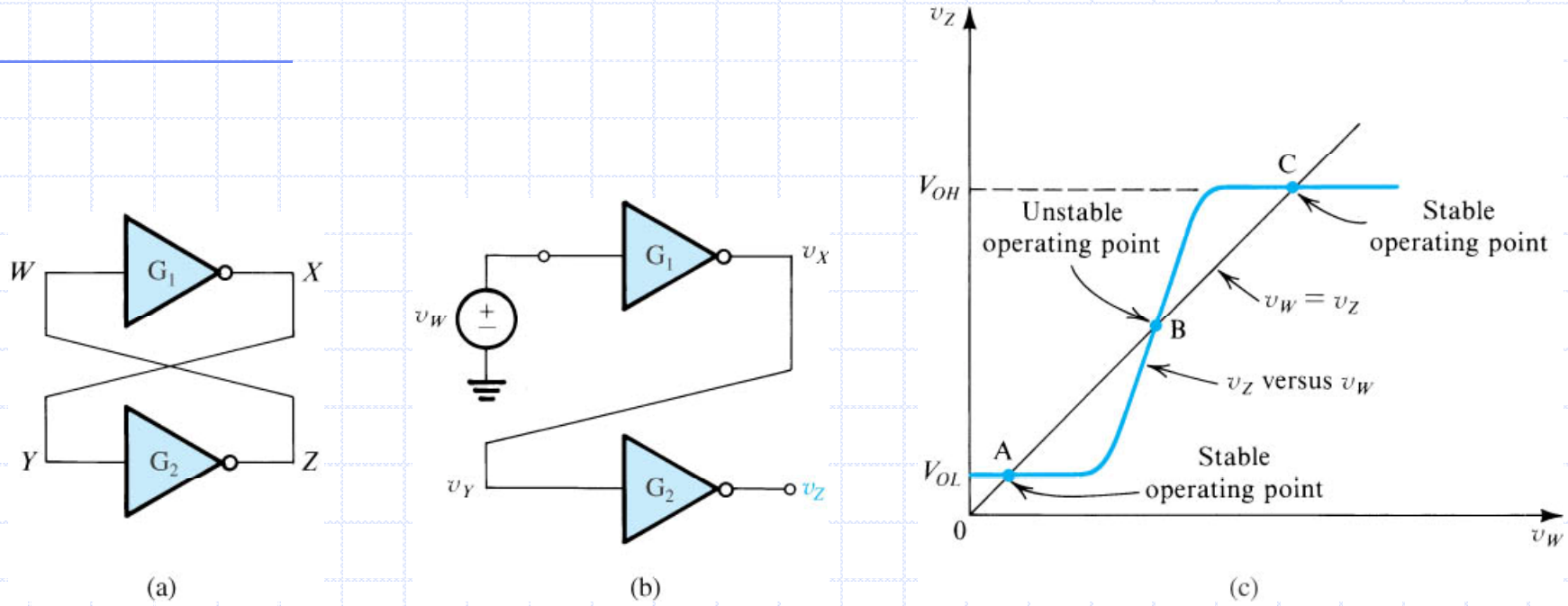
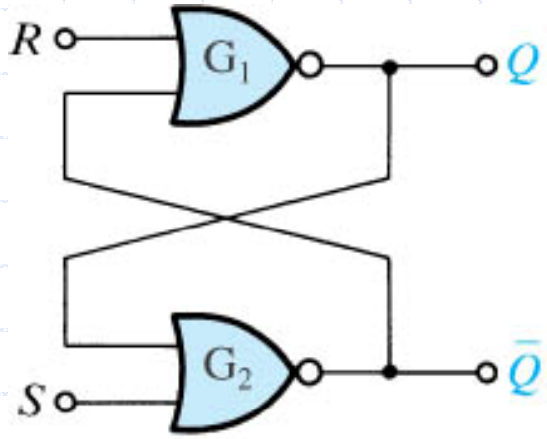


Figure 11.1 **(a)** Basic latch. **(b)** The latch with the feedback loop opened. **(c)** Determining the operating point(s) of the latch.

- Latch can store one bit of information
  - v_X is high & v_Z is low = 1
- Two stable operating points A & C.
- Unstable operating point B

11.1.2 The SR Flip-Flop



(a)

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	Not used

(b)

Figure 11.2 **(a)** The set/reset (SR) flip-flop and **(b)** its truth table.

- Memory state : S and R inputs are low

11.1.3 CMOS Implementation of SR Filp-Flops

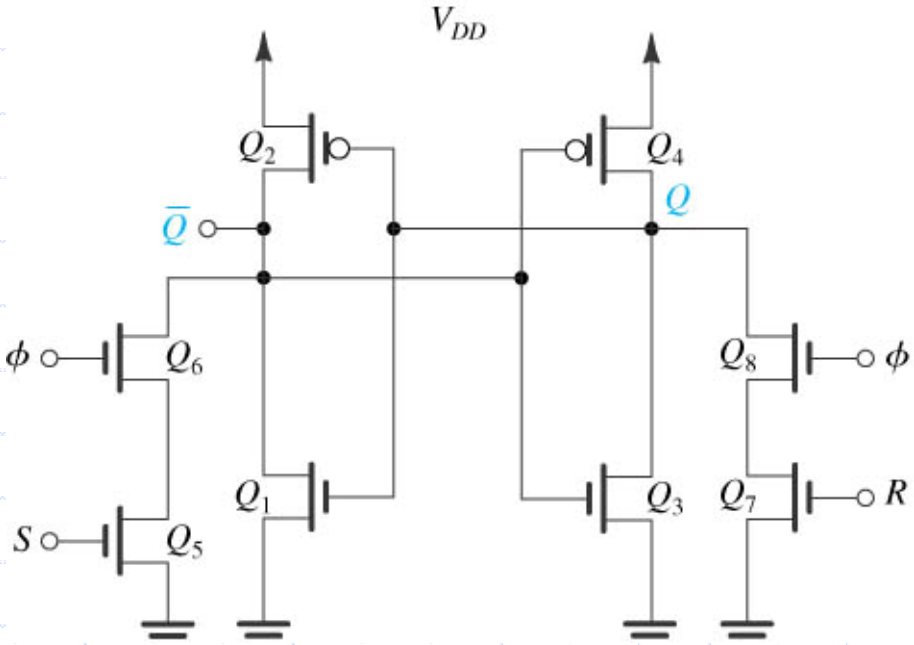
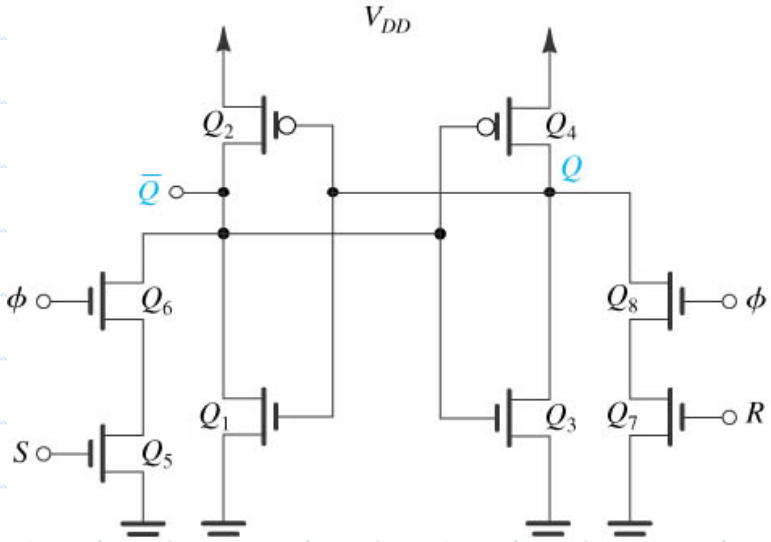


Figure 11.3 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

- Clock signal(Φ) is high
  → set or reset action performed.

11.1.3 CMOS Implementation of SR Filp-Flops

- Example 11.1



$\mu_n C_{ox} = 2.5\mu_p C_{ox} = 50\mu A/V^2$

$V_{tn} = |V_{tp}| = 1V, \qquad V_{DD} = 5V$

Inverter

$(W/L)_n = 4\mu m/2\mu m$

$(W/L)_p = 10\mu m/2\mu m$

The four NMOS transistors in the set-reset circuit have equal W/L ratios. Determine the minimum value required for this ratio to ensure that the flip-flop will switch.

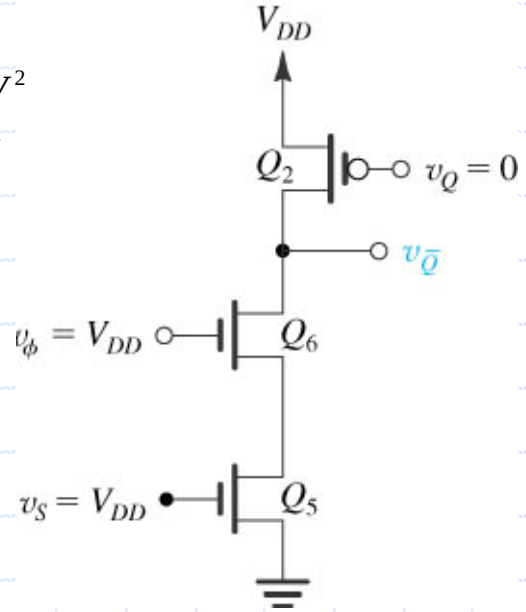


Figure 11.4 The relevant portion of the fli p-flop circuit of Fig. 11.3 for determining th e minimum *W*/*L* ratios of Q_5 and Q_6 needed to ensure that the flip-flop will switch.

11.1.3 CMOS Implementation of SR Filp-Flops

Example 11.1(Cont'd)

Assume v_Q=0, the circuit is in effect a pseudo-NMOS gate

V_{OL} of inverter is lower than $V_{DD}/2$ ⇨ select W/L ratios for Q5 and Q6

$I_{Q2} = I_{Q5} = I_{Q6}$ (at $v_{\bar{Q}} = V_{DD}/2$)

Q5,Q6 is approximately equivalent to a single transistor Whose W/L is half the W/L of each of Q5 and Q6

$v_{\bar{Q}} = V_{DD}/2$ ⇨ equivalent transistor & Q2 : triode region

$$50\times\frac{1}{2}\times(\frac{W}{L})_5[(5-1)\times\frac{5}{2}-\frac{1}{2}\times(\frac{5}{2})^2]=20\times\frac{10}{2}[(5-1)\times\frac{5}{2}-\frac{1}{2}\times(\frac{5}{2})^2]$$

$$\therefore\quad (\frac{W}{L})_5=(\frac{W}{L})_6=4$$

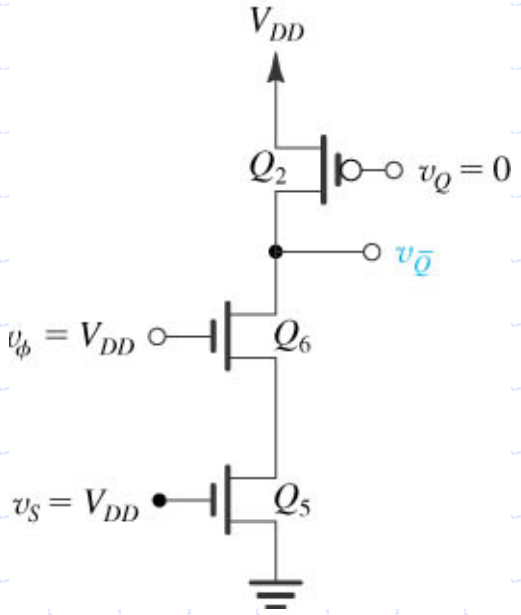


Figure 11.4 The relevant portion of the fli p-flop circuit of Fig. 11.3 for determining th e minimum *W*/*L* ratios of Q_5 and Q_6 needed to ensure that the flip-flop will switch.

11.1.4 A Simpler CMOS Implementation of the Clocked SR Flip-Flop

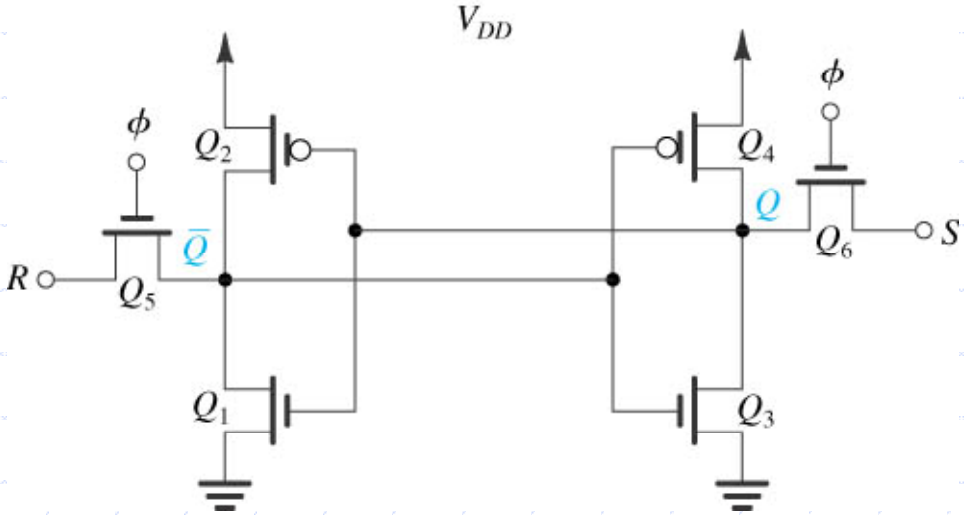


Figure 11.5 A simpler CMOS implementation of the clocked SR flip-flop.

- Pass-transistor logic is employed
- Very popular in the design of static random-access memory (SRAM)

11.1.5 D Flip-Flop Circuits

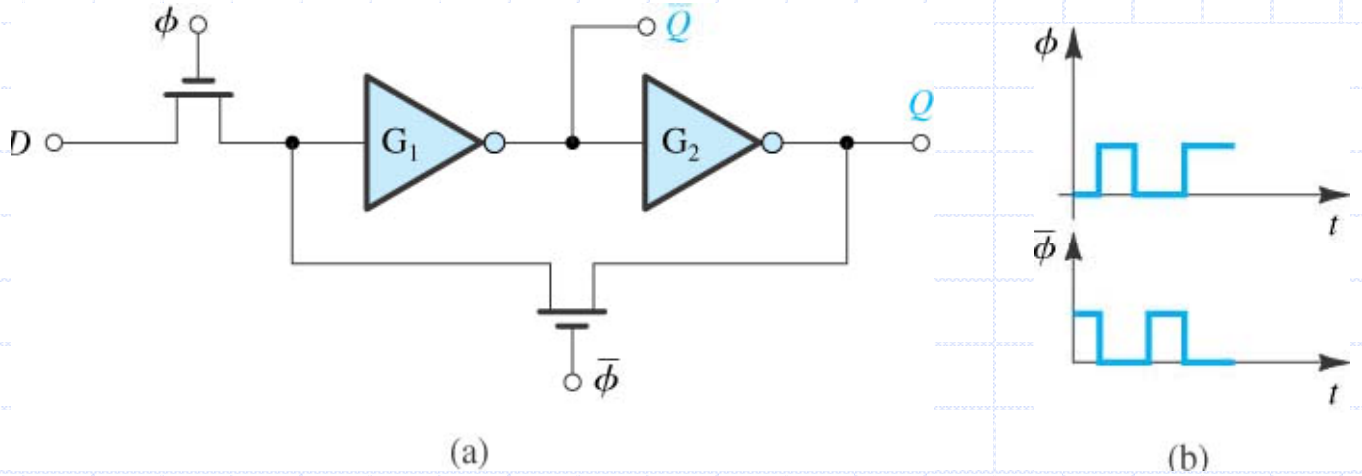


Figure 11.7 A simple implementation of the D flip-flop.

- Simple implementation of the D flip-flop:
  - Φ = 1 and Φ = 0: the loop is open and Q is determined by D.
  - Φ = 0 and Φ = 1: the loop is closed and the flip-flop is in latch mode.
  - Two-phase non-overlapping clock is required for D flip-flop operation.
  - Major drawback: the output simply follows the signal on the D input line during Φ.

11.1.5 D Flip-Flop Circuits (cont.)

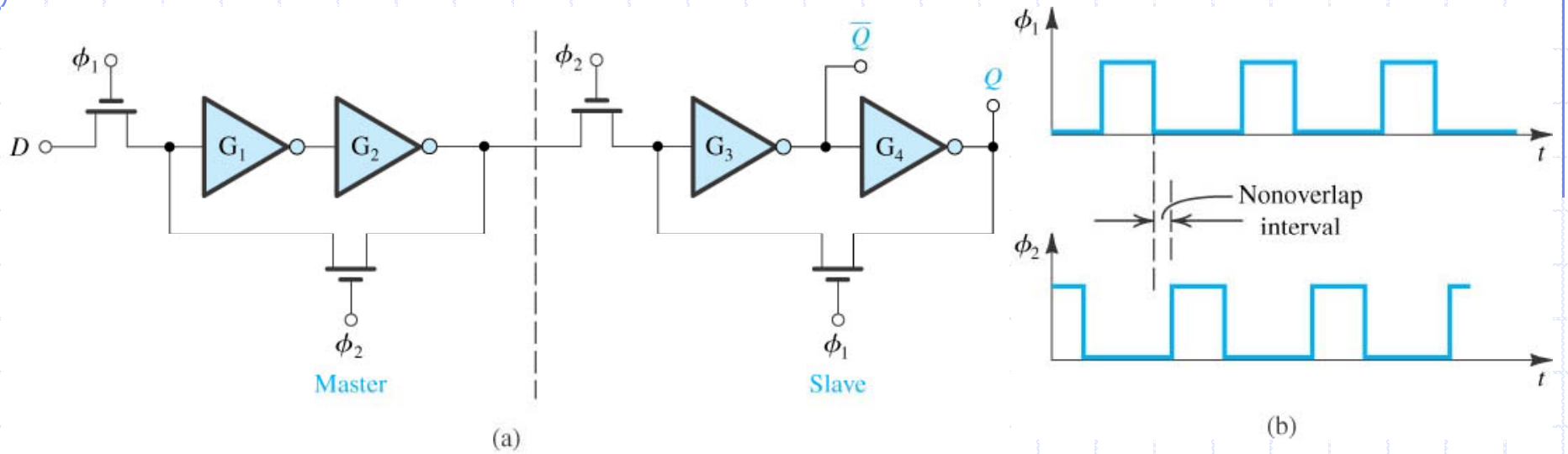


Figure 11.8 **(a)** A master–slave D flip-flop. The switches can be, and usually are, implemented with CMOS transmission gates. **(b)** Waveforms of the two-phase nonoverlapping clock required.

- Two clock phases, Φ_1&Φ_2, must be nonoverlapping.
- Positive transition of clock Φ_2 the output Q adopts the value of D.
- During the nonoverlap interval, feedback loops open
  → capacitances maintain most of their charge.
- Nonoverlap interval should be kept reasonably short(one-tenth or less of the clock period, and of the order of 1ns or so in current practice)

11.2 MULTIVIBRATOR CIRCUITS

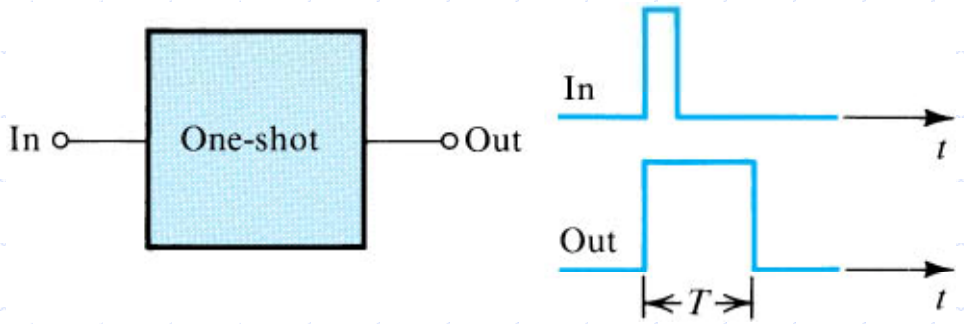
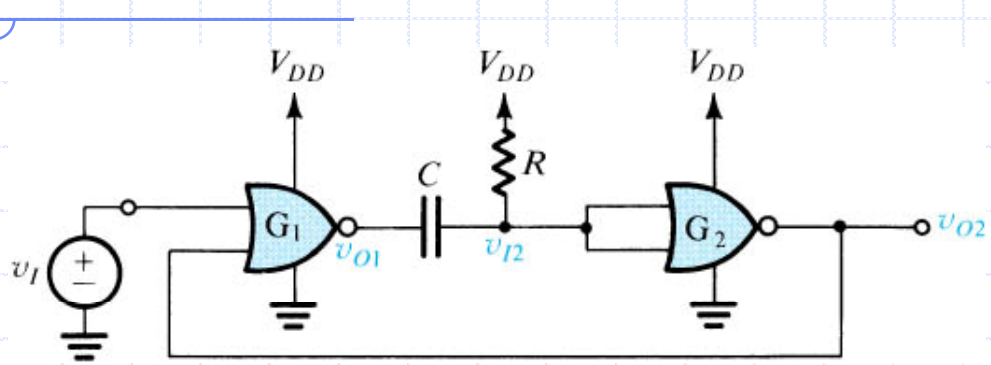


Figure 11.9 The monostable multivibrator (one-shot) as a functional block, shown to be triggered by a positive pulse. In addition, there are one shots that are triggered by a negative pulse.

- Bistable multivibrator (two stable states, e.g. flip-flop).
- Monostable multivibrator (one stable state + quasi-stable state, e.g. pulse stretcher or pulse standardizer).
- Astable multivibrator (no stable states + two quasi-stable states, e.g. periodic pulse generator).

11.2.1 A CMOS Monostable Circuit



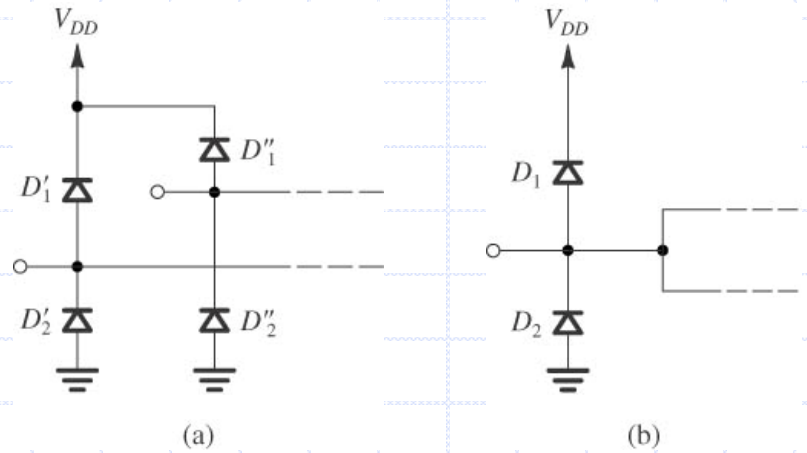


Figure 11.10 A monostable circuit using CMOS NOR gates. Signal source v_I supplies positive trigger pulses.

- Commercially available CMOS gates have a special arrangement of diodes connected at their input terminals
- Prevent the input voltage signal from rising above the supply voltage V_{DD} and from falling below ground voltage.
- Effect on the operation of the inverter-connected gate G_2.
  - The diodes provide a low-resistance path to the power supply for voltages exceeding the power supply limits, the input current for intermediate voltages is essentially zero.

11.2.1 A CMOS Monostable Circuit (cont.)

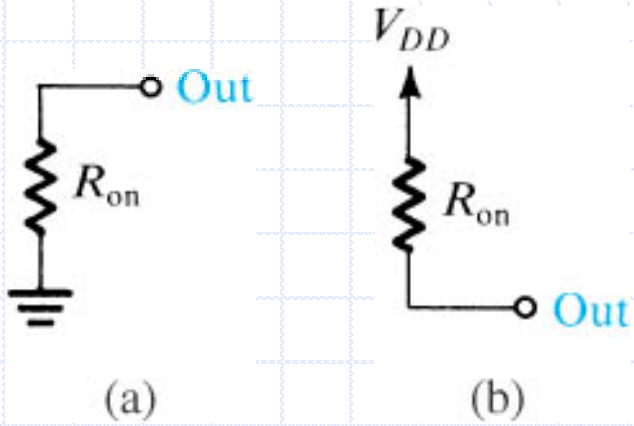


Figure 11.12 Output equivalent circuit of CMOS gate when the output is **(a)** low and **(b)** high.

- Approximate output equivalent circuits of the gate.
  - Fig.11.12(a) : when the gate output is low. In this state, current can flow from the external circuit into the output terminal of the gate; the gate is said to be sinking current.
  - Fig.11.12(b) : when the gate output is high. In this state, current can flow from V^{DD} through the output terminal of the gate into the external circuit; the gate is said to be sourcing current.

11.2.1 A CMOS Monostable Circuit (cont.)

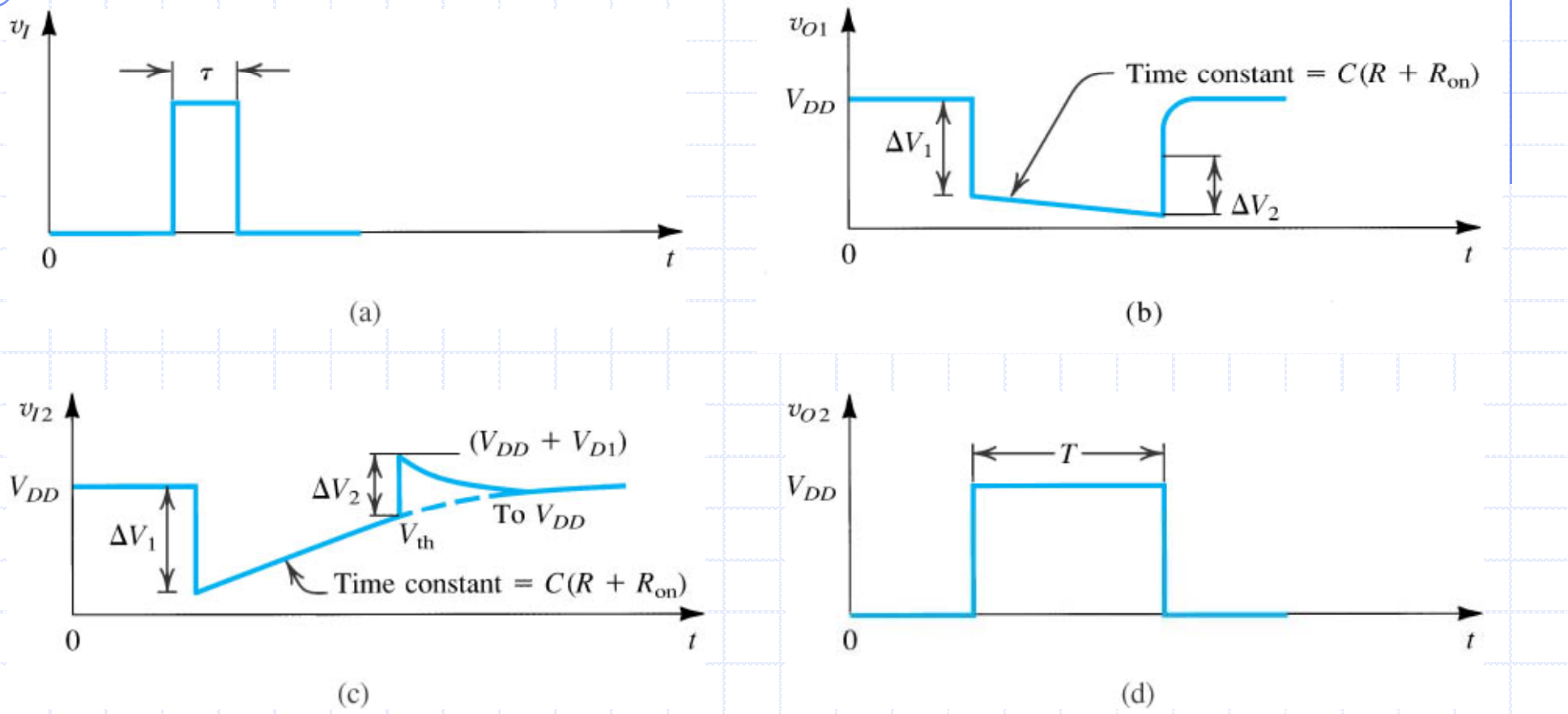
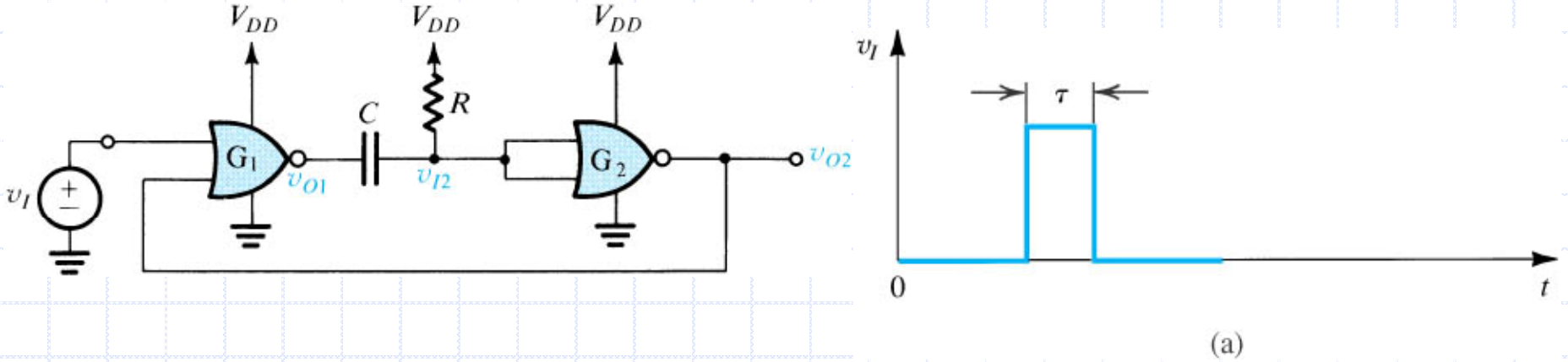


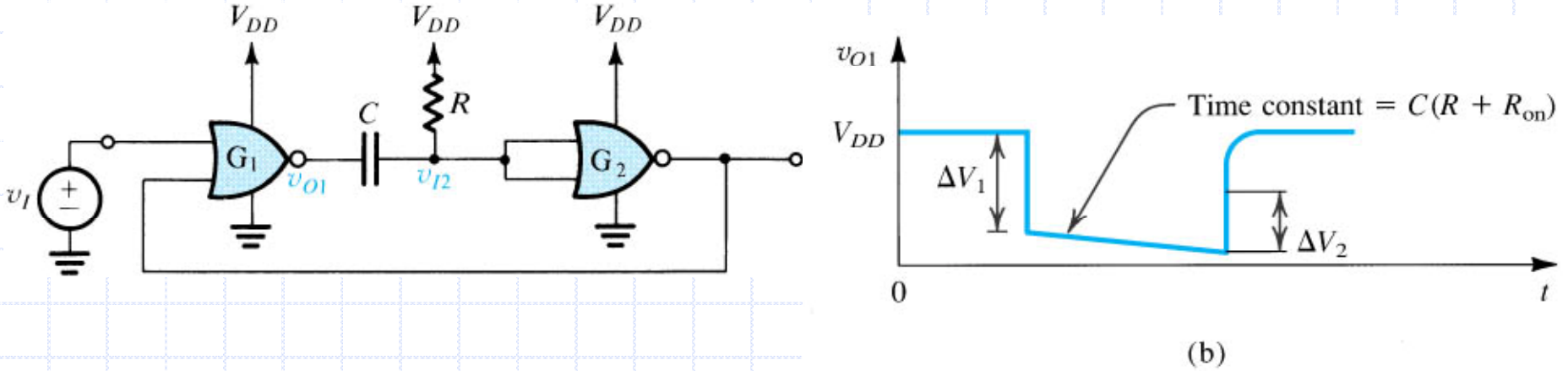
Figure 11.13 Timing diagram for the monostable circuit in Fig. 11.10.

11.2.1 A CMOS Monostable Circuit (cont.)



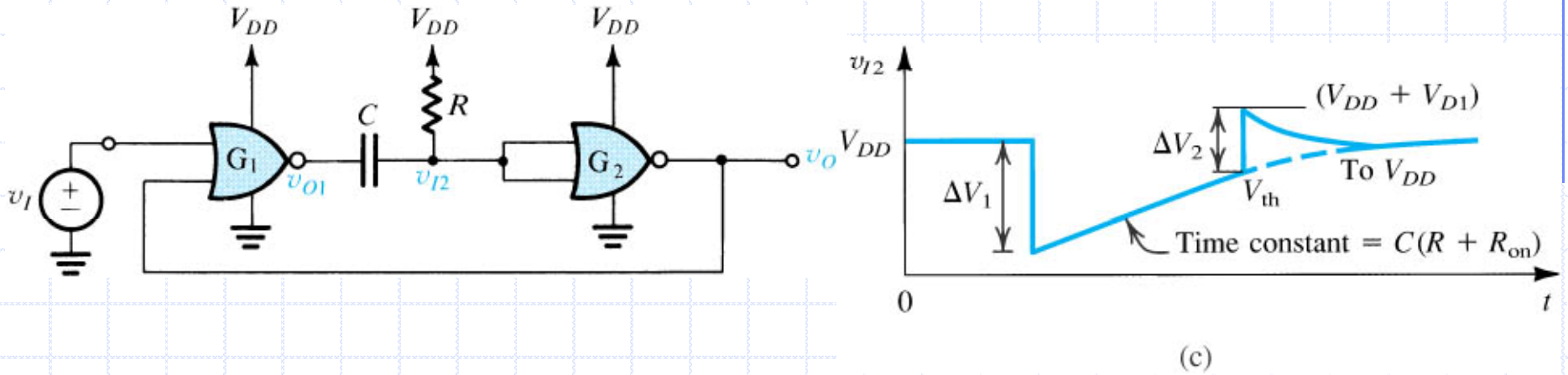
1. Stable state of the monostable circuit (the state of the circuit before the trigger pulse is applied): The output of G_1 is high at V_{DD} , the capacitor is discharged, and the input voltage to G_2 is high at V_{DD}.
   - The output of G_2 is low, at ground voltage.
   - Low voltage is fed back to G_1; since v_I also is low, the output of G_1 is high, as initially assumed.

11.2.1 A CMOS Monostable Circuit (cont.)



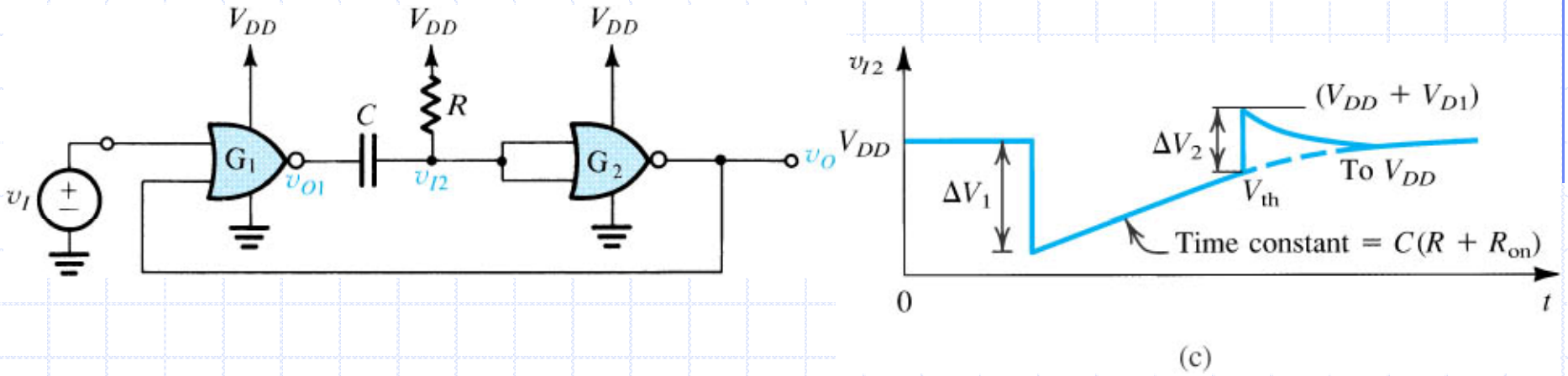
2. Trigger pulse is applied: The output of G_1 will go low (but its output will not go all the way to 0V). The output of G_1 drops by a value ΔV_1.
   - Returning to G_2, the drop of voltage at its input causes its output to go high (to V_{DD}).
   - Keeps the output of G_1 low even after the triggering pulse has disappe ared.
   - The Circuit is now in the quasi-stable state.

11.2.1 A CMOS Monostable Circuit (cont.)



3. Operation in the quasi-stable state : The current through R, C, and R_{on} causes C to charge, and the voltage V_{I2} rises exponentially toward V_{DD} with a time constant $C(R + R_{on})$.
   - V_{I2} continue to rise until it reaches V_{th} of inverter G_2
   - G_2 will switch and its output v_{O2} will go to 0V, which will in turn cause G_1 to switch.

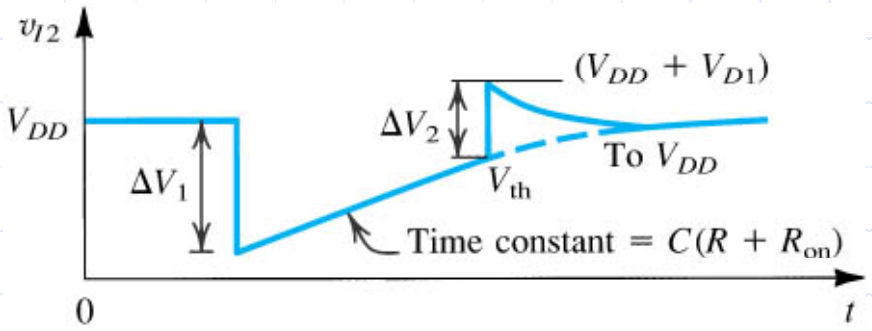
11.2.1 A CMOS Monostable Circuit (cont.)



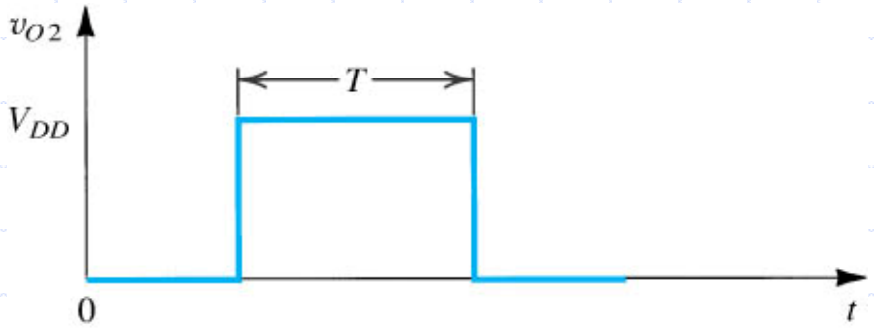
- The output of G_1 will attempt to rise to V_{DD} (instantaneous rise). Limited to an amount ΔV_2.

  $\Delta V_2 = V_{DD} + V_{D1} - V_{th}$
- V_{O1} rise. And the input of G_2 will rise by an equal amount ΔV_2.
- Now $V_{I2} > V_{DD}$, current will flow from the output of G_1 through C and then through the parallel combination of R and D_1.
- This current discharges C until V_{I2} drops to V_{DD} and v_{O1} rises to V_{DD}.

11.2.1 A CMOS Monostable Circuit (cont.)



(c)



(d)

- The monostable circuit should not be retriggered until the capacitor has been discharged(recovery time : the capacitor discharge interval).

$$V_{I2}(t) = V_{DD} - \Delta V_1 e^{-t/\tau_1} \qquad \tau_1 = C(R + R_{on})$$

Substituting for t=T and $v_{I2}(T)=V_{th}$

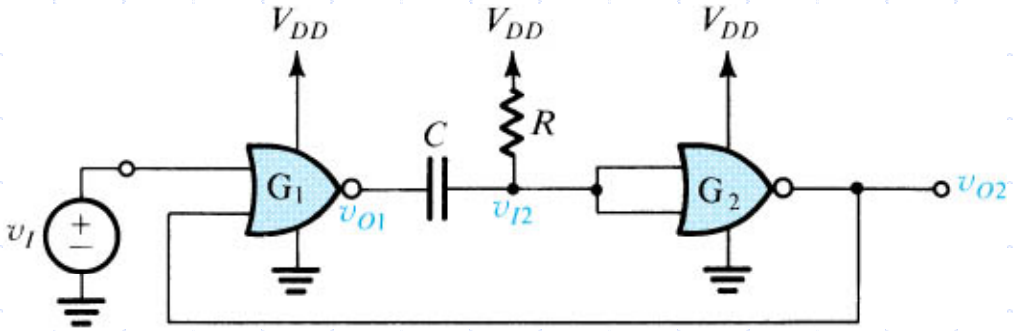
$$T = C(R + R_{on}) \ln\left(\frac{R}{R + R_{on}} \frac{V_{DD}}{V_{DD} - V_{th}}\right)$$

11.2.1 A CMOS Monostable Circuit (cont.)

- Problem 11.12

$R_{on} = 100\Omega,\ V_{DD} = 5V,\ V_{th} = 0.4V_{DD}$

$C = 1\mu F$



To generate an output pulse of duration T=1s, R=?

$$T = C(R + R_{on})\ln\left(\frac{R}{R + R_{on}}\frac{V_{DD}}{V_{DD} - V_{th}}\right)$$

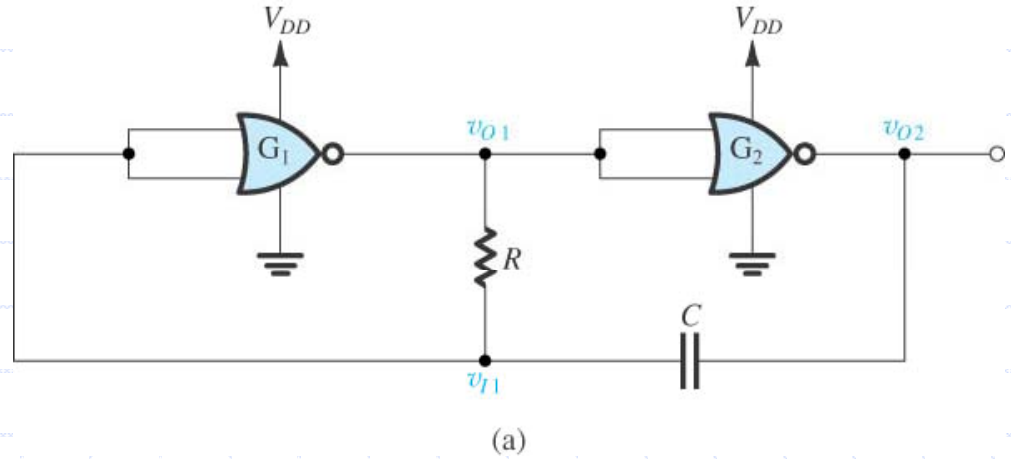
$$1 = 10^{-6}(R + 100)\ln\left(\frac{R}{R + 100}\frac{5}{5 - 0.4 \times 5}\right)$$

Neglect R_{on}

$$R = 10^6 / \ln\left(\frac{1}{0.4}\right) = 1.958M\Omega$$

Clearly, for this R, R_{on} can be neglected ($R >> R_{on}$)

11.2.2 An Astable Circuit



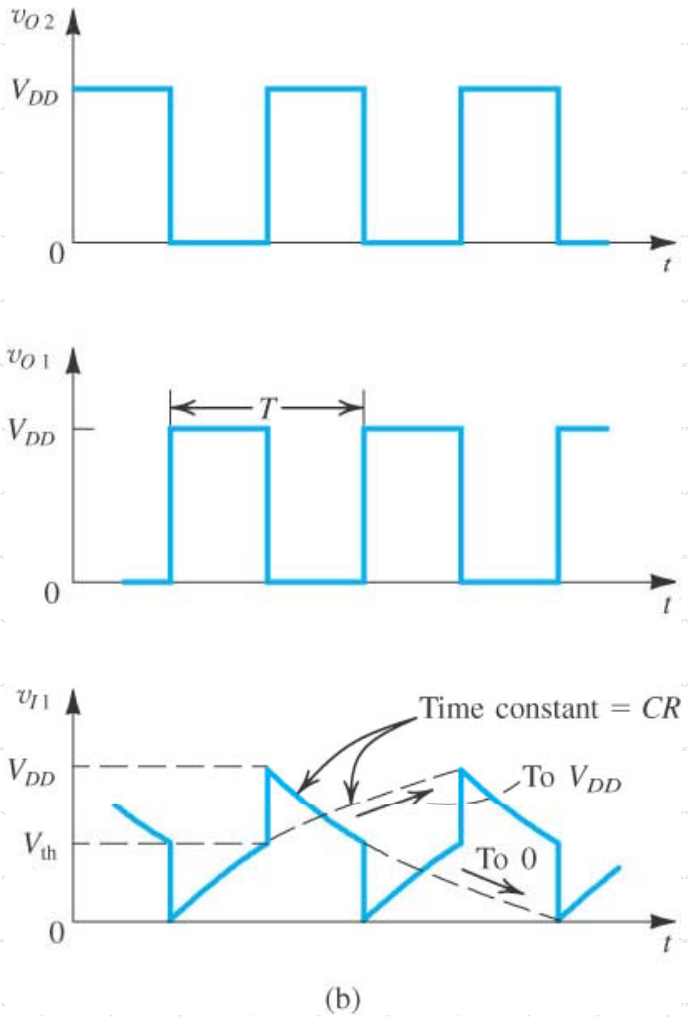


Figure 11.15 **(a)** A simple astable multivibrator circuit using CMOS gates. **(b)** Waveforms for the astable circuit in (a). The diodes at the gate input a re assumed to be ideal and thus to limit the voltage v_{I1} to 0 and V_{DD}.

- Assume that NOR gates are of the CMOS family
- Neglect the finite output resistance of the CMOS gate
- Assume that the clamping diodes are ideal : The wave form of Fig. 11.15(b) are obtained

11.2.3 The Ring Oscillator

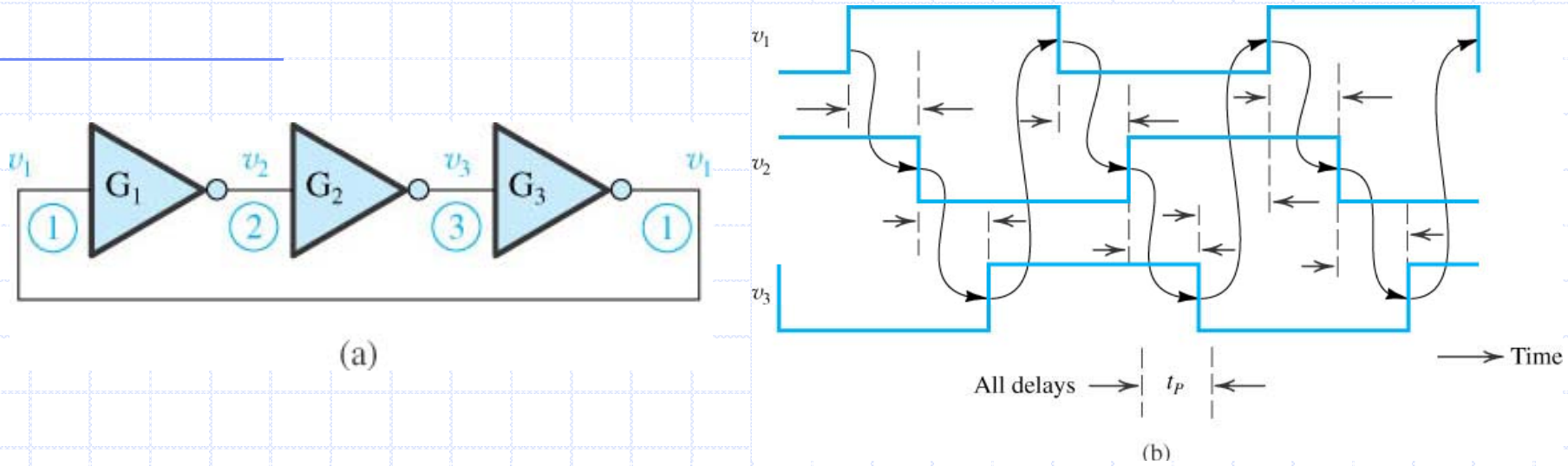


Figure 11.16 **(a)** A ring oscillator formed by connecting three inverters in cascade. (Normally at least five inverters are used.) **(b)** The resulting waveform. Observe that the circuit oscillates with frequency $1/6t_P$.

- The ring oscillator is formed by connecting an odd number of inverters in a loop.
- Usually at least five inverters are used.
- A ring with N inverters will oscillate with period of $2Nt_P$ and frequency $1/2Nt_P$.
- Ring oscillator provides a relatively simple means for measuring the inverter propagation delay.