Part II Electrical Properties of Materials

Chap. 7 Electrical Conduction in Metals and Alloys

Chap. 8 Semiconductors

Chap. 9 Electrical Properties of Polymers, Ceramics, Dielectrics, and Amorphous Materials

8.6 Compound Semiconductors

GaAs (III-V compound)

- larger band gap compared to Si
- larger electron mobility due to smaller electron effective mass (Fig 5.24)
- direct band gap (chap 12) : optical properties

Applications

- High-frequency devices
- Laser / light-emitting diodes (LED)

8.6 Compound Semiconductors

Other compound semiconductors

(applications: optoelectronic devices)

Group III-V elements

-GaP, GaN, InP, InAs, InSb, AlSb

Group II-VI elements

-ZnO, ZnS,ZnSe, CdS,CdTe,HgS

Group IV-VI

-PbS, PbSe, and PbTe

Ternary or quaternary alloys

-$Al_xGa_{1-x}As$, $Al_xGa_{1-x}As_ySb_{1-y}$, $GaAs_{1-x}P_x$:LEDs

$GaAs_{1-x}As$ also used in modulation-doped field-effect transistors (MODFET)

Silicon carbide: Group IV-IV

- band gap 3eV, very high temperature(700^{o}C) device
- Emit light in the blue end of the visible spectrum

8.7 Semiconductor Devices

8.7.1 Metal-Semiconductor Contacts

Types of contacts in semiconductor/metal

rectifying contact (8.7.2)

widely utilized in electronic devices to convert alternating current into direct current

ohmic contact

electron can flow in both ways and obeys Ohm's law

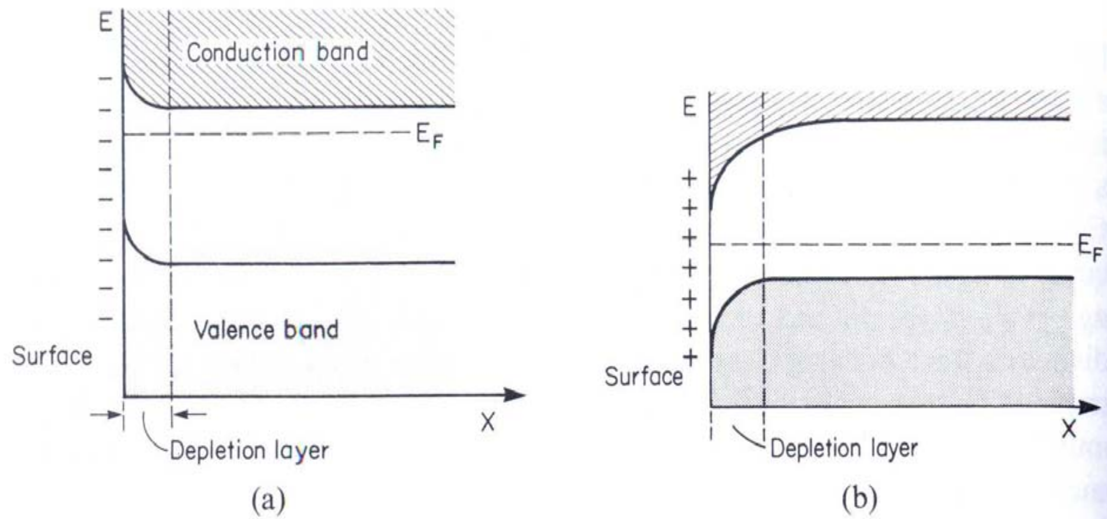


Figure 8.12. (a) Band diagram for an *n*-type semiconductor whose surface has been negatively charged. (b) Band diagram for a *p*-type semiconductor, the surface of which is positively charged. *X* is the distance from the surface.

Band diagram for n-type and p-type semiconductors (Fig 8.12)

n- type : surface negatively charged → repelling force on electron band edge → bent upward , **depletion layer** (*space-charge region*)

p-type: band edge bent downward

8.7.2 Rectifying Contacts (Schottky Barrier Contacts)

Work function, ϕ : the energy difference between the Fermi energy and the ionization energy which is necessary to transport an electron from E_F to infinity

Metal / n-type semiconductor, $\phi_M > \phi_S$: After contact (Fig 8.13b), electrons flow from semiconductor "down" to metal until Fermi energies of both solids are equal → the metal will be charged negatively and potential barrier is formed just as shown in Fig 8.12

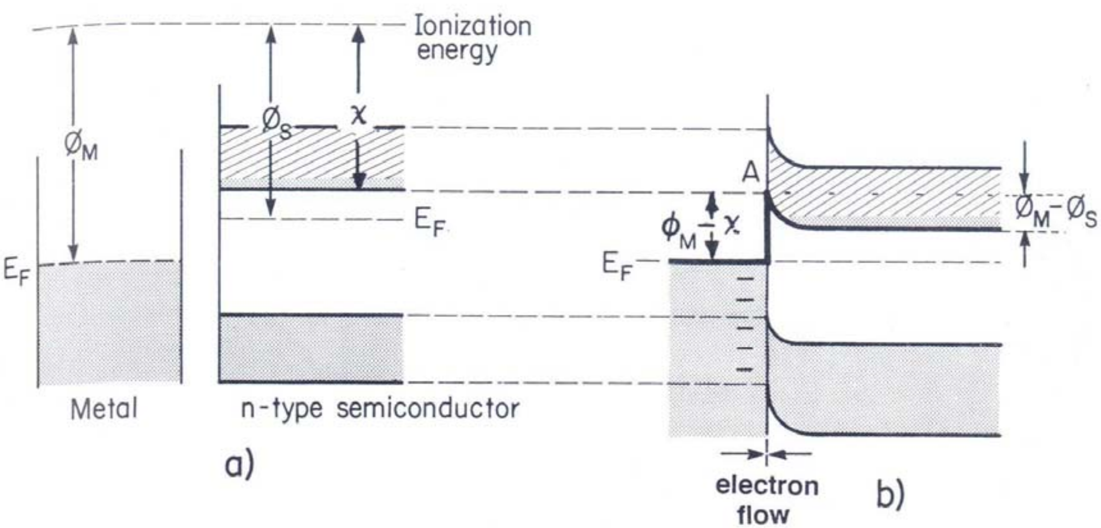


Figure 8.13. Energy bands for a metal and an *n*-type semiconductor (a) before and (b) after contact. $\phi_M > \phi_S$. The potential barrier is marked with heavy lines. χ is the *electron affinity*.

In equilibrium state, electrons from both sides cross the potential barrier. This electron flow constitutes the so-called **diffusion current**

8.7.2 Rectifying Contacts (Schottky Barrier Contacts)

Metal / p-type semiconductor, $\phi_M < \phi_S$

Electrons diffuse from metal into the semiconductor, thus charging the metal and, therefore, the surface of the semiconductor positively. Consequently a downward potential barrier is formed.

Contact potential:

the potential height for an electron diffusing from the semiconductor into metal: $\phi_M - \phi_S$ height of the potential barrier from metal side : $\phi_M - \chi$, where χ electron affinity

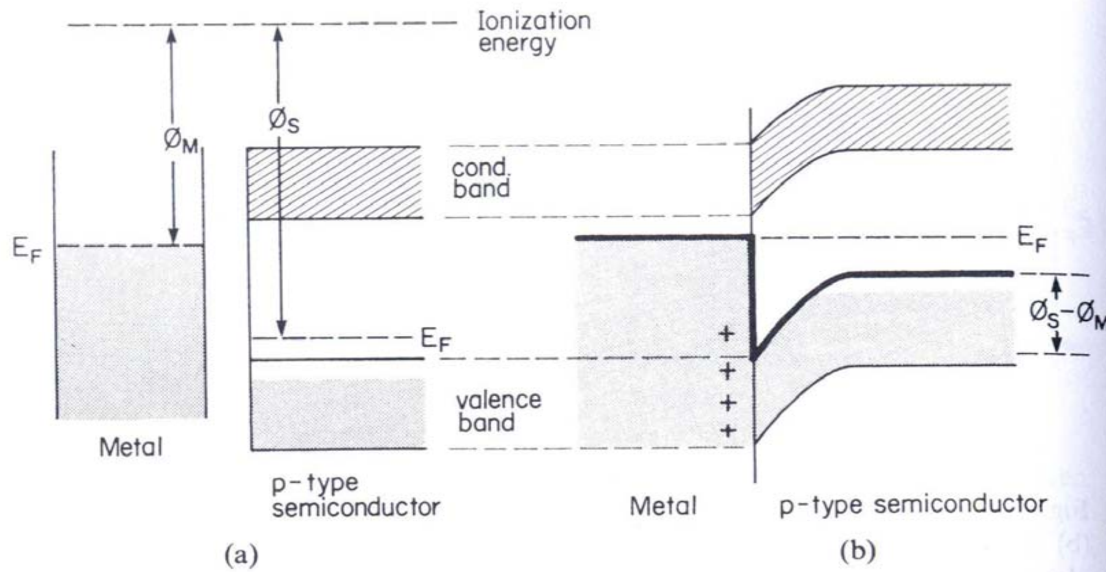


Figure 8.14. Energy bands for a metal and a *p*-type semiconductor (a) before and (b) after contact. $\phi_M < \phi_S$.

8.7.2 Rectifying Contacts (Schottky Barrier Contacts)

Net current flow in metal / n-type semiconductor by d.c biasing

- **Reverse bias** (when metal is connected to the negative terminal) : metal is charged even more negatively → the electron in the semiconductor are repelled even more → the potential barrier is increased and depletion layer becomes wider (Fig 8.15a)

Both barrier are relatively high, the diffusion currents in both directions are negligible, voltage independent small drift constant from metal into the semiconductor

- **Forward Bias** (semiconductor is connected to negative terminal)

The potential barrier reduced. the depletion layer is narrow

: a large electron flow from semiconductor into metal

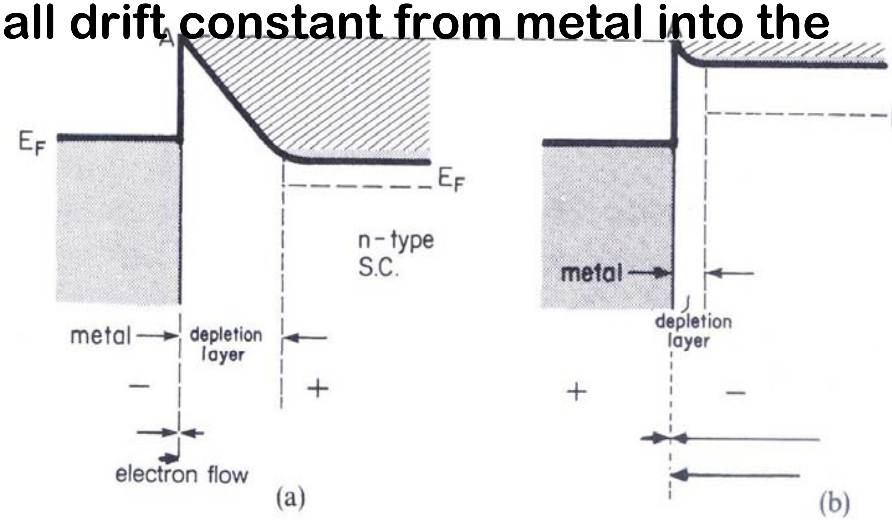


Figure 8.15. Metal–semiconductor contact with two polarities: (a) reverse bias and (b) forward bias. The number of electrons that flow in both directions and the net current is indicated by the length of the arrows. The potential barriers are marked by heavy lines.

8.7.2 Rectifying Contacts (Schottky Barrier Contacts)

The voltage current characteristic (Fig 8.16a)

Rectifier : convert alternating current into direct current (Fig 8.16b)

The current that flows from the metal into semiconductor

$$I_{MS} = ACT^2 \exp\left[-\left(\frac{\phi_M - \chi}{k_B T}\right)\right]$$

where, *A* is the area of contact (see Fig. 8.13) and *C* is a constant

The current flowing from semiconductor into the metal

$$I_{MS} = ACT^2 \exp\left[-\left(\frac{\phi_M - \phi_S - eV}{k_B T}\right)\right]$$

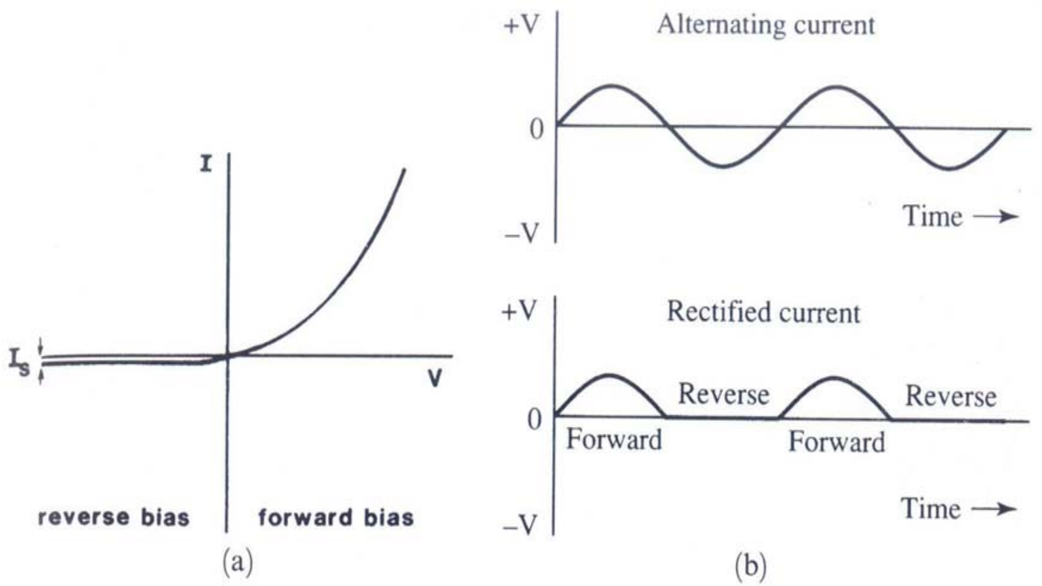


Figure 8.16. (a) Characteristic of a rectifier. The reverse current is grossly exaggerated! (b) Voltage versus time curves to demonstrate the behavior of an alternating current and a current for which the negative voltage has been eliminated.

8.7.2 Rectifying Contacts (Schottky Barrier Contacts)

The net current $I_{net} = I_{SM} - I_{MS}$ consists of namely, the saturation current

$$I_S = ACT^2 \exp\left[-\left(\frac{\phi_M - \phi_S}{k_B T}\right)\right]$$

and voltage-dependent term. The net current is obtained by combining the last two equation

$$I_{net} = I_S\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right]$$

Forward bias (positive *V*) the net current increase exponentially with *V*

8.7.3 Ohmic Contacts (Metallization)

Ohmic contact: no barrier exists for the flow of electrons in either diction (Fig 8.17c)

For the case of metal / n-type semiconductor contact, and $\phi_M < \phi_S$, electron flow from metal to semiconductor, charging metal positively.(cf, another case : metal / n-type semiconductor contact, and $\phi_M > \phi_S$)

The band of semiconductor bend "downward" and no barrier

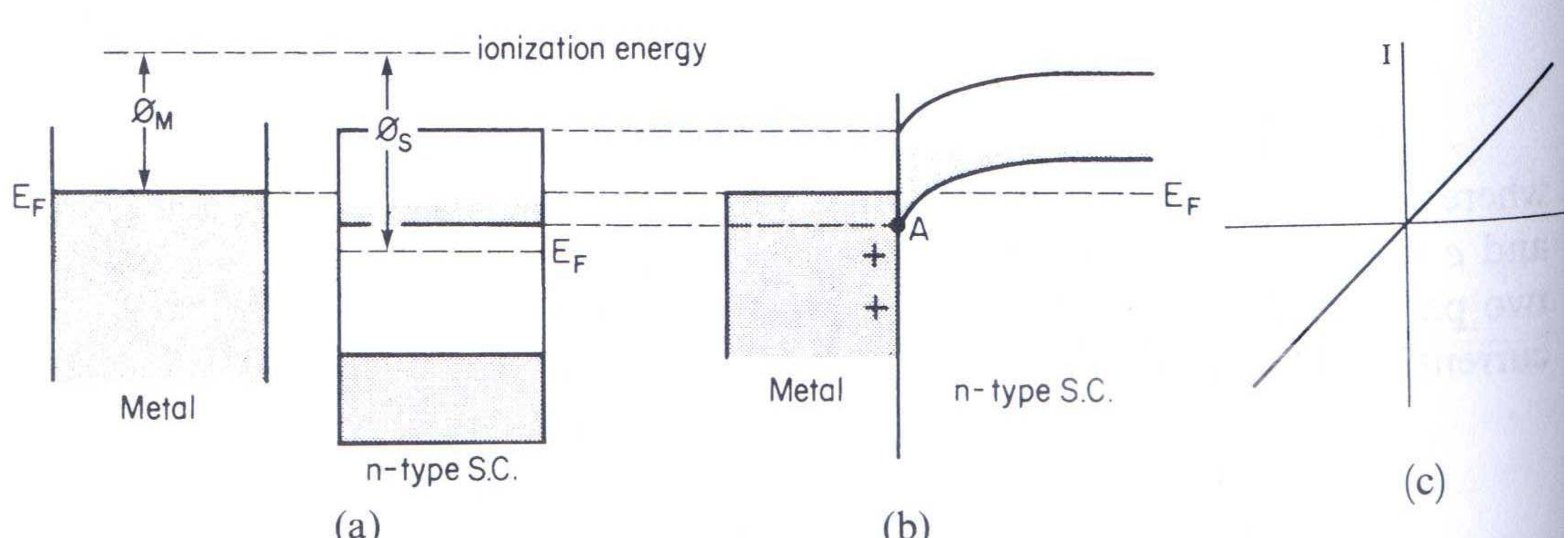


Figure 8.17. Ohmic contact between metal and *n*-type semiconductor ($\phi_M < \phi_S$). (a) Metal and semiconductor are separate. (b) Metal and semiconductor are in contact. (c) Current–voltage characteristic.

8.7 Semiconductor Devices

8.7.4 *p-n* Rectifier (Diode)

After p-n contact : electron flow from higher level (*n*-type) "down" into p-type so that p-slide is negatively charged

Conduction band: electron in the p-region diffuse "down" into *n*-region, in equilibrium state the number of electrons crossing the junction in both directions is identical

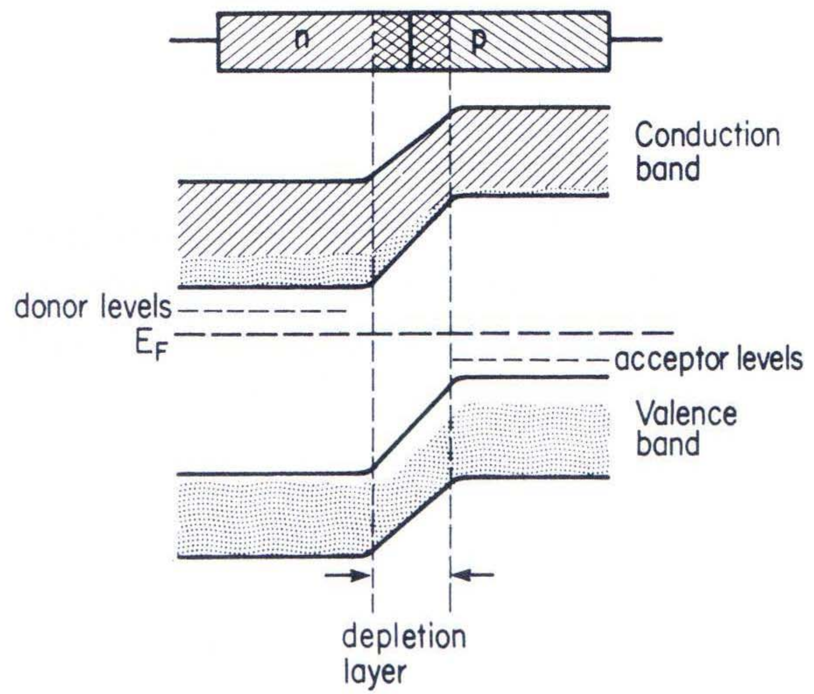


Figure 8.18. Schematic band diagram for a *p–n* junction (diode) in equilibrium.

8.7 Semiconductor Devices

8.7.4 *p-n* Rectifier (Diode)

" quasi-Fermi levels" (Fig 8.19a)

Electron density varies in the junction from the *n*-side to the *p*-side by many orders of magnitude, while electron current is almost constant. Consequently, the E_F is almost constant over depletion layer

External potential applied (Fig 8.19)

- Reverse bias (connecting positive terminal to n-side): depletion layer becomes wider and potential barrier grows higher

- Forward bias: barrier decreases in height, a large net electron flow occurs from *n*-type to *p*-type region

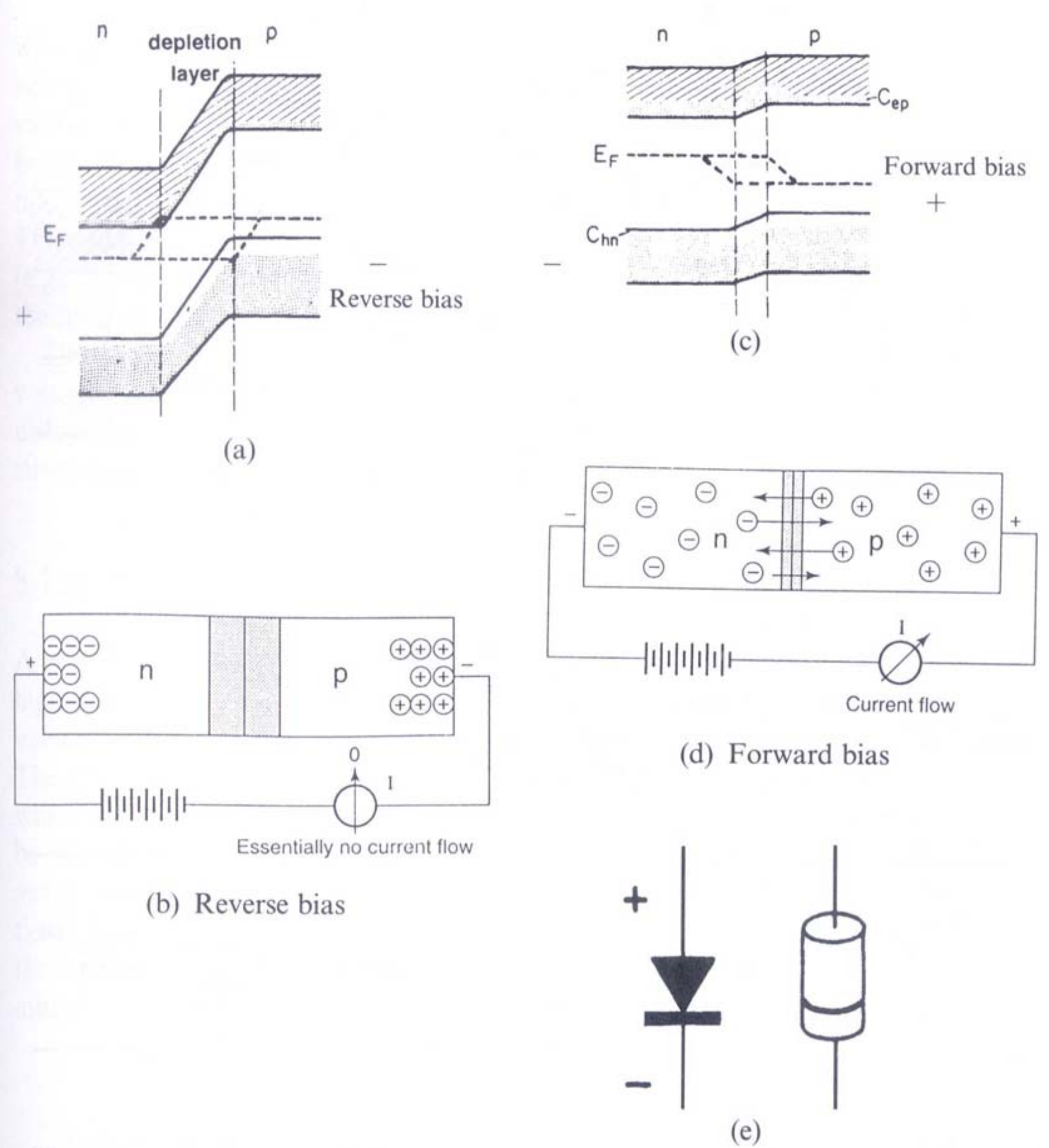


Figure 8.19. (a) + (b) Reverse and (c) + (d) forward biasing of a *p–n* junction (diode). (e) Symbol of a *p–n* rectifier in a circuit and designation of polarity in an actual rectifier.

8.7.4 *p-n* Rectifier (Diode)

The diffusion constant is connected with the mobility (Einstein relation)

$$D_{\mathrm{ep}} = \frac{\mu_{\mathrm{ep}} k_{\mathrm{B}} T}{e}$$

The saturation current, I_S in reverse bias, Shockley equation (ideal diode law)

$$I_{\mathrm{S}} = Ae\left(\frac{C_{\mathrm{ep}} D_{\mathrm{ep}}}{L_{\mathrm{ep}}} + \frac{C_{\mathrm{hn}} D_{\mathrm{hn}}}{L_{\mathrm{hn}}}\right)$$

C_{hn}: equilibrium concentration of the holes in *n*-region, C_{ep} :concentration of electron in the *p*-region, D: diffusion constant, L: diffusion length

The minority carrier diffusion length is given by a reinterpretation of a well known equation of thermodynamics,

$$L_{\mathrm{ep}} = \sqrt{D_{\mathrm{ep}} \cdot \tau_{\mathrm{ep}}}$$

while τ_{ep} is the lifetime of electrons in the p-type region before these electrons are annihilated by recombination with holes

8.7.5 Zener Diode

- **Breakdown:** when the reverse voltage is increased above a critical value, high electric filed causes some electrons to become accelerated with a velocity at which **impact ionization** occurs → **avalanching** process

- **Zener breakdown (Tunneling):** another breakdown process; when the doping is heavy and thus the barrier width becomes very thin (< 10nm), applying high enough reverse voltage causes the bands to shift to the degree that some electron in the valence band of *p*-side are apposite to empty states in the conduction band of *n*-side and these electron can tunnel through the depletion layer (Fig 8.20b) ; a circuit protection device (Fig 8.20d)

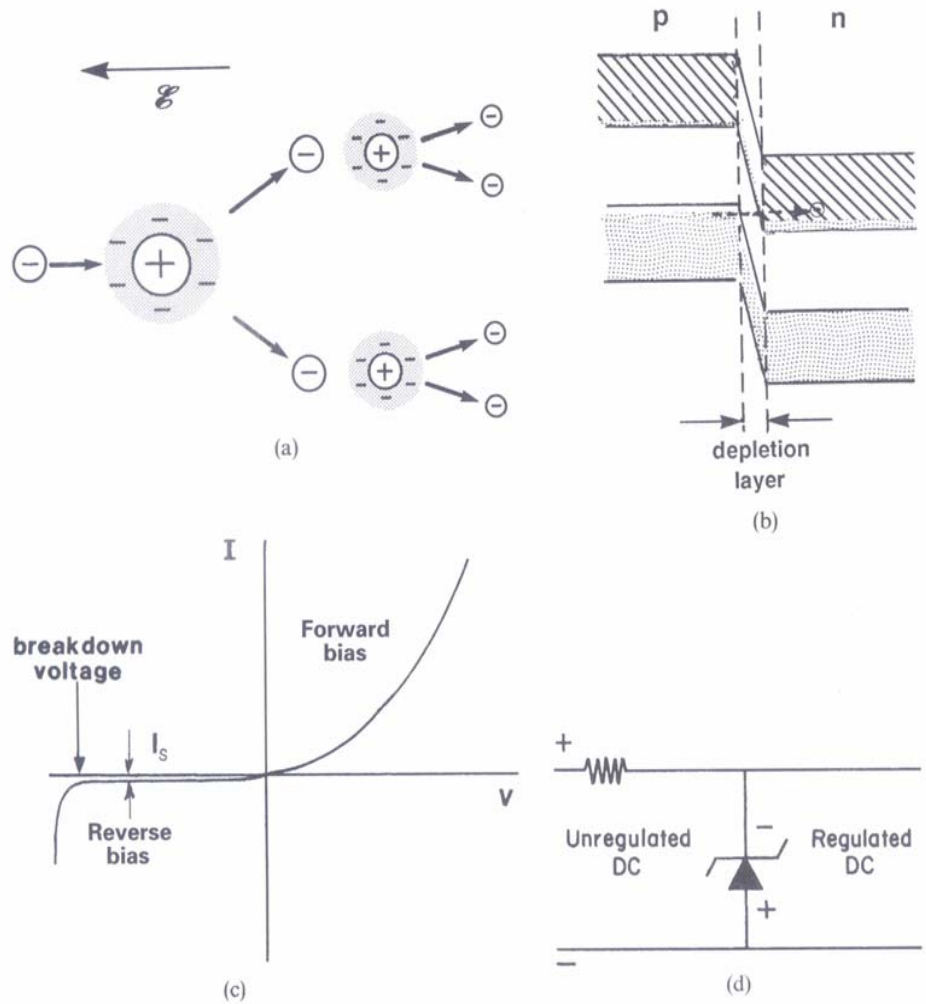


Figure 8.20. (a) Electron avalanche created at breakdown voltage. (b) Tunneling (Zener breakdown). (c) Voltage–current characteristic of a *p–n* diode exhibiting a breakdown voltage at a large reverse voltage. As in Fig. 8.16(a), I_s is shown grossly exaggerated. (d) Zener diode in a circuit for voltage regulation.

8.7 Semiconductor Devices

8.7.6 Solar Cell (Photodiode)

: a *p-n* junction diode

1. Light of high energy fall on or near the depleted area

2. Electron are lifted from the valence band into the conduction band, leaving holes in the valence band

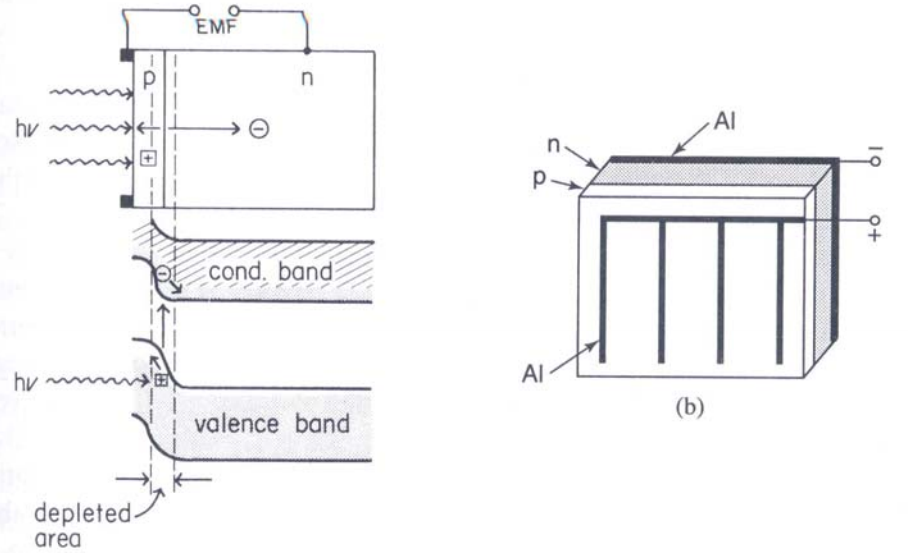


Figure 8.21. Solar cell; the *p*-region is only about 1 μm thick. (a) side view; (b) Front view.

3. The electron in the depleted area immediately "roll down" into the *n*-region, whereas the holes are swept into the *p*-region

→ The carriers can be measured in an external circuit (photographic exposure meter) or used to generate electrical energy

In order to increase the effective area of the junction (Fig 8.21)

- extremely thin *p*-type region (1 μ*m*) :light radiation through *p*-region
- narrow metal electrode (in the form of strips)

Semiconductors

8.7 Semiconductor Devices

8.7.6 Solar Cell (Photodiode)

- **The closer a carrier was created to the *p-n* boundary, the larger is its change of contributing to the current. (the electron - hole created some distance away from the depleted region, do not separated by junction field and eventually recombine; do not contribute to the electric current) : see Fig 8.22**

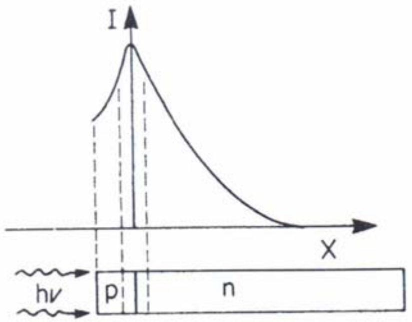


Figure 8.22. Schematic representation of the contribution of electrons and holes to the photocurrent (I) with respect to the distance x from the p–n junction.

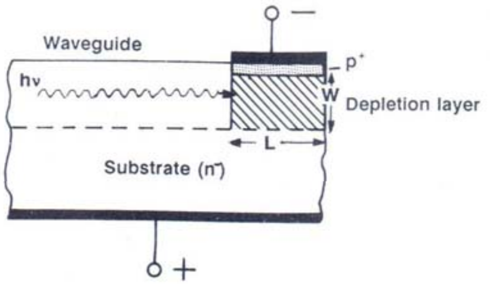


Figure 8.23. Schematic of a transverse-type photodiode that is connected to a light-carrying medium such as an optical fiber or a waveguide ($L \approx 100\,\text{nm}$).

- **Quantum efficiency**

$$\eta = 1 - \frac{\exp(-\alpha W)}{1+\alpha L}$$

***W, L*: the width and length of depletion region**

α : a parameter that determines the degree of photon absorption by the electrons

8.7 Semiconductor Devices

*8.7.7 Avalanche Photodiode

- A *p-n* photodiode that is operated in a high reverse bias mode, i.e. at near-breakdown voltage

1. Electron and holes created by transition from the valence band into the conduction band by the incident light, are accelerated through the depleted area with high velocity → which, in turn, ionize the lattice atom and generate secondary hole-electron pairs, thus generate even more hole-electron pairs → photo current gain
2. Low light-level application, detectors in long-distance, fiber optics telecommunication system

8.7 Semiconductor Devices

*8.7.8 Tunnel Diode

A *p-n* junction diode - depleted area is very narrow ; → heavy doping Fermi energy extends into the valence band of *p*-type semiconductor

energy band diagram and I-V characteristic : Fig 8.24

- The voltage is increase to 100mV (in Fig 8.24d), the potential barrier might be decreased do much that, opposite to the filled *n*-conduction state, no tunneling take place; current decreases with increasing forward voltage: “**negative current-voltage characteristic**” : c-d region

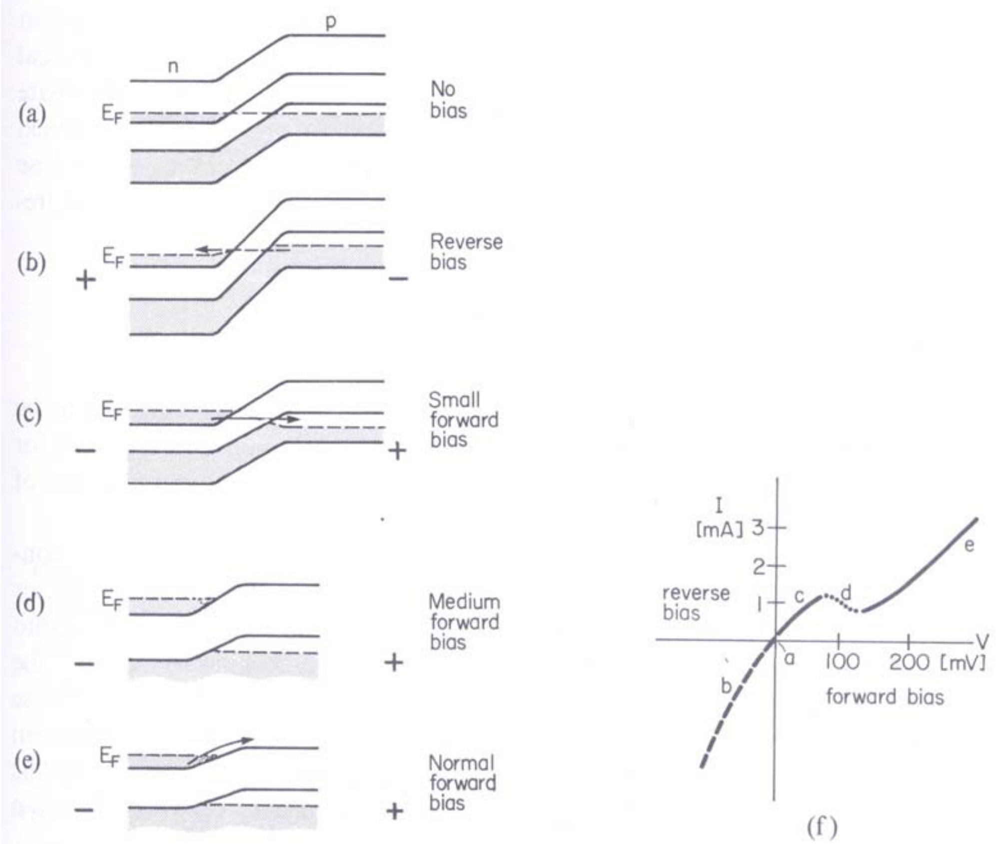


Figure 8.24. (a)–(e) Schematic energy band diagrams for highly doped *n*- and *p*-type semiconductors (tunnel diode). (a) No bias. (b) Reverse bias. (c) Small forward bias. (d) Medium forward bias. (e) “Normal” forward bias. (f) Voltage–current characteristic for a tunnel diode.

8.7 Semiconductor Devices

8.7.9 Transistors

Bipolar Junction Transistor

n-p-n transistor (*n-p* diode back to back with *p-n* diode) ; three connections of the transistor are called emitter(E), base(B), and collector(C)

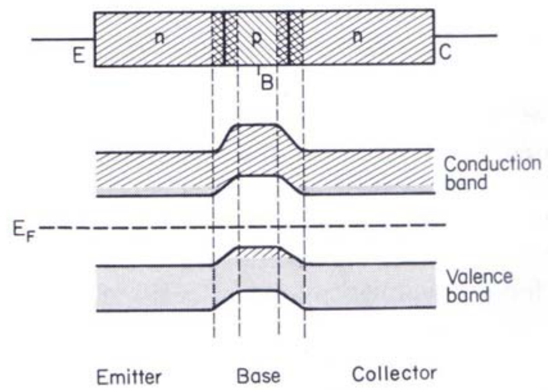


Figure 8.25. Schematic band diagram of an unbiased *n–p–n* bipolar junction transistor.

- For the amplification of a signal, the "diode" consisting of emitter and base is forward biased, whereas the base-collector "diode" is strongly reverse biased (Fig 8.26a)

1.The electrons injected into the emitter needed to have enough energy to be able to "climb" the potential barrier into the base region.

2.The electron diffuse through the base area until they heave reached the depletion region between base and collector.

3.The electrons are accelerated in the strong electric field produced by the collector voltage → this acceleration case amplification of the input a.c signal

8.7 Semiconductor Devices

8.7.9 Transistors

Bipolar Junction Transistor

The electron flow from emitter to collector can be controlled by the bias voltage on the base

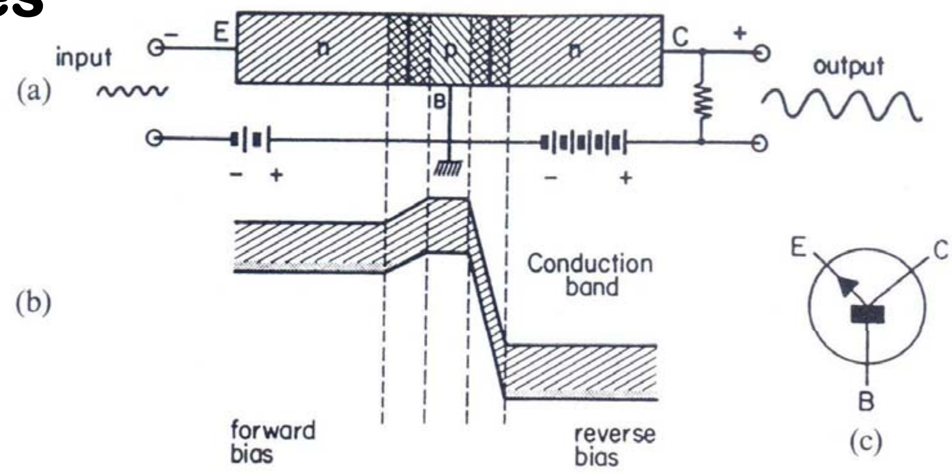


Figure 8.26. (a) Biasing of an *n–p–n* bipolar transistor. (b) Schematic band diagram (partial) of a biased *n–p–n* bipolar transistor. (c) Symbol used for a bipolar *n–p–n* transistor.

- A large positive (forward) bias decreases the potential barrier and the width of the depleted region between emit

→ The electron injection into the *p*-area is relatively high

- A small, but still positive base voltage results in a comparatively larger barrier height and in a wider depletion area, which causes a smaller electron injection from the emitter into the base area.

- the strong collector signal mimics the waveform of the input signal

: this feature is utilized for the amplification of music or voice, etc

8.7 Semiconductor Devices

8.7.9 Transistors

Metal-Oxide-Semiconductor Field-Effect Transistor

- A field-effect transistor consists of a channel through which the charge carriers need to pass on their way from a *source* (S) to the *drain* (D)

- The electrons that flow from the source to the drain can be controlled by an electric field which is established by applying a voltage to the so-called *gate* (G)

- The gate electrode is electrically insulated from the channel by a thin oxide layer which prevent a d.c current to flow from gate to channel

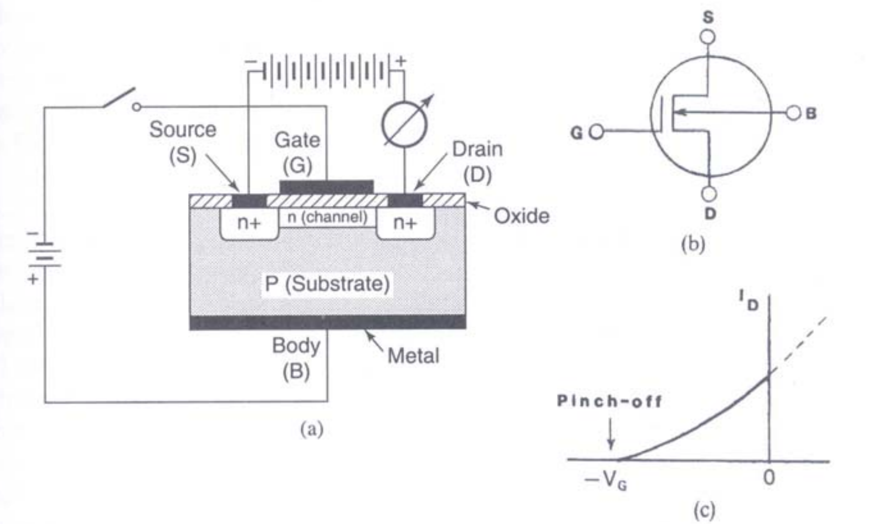


Figure 8.28. (a) Schematic representation of an *n*-channel depletion- (normally on) type MOSFET. The dark areas symbolize the (aluminum) metallizations. The "oxide" layer may consist of SiO_2, nitrides (Si_3N_4), oxinitrides ($Si_3N_4-SiO_2$), or multilayers of these substances. This layer is about 10 nm thick. The gate voltage is applied between terminals G and B. Quite often the B and S terminals are interconnected. (b) Circuit symbol for *n*-channel depletion-type MOSFET. (c) Gate voltage/Drain current characteristic ("Transfer" characteristic). For positive gate voltages (dashed portion of the curve) the device can operate in the "enhancement mode" (see Fig. 8.29(c)).

8.7 Semiconductor Devices

8.7.9 Transistors

Metal-Oxide-Semiconductor Field-Effect Transistor

Two types of MOSFETs are common:

1. **Depletion-type MOSFET or "normally on" MOSFET**

- Consists of high-doped source and drain regions and a low doped channel, all of the same polarity (e.g. *n*-type): Fig8.28a
- The channel width is controlled by the voltage between gate and body
- A negative charge on the gate drives the channel electrons away from the gate and towards the substrate; the conductive region of the channel becomes narrowed by a negative gate voltage.
- The more negative voltage (V_G), the smaller the current through the channel from source to drain until eventually the current is pinched off (Fig 8.28c)

8.7 Semiconductor Devices

8.7.9 Transistors

Metal-Oxide-Semiconductor Field-Effect Transistor

2. Enhancement-type MOSFET or "normally-off" MOSFET

- No built-in channel for electron conduction at least as long as no gate voltage is applied.
- If large enough positive voltage is applied to the gate, most of the holes immediately below the gate oxide are repelled, i.e., they are driven into the substrate, thus removing possible recombination sites and negative charge carriers are attracted into this channel; a path for the electrons between source and drain can be created by a positive gate voltage

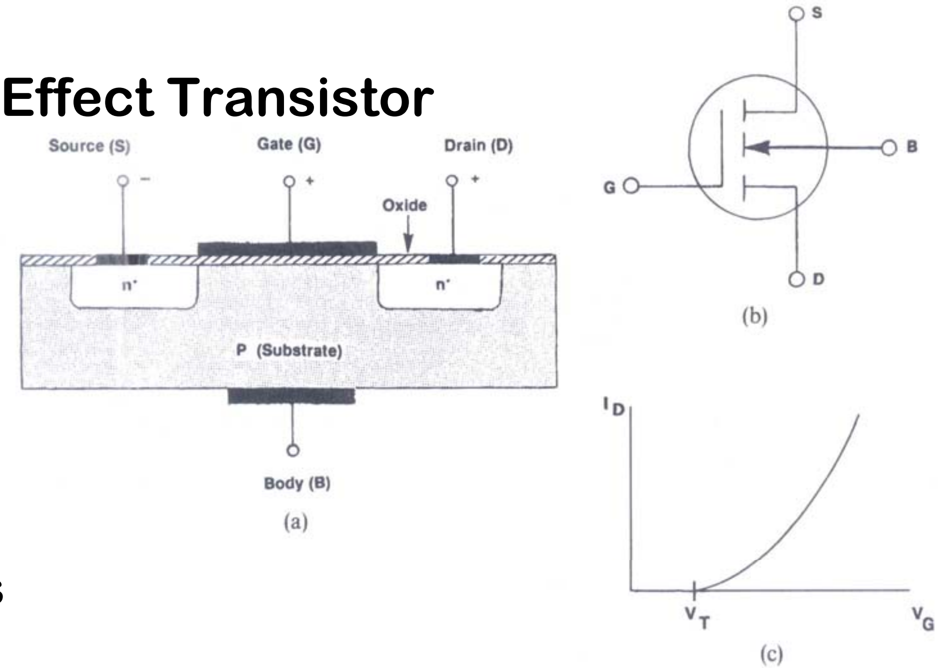


Figure 8.29. (a) Enhancement (normally-off)-type *n*-channel MOSFET. For details, see the caption of Fig. 8.28. (b) Circuit symbol. (The broken line indicates that the path between S and D is normally interrupted.) (c) Gate voltage (V_G)/drain current (I_D) characteristic. V_T is the threshold gate voltage above which a drain current sets in.

- Usages: memories, microcomputers, logic circuits, amplifiers, analog switches and operational amplifiers

8.7 Semiconductor Devices

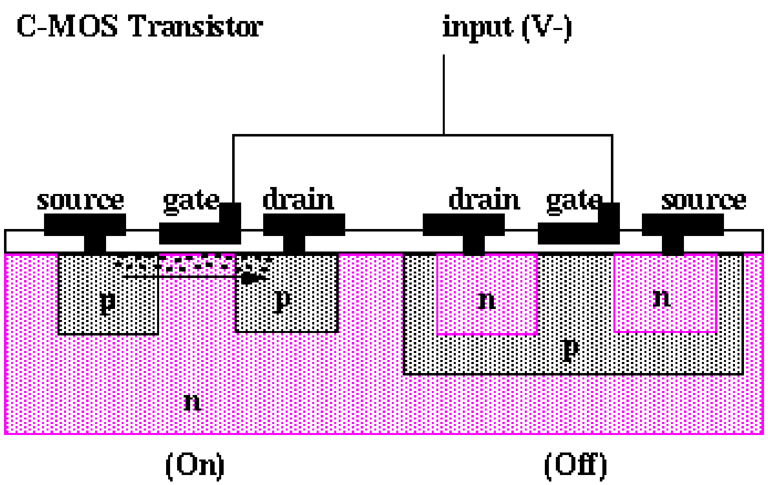
8.7.9 Transistors

Metal-Oxide-Semiconductor Field-Effect Transistor

CMOSFET: *complementary* MOSFET

- Both an n-channel and a p-channel device are integrated on one chip and wired in series

- This tandem device has become the dominant technology for information processing, because of its low operating voltage (0.1V), low powder consumption, and short channel length with accompanying high speed



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Semiconductors

8.7 Semiconductor Devices

8.7.10. Quantum Semiconductor Devices

-To explain the nature of a quantum device: recall “the behavior of one electron in a potential well (Sec 4.2)”

- *Size quantization* : dimensions of the crystalline solid are reduced to the size of the wavelength of electron (e.g., 20nm for GaAs ; → density of state, Z(E) is quantized

- A small-band gap material is sandwiched between two layers of a “wide-band gap material (Fig 8.33a,b): the configuration for which all three dimensions of the center materials have values near the electron wavelength, is called **quantum dot** (quantum wire for 2-d, **quantum well** for 1-d confinement) → potential barrier between two GaAs region

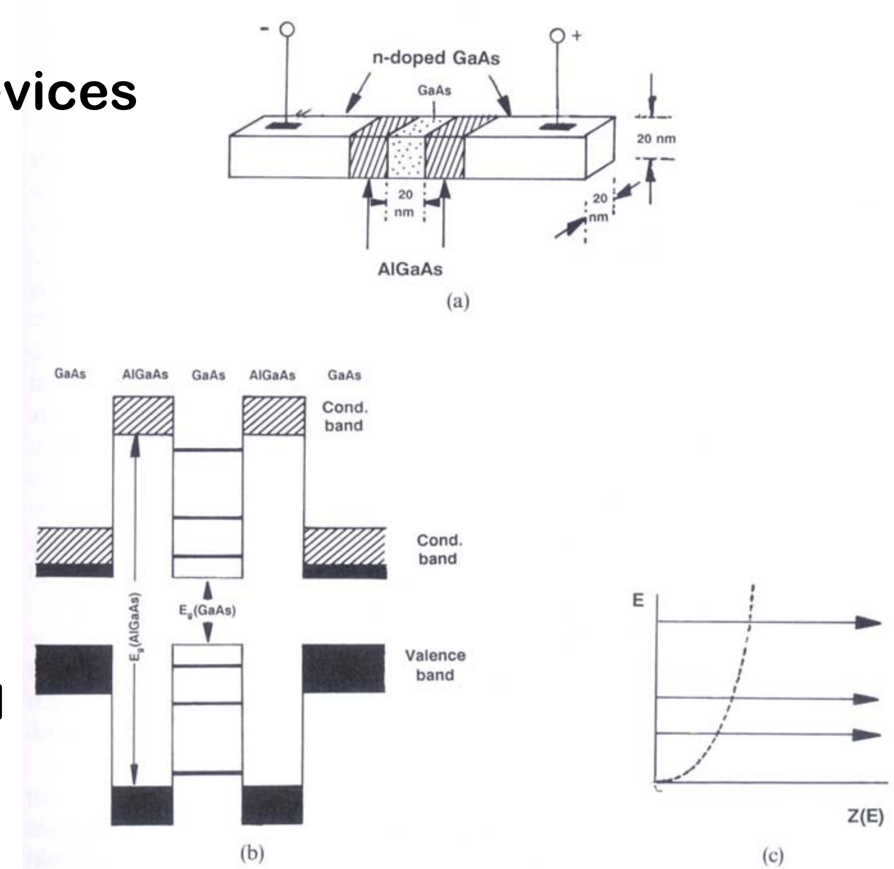

Figure 8.33. (a) Schematic representation of a quantum dot structure. (b) Energy levels for GaAs for the quantum dot structure depicted in (a). (*Note*: The gap energy difference between GaAs (E_g = 1.42 eV) and AlGaAs is greatly exaggerated. This difference may be as small as 0.2 eV.) (c) Discontinuous density of energy states for a quantum dot structure. The dashed parabola indicates the density of states for a bulk crystal, as is known from Fig. 6.4.

8.7 Semiconductor Devices

8.7.10. Quantum Semiconductor Devices

- Fig 8.34: If a large voltage is applied to the device, the conduction band of the *n*-doped GaAs is raised to a level at which its conduction electrons are at the same height as an empty energy state of the center GaAs region.

→ At this point, the electrons are capable of tunneling though the potential barrier formed by the AlGaAs region and thus reach one of these discrete energy state

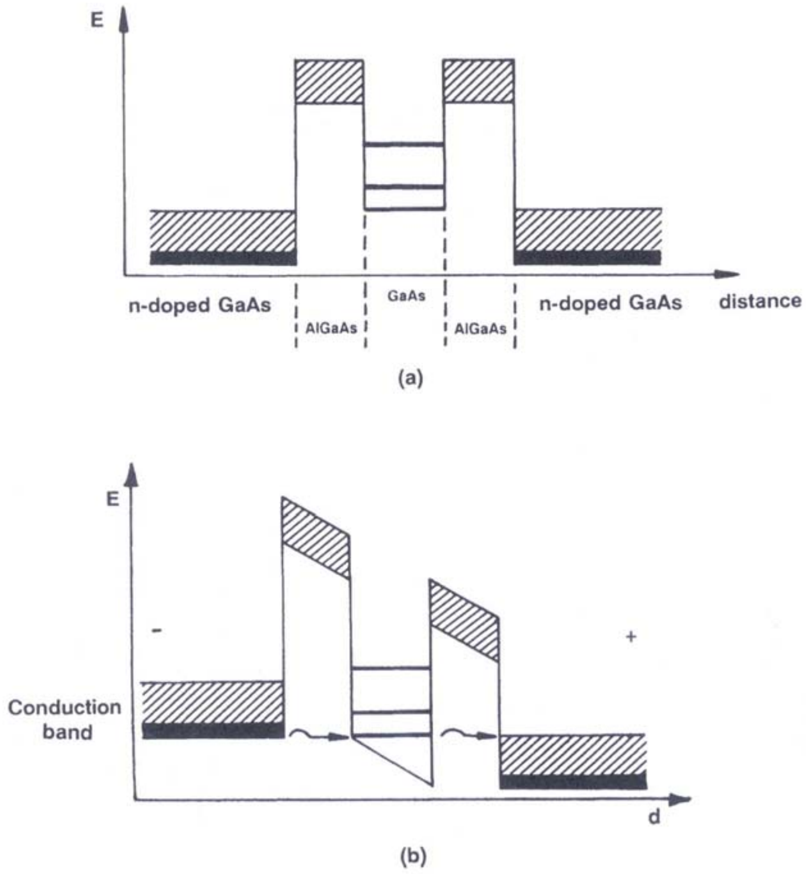

Figure 8.34. Parts of two energy band structures for the quantum device shown in Fig. 8.33. For simplicity, only the conduction bands are shown. (a) No applied voltage. (b) With applied voltage, which facilitates electron tunneling from the conduction band of the *n*-doped GaAs into an empty energy level of the center GaAs region.

8.7 Semiconductor Devices

8.7.10. Quantum Semiconductor Devices

- If a slightly higher voltage is applied, the electrons of the n-doped GaAs are no longer at par with an empty energy level and tunneling comes to a near standstill a I-V characteristic with negative differential resistance (Fig 8.35)

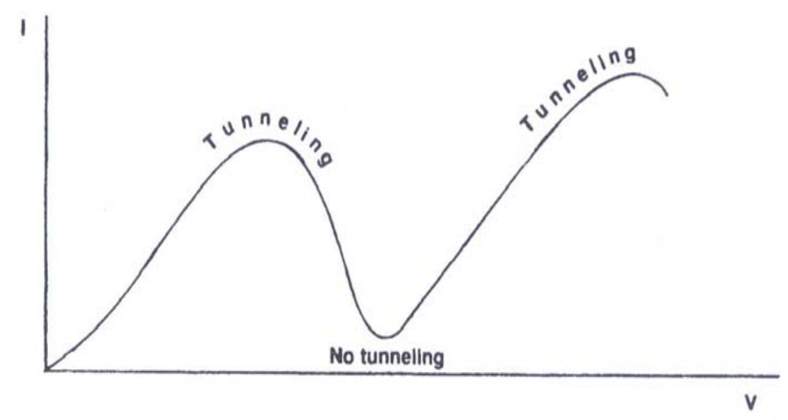

Figure 8.35. Current–voltage characteristic of a quantum dot device as depicted in Figs. 8.33 and 8.34.

- An array of a multitude of quantum wells stacked on top of each other : The periodic arrangement of wide-band gap and narrow band gap materials is called *supperlattice*

- Quantum devices are about one-hundredth of the size of presently known FETs

- The major problems have still to be overcome concerning interconnections, device architecture, and fabrication of three-terminal devices

8.7 Semiconductor Devices

8.7.11. Semiconductor Device Fabrication

(Text reading p.146-155)

Techniques for single-crystal growth

1.Czochralski

2. Float-zone technique

3. Bridgman tech

Once the rods have been obtained,

They are sliced, lapped, etched, and

polished to obtain 0.3-0.4mm thick

wafers

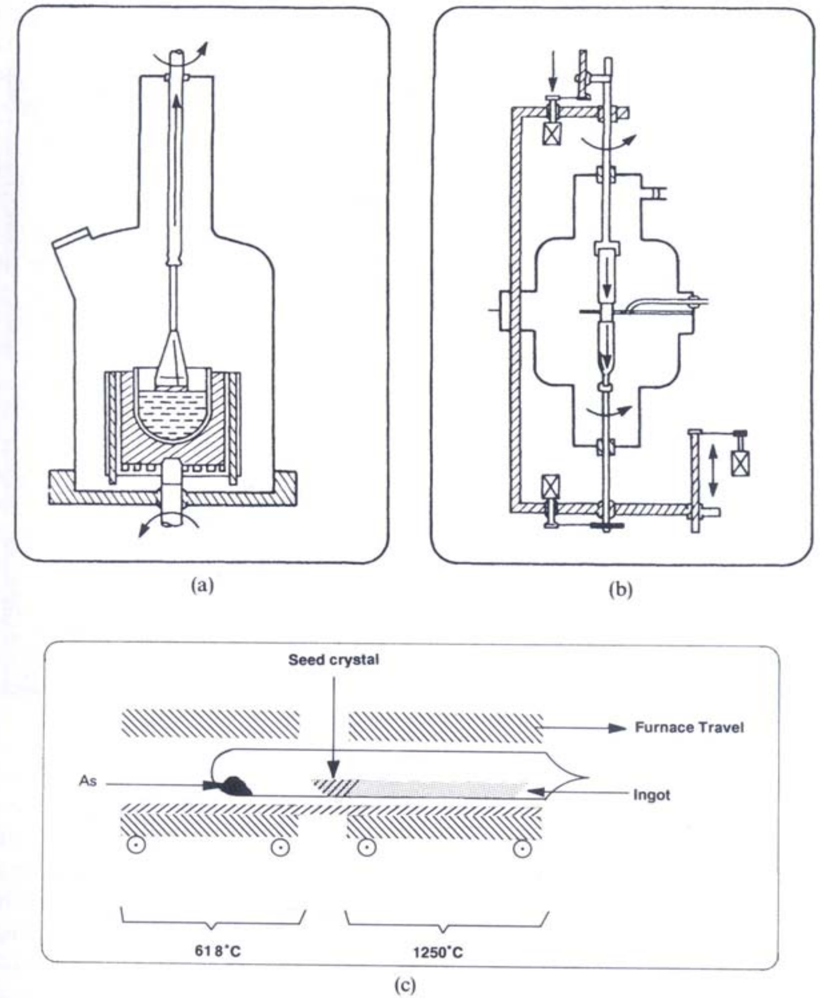

Figure 8.36. Techniques for single-crystal growth. (a) Czochralski method. Heating is performed by radio frequency coils or (for big crucibles) by resistance heating. (b) Float zone method. (c) Bridgman method (demonstrated for GaAs). (d) A 300 mm (12 inch) silicon single crystal is removed from the crucible. (Courtesy Wacker Siltronic AG)

8.7 Semiconductor Devices

8.7.11. Semiconductor Device Fabrication

Device fabrication on the wafers

- Surface oxidation,
- Photolithography
- Oxide Etch
- Photoresist Strip
- Doping
- Metallization
- Packaging

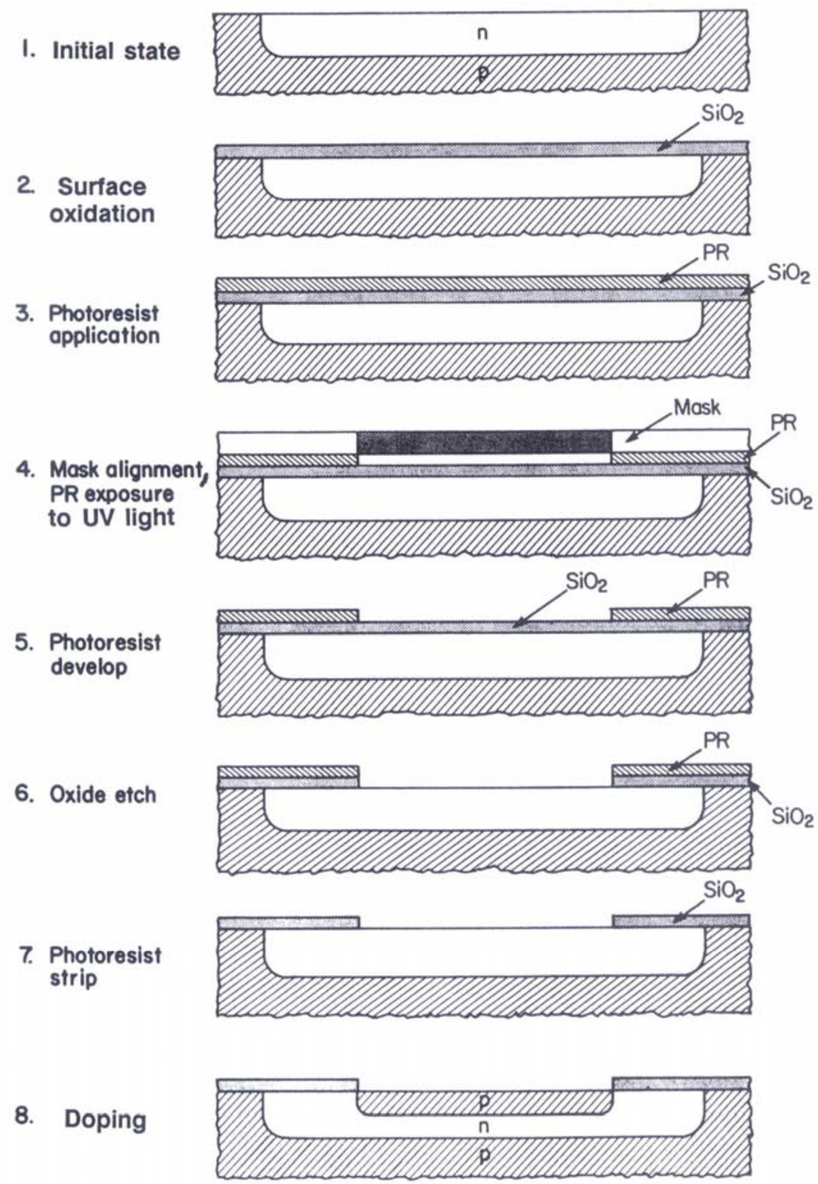

Figure 8.37. Photoresist (PR) masking sequence to obtain a p–n–p bipolar transistor