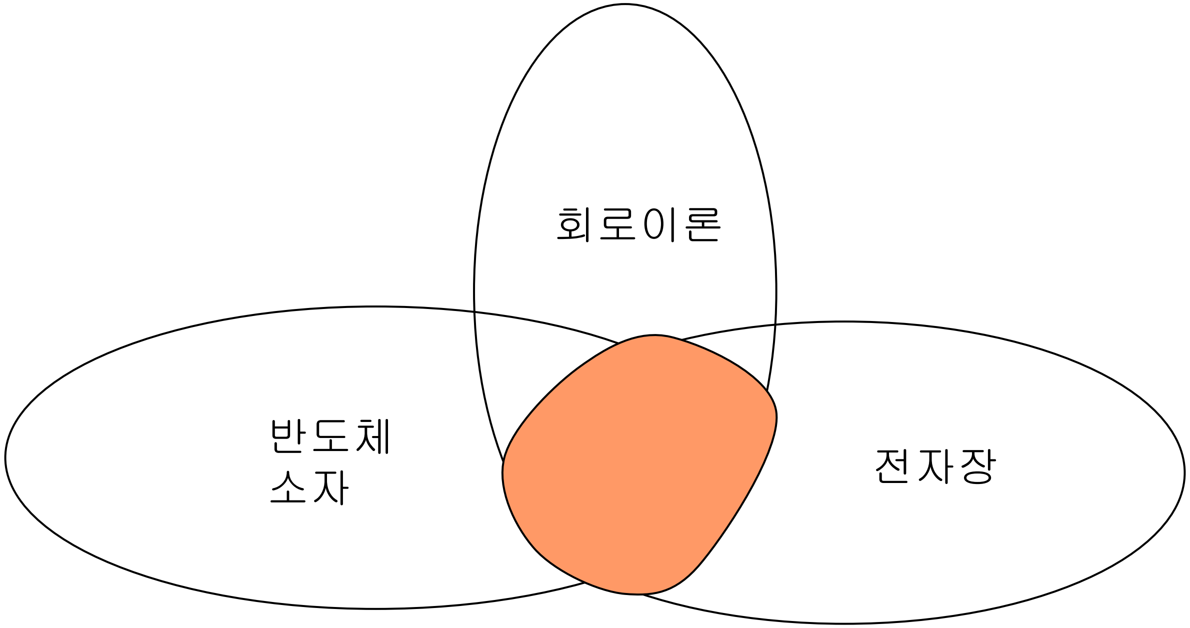
Microelectronics Circuits 1 Review

Prof. Y.Kwon

Electronic Circuits



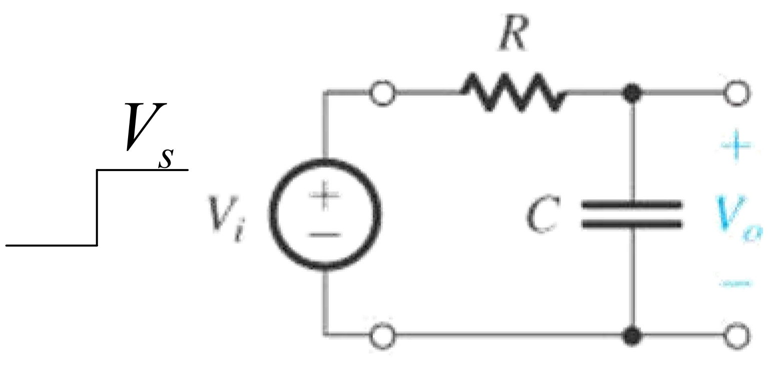
- Static phenomenon only
- Simplified transistor model : MOSFET and BJT
- Interested in “voltage” gain rather than “power” gain
- Consists of “analog” integrated circuit and “digital” integrated circuit

Contents to Cover in this Course and Evaluation

- Chap 8 : Feedback Amplifier
- Chap 9 : Operational Amplifier
- Chap 12 : Filters and Tuned Amplifier (12.1 ~ 12.7)
- Chap 13 : Signal Generators and Waveform-Shaping Circuits (13.1~13.5)
- Chap 14 : Output Stage and Power Amplifiers (14.1 ~ 14.5)
- Chap 10 & 11 : Basics of Digital Circuits

- Evaluation
  - Two mid terms and One final exam
  - Attendance
  - Homework

Physical understanding of STC



(a)

$$V_o = \frac{Q}{C}$$

$$Q(t=0^-) = 0 \rightarrow V_o(t=0^-) = 0$$

$$V_o = (t=\infty) = V_s \rightarrow Q(t=\infty) = C * V_s$$

$Q(t) = \int_0^t I(\tau)d\tau$ →requires large I to reduce t

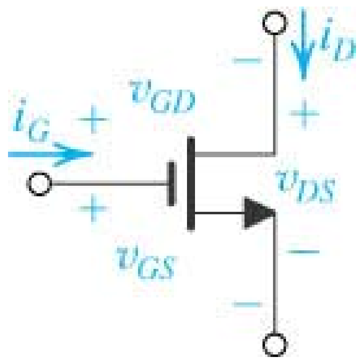
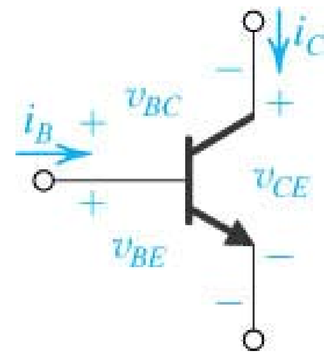
$I = \frac{V_I - V_s}{R}$ →requires small R

Time Constant = RC

takes more charge to raise voltage level

Comparison of the MOSFET & the BJT

TABLE 6.3 **Comparison of the MOSFET and the BJT**

	NMOS	npn
Circuit Symbol		

To Operate in the Active Mode, Two Conditions Have To Be Satisfied

NMOS

(1) Induce a channel;

$$V_{GS} \geq V_t, V_t = 0.5-0.7 \text{ V}$$

Let $V_{GS} = V_t + v_{ov}$

(2) Pinch-off channel at drain;

$$V_{GD} < V_t$$

or equivalently,

$$v_{DS} \geq V_{OV}, V_{ov} = 0.2\text{-}0.3\text{V}$$

npn

(1)Forward-bias EBJ;

$$v_{BE} \geq V_{BE\,on}, V_{BE\,on} \cong 0.5V$$

(2)Reverse-bias CBJ;

$$v_{BC} < V_{BCon}, V_{BCon} \cong 0.4\text{V}$$

or equivalently

$$v_{CE} \geq 0.3\text{V}$$

Comparison of the MOSFET & the BJT

Current-Voltage Characteristics in the Active Region

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2\left(1 + \frac{v_{DS}}{V_A}\right)$$

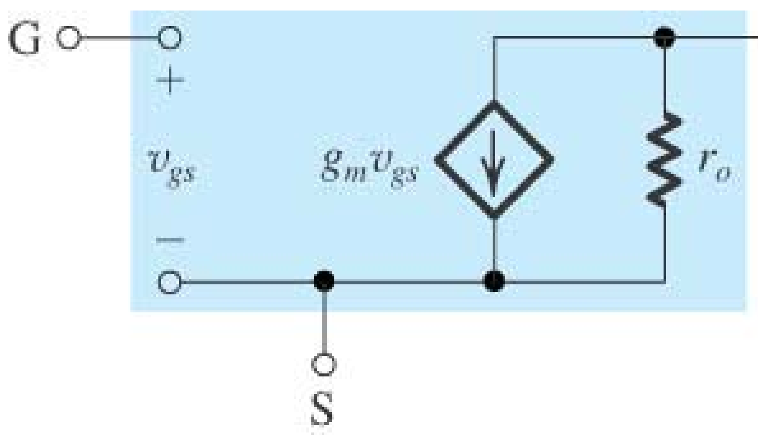
$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v^2_{ov}\left(1 + \frac{v_{DS}}{V_A}\right)$$

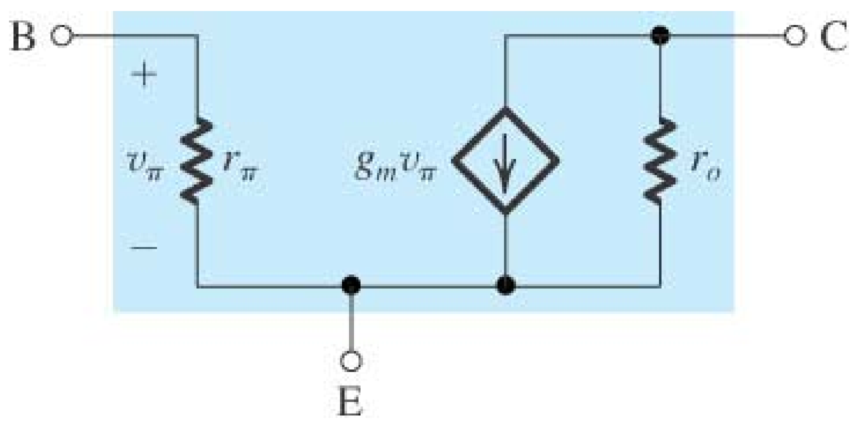
$$i_G = 0$$

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

$$i_B = i_C/\beta$$

Low-Frequency Hybrid-π Model





Comparison of the MOSFET & the BJT

	MOSFET	BJT
Transconductance g_m	$g_m = I_D/(V_{ov}/2)$ $g_m = (\mu_n C_{ox})\left(\frac{W}{L}\right)V_{ov}$ $g_m = \sqrt{2(\mu_n C_{ox})\left(\frac{W}{L}\right)I_D}$	$g_m = I_C/V_T$
Output resistance r_0	$r_0 = V_A/I_D = \frac{V'_A L}{I_D}$ $\Rightarrow r_0$ is inversely proportional to the bias current.	$r_0 = V_A/I_C$
Input Resistance with Source (Emitter) Grounded	∞	$r_\pi = \beta/g_m$

Comparison of the MOSFET & the BJT

Intrinsic Gain

$A_0 = g_m r_o$

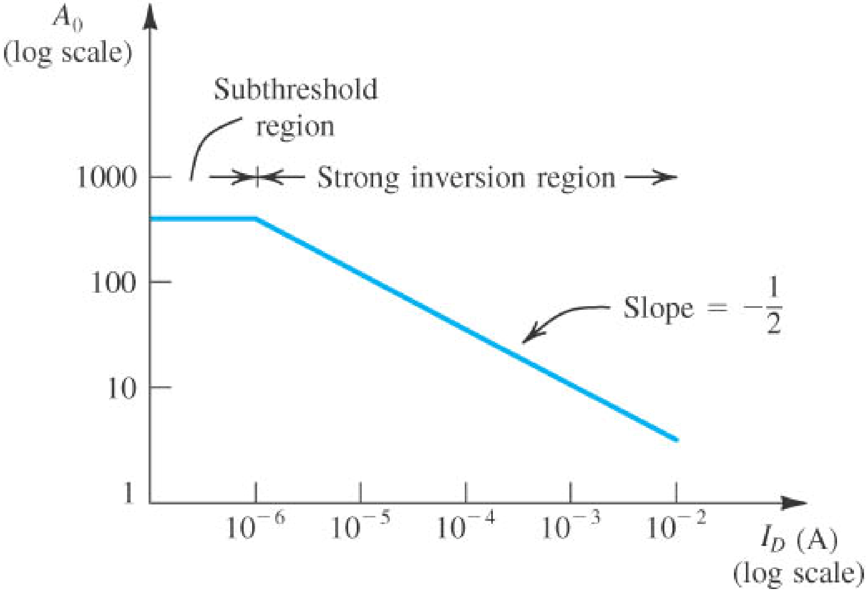
$$A_0 = V_A / (V_{OV} / 2)$$

$$A_0 = \frac{2V_A' L}{V_{OV}}$$

$$A_0 = \frac{V_A' \sqrt{2\mu_n C_{ox} WL}}{\sqrt{I_D}}$$

$$A_0 = g_m r_o = \frac{I_C}{V_T} \cdot \frac{V_A}{I_C} = V_A / V_T$$

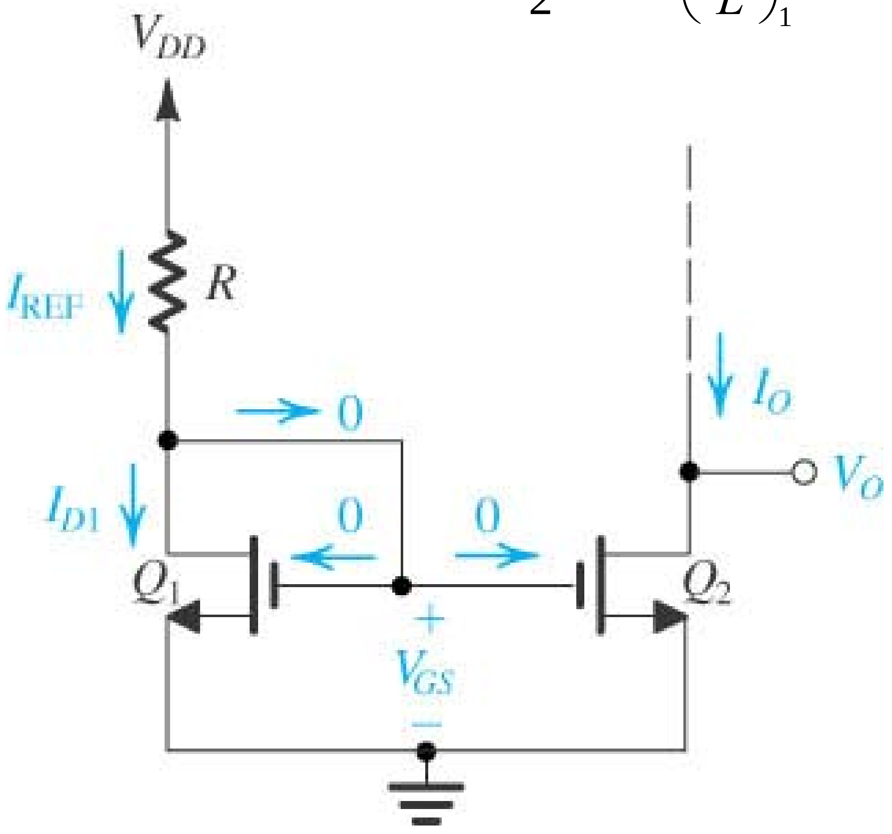
$$A_0 = 1000 \sim 5000 V/V$$



Current Mirror Circuit

Transistor Q_1 : Drain is shorted to its gate. $\Rightarrow$ Saturation mode

$$i_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{tn}\right)^2$$



Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

R : In most cases, outside the IC chip

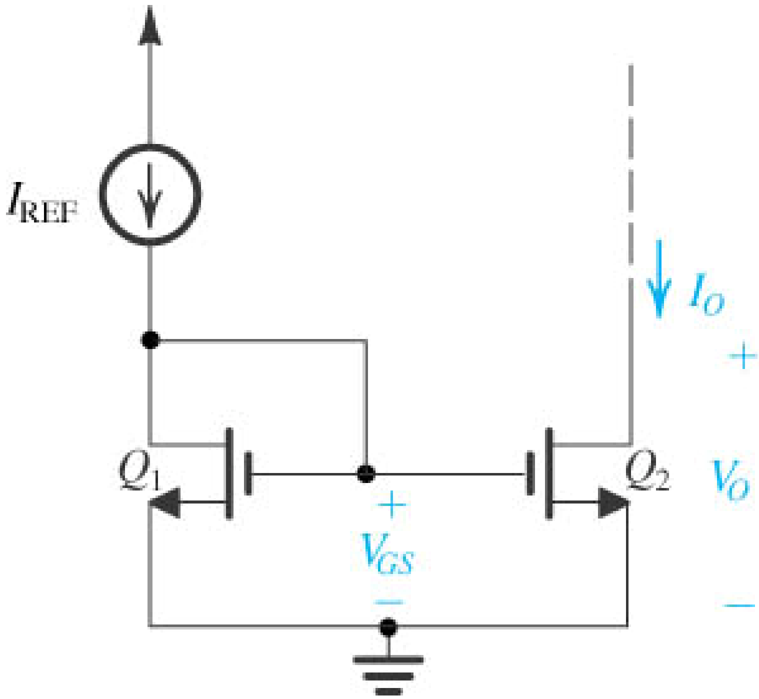
Assuming Q_2 in the satuaration mode,

$$I_O = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2 \left(V_{GS} - V_{tn}\right)^2$$

$$\Rightarrow \frac{I_O}{I_{REF}} = \frac{\left(W/L\right)_2}{\left(W/L\right)_1}$$

I_O / I_{REF} is soley determined by the geometries of the transistors.

Current Mirror Circuit



To ensure that Q_2 is saturated,

$V_O \geq V_{GS} - V_t$ or equivalentely $V_O \geq V_{OV}$.

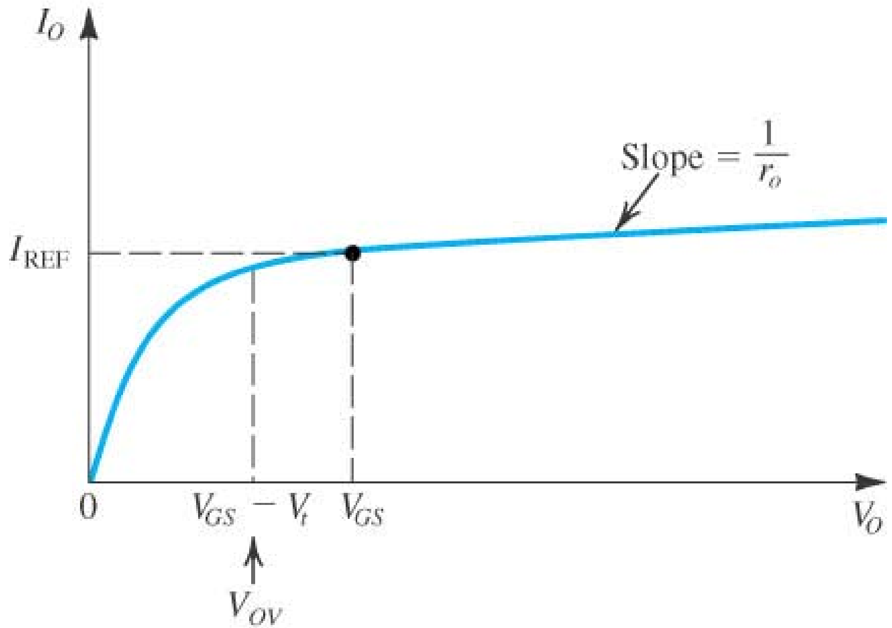
At $V_O = V_{GS}$, $I_O = I_{REF}$.

As V_O increases above V_{GS},

I_O will increase according to

the incremental output resistance r_{02} of Q_2.

Current Mirror Circuit



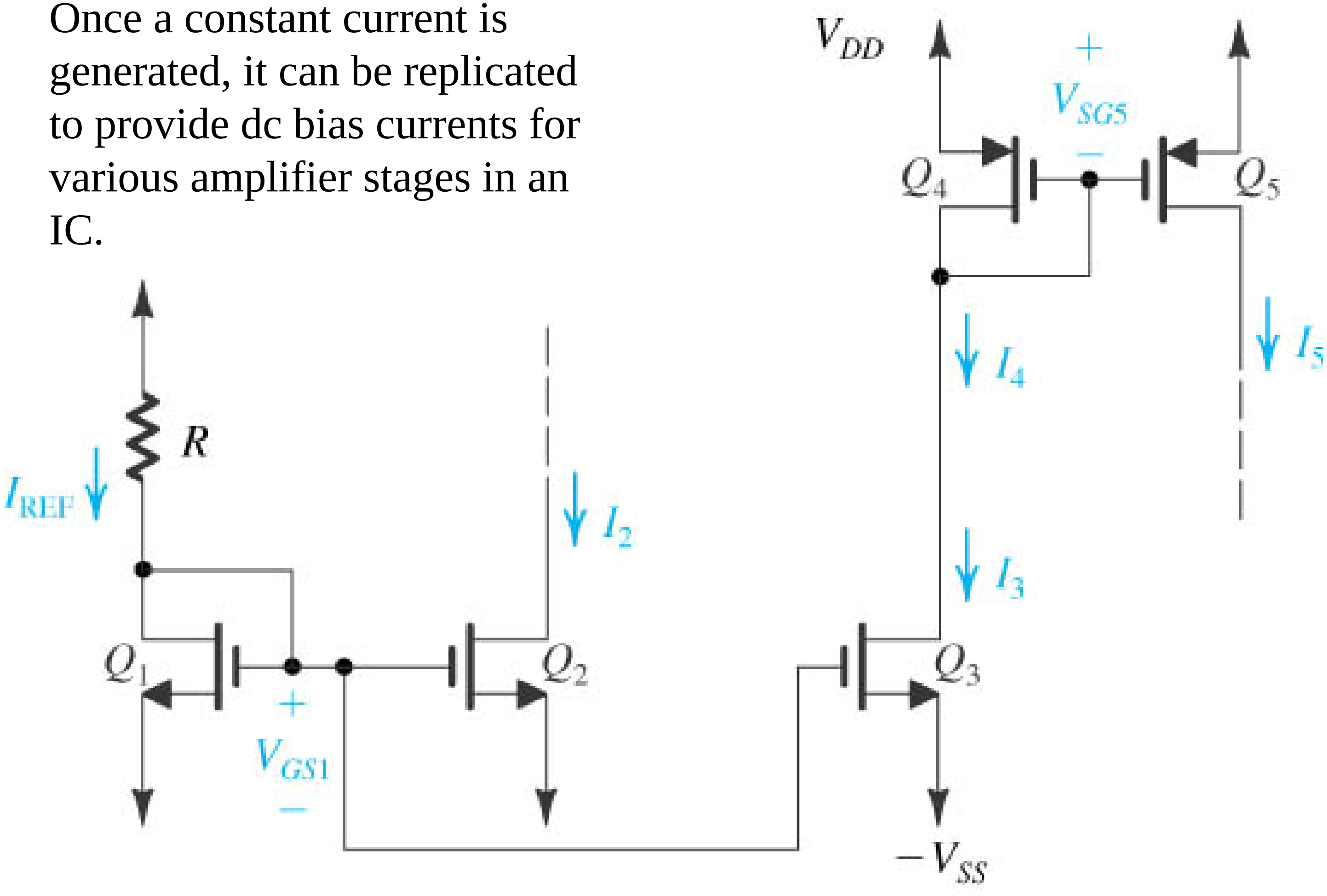
As V_O is increases above V_{GS}, I_O will increase according to the incremental output resistance r_{02} of Q_2.

$$R_o \equiv \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O}$$

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF} \left(1 + \frac{V_O - V_{GS}}{V_{A2}}\right)$$

Current Steering Circuit

Once a constant current is generated, it can be replicated to provide dc bias currents for various amplifier stages in an IC.



F_H Estimation : Open-circuit time constant Method

- High Frequency Gain Function : $A(s) = A_M F_H(s)$ A_M : *Midband Gain*

$$F_H(s) = \frac{(1+s/\omega_{Z1})(1+s/\omega_{Z2})\cdots(1+s/\omega_{Zn})}{(1+s/\omega_{P1})(1+s/\omega_{P2})\cdots(1+s/\omega_{Pn})} = \frac{1+a_1 s + a_2 s^2 + \cdots + a_n s^n}{1+b_1 s + b_2 s^2 + \cdots + b_n s^n}$$

$$b_1 = \frac{1}{\omega_{P1}} + \frac{1}{\omega_{P2}} + \cdots + \frac{1}{\omega_{Pn}}$$

- Practical Bandwidth is determined by 3dB roll-off point (ω_H)

- When dominant pole exists, $F_H(s) \cong \dfrac{1}{1+s/\omega_{P1}}$ & $\omega_H \cong \omega_{P1}$

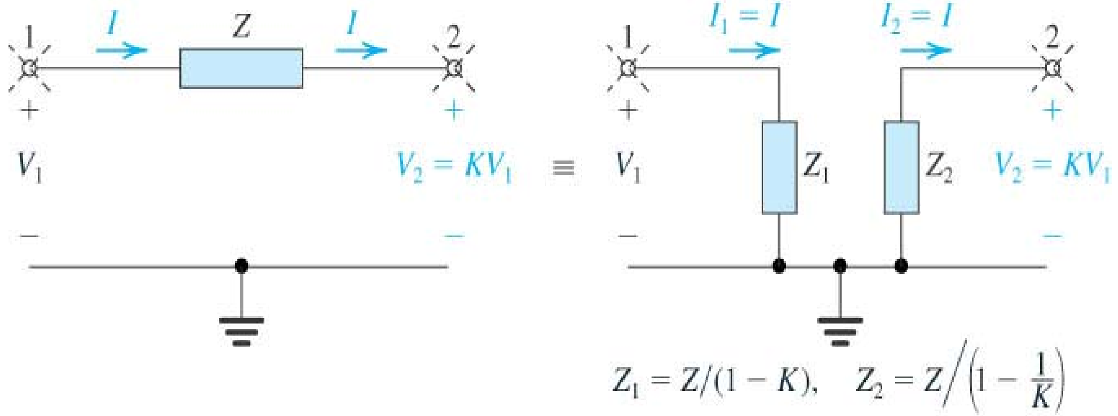
- Gray and Searle → $b_1 = \sum_i C_i R_{io}$
- IF there is dominant pole,

$$b_1 \cong \frac{1}{\omega_{P1}} \rightarrow \omega_H \approx \omega_{P1} \approx \frac{1}{b_1} = \frac{1}{\left|\sum_i C_i R_{io}\right|}$$

- This result are very good even if no dominant pole exists.

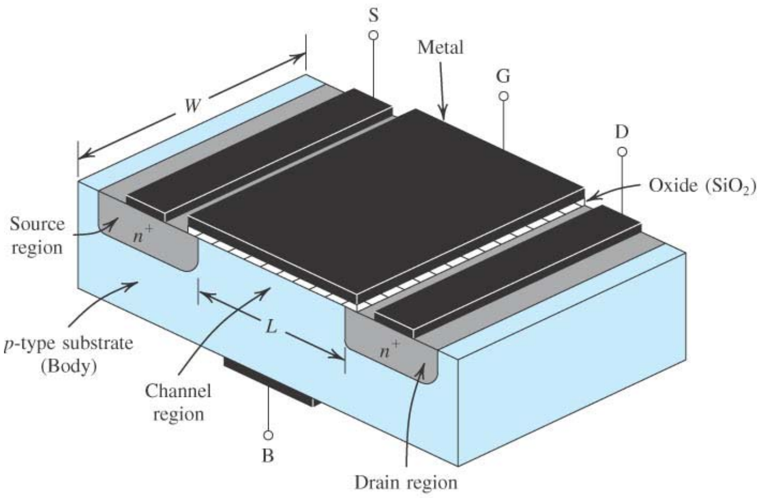
Miller's Theorem

- When the circuit conditions remain to make $V_1 = KV_2$



- Proof : derive the same I/V relationship at both ports
- $(1-K)$ → Miller multiplication ("Miller Effect") for conductance or susceptance

The MOSFET internal capacitances and high-frequency model



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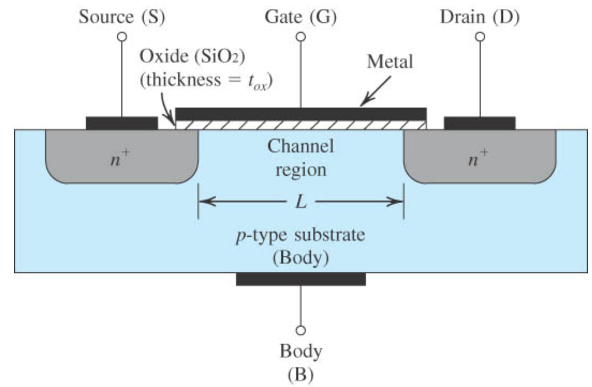

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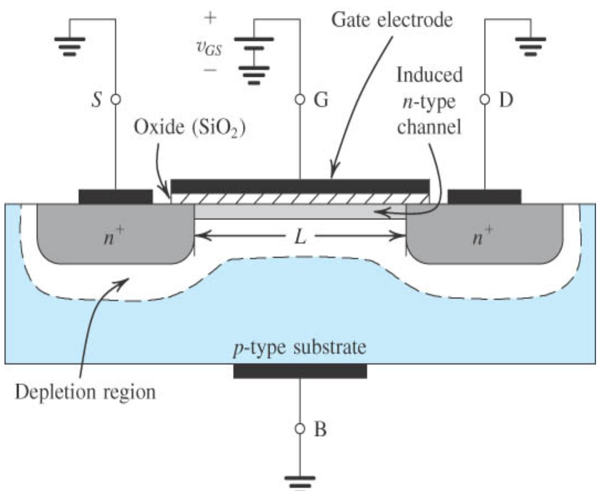


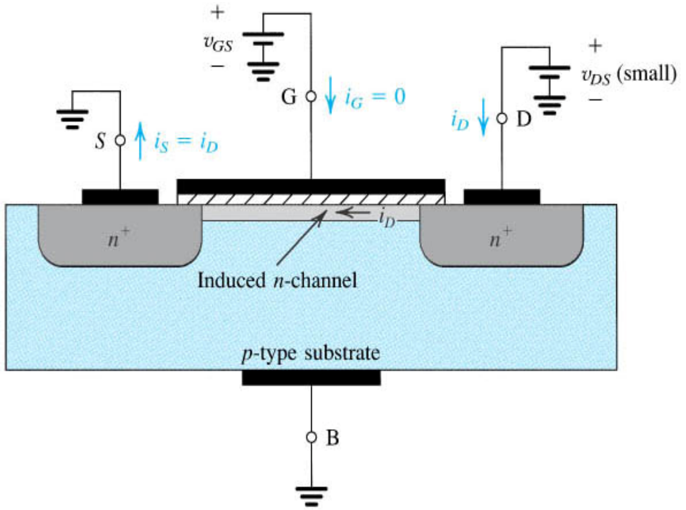
Five capacitance

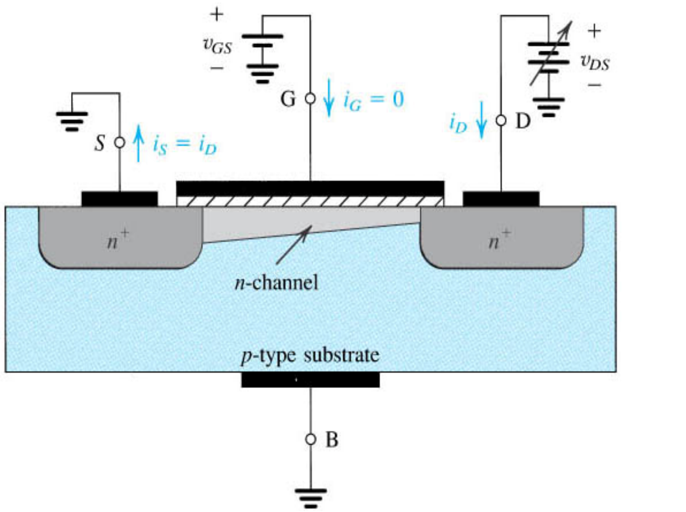
C_{gs}, C_{gd}, C_{gb}, C_{sb} and C_{db}

The MOSFET internal capacitances and high-frequency model

- The gate capacitive effect
  - Triode region
    - $C_{gs} = C_{gd} = 1/2WLC_{ox}$
  - Saturation region
    - $C_{gs} = 2/3WLC_{ox}$
    - $C_{gd} = 0$
  - Cutoff
    - $C_{gs} = C_{gd} = 0$
    - $C_{gb} = WLC_{ox}$
- The junction capacitances

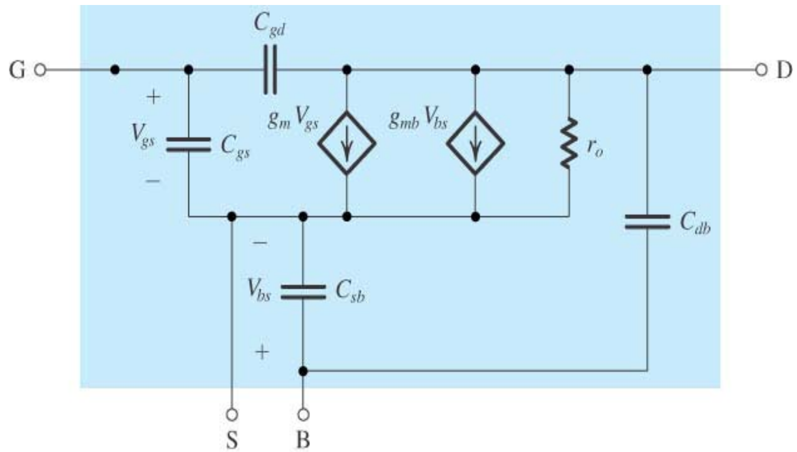
$$C_{sb} = \frac{C_{sbo}}{\sqrt{1+\frac{V_{SB}}{V_o}}}, \quad C_{db} = \frac{C_{dbo}}{\sqrt{1+\frac{V_{DB}}{V_o}}}$$





The MOSFET internal capacitances and high-frequency model

- The high-frequency MOSFET model



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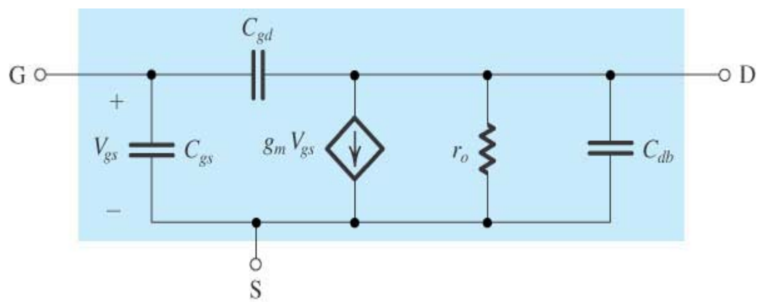

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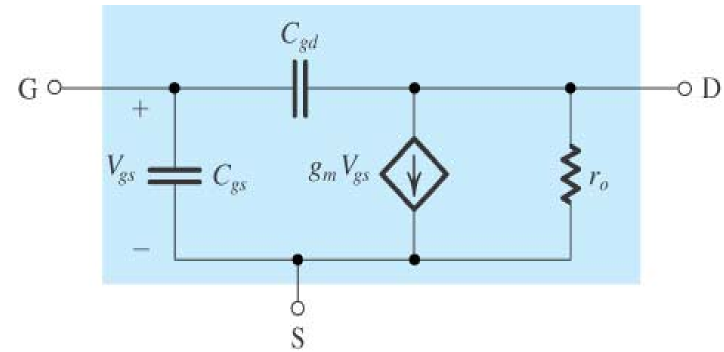


(c)

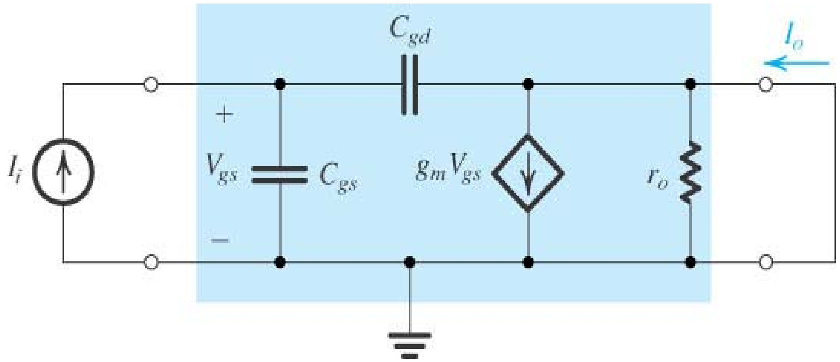
(a) High-frequency equivalent circuit model for the MOSFET.

(b) The equivalent circuit for the case in which the source is connected to the substrate (body).

(c) The equivalent circuit model of (b) with C_{db} neglected (to simplify analysis).

The MOSFET internal capacitances and high-frequency model

- The MOSFET unity-gain frequency (f_T)



Determining the short-circuit current gain I_o/I_i.

The frequency at which the short-circuit curent-gain of the common-source configuration becomes unity.

$$I_o = g_m V_{gs} - sC_{gd} V_{gs}$$

$$I_o \cong g_m V_{gs}$$

$$V_{gs} = I_i / s(C_{gs} + C_{gd})$$

$$\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})}$$

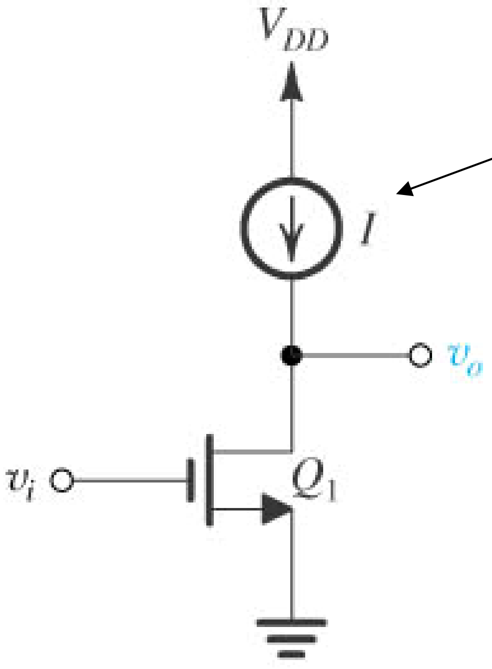
For physical frequencies $s = j\omega$

$$\omega_T = g_m / (C_{gs} + C_{gd})$$

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Typically, f_T ranges from about 100MHz for the older technologies (e.g., a 5-um CMOS process) to many GHz for newer high-speed technologies (e.g., a 0.13-um CMOS process).

CS Amplifier



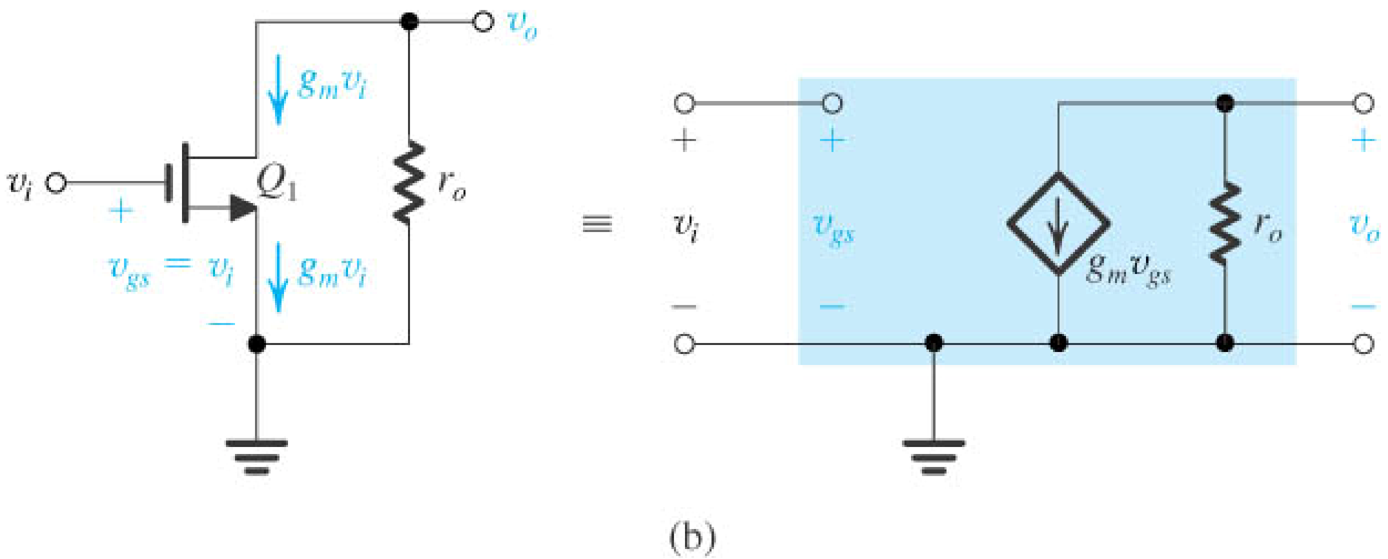
(a)

(1) The current source can be implemented using a PMOS transistor.
➔ Active load

(2) Obviously, Q_1 is biased at $I_D = I$.
But what are V_{DS} and V_{GS}?

➔ We just assume that the MOSFET is biased to operate in the saturation region throughout this chapter.

CS Amplifier



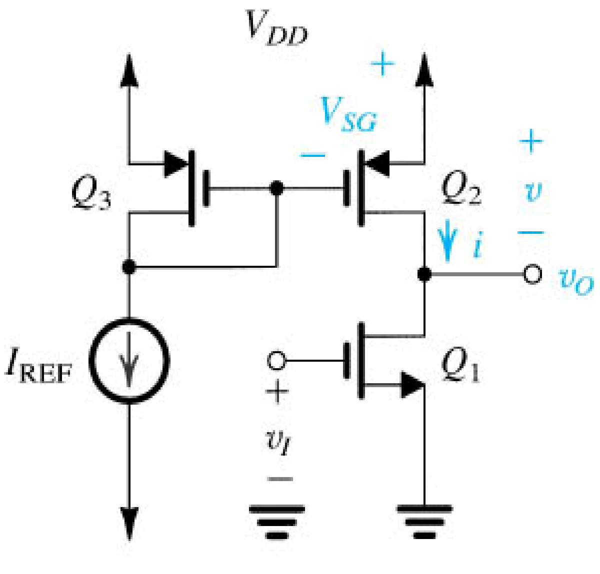
$$R_i = \left.\frac{v_i}{i_i}\right|_{RL=\infty} = \infty$$

$$A_{vo} = \left.\frac{v_o}{v_i}\right|_{RL=\infty} = -g_m r_o$$

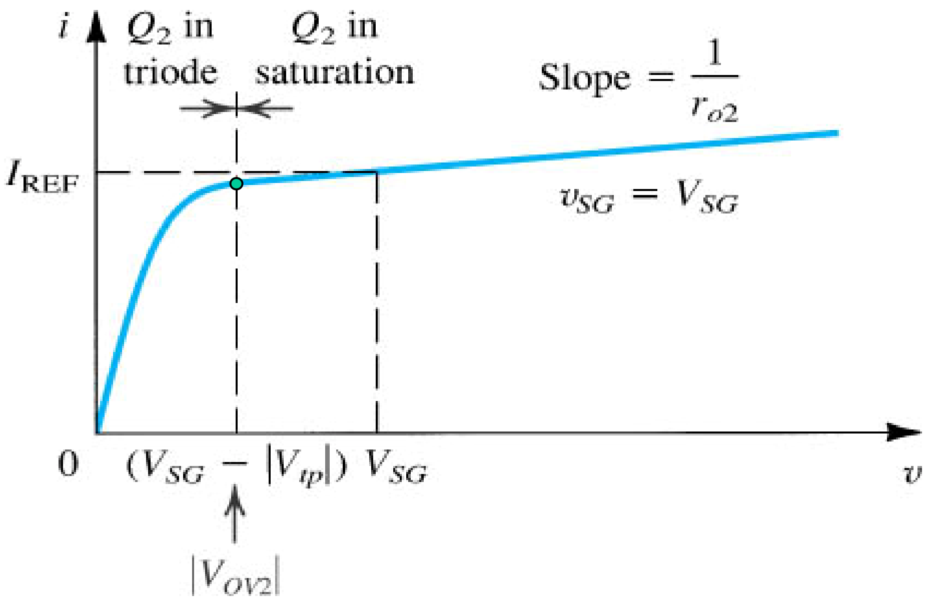
$$R_o = \left.\frac{v_x}{i_x}\right|_{vi=0} = r_o$$

$A_0 = g_m r_o$: Intrinsic gain of MOSFET

CS Amplifier



(a)



(b)

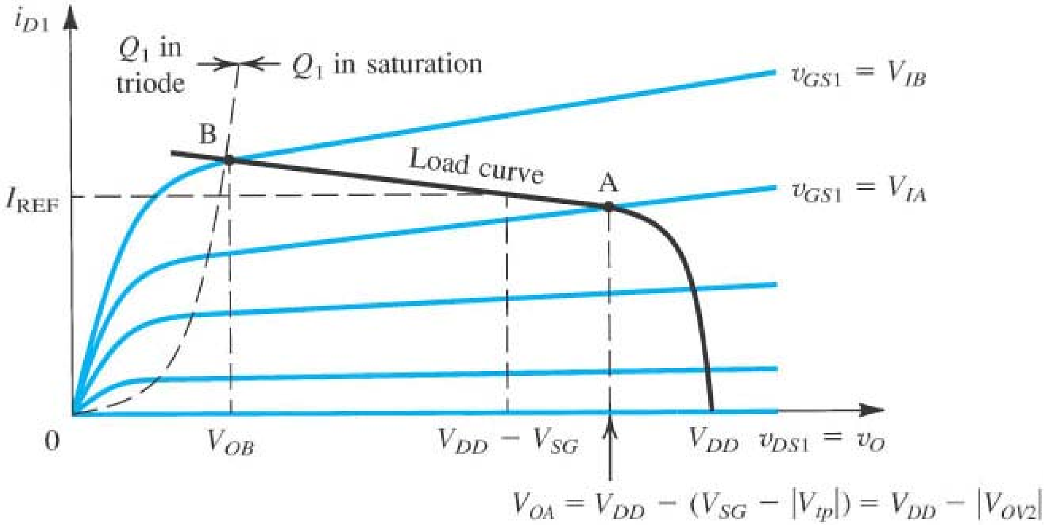
The value of V_{SG} is set by passing the reference bias current I_{REF} through Q_3.

When $v = v_{SD}$ exceeds $\left(V_{SG} - \left|V_{tp}\right|\right)$, Q_2 operates in satuaration.

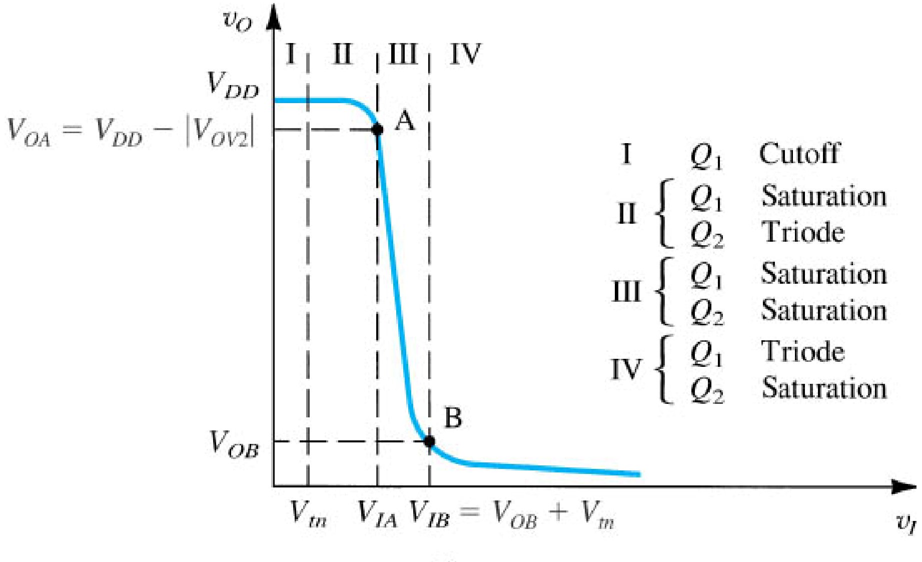
When Q_2 operates in satuaration, Q_2 behaves as a current source.

When Q_2 is in satuaration, it exhibits a finite incremental resistance : $r_{o2} = \dfrac{\left|V_{A2}\right|}{I_{REF}}$

CS Amplifier

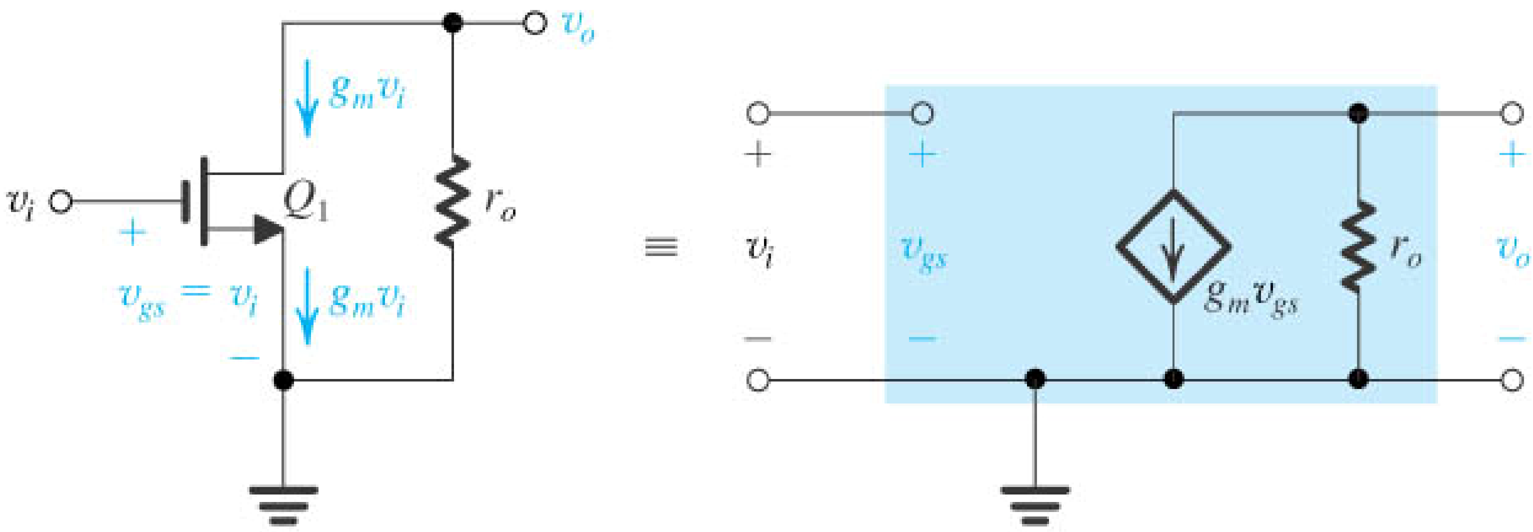


When the amplifier is biased at a point in region III, small signal voltage gain can be determined by replacing Q_1 with its small signal model and Q_2 with its output resistance r_{o2}.

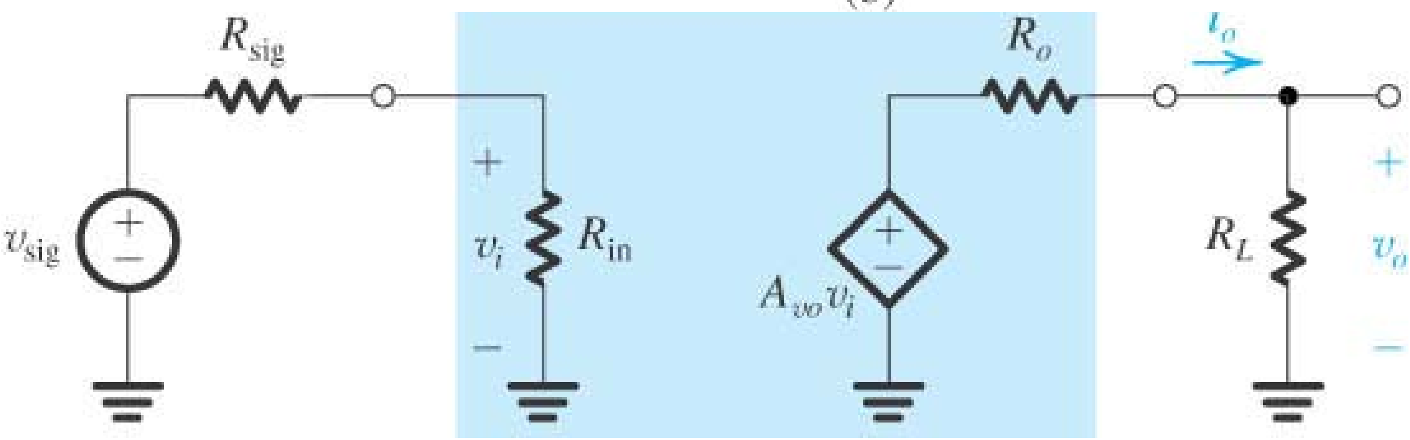


(d)

CS Amplifier



(b)



$$A_{vo} = -g_m r_o$$

$$R_o = \left.\frac{v_x}{i_x}\right|_{vi=0} = r_o$$

CS Amplifier

$A_v \equiv \dfrac{v_o}{v_i} = A_{vo}\dfrac{R_L}{R_L + R_O}$, and in this case $A_{vo} = -\left(g_{m1} r_{o1}\right)$, $R_O = r_{o1}$, and $R_L = r_{o2}$.

$$A_v = -\left(g_{m1} r_{o1}\right)\frac{r_{o2}}{r_{o2} + r_{o1}} = -g_{m1}\left(r_{o1} \| r_{o2}\right)$$

Or from the other circuit, $v_o = -\left(g_{m1} v_i\right)\left(r_{o1} \| r_{o2}\right)$

CS Amplifier

CMOS common-source amplifier

(1) Voltage gain of 15 to 100

(2) Very high input resistance

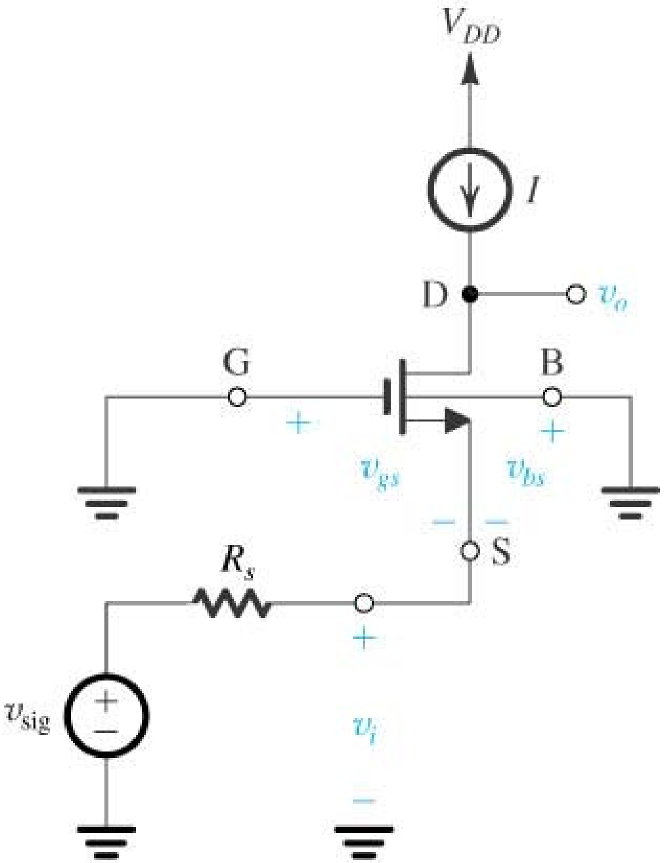
(3) Output resistance is also high.

Two final comments

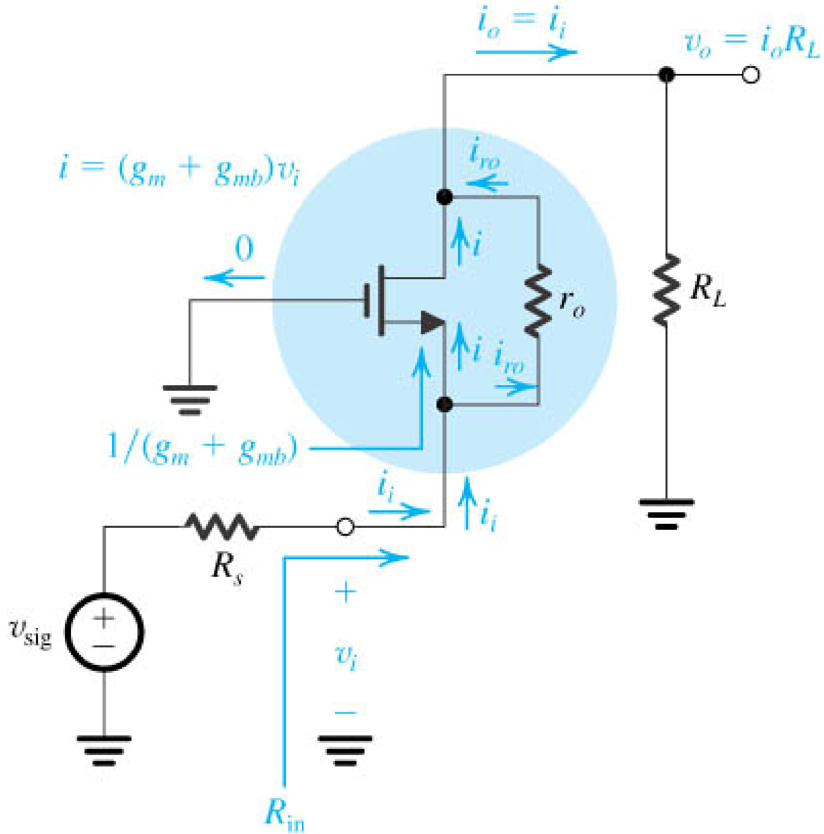
(1) The circuit is not affected by the body effect since the source terminals of both Q_1 and Q_2 are at signal ground.

(2) The circuit operates in region III, which is ensured by the negative feedback: the circuit is usually part of a larger amplifier (Chapters 7 and 9).

Common-Gate Amplifier



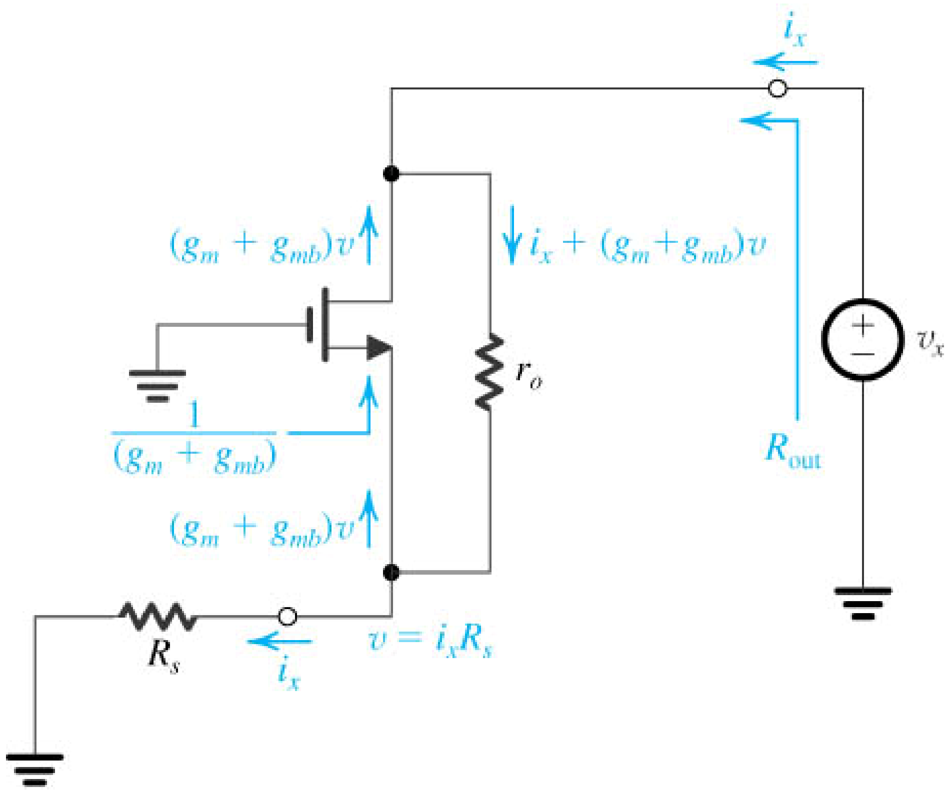
(a)



(c)

- V_b is different from V_s.
- Circuits to calculate R_{in}

Common-Gate Amplifier



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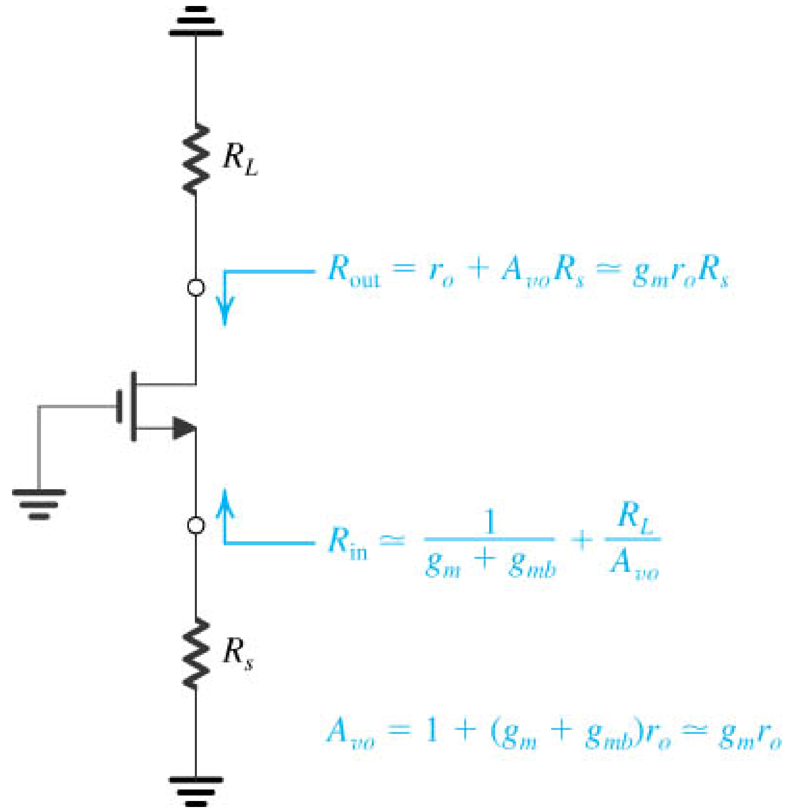
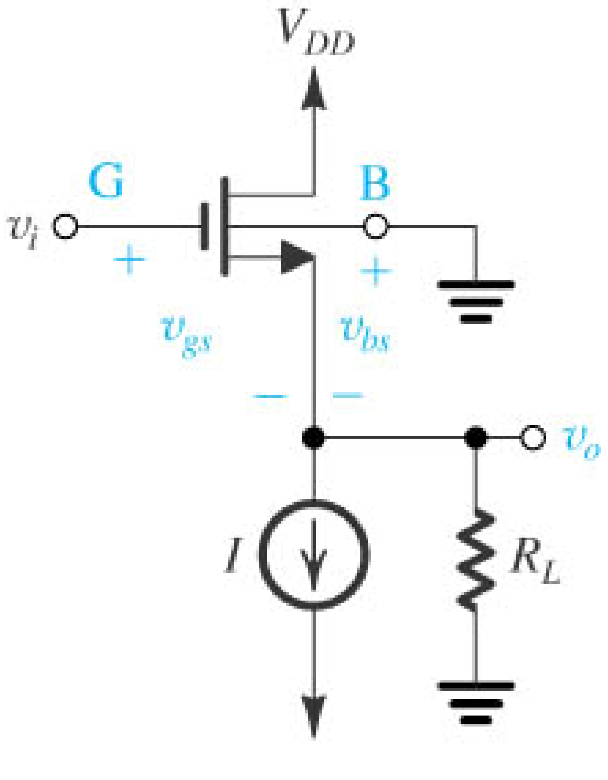
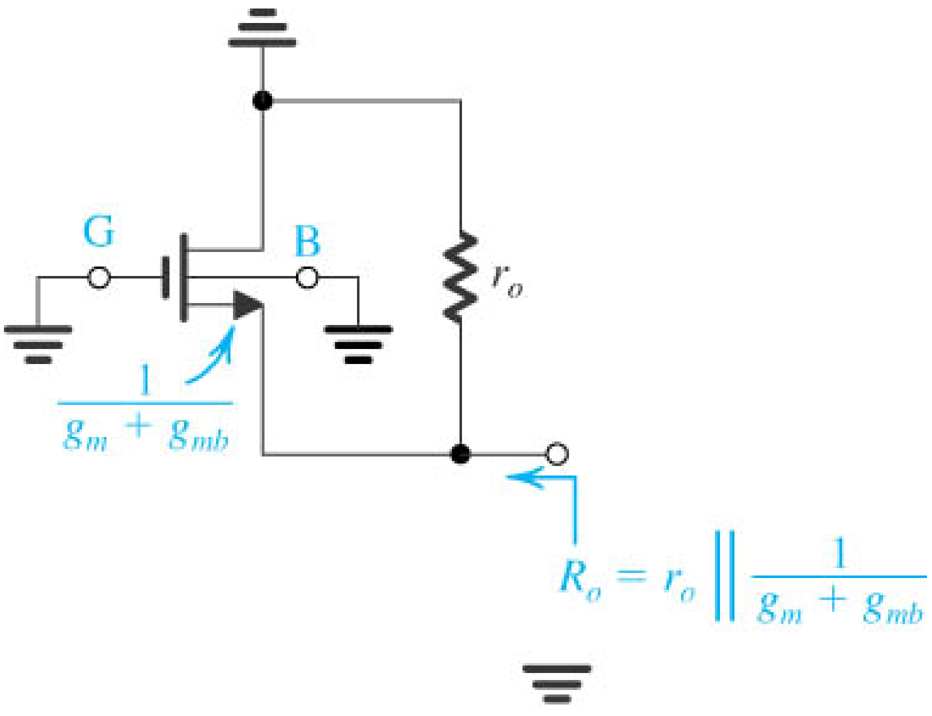


- Circuits to calculate R_{out}
- Impedance transformation

Source Follower



(a)



(d)

- No voltage gain (~1).
- Circuits to calculate R_{out}