10.3.8 Transistor Sizing

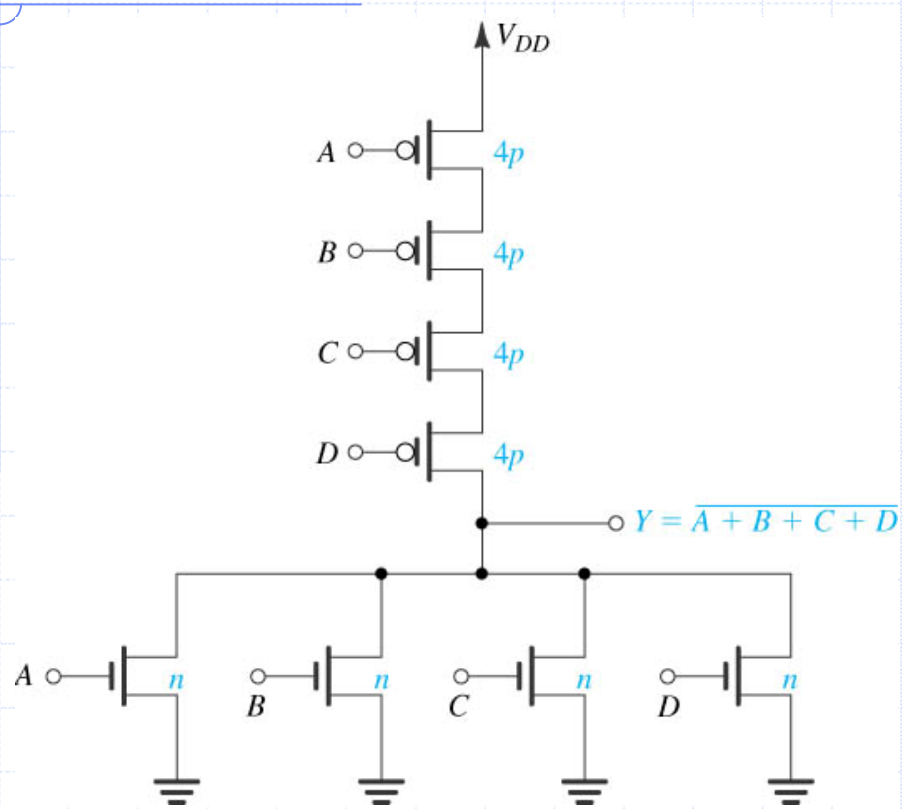


Figure 10.16 Proper transistor sizing for a four-input NOR gate.

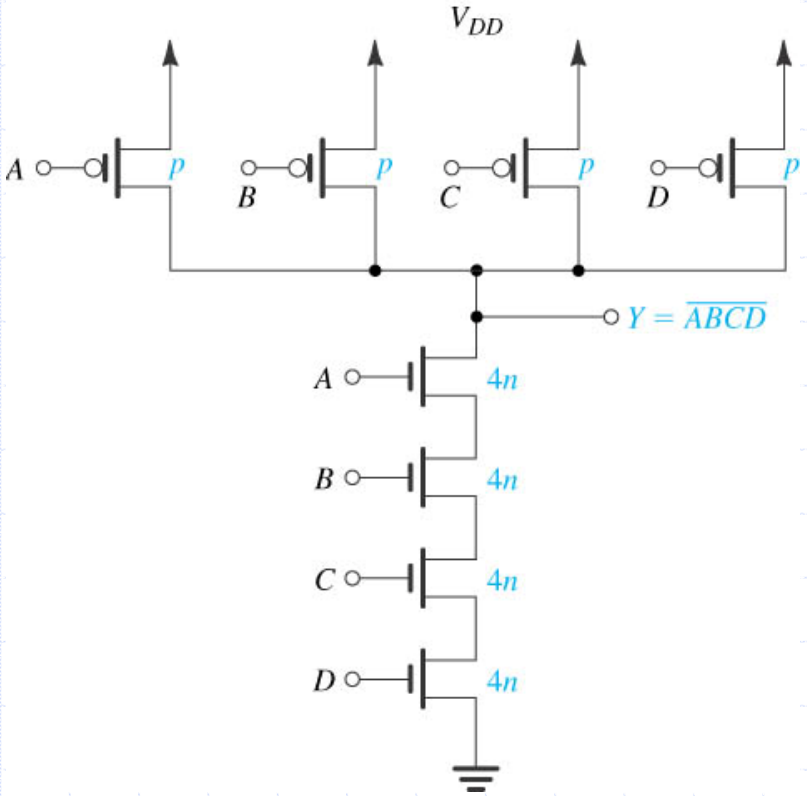
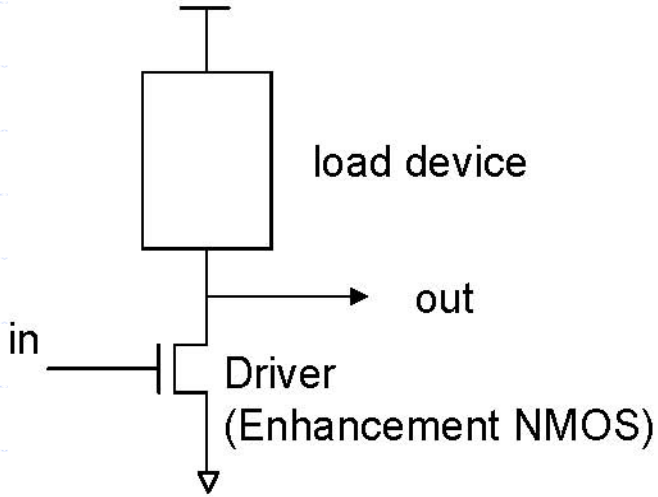


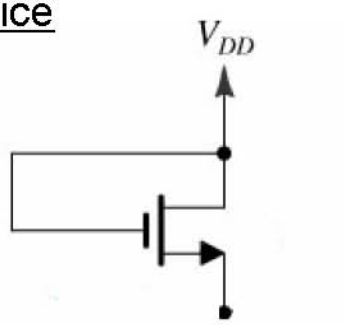
Figure 10.17 Proper transistor sizing for a four-input NAND gate.

10.4 Pseudo-NMOS Logic Circuits

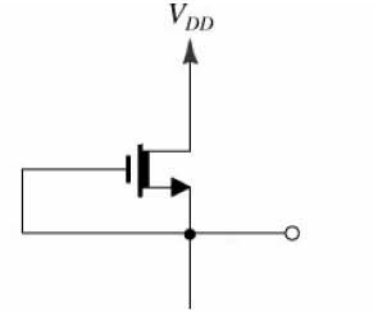
MOS inverter



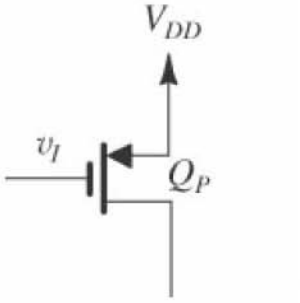
Load device



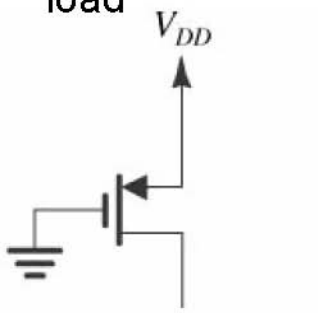
① Enhancement NMOS load



② Depletion NMOS load



③ CMOS inverter load



④ Pseudo-NMOS load

10.4.1 The Pseudo-NMOS Inverter

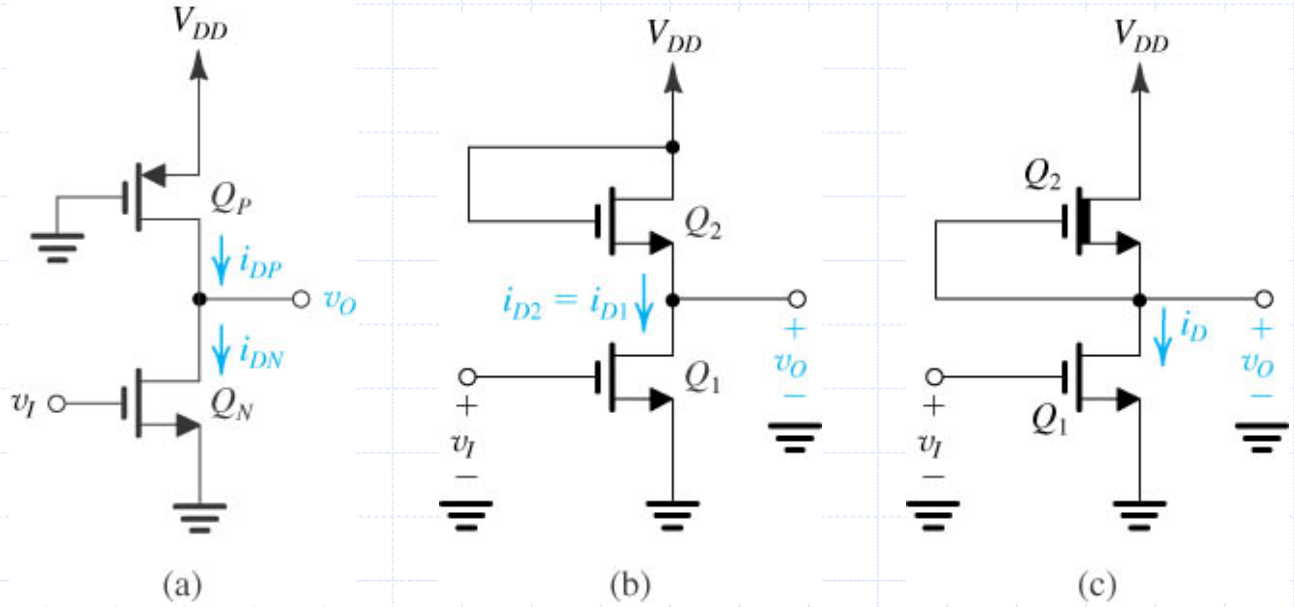


Figure 10.19 **(a)** The pseudo-NMOS logic inverter. **(b)** The enhancement-load NMOS inverter. **(c)** The depletion-load NMOS inverter.

10.4.2 Static Characteristics

Static Characteristics

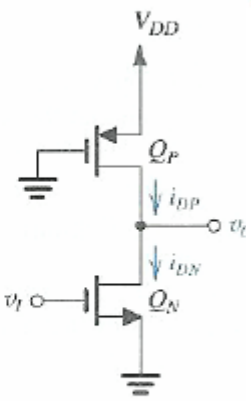
- Load curve represents a much lower saturation current.
- k_n is usually greater than k_p by a factor of 4 to 10.
- $V_{OH} = V_{DD}$
- $V_{OL} > 0$ (nonzero V_{OL} for pseudo-NMOS)

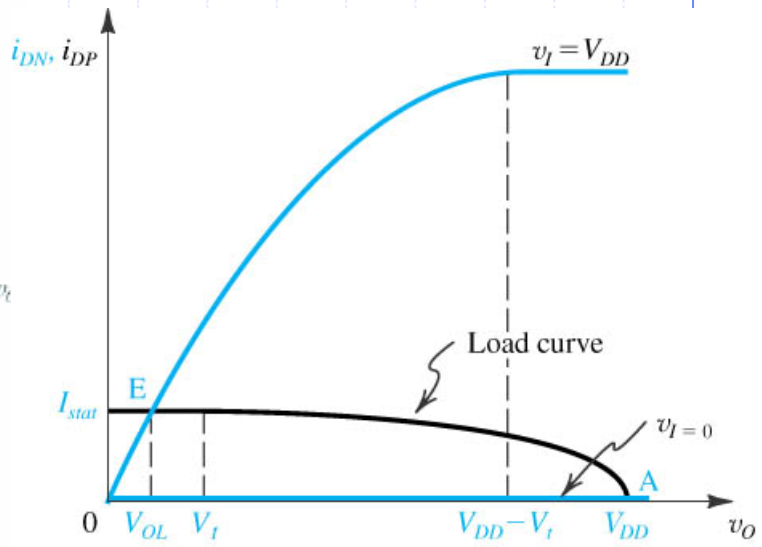
$$i_{DN} = \frac{1}{2}k_n(v_I - V_t)^2 \quad \text{for } v_O \geq v_I - V_t \quad \text{(saturation)}$$

$$i_{DN} = k_n\left[(v_I - V_t)v_O - \frac{1}{2}v_O^2\right] \quad \text{for } v_O \leq v_I - V_t \quad \text{(triode)}$$

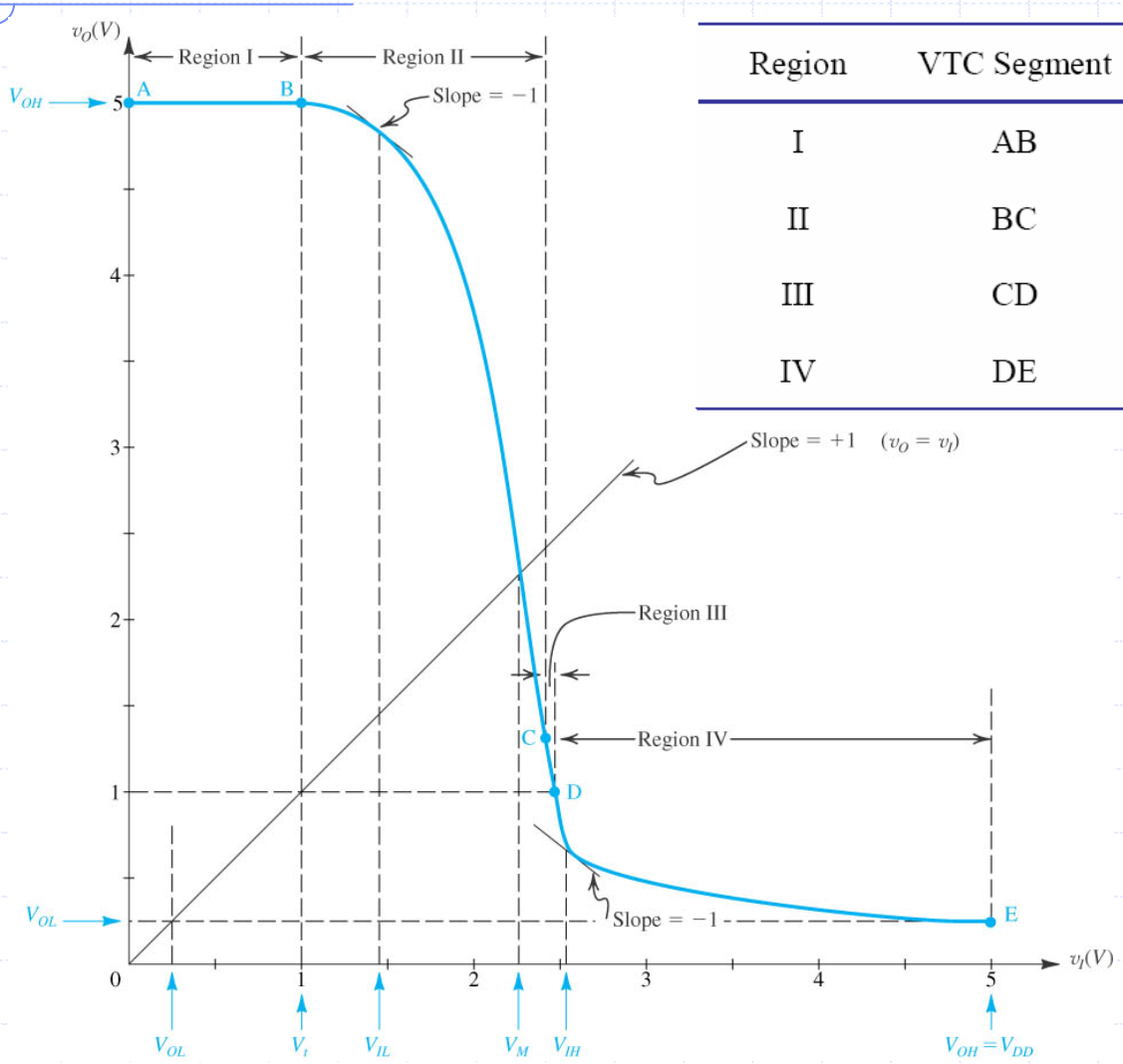
$$i_{DP} = \frac{1}{2}k_p(V_{DD} - V_t)^2 \quad \text{for } v_O \leq V_t \quad \text{(saturation)}$$

$$i_{DP} = k_p\left[(V_{DD} - V_t)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2\right] \quad \text{for } v_O \geq V_t \quad \text{(triode)}$$





10.4.3 Derivation of the VTC



Region	VTC Segment	Q_N	Q_P	Condition
I	AB	Cut-off	Triode	$v_I < V_t$
II	BC	Saturation	Triode	$v_O > v_I - V_t$
III	CD	Triode	Triode	$V_t < v_O < v_I - V_t$
IV	DE	Triode	Saturation	$v_O < V_t$

10.4.4 Dynamic Operation

$$i_{DP}(0) = \frac{1}{2} k_P' \left(\frac{W}{L}\right)_P (V_{DD} - V_t)^2$$

$$i_{DP}(t_{PLH}) = k_P' \left(\frac{W}{L}\right)_P \left[(V_{DD} - V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2 \right]$$

$$i_{DP}\big|_{av} = \frac{1}{2}\left[i_{DP}(0) + i_{DP}(t_{PLH}) \right]$$

$$t_{PLH} = \frac{C\Delta V}{i_{DP}\big|_{av}} = \frac{CV_{DD}/2}{i_{DP}\big|_{av}}$$

for $V_t \cong 0.2V_{DD}$,

$$t_{PLH} = \frac{1.7C}{k_P' \left(\frac{W}{L}\right)_P V_{DD}}$$

for a large value of r,

$$t_{PHL} \cong \frac{1.7C}{k_N' \left(\frac{W}{L}\right)_N V_{DD}}$$

10.4.6 Gate Circuits

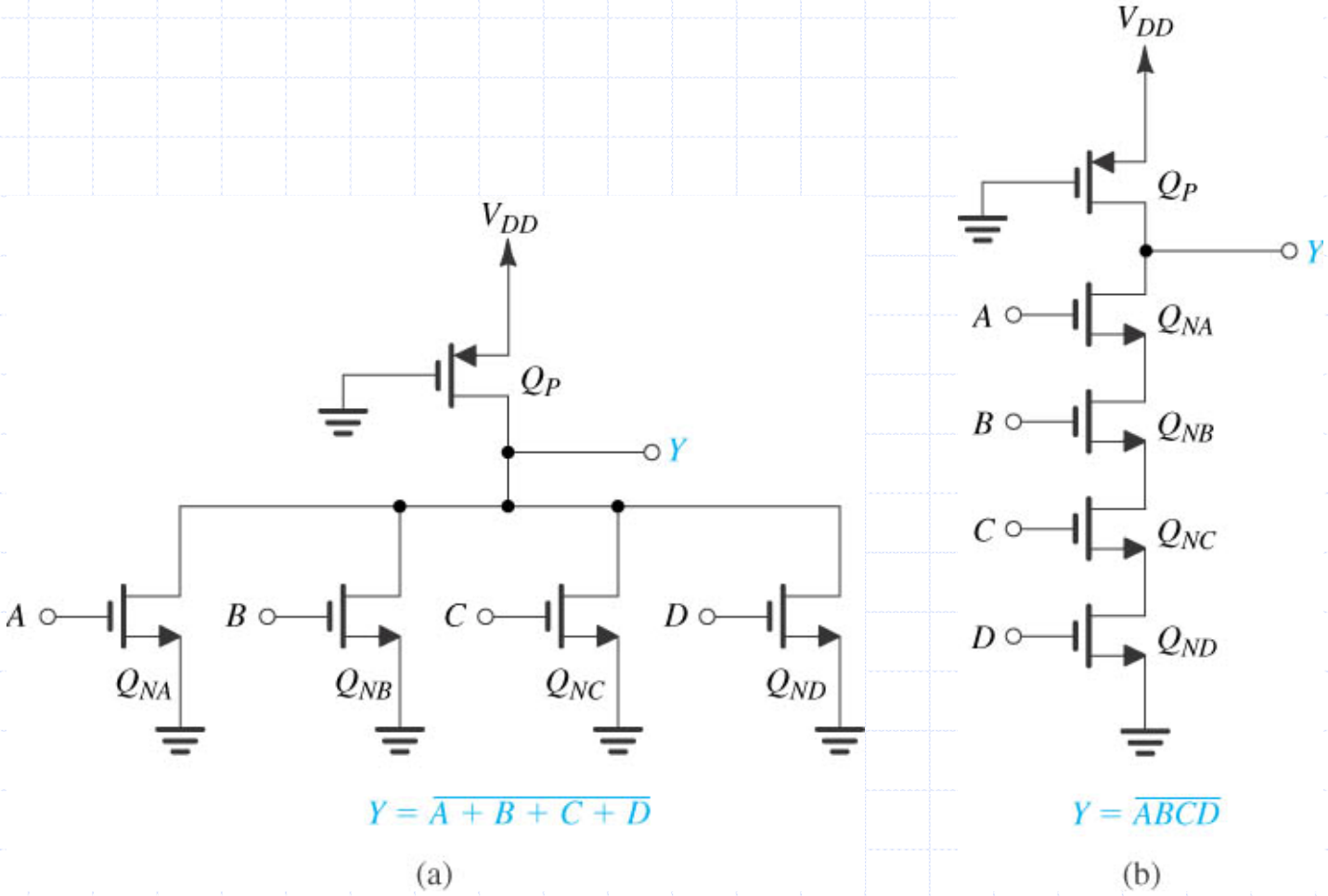
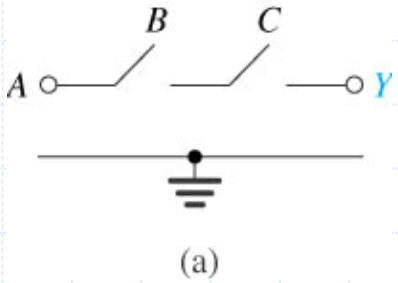


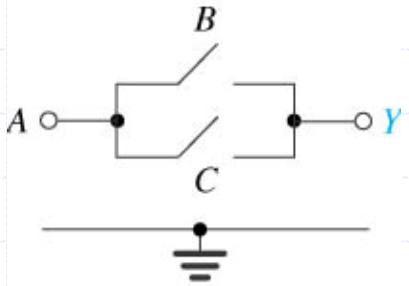
Figure 10.22 NOR and NAND gates of the pseudo-NMOS type.

10.5 Pass-Transistor Logic Circuits



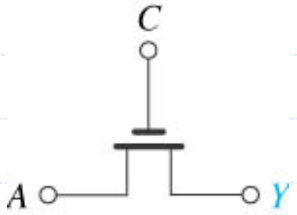
(a)

Series Y = ABC



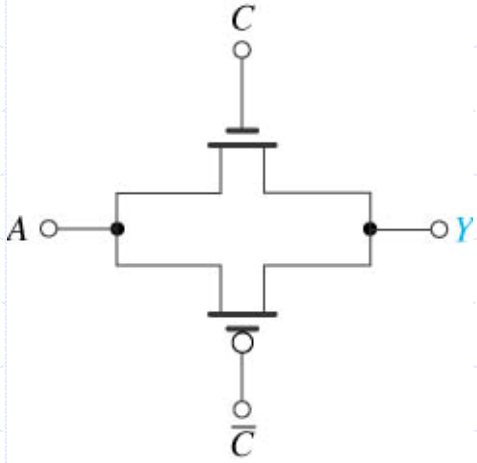
(b)

Parallel Y = A(B+C)



(a)

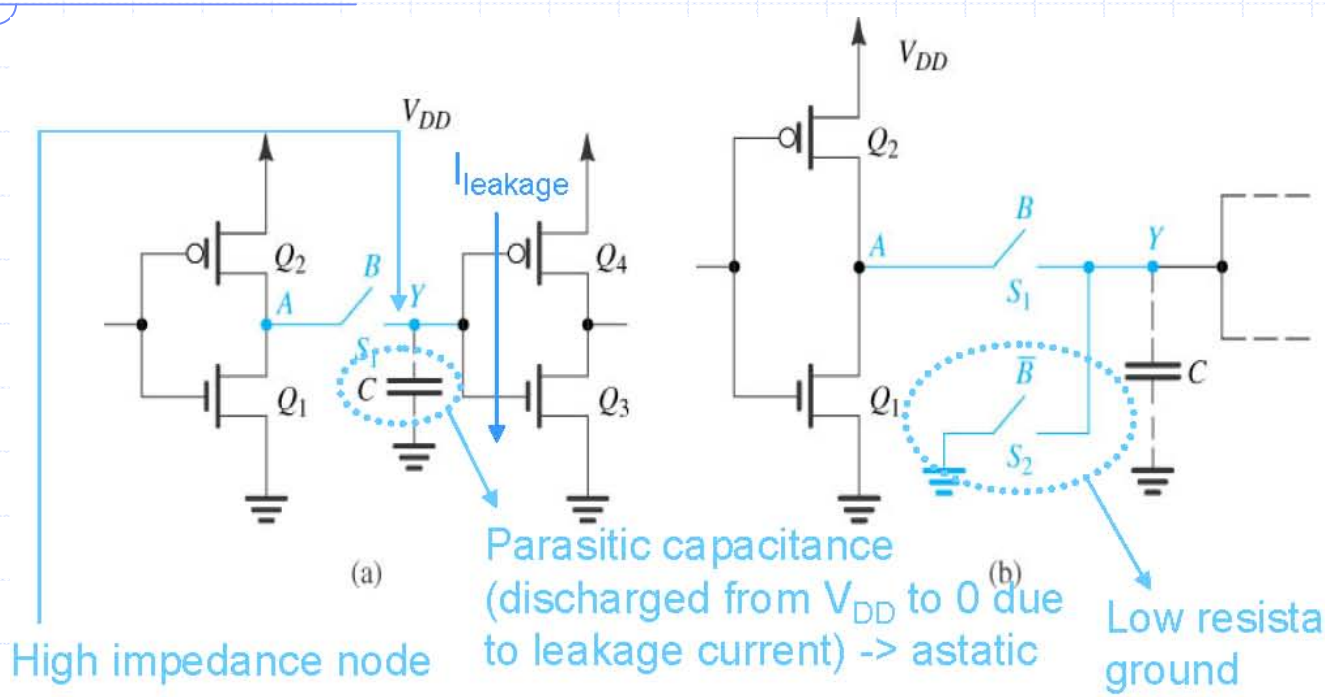
Single NMOS gate



(b)

Transmission gate

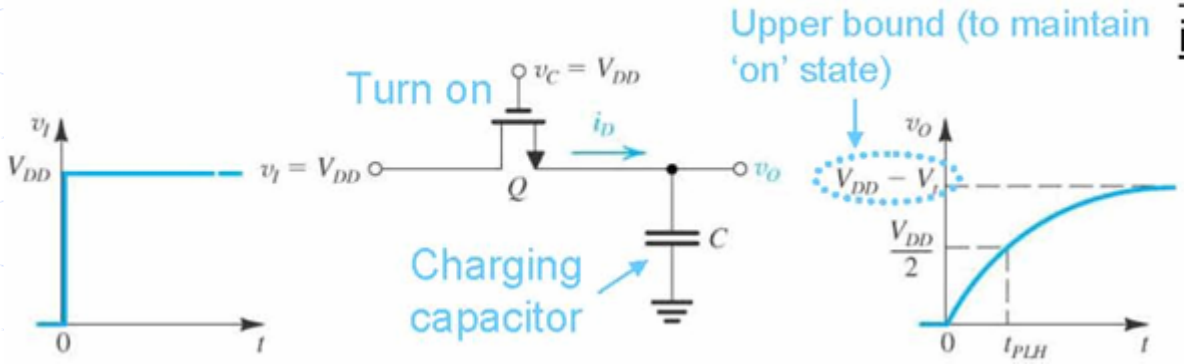
10.5.1 An Essential Design Requirement



Static circuit requirement

every circuit node has at all times a low-resistance path to V_{DD} or ground to be static.

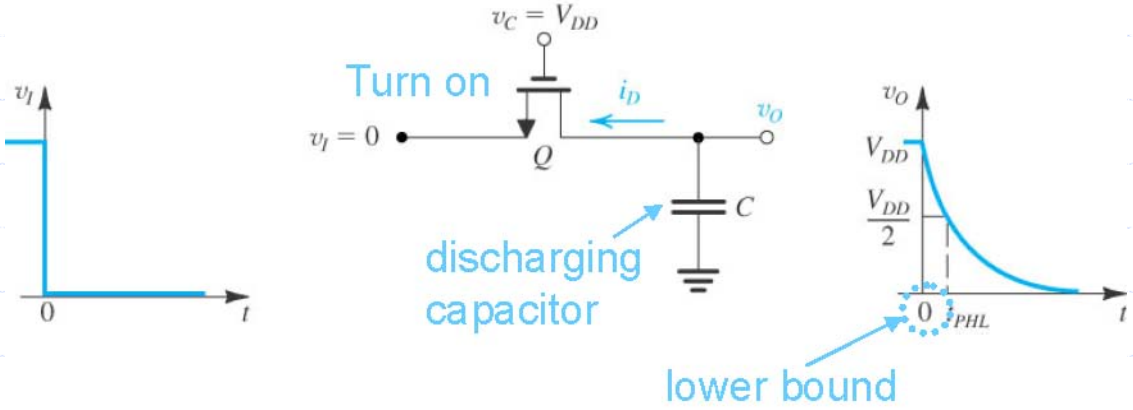
10.5.2 Operation with NMOS Transistors as Switches



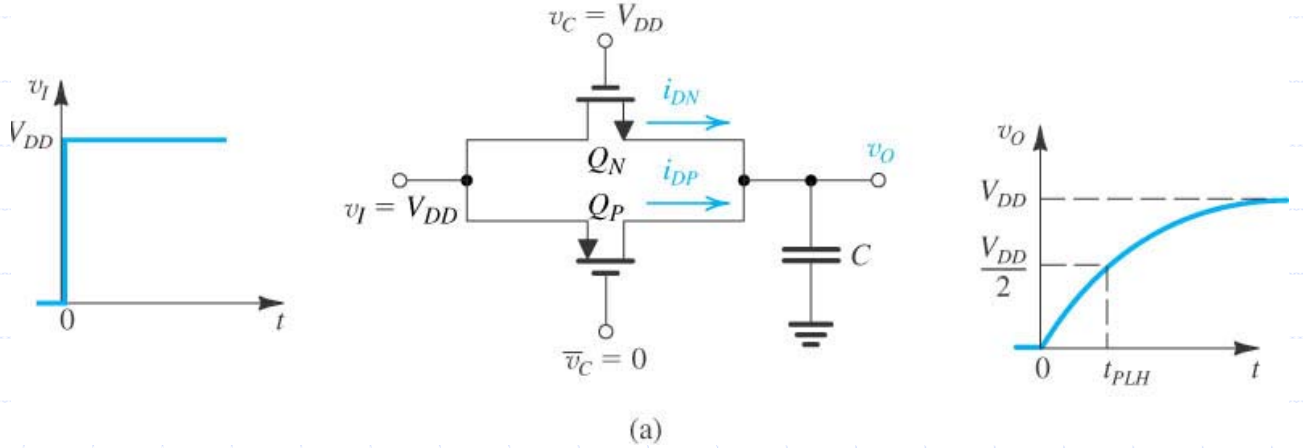
Single NMOS transistor when input is high

$$i_D = \frac{1}{2} k_n (V_{DD} - v_o - V_t)^2$$

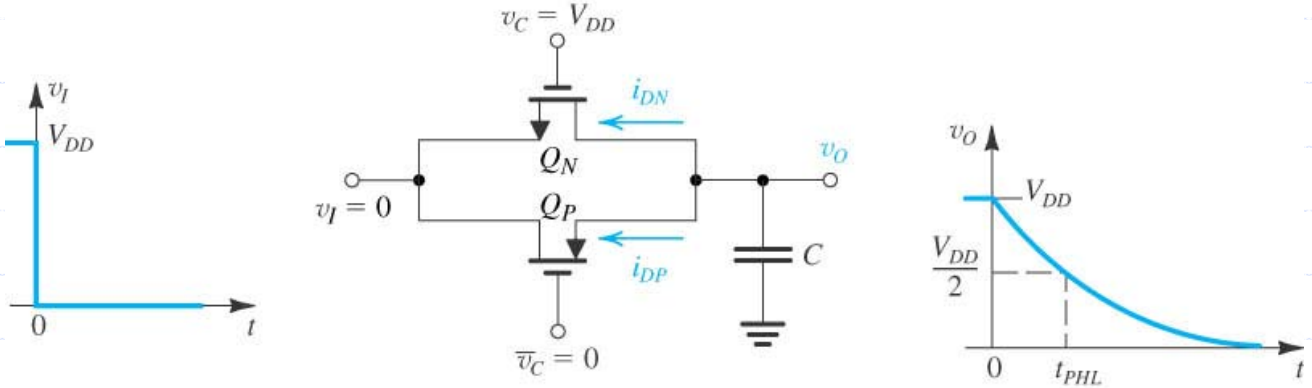
$$V_t = V_{t0} + \gamma(\sqrt{v_o + 2\phi_f} - 2\sqrt{2\phi_f})$$



10.5.3 The Use of CMOS Transmission Gates as Switches

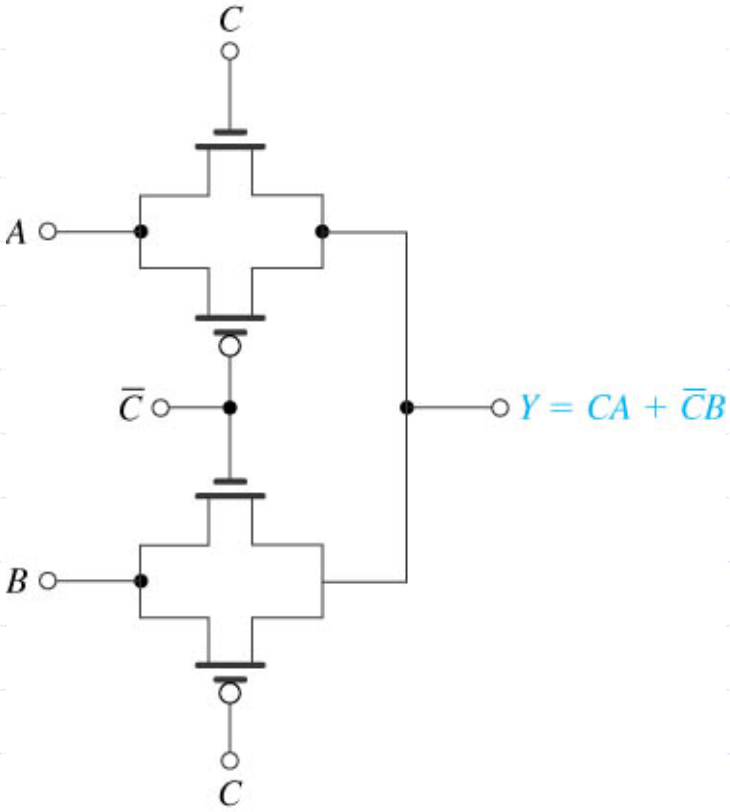


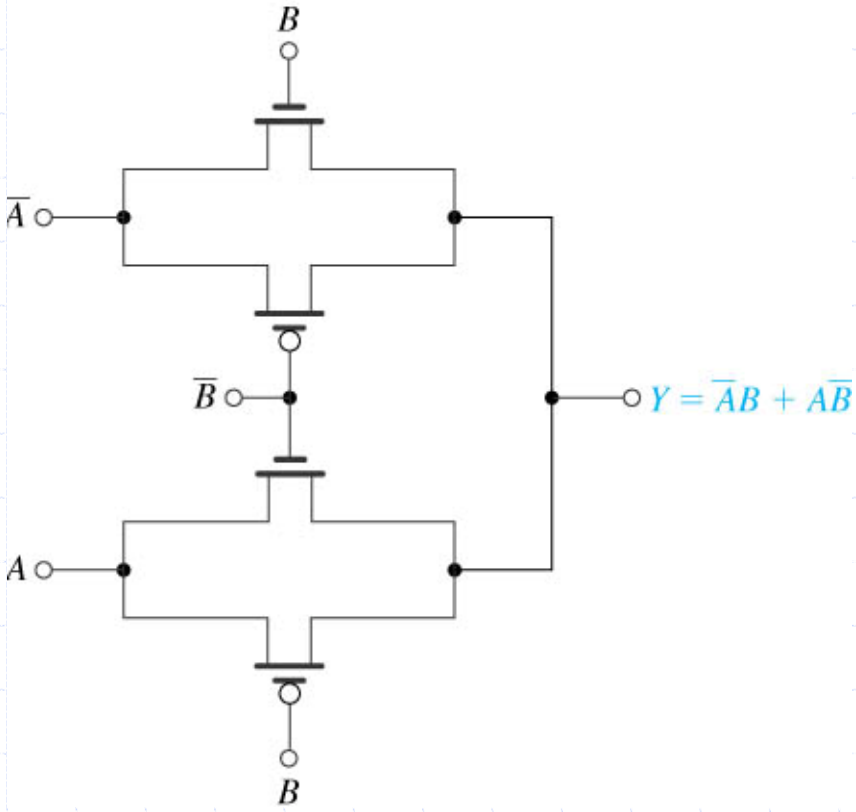
(a)



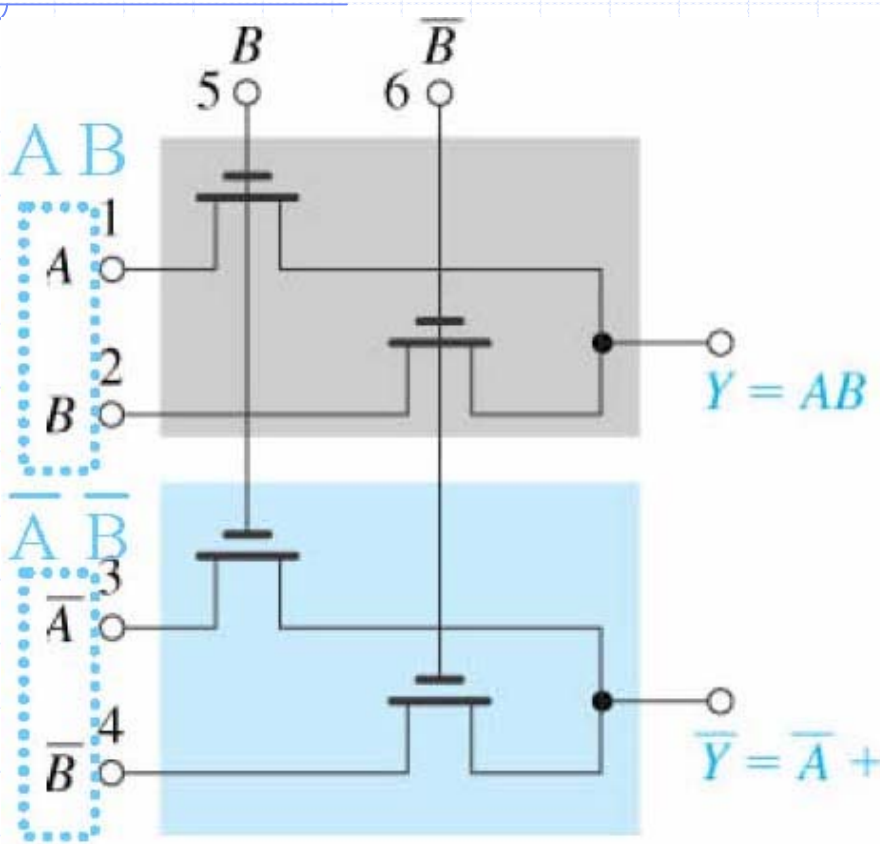
(b)

10.5.4 Pass-Transistor Logic Circuit Examples





10.5.4 Pass-Transistor Logic Circuit Examples



$$Y = AB + B\overline{B} = AB$$

$$Y = \overline{A}B + \overline{B}\overline{B} = \overline{A}B + \overline{B}$$

$$= \overline{A}B + (1 - B) = 1 - B(1 - \overline{A})$$

$$= 1 - AB = \overline{AB}$$

10.6 Dynamic Logic

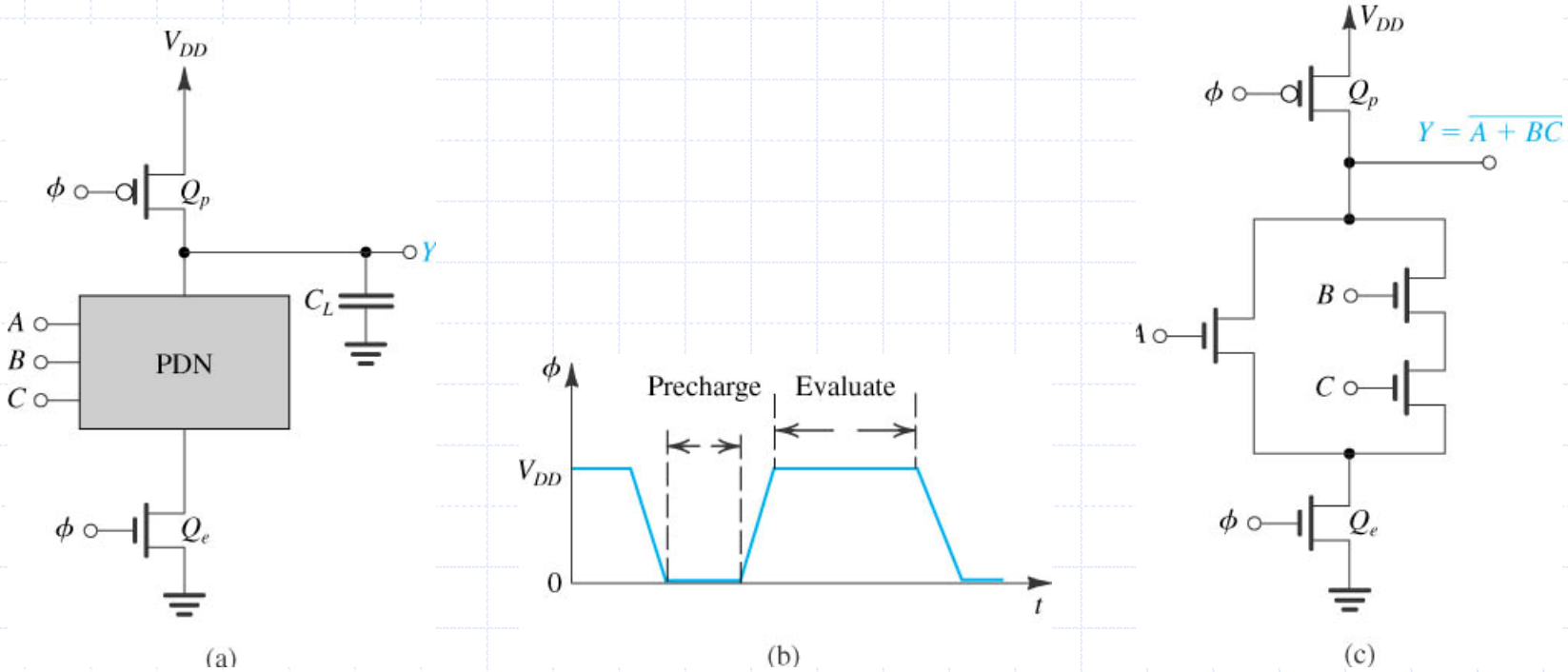


Figure 10.33 **(a)** Basic structure of dynamic-MOS logic circuits. **(b)** Waveform of the clock needed to operate the dynamic logic circuit. **(c)** An example circuit.

10.6.2 Non-ideal Effects

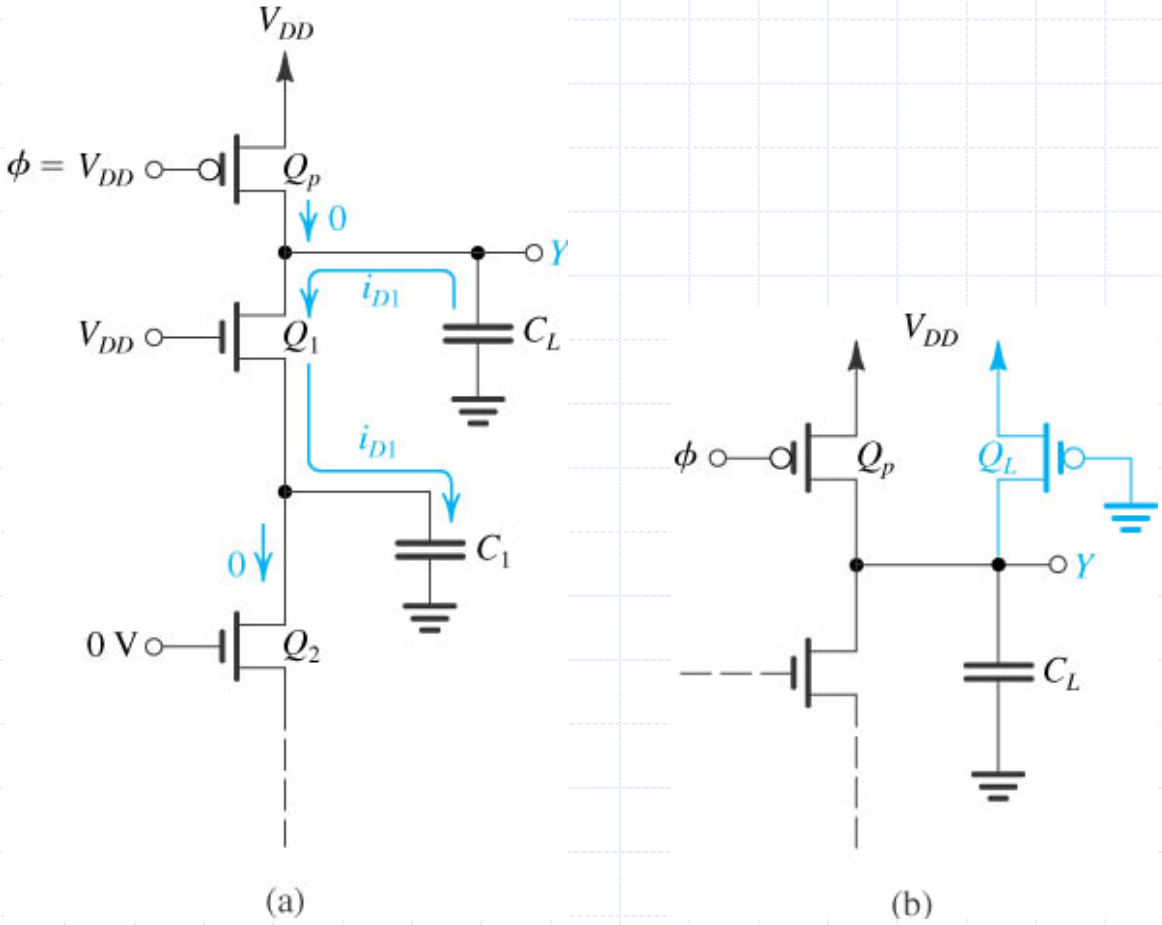


Figure 10.34 **(a)** Charge sharing. **(b)** Adding a permanently turned-on transistor Q_L solves the charge-sharing problem at the expense of static power dissipation.

10.6.2 Non-ideal Effects

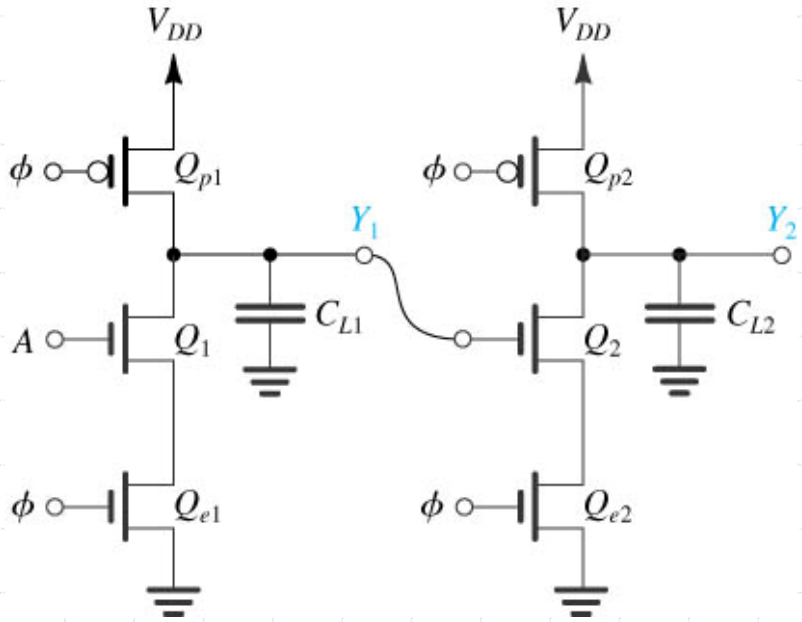
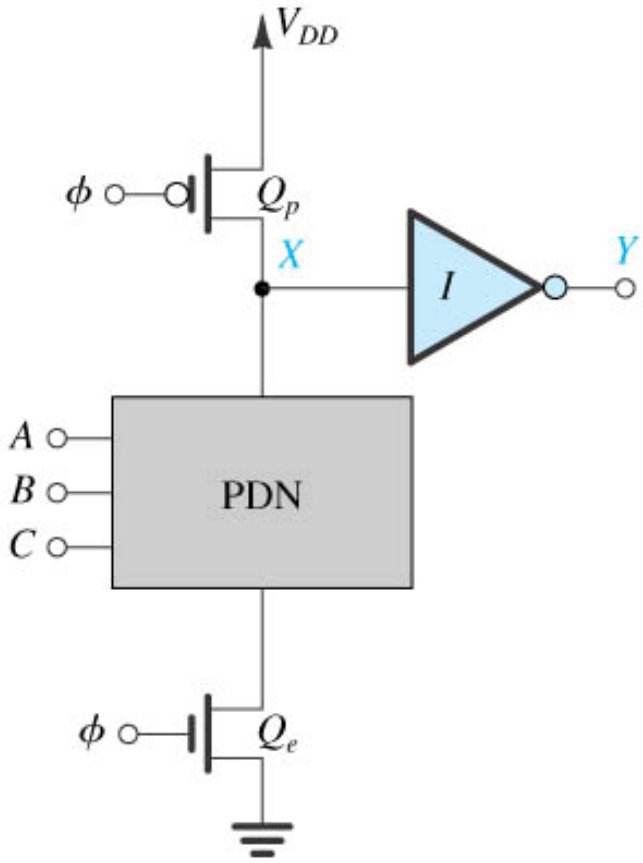


Figure 10.35 Two single-input dynamic logic gates connected in cascade. With the input A high, during the evaluation phase C_{L2} will pa rtially discharge and the output at Y_2 will fall lower than V_{DD}, which can cause logic malfunction.

10.6.3 Domino CMOS Logic



- **Domino logic**
  - N-type dynamic logic + inverter
  - Cascadable gates
  - During the precharge,
    X -> VDD, Y -> ‘0’
  - During the evaluation,
    Y -> VDD or Y -> ‘0’

10.6.3 Domino CMOS Logic

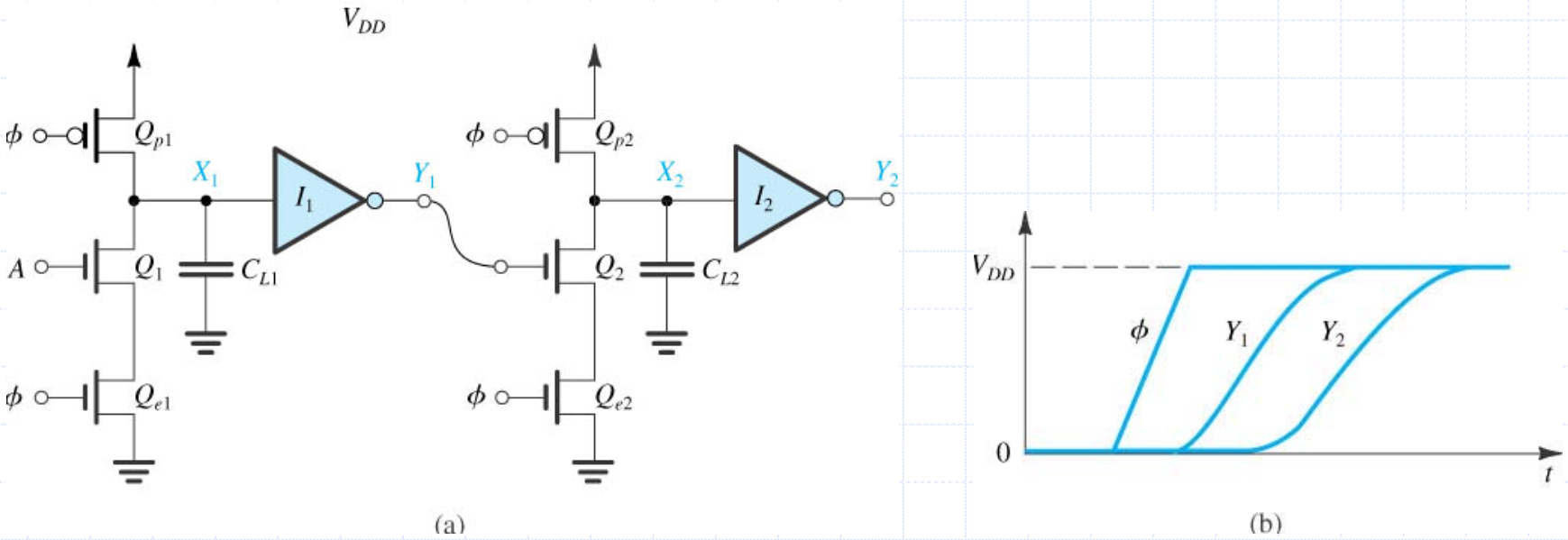


Figure 10.37 **(a)** Two single-input domino CMOS logic gates connected in cascade. **(b)** Waveforms during the evaluation phase.