2007 Fall: Electronic Circuits 2

CHAPTER 11

Memory and Advanced Digital Circuits

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Introduction

- **Combinational circuits :** depends on the present values of the input

- **Sequential circuits** : memory included.

  → output depends not only on the present inputs but also on the previous inputs.

  → timing generator (clock) required.

- **Two approaches for providing memory**

  - Static : positive feedback (bistable circuit)

  - Dynamic : charge on a capacitor → need refresh
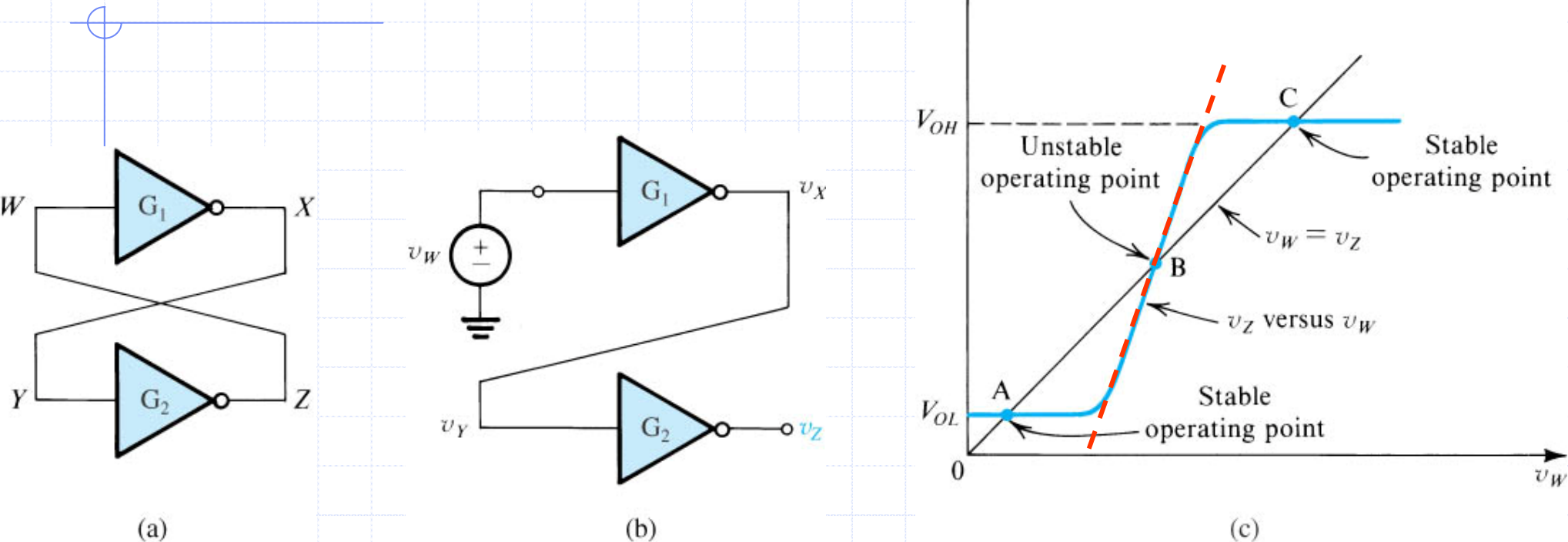
11.1.1 The Latch

Figure 11.1 **(a)** Basic latch. **(b)** The latch with the feedback loop opened. **(c)** Determining the operating point(s) of the latch.

◆ Latch can store one bit of information
  - v_X is high & v_Z is low = 1

◆ two stable operating points A & C. → regenerative (loop gain > 1)

◆ unstable operating point B

11.1.2 The SR Flip-Flop

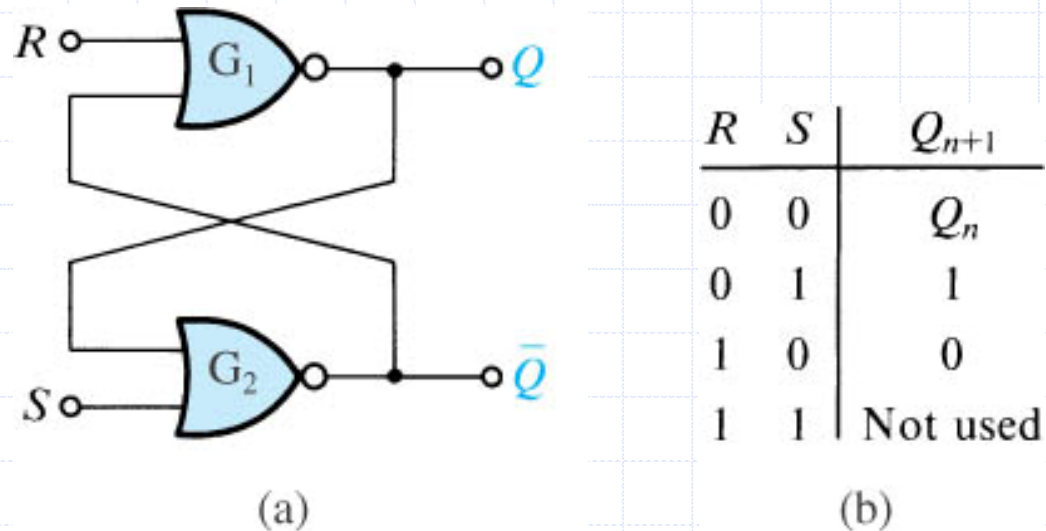Figure 11.2 **(a)** The set/reset (SR) flip-flop and **(b)** its truth table.

- Flip-flop = latch + triggering circuit
- S=R=0 → memory (or rest) state → retains the value
- S=1, R=0 → $\overline{Q}$=0, Q=1 (set) → retained after S returns to 0
- S=1, R=1 → $\overline{Q}$=0, Q=0 → undefined, but depends on which one returns to zero first.

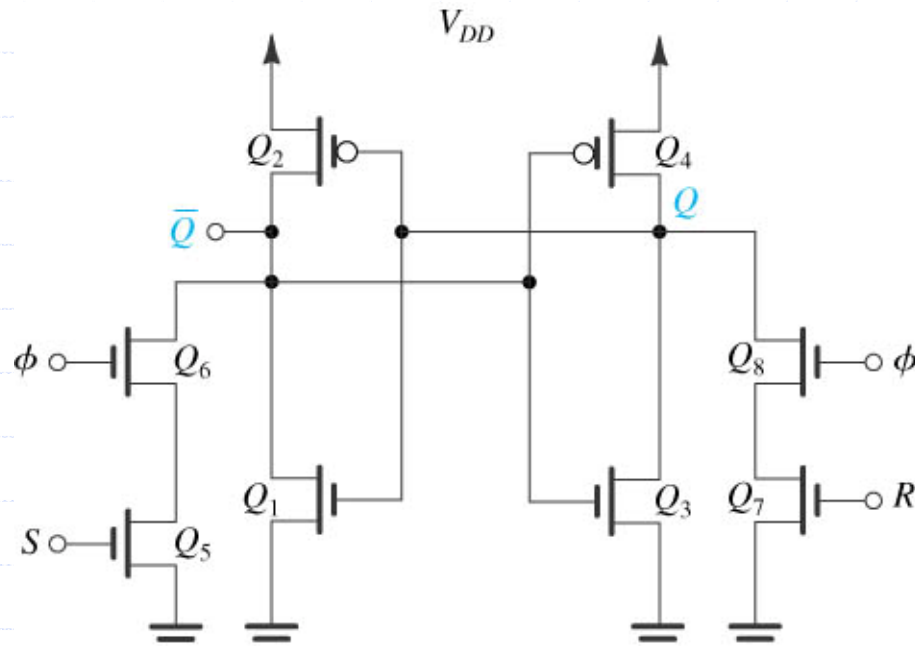# 11.1.3 CMOS Implementation of SR Filp-Flops

Figure 11.3 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

- Clock signal(Φ) is high $\rightarrow$ set or reset action performed.
- S=1 $\rightarrow \overline{Q} \downarrow \rightarrow V_{Q3} \downarrow \rightarrow Q \uparrow \rightarrow V_{Q1} \uparrow \rightarrow \overline{Q} \downarrow$ (regenerative)

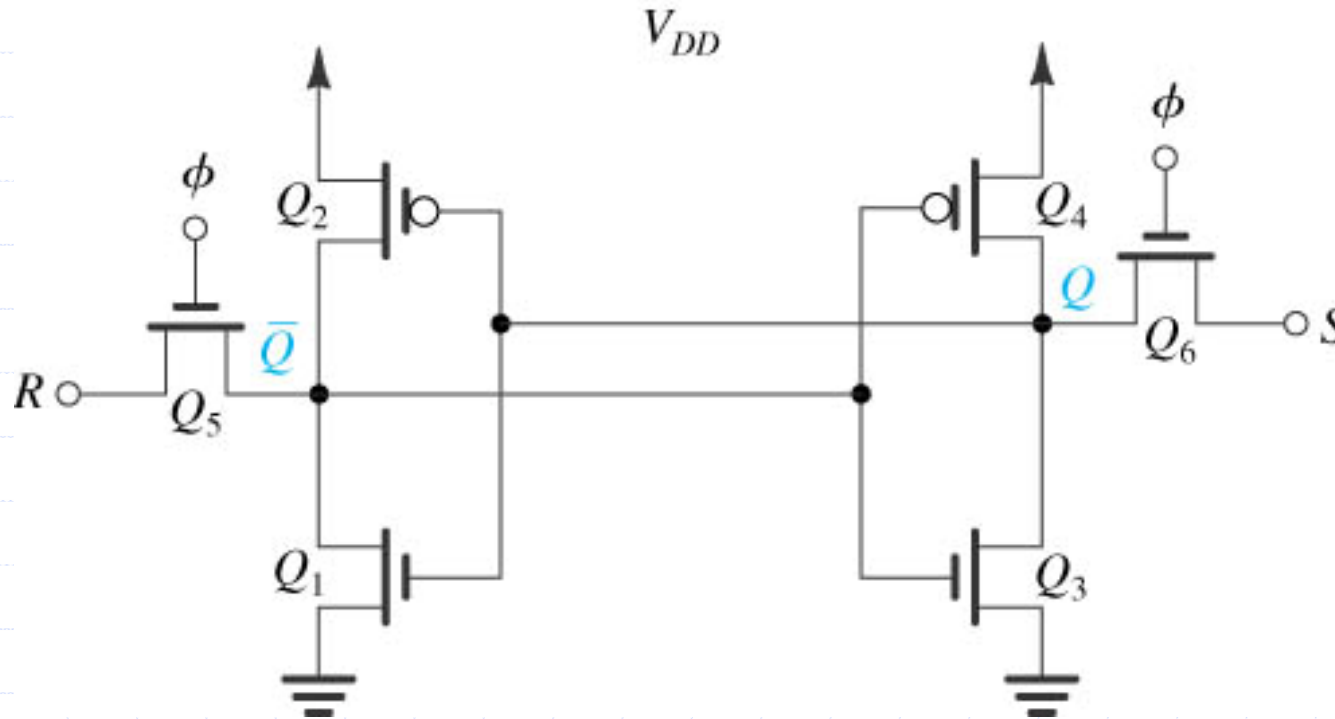# 11.1.4 A Simpler CMOS Implementation of the Clocked SR Flip-Flop

Figure 11.5 A simpler CMOS implementation of the clocked SR flip-flop.

- Pass-transistor logic is employed
- Very popular in the design of static random-access memory (SRAM)
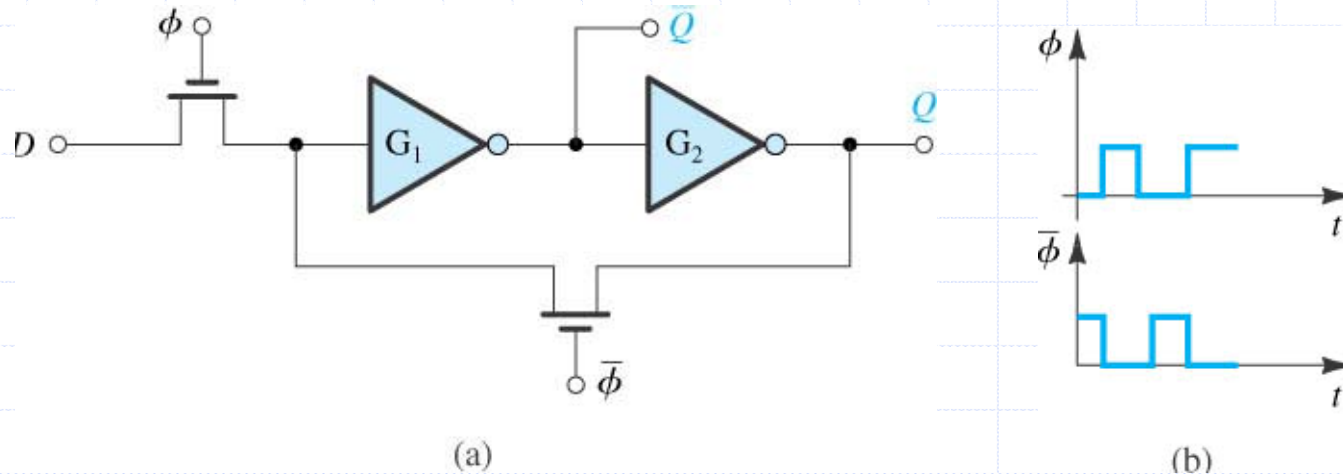
11.1.5 D Flip-Flop Circuits

Figure 11.7 A simple implementation of the D flip-flop.

◆ Simple implementation of the D flip-flop:

- $\Phi = 1$ and $\overline{\Phi} = 0$: the loop is open and Q is determined by D.
- $\Phi = 0$ and $\overline{\Phi} = 1$: the loop is closed and the flip-flop is in latch mode. →latch stores the value of D right before the clock went down.
- two-phase non-overlapping clock is required for D flip-flop operation.
- Major drawback: the output simply follows the signal on the D input line during Φ.
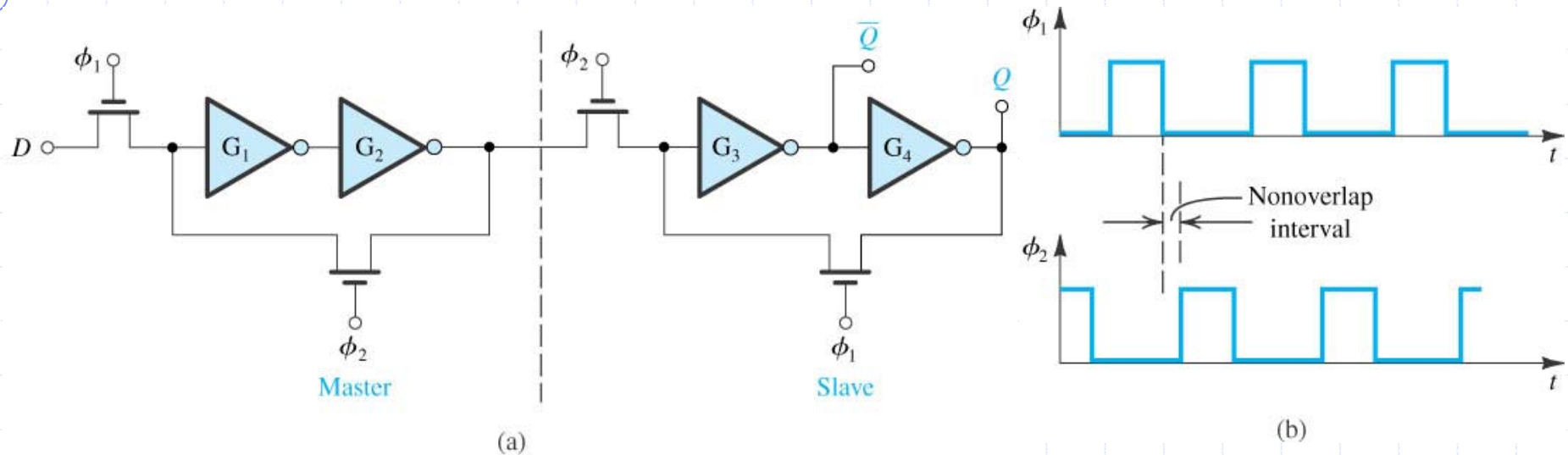
11.1.5 D Flip-Flop Circuits (cont.)

Figure 11.8 (a) A master–slave D flip-flop. The switches can be, and usually are, implemented with CMOS transmission gates. **(b)** Waveforms of the two-phase nonoverlapping clock required.

◆ Two clock phases, Φ_1&Φ_2, must be nonoverlapping.

◆ Positive transition of clock Φ_2 the output Q adopts the value of D.

◆ During the nonoverlap interval, feedback loops open

→ capacitances maintain most of their charge.

◆ Nonoverlap interval should be kept reasonably short(one-tenth or less of the clock period, and of the order of 1ns or so in current practice)
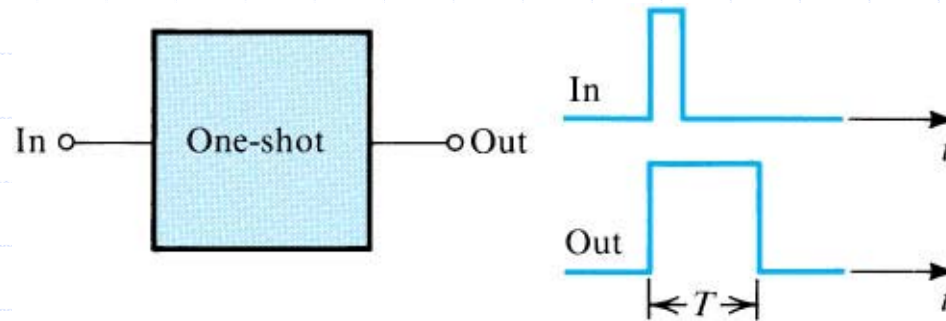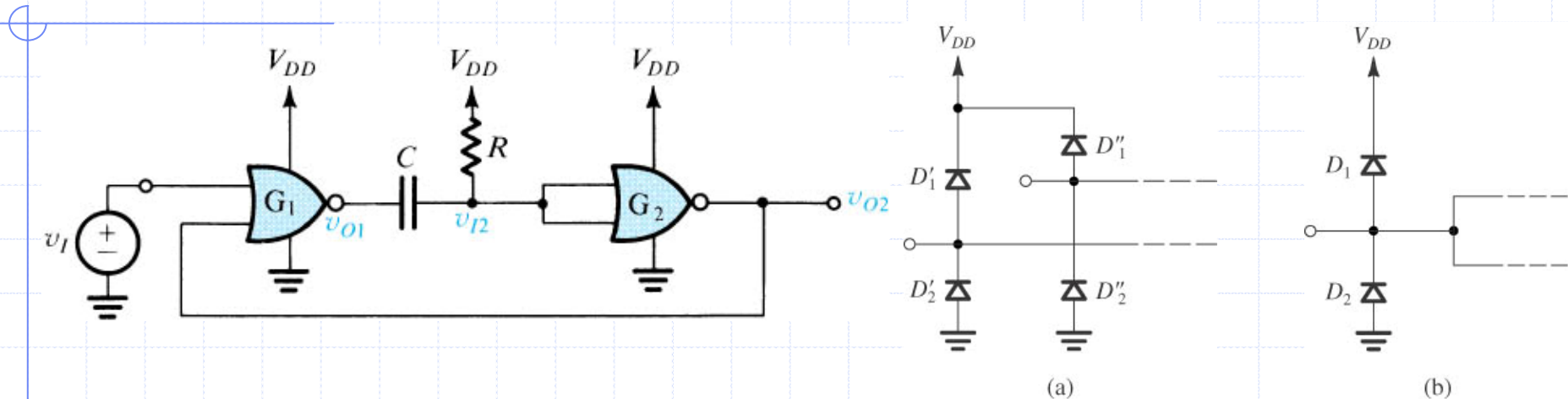
11.2 MULTIVIBRATOR CIRCUITS

Figure 11.9 The monostable multivibrator (one-shot) as a functional block, shown to be triggered by a positive pulse. In addition, there are one shots that are triggered by a negative pulse.

◆ Bistable multivibrator (two stable states, e.g. flip-flop).

◆ Monostable multivibrator (one stable state + quasi-stable state, e.g. pulse stretcher or pulse standardizer).

◆ Astable multivibrator (no stable states + two quasi-stable states, e.g. periodic pulse generator).

11.2.1 A CMOS Monostable Circuit

(a)   (b)

◆ Commercially available CMOS gates have a special arrangement of diodes connected at their input terminals

◆ Prevent the input voltage signal from rising above the supply voltage V_{DD} and from falling below ground voltage.

◆ Effect on the operation of the inverter-connected gate G_2.

 ▪ The diodes provide a low-resistance path to the power supply for voltages exceeding the power supply limits, the input current for intermediate voltages is essentially zero.
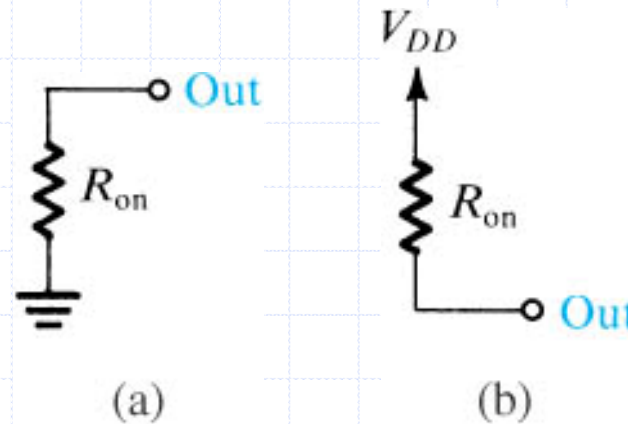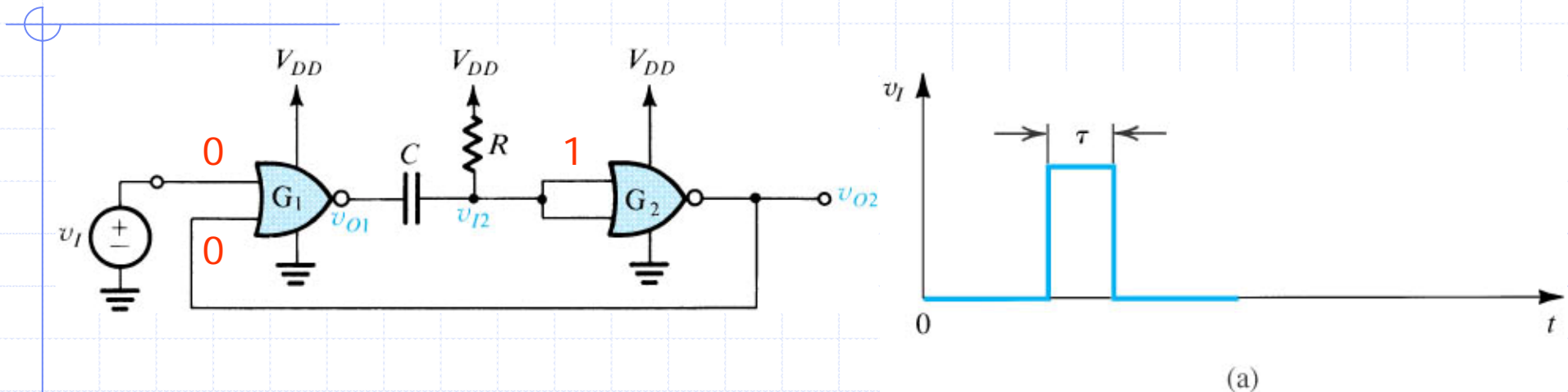
11.2.1 A CMOS Monostable Circuit (cont.)

Figure 11.12 Output equivalent circuit of CMOS gate when the output is **(a)** low and **(b)** high.

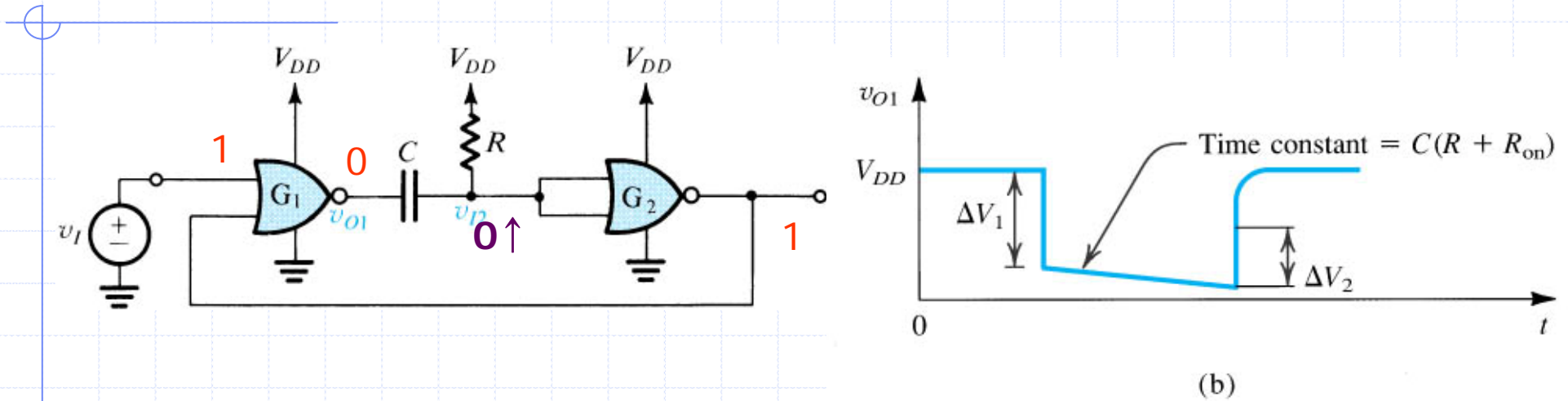◆ Approximate output equivalent circuits of the gate.

- Fig.11.12(a) : when the gate output is low. In this state, current can flow from the external circuit into the output terminal of the gate; the gate is said to be sinking current.
- Fig.11.12(b) : when the gate output is high. In this state, current can flow from V^{DD} through the output terminal of the gate into the external circuit; the gate is said to be sourcing current.
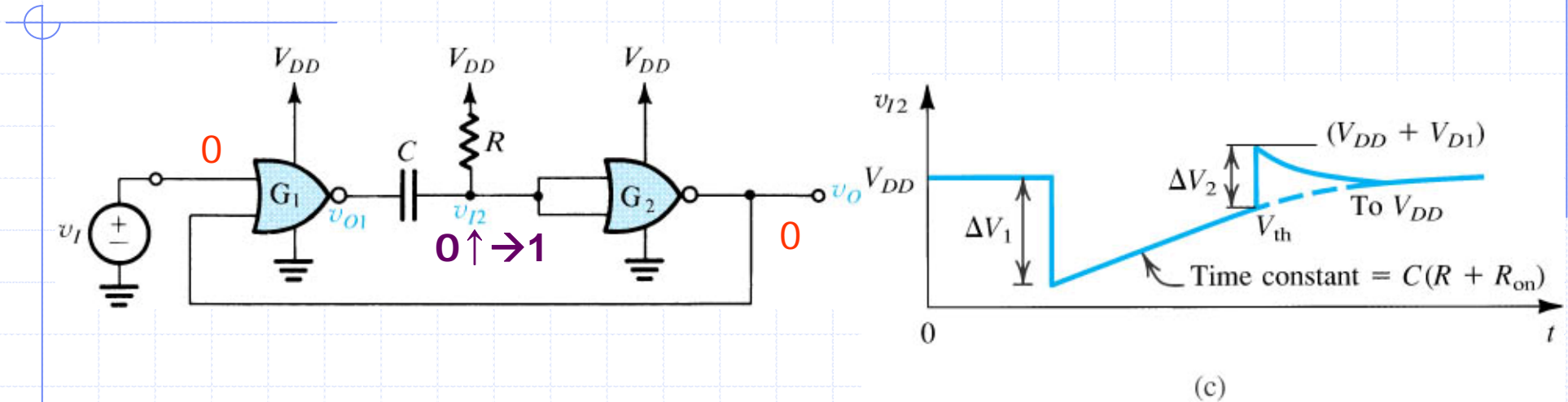
11.2.1 A CMOS Monostable Circuit (cont.)

(a)

1. Stable state of the monostable circuit (the state of the circuit before the trigger pulse is applied): The output of G_1 is high at V_{DD}, the capacitor is discharged, and the input voltage to G_2 is high at V_{DD}.

   ▪ The output of G_2 is low, at ground voltage.

   ▪ Low voltage is fed back to G_1; since v_I also is low, the output of G_1 is high, as initially assumed.

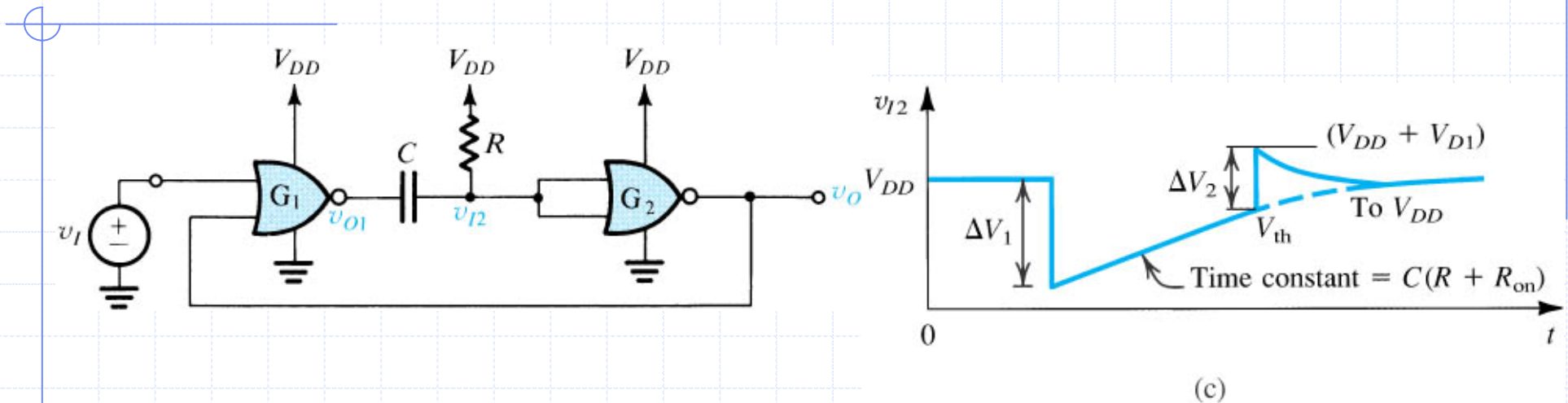# 11.2.1 A CMOS Monostable Circuit (cont.)

(b)

2. **Trigger pulse is applied:** The output of G_1 will go low (but its output will not go all the way to 0V). The output of G_1 drops by a value ΔV_1.

   - $G_2 \rightarrow$ the drop of voltage at its input causes its output to go high (to V_{DD}).
   - Keeps the output of G_1 low even after the triggering pulse has disappeared.
   - The Circuit is now in the quasi-stable state.

11.2.1 A CMOS Monostable Circuit (cont.)

(c)

3. Operation in the quasi-stable state : The current through R, C, and R_{on} causes C to charge, and the voltage V_{I2} rises exponentially toward V_{DD} with a time constant $C(R + R_{on})$.

- V_{I2} continue to rise until it reaches V_{th} of inverter G_2
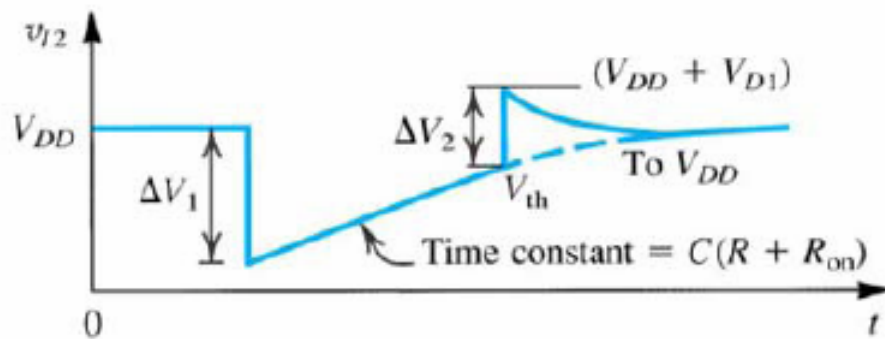- G_2 will switch and its output v_{O2} will go to 0V, which will in turn cause G_1 to switch on toward V_{DD}.
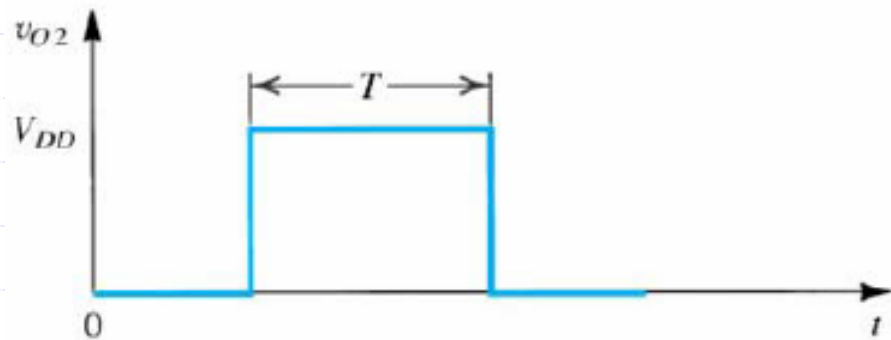
11.2.1 A CMOS Monostable Circuit (cont.)

(c)

- The output of G_1 will attempt to rise to V_{DD} (instantaneous rise). Limited to an amount ΔV_2 by the limiting action of diode.

  $$\Delta V_2 = V_{DD} + V_{D1} - V_{th}$$

- V_{O1} rise. And the input of G_2 will rise by an equal amount ΔV_2.
- Now $V_{I2} > V_{DD}$, current will flow from the output of G_1 through C and then through the parallel combination of R and D_1.
- This current discharges C until V_{I2} drops to V_{DD} and v_{O1} rises to V_{DD}.

11.2.1 A CMOS Monostable Circuit (cont.)

(c)

(d)

Figure 11.13 Timing diagram for the monostable circuit in Fig. 11.10.

※ The monostable circuit should not be retriggered until the capacitor has been discharged (recovery time: the capacitor discharge interval).

$$v_{I2}(t) = V_{DD} - \Delta V_1 e^{-t/\tau 1}$$

$$\tau_1 = C(R + R_{on})$$

Substituting for $t = T$ and $v_{I2}(T) = V_{th}$.

$$T = C(R + R_{on}) \ln(\frac{R}{R + R_{on}} \frac{V_{DD}}{V_{DD} - V_{th}})$$
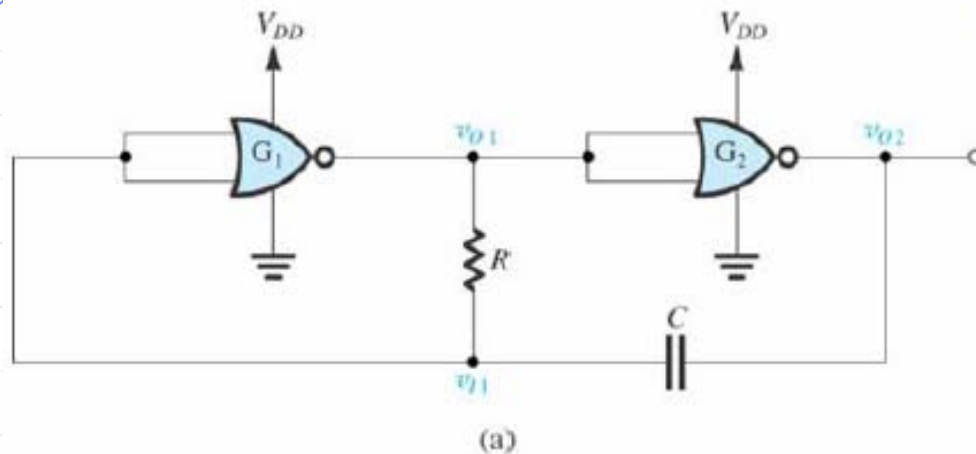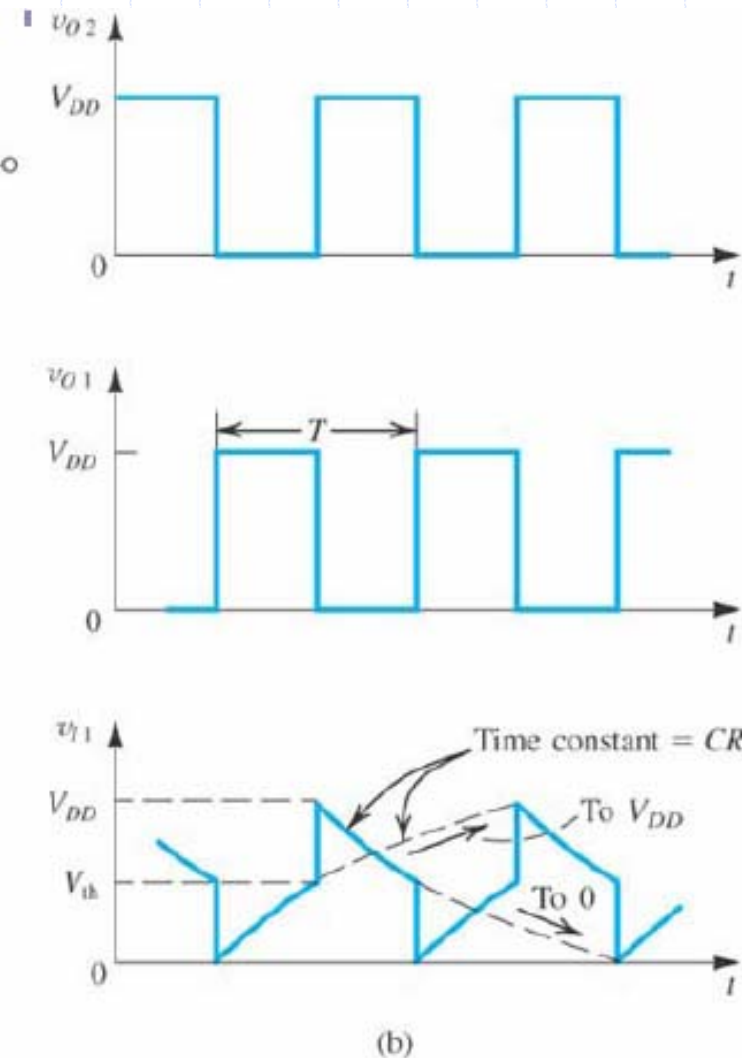
11.2.2 An Astable Circuit

Figure 11.15 (a) A simple astable multivibrator circuit using CMOS gates. (b) Waveforms for the astable circuit in (a). The diodes at the gate input are assumed to be ideal and thus to limit the voltage v_{I1} to 0 and V_{DD}.

- Assume that the NOR gates are of the CMOS family.
- Neglect the finite output resistance of the CMOS gate.
- Assume that the clamping diodes are ideal.
→ The waveforms of Fig. 11.15(b) are obtained.

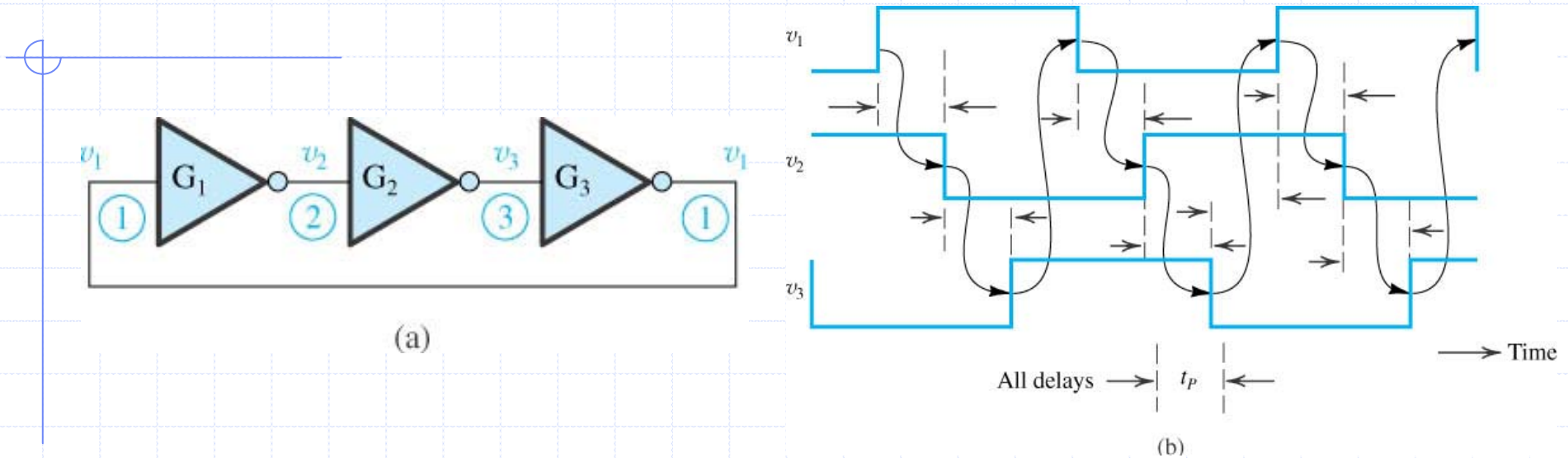Chapter 11

11.2.3 The Ring Oscillator

Figure 11.16 (a) A ring oscillator formed by connecting three inverters in cascade. (Normally at least five inverters are used.) **(b)** The resulting waveform. Observe that the circuit oscillates with frequency $1/6t_P$.

- The ring oscillator is formed by connecting an odd number of inverters in a loop.

- Usually at least five inverters are used.

- A ring with N inverters will oscillate with period of $2Nt_P$ and frequency $1/2Nt_P$.

- Ring oscillator provides a relatively simple means for measuring the inverter propagation delay.