Topics in IC Design

T-Coil

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Introduction

- Inductors produce peaking, thereby giving bandwidth extension.
- T-coil (Tee-Coil) produces even more bandwidth extension by giving negative inductance.



Dot convention Same direction : k > 0Opposite direction : k < 0 $M = k\sqrt{L_1L_2}$ $|k| \le 1$

 $|\mathbf{k}| = 1$ when inductors share all of their magnetic flux.

Introduction

Introduced by Ginzton in 1948 as part of distributed amplifier.



^[0] Ginzton, Proc IRE, 1948

T-Coil

Common Source Amplifier



Without T-Coil,

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -g_m R_D \frac{1}{1 + s R_D C_L}$$
$$f_{3dB} = 1/2\pi R_D C_L$$

With T-Coil,

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -g_m R_D \frac{a_2 s^2 + a_1 s + 1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1}$$
where
$$a_2 = (L_1 + L_2 + 2M) C_B$$

$$a_1 = (L_2 + M) / R_D$$

$$b_4 = C_B C_L (L_1 L_2 - M^2)$$

$$b_3 = C_B C_L R_D (L_1 + L_2 + 2M)$$

$$b_2 = C_B (L_1 + L_2 + 2M) + C_L L_2$$

$$b_1 = R_D C_L.$$

[1] B. Razavi, ISSC Magazine, 2015

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When two zeros in the numerator are cancelled by two of the four poles in the denominator, the second-order transfer function is obtained.

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -g_m R_D \frac{\omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2}$$

Given R_D and C_L, what are C_B, L, and M, assuming L₁ = L₂ = L
 (symmetric T-Coil)?

$$b_4 \omega_n^2 = a_2$$

$$b_3 \omega_n^2 = a_2 2\zeta \omega_n + a_1$$

$$b_2 \omega_n^2 = a_2 \omega_n^2 + a_1 2\zeta \omega_n + 1$$

$$b_1 \omega_n^2 = a_1 \omega_n^2 + 2\zeta \omega_n$$

 Four equations must be satisfied with five variables (C_B, L, M, ζ, ω_n). Out of numerous solutions, what is the best transfer function <u>that maximizes the bandwidth</u>?

• Let *k*=*M*/*L* and simplify 4 equations.



Then, determine ζ that maximizes the bw.

[1] B. Razavi, ISSC Magazine, 2015

• With the following 2nd order transfer function,

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -g_m R_D \frac{\omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2}$$

• 3-dB BW with T-Coil is

$$\omega_{BW,T-Coil}^{2} = \left[1 - 2\zeta^{2} + \sqrt{\left(1 - 2\zeta^{2}\right)^{2} + 1}\right]\omega_{n}^{2}$$
$$= \left[1 - 2\zeta^{2} + \sqrt{\left(1 - 2\zeta^{2}\right)^{2} + 1}\right]\frac{16\zeta^{2}}{R_{D}^{2}C_{L}^{2}}$$

which is maximized when $\zeta = \sqrt{2}/2$.

Then

$$\omega_{BW,T-Coil} = \omega_n = 2\sqrt{2} \frac{1}{R_D C_L}$$
$$= 2.828 \omega_{3dB}$$

[1] B. Razavi, ISSC Magazine, 2015

• The maximum bandwidth solution is

$$L = \frac{3}{8} R_D^2 C_L, M = \frac{1}{3} L, C_B = \frac{1}{8} C_L, \omega_n = 2\sqrt{2}/R_D C_L$$

which extends the bandwidth by 2.828.

Features of Symmetric T-Coil

What are its input impedances Z_{in1} and Z_{in2}?



Under the maximum bandwidth condition,

$$Z_{in1} = R_D$$

$$Z_{in2} = \infty$$

T-Coil is transparent. C_L is not seen. Can be used for return loss (RL) minimization.

Features of Symmetric T-Coil

• What is the transfer function to the resistor node?



• Under the maximum bandwidth condition,

$$\frac{V_R}{V_{in}}(s) = -g_m R_D \frac{s^2 - 2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

- All-pass function with infinite bandwidth!
- Extra **phase delay** could be a problem.

$$\Delta \emptyset(\omega) = -2 \arctan[\frac{2\zeta \omega_n \omega}{\omega_n^2 - \omega^2}]$$

- With one less constraint (L₁≠L₂), more freedom for design is utilized to extend the bandwidth at the cost of higher design complexity.
- Given R_D and C_L , what are C_B , L_1 , L_2 , and M?

$$b_4 \omega_n^2 = a_2$$

$$b_3 \omega_n^2 = a_2 2\zeta \omega_n + a_1$$

$$b_2 \omega_n^2 = a_2 \omega_n^2 + a_1 2\zeta \omega_n + 1$$

$$b_1 \omega_n^2 = a_1 \omega_n^2 + 2\zeta \omega_n$$

• Four equations must be satisfied with five variables $(C_B, L_1, L_2, M, \omega_n, and \zeta = 2/\sqrt{2})$. Out of numerous solutions, what is the best transfer function that maximizes the bandwidth, $\omega_{3dB,T-Coil}$?

- No closed-form analytical solution was found.
- So, first assume L₁=L, L₂=bL, M= mL, with constraint of the coupling coefficient

$$k = \frac{M}{\sqrt{L_1 L_2}} = \frac{m}{\sqrt{b}} < 1$$

[3] S.C.D.Roy, IETE Journal of Research, 2016

- b=1 (Symmetric T-Coil)
- b=1, m=0.333 (k=0.333), $L = 0.375R_D^2C_L$, $C_B = 0.125C_L$, $\omega_n = 2.828/R_DC_L$
- b<1, what are m(k), L, C_B , ω_n ? (using Mathematica)

 $b=1.0, m= 0.333 \ (k=0.333), L = 0.375R_D^2C_L, C_B = 0.1250C_L, \omega_n = 2.828/R_DC_L$ $b=0.9, m= 0.378 \ (k=0.398), L = 0.406R_D^2C_L, C_B = 0.1074C_L, \omega_n = 2.939/R_DC_L$ $b=0.8, m= 0.412 \ (k=0.460), L = 0.444R_D^2C_L, C_B = 0.0916C_L, \omega_n = 3.062/R_DC_L$ $b=0.7, m= 0.436 \ (k=0.521), L = 0.492R_D^2C_L, C_B = 0.0772C_L, \omega_n = 3.202/R_DC_L$ $b=0.6, m= 0.449 \ (k=0.580), L = 0.553R_D^2C_L, C_B = 0.0639C_L, \omega_n = 3.367/R_DC_L$ $b=0.5, m= 0.451 \ (k=0.638), L = 0.635R_D^2C_L, C_B = 0.0514C_L, \omega_n = 3.572/R_DC_L$ $b=0.4, m= 0.440 \ (k=0.696), L = 0.751R_D^2C_L, C_B = 0.0396C_L, \omega_n = 3.838/R_DC_L$ $b=0.3, m= 0.414 \ (k=0.756), L = 0.931R_D^2C_L, C_B = 0.0178C_L, \omega_n = 4.215/R_DC_L$ $b=0.2, m= 0.366 \ (k=0.818), L = 1.250R_D^2C_L, C_B = 0.0078C_L, \omega_n = 6.176/R_DC_L$

Practical Implementation

- Coupling coefficient of greater than 0.7 is not practical with on-chip spiral inductor.
- So, b=0.4, m= 0.440 (k=0.696), $L = 0.751R_D^2C_L$, $C_B = 0.0396C_L$, $\omega_n = 3.838/R_DC_L$ is the practical limit.



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Output at Resistor Load





1) transfer function to
$$R_D$$
?

$$\frac{V_R}{V_{in}}(s) = ?$$

2) impedance seen from either side of the T-Coil?

$$Z_{in1} = ?$$
$$Z_{in2} = ?$$

T-Coil Design Flow

• Design flow

- For given C_L and R_D , determine L_1 , L_2 , k, and C_B .
- Design T-coil in a 3-D EM tool and extract S-parameter or circuit model.
- Perform circuit simulation including parasitic resistance and capacitance.

Parasitic RC

- If using top metal, a 100 pH of inductor has series resistance of $5 \sim 10 \Omega$.
- Natural bridge capacitance is known to be 10 ~ 30 fF.

Realistic limitation

- k can't be over +0.7 in the chip.
- Self-resonance limits large k and L.

Eye Diagram Optimization

• Maximally Flat Gain ($\zeta = 1/\sqrt{2}$) vs Maximally Flat Phase Delay ($\zeta = 1$)



• Minimum Jitter Condition: Minimum phase delay variation

[4] W Bae, TVLSI, 2017

Asymmetric T-Coil Simulation

C_L = 200 fF, R_T = 50 Ω $\zeta = 1/\sqrt{2}$, k = 0.45 (BW = 15.92 GHz) L = 219 pH, b = 0

 $ζ = 1/\sqrt{2}, k = 0.45$ L = 219 pH, b = 0.815
C_B = 18.74 fF

Two T-coils :

 Maximally flat gain @ k = 0.45
 Maximally flat phase delay around 1. (L = 200 pH)



Asymmetric T-Coil Simulation

C_L = 200 fF, R_T = 50 Ω $\zeta = 1/\sqrt{2}$, k = 0.45

(BW = 15.92 GHz) L = 219 pH, b = 0.815 $C_{B} = 18.74 \text{ fF}$

Two T-coils : 1. Maximally flat gain @ k = 0.45 2. Maximally flat phase delay around 1. (L = 200 pH)

No T-coil







Return Loss Reduction

• Minimize Return Loss at TX driver and RX receiver.



• Effect of Large ESD Capacitance is removed.

[5] M.Kossel, JSSC, 2008 [6] M.S.Keel, EOS/ESD, 2015

TX Optimization



56Gb/s eye diagram



No T-coil

k = 0.5, L = 200 pH, b = 0.3

k = -0.25, L = 250 pH, b = 0.4

Example: ESD Diode Isolation



3.5: A 16-to-40Gb/s Quarter-Rate NRZ/PAM4 Dual-Mode Transmitter in 14nm CMOS

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[7] J.Kim, ISSCC, 2015

International Solid-State Circuits Conference

Example: ESD Separation



[8] C.Y.Lin, IEEE Transactions on Electron Devices. 2013

Example: Double T-Coil



[9] G.Steffan, ISSCC, 2017

International Solid-State Circuits Conference

Example: π **Coil with 4 ports**



[10] J Kim, JSSC, 2019

References

- [0] E. Ginzton et. al, "Distributed Amplification," *Proc. IRE*, vol. 36, pp. 956–969, Aug. 1948.
- [1] Razavi, Behzad, "The bridged T-coil [a circuit for all seasons]." IEEE Solid-State Circuits Magazine 7.4 (2015): 9-13.
- [2] Paramesh, Jeyanandh, and David J. Allstot. "Analysis of the bridged T-coil circuit using the extra-element theorem." IEEE Transactions on Circuits and Systems II: Express Briefs 53.12 (2006): 1408-1412.
- [3] Dutta Roy, Suhash C. "A Theoretical Investigation into the Limits of Bandwidth Enhancement with the Asymmetrical Bridged T-Coil Network." IETE Journal of Research 62.3 (2016): 379-386.
- [4] Bae, Woorham, Borivoje Nikolić, and Deog-Kyoon Jeong. "Use of phase delay analysis for evaluating wideband circuits: An alternative to group delay analysis." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 25.12 (2017): 3543-3547.
- [5] Kossel, Marcel, et al. "A T-Coil-Enhanced 8.5 Gb/s High-Swing SST Transmitter in 65 nm Bulk CMOS With ≪-16 dB Return Loss Over 10 GHz Bandwidth." IEEE Journal of Solid-State Circuits 43.12 (2008): 2905-2920.
- [6] Keel, Min-Sun, and Elyse Rosenbaum. "CDM-reliable T-coil techniques for highspeed wireline receivers." 2015 37th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD). IEEE, 2015.

References

- [7] Kim, Jihwan, et al. "3.5 A 16-to-40Gb/s quarter-rate NRZ/PAM4 dual-mode transmitter in 14nm CMOS." 2015 IEEE International Solid-State Circuits Conference-(ISSCC) Digest of Technical Papers. IEEE, 2015.
- [8] Lin, Chun-Yu, Li-Wei Chu, and Ming-Dou Ker. "Robust ESD protection design for 40-Gb/s transceiver in 65-nm CMOS process." IEEE transactions on electron devices 60.11 (2013): 3625-3631.
- [9] Steffan, Giovanni, et al. "6.4 A 64Gb/s PAM-4 transmitter with 4-Tap FFE and 2.26 pJ/b energy efficiency in 28nm CMOS FDSOI." 2017 IEEE International Solid-State Circuits Conference (ISSCC). IEEE, 2017.
- [10] Kim, Jihwan, et al. "A 112 Gb/s PAM-4 56 Gb/s NRZ reconfigurable transmitter with three-tap FFE in 10-nm FinFET." IEEE Journal of Solid-State Circuits 54.1 (2019): 29-42.