Topics in IC Design

2.1 Introduction to Phase-Locked Loop

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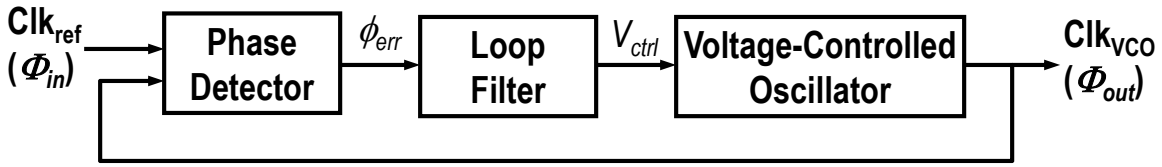
2020 Fall

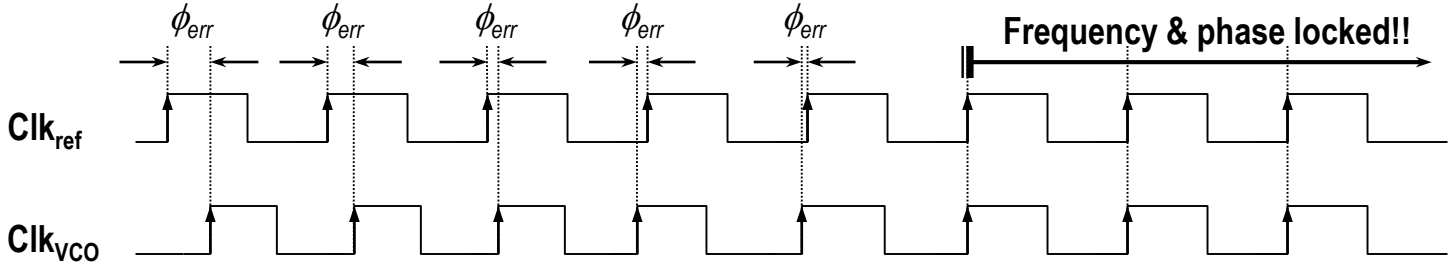
Outline

- Introduction
- Charge-Pump PLL building blocks
- Charge-Pump PLL dynamics
- Clock Synthesizers

What is PLL?

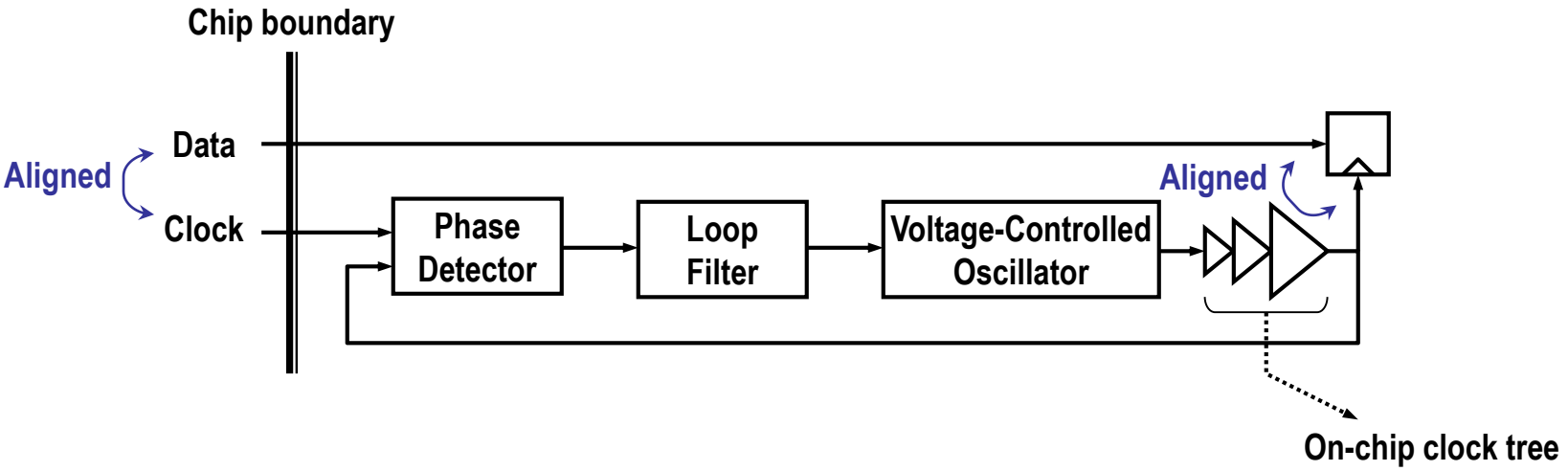
- A negative feedback system where an oscillator-generated signal is frequency and phase locked to a reference signal





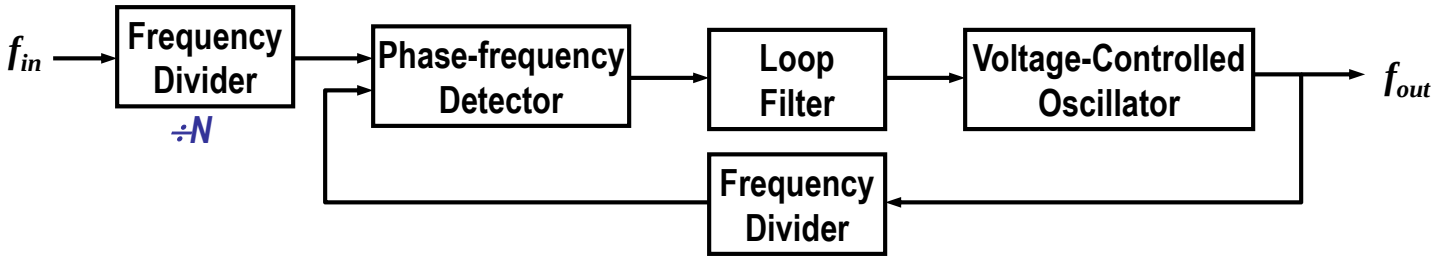
PLL Applications (1)

- On-chip clock generator with reduced skew – Zero delay buffer
- Resolves skew problem due to on-chip clock tree



PLL Applications (2)

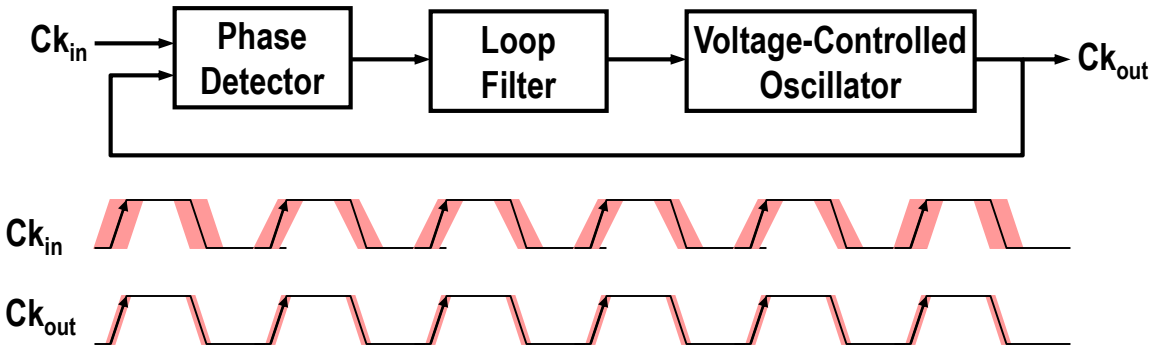
- Clock frequency multiplication – On-chip clock generation
- Frequency synthesizer – Many RF applications



$$f_{out} = \frac{M}{N} f_{in}$$

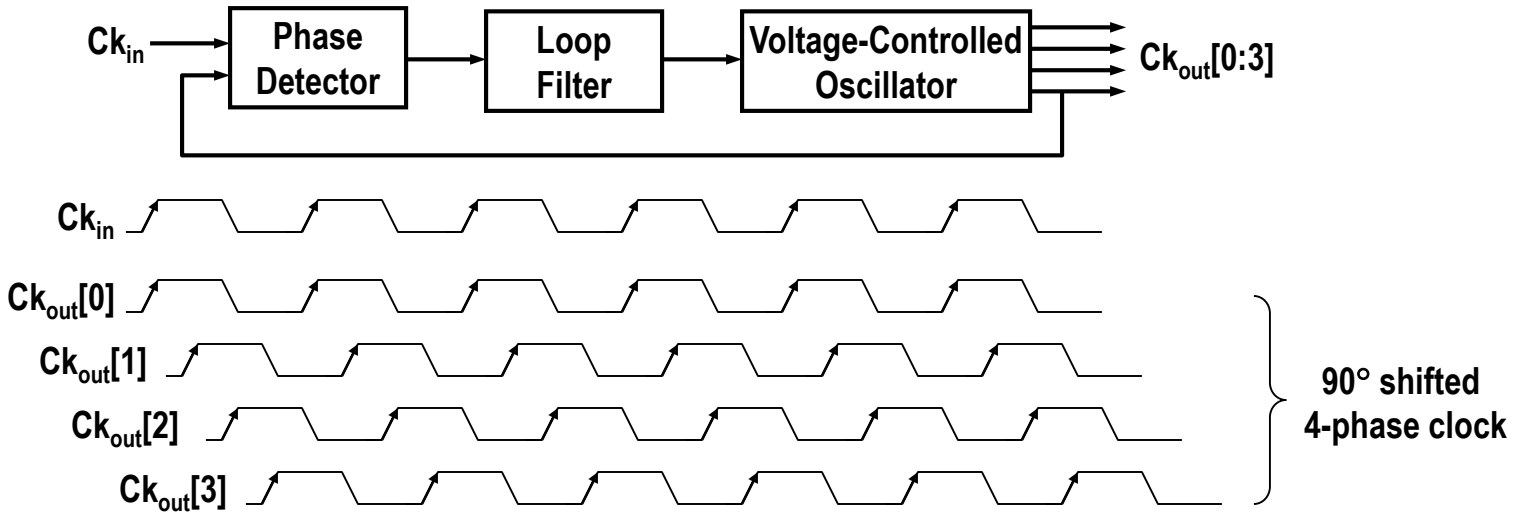
PLL Applications (3)

- Jitter reduction
- PLL filters out low frequency jitter of input clock



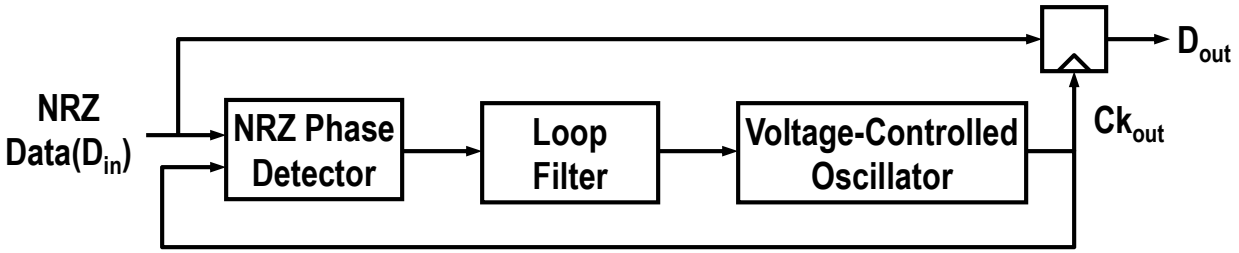
PLL Applications (4)

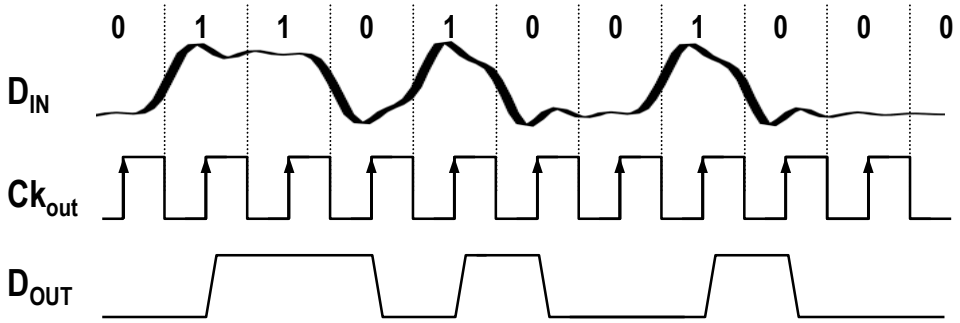
- Multi-phase clock generation
- Multi-phase clock is very useful in many applications



PLL Applications (5)

- Clock and data recovery
- Extracts timing information from NRZ data pattern





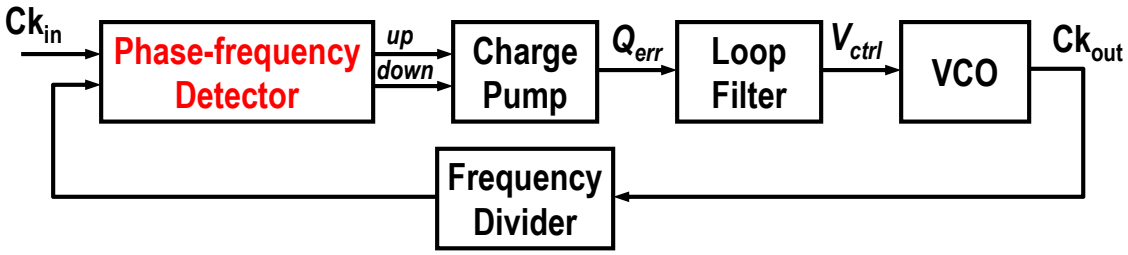
PLL aligns falling edge of Ck_{out} with data transition, so that the data is sampled at optimal point!!

PLL Building Blocks

- Voltage controlled oscillator (VCO)
- Phase detector (PD)
- Charge pump (CP)
- Loop filter (LF)
- Frequency divider

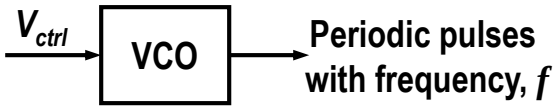
Charge-Pump PLL

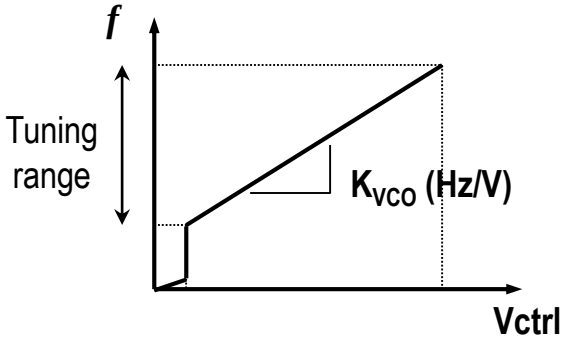
- Most of recent PLLs are of the charge-pump type
- PFD + CP – Converts digital phase-error signal to analog current
- 4 essential building blocks – VCO, PFD, CP, and loop filter
- 1 optional building block – Frequency divider



VCO

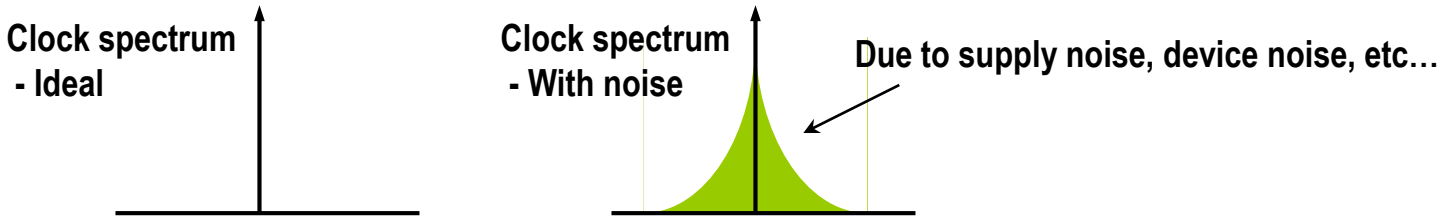
- Self-resonating clock generator
- LC tank, ring oscillator, relaxation oscillator …
- Performance parameters
  - ✓ Center frequency (No meaning for CP-PLL)
  - ✓ Tuning range
  - ✓ Tuning linearity
  - ✓ Power dissipation
  - ✓ Supply rejection ratio
  - ✓ Spectral purity





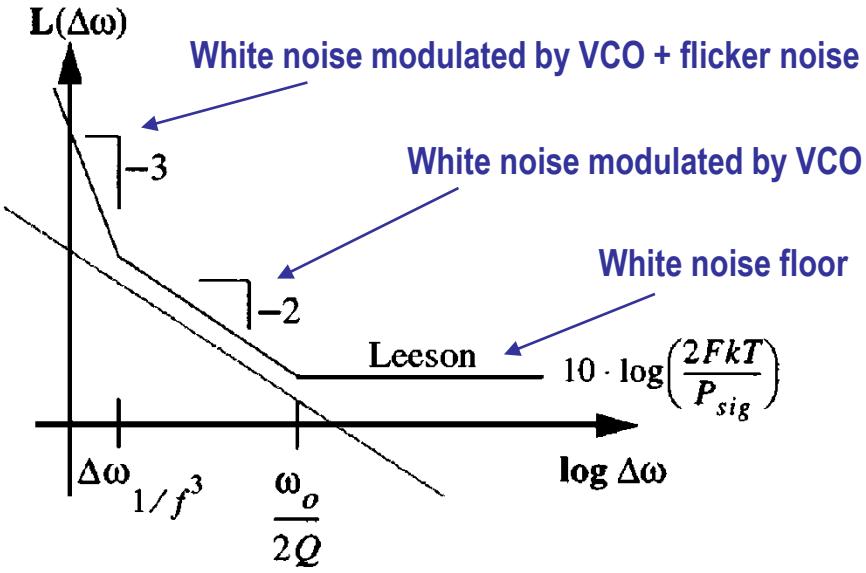
VCO

- VCO gain – K_{VCO} (Hz/V or rad/s/V)
  - ✓ Large gain means wide tuning range, but more sensitive to control line noise in PLL
- Phase noise of VCO
  - ✓ If input clock is clean, VCO is a dominant noise source in PLL
  - ✓ White noise is modulated by VCO as a “skirt-like shape”



VCO Phase Noise Model

- Leeson's model



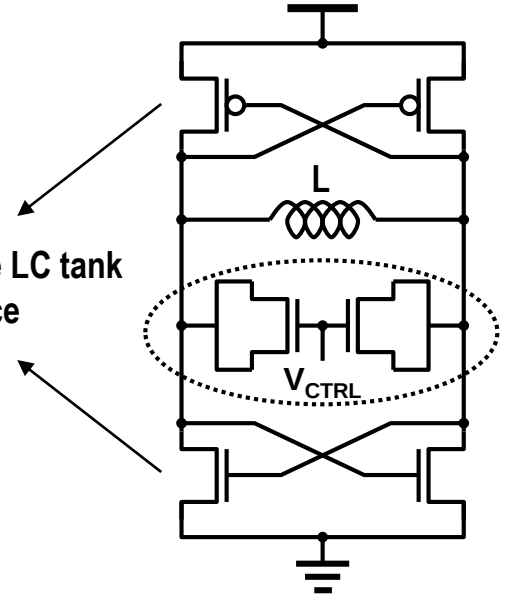
$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_{\text{sig}}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right]$$

Low Noise VCO

- Use high-Q resonator
- Maximize signal swing – May result in more power dissipation
- Fast slew rate – Reduces signal transition time
- Symmetrical waveform
  - Robustness against flicker noise
  - Reduces low frequency phase noise

LC-Tank Oscillator

- LC resonator as VCO
  - ☺ Low noise
  - ☺ Insensitive to PVT variation
  - ☺ High-frequency
  - ☹ Narrow tuning range
  - ☹ Requires additional fabrication steps for spiral inductor – Thick top metal



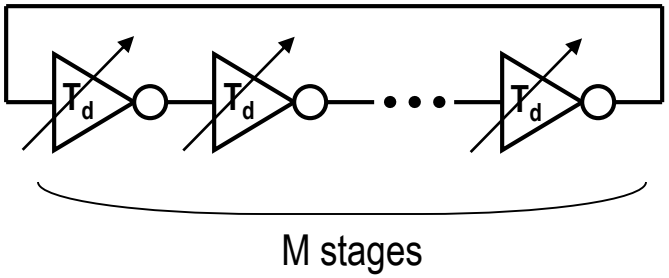
Negative resistance to compensate LC tank loss due to finite metal conductance

MOS varactor for frequency control : C_{var}

$$f = \frac{1}{2\pi\sqrt{LC_{var}}}$$

Ring Oscillator

- Chain of variable delay elements
  - ☺ Easy to implement
  - ☺ Low cost
  - ☺ Wide range
  - ☹ Very sensitive to PVT variation
  - ☹ Noisier than LC-tank



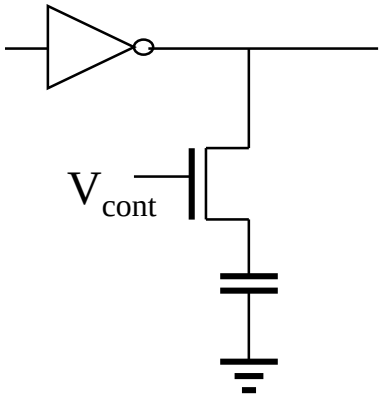
Odd number of inversions

$$f = \frac{1}{2MT_d}$$

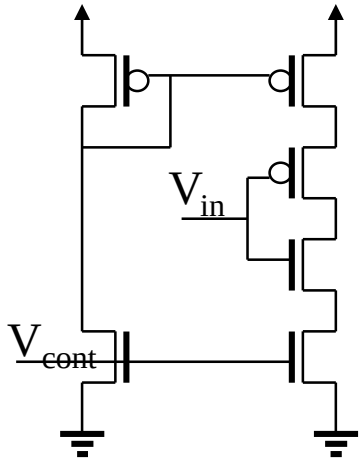
$$T_d = \frac{C\Delta V}{I} \quad \Rightarrow$$

Single stage delay: Delay is controlled by varying C or ΔV or I

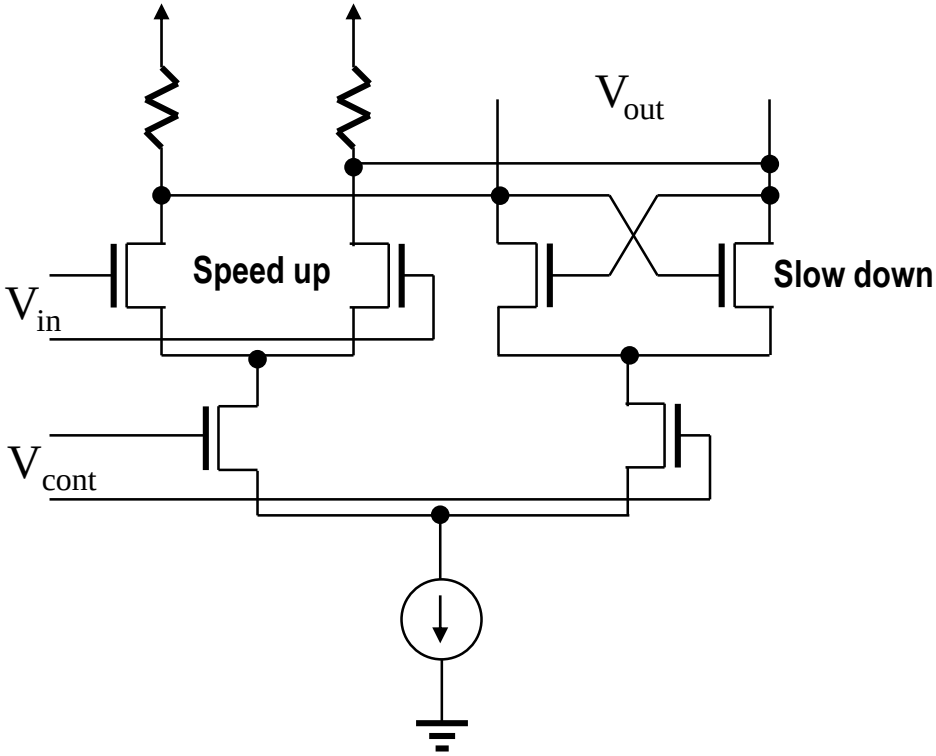
Delay Element Examples



(a) Capacitive tuning



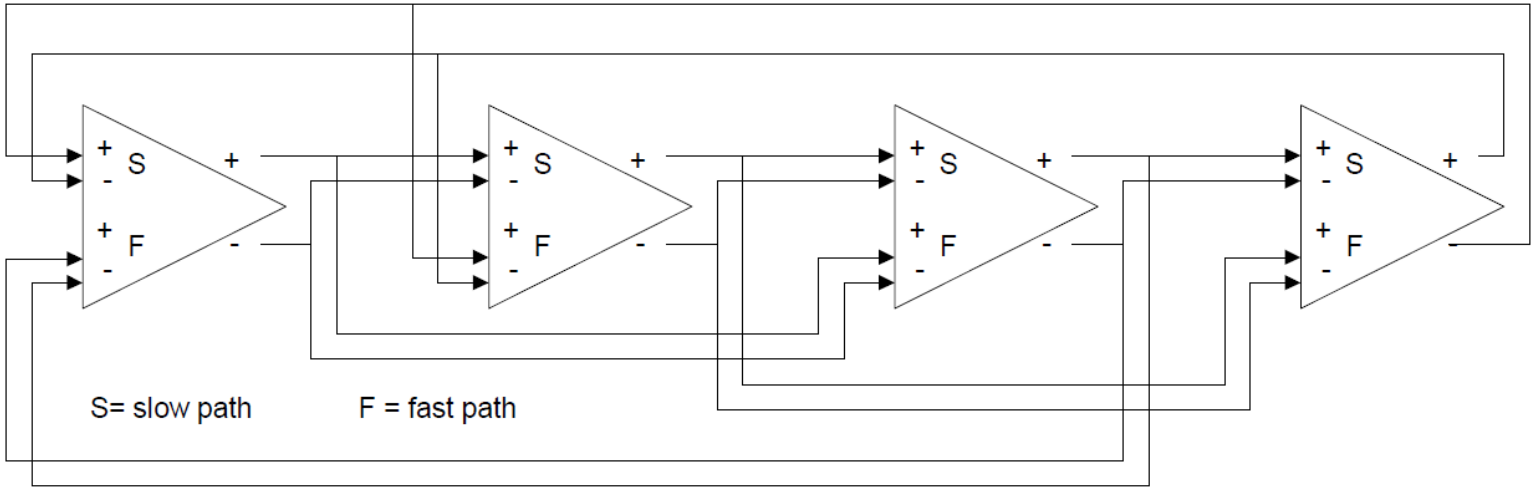
(b) Starved inverter



(c) Delay variation by positive feedback

Multipath Oscillator

- When oscillation frequency is low. Extend the frequency by 30%.
- One input of the delay inverter comes from the previous delay stage
- Extra input comes early from the 2nd previous delay stage
- Must be careful about the false mode.
  - Check with various initial conditions

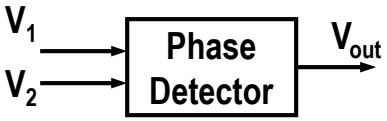


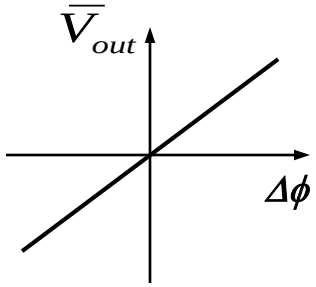
Design Tips on Ring Oscillator

- RO phase noise is too large for high precision PLL applications - the main source of PLL output jitter
- Differential structure for less supply sensitivity
- Latch added at the output for faster rise/fall times
- Too many stages can cause harmonic lock
- Symmetric rise/fall times for less phase noise against flicker noise
- Multipath RO for higher frequency
- PVT variation can cause 1:3 oscillating frequency
- Possible use of LD regulator for less variation and less jitter
- Use of supply as the control voltage
  - Level translation is required
  - Less swing might increase jitter

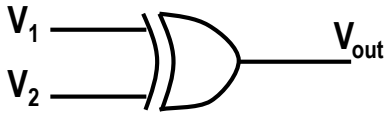
Phase Detector

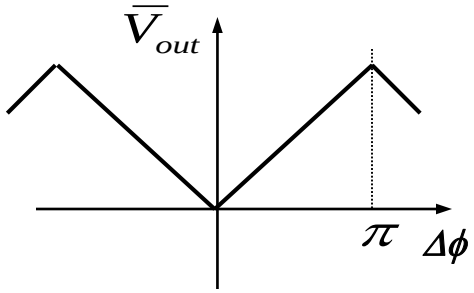
- Definition

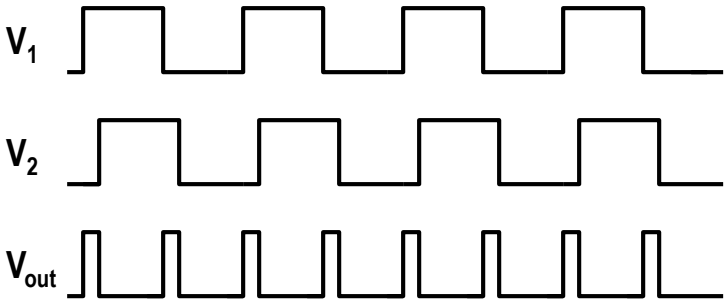




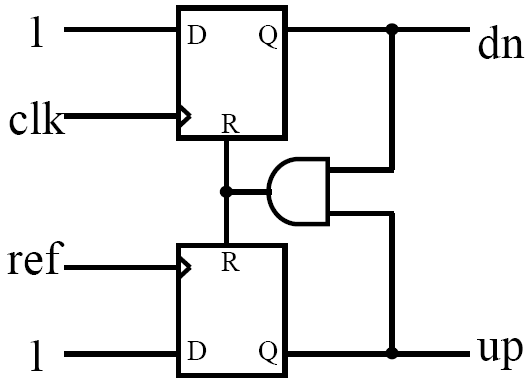
- XOR gate as phase detector

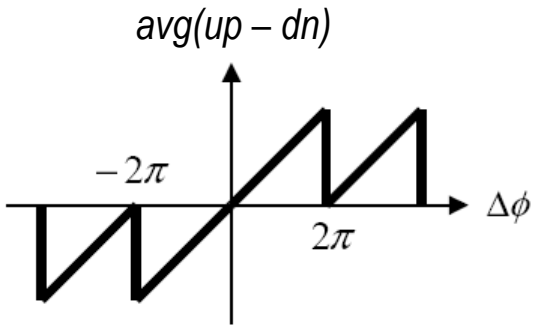




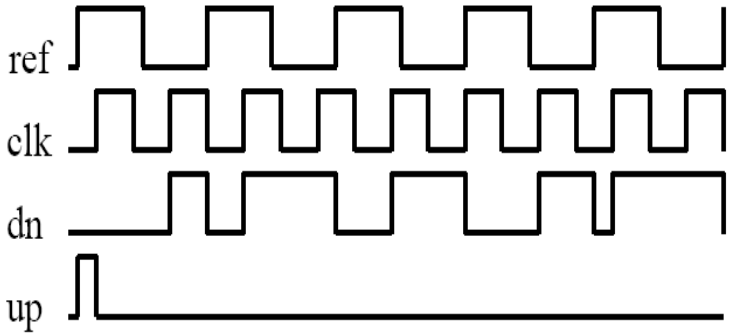


Phase Frequency Detector

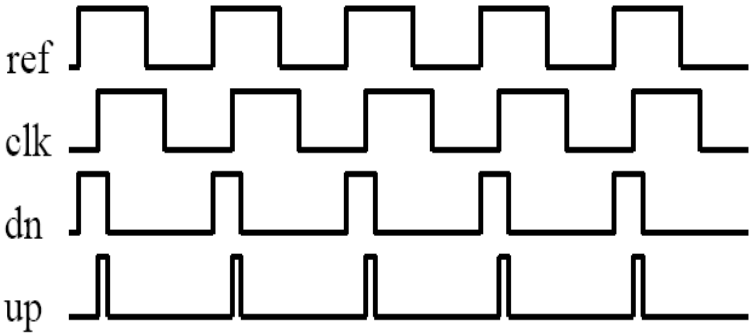




Different frequency (Frequency detection)

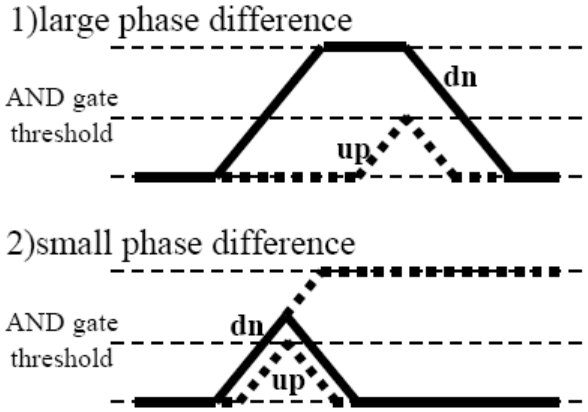


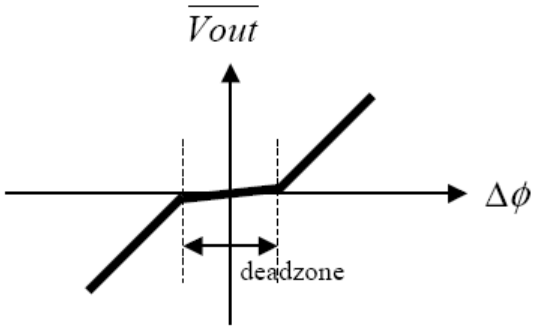
Same frequency (Phase detection)



PFD Non-ideality

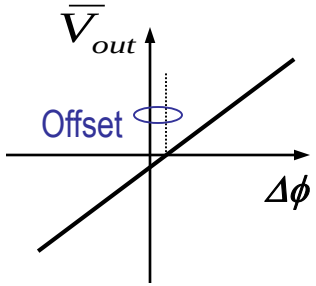
- Dead zone – Occurs when PFD doesn't respond to small phase errors





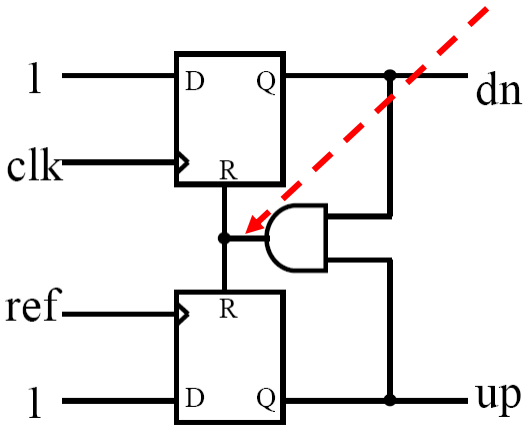
DN pulse is too narrow - ignored by charge pump

- Phase offset – Due to circuit or device mismatch



Design Tips on PFD

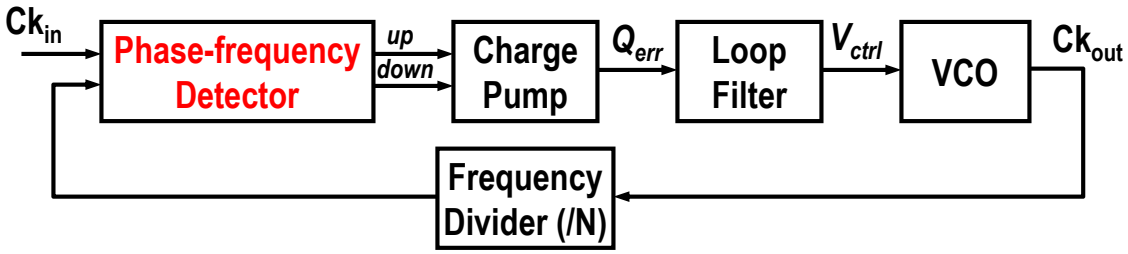
- Intentionally introduce delay by adding delay on reset path
  - Identical wide pulses on up and dn in the locked state must be cancelled in the charge pump



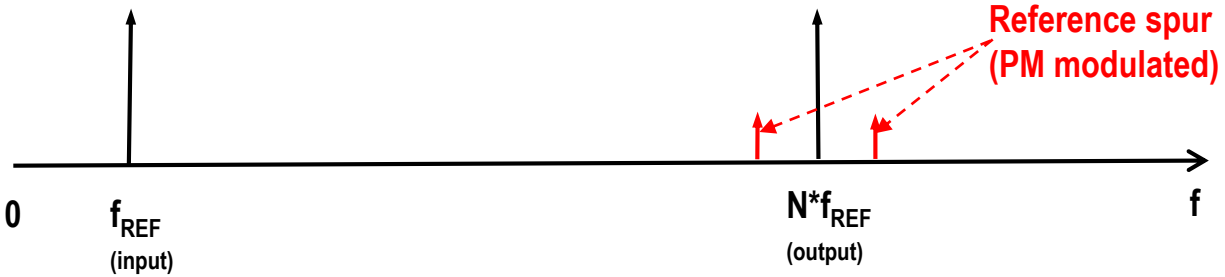
- Reduce delay offset in up and dn path to the charge pump
  - Reference spur appears at PLL output

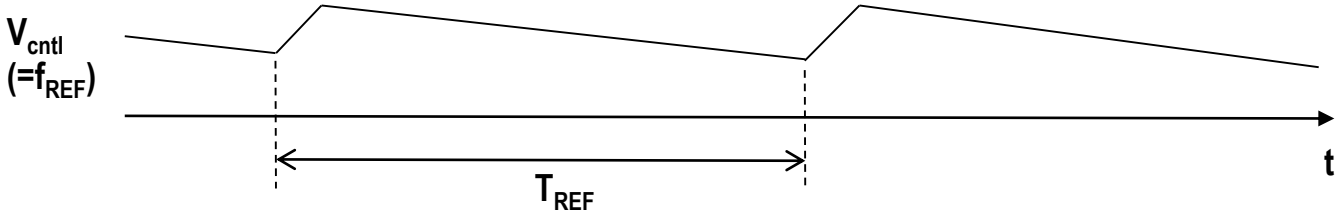
Reference Spur

- In the frequency multiplier



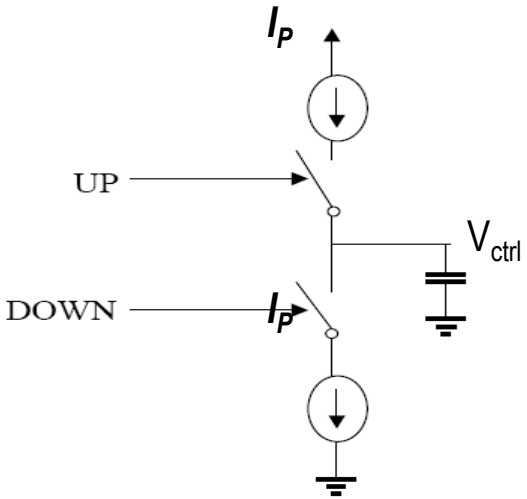
Clock power spectrum

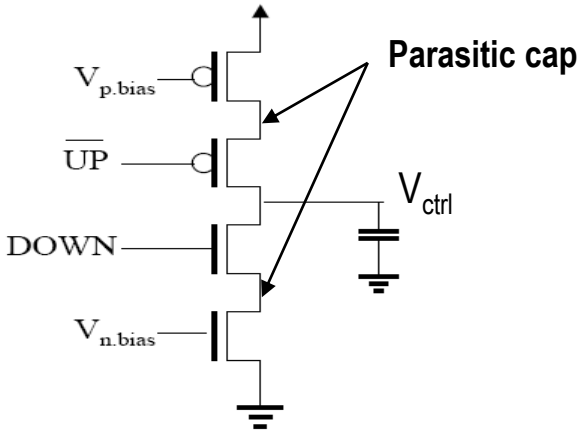




Charge Pump

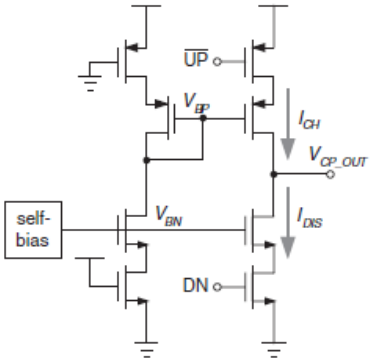
- Converts PFD phase error(digital) to charge(analog)
- Issues
  - ✓ Equal up/down current over entire V_{ctrl} range
  - ✓ Minimum coupling between switching signals & V_{ctrl}
  - ✓ PVT insensitive pumping current
  - ✓ Charge sharing between loop filter cap & CP internal nodes
  - ✓ Output resistance of the transistors





Design tips on Charge Pump

- A differential charge pump is more accurate
- Equalize up/down current over the entire voltage range



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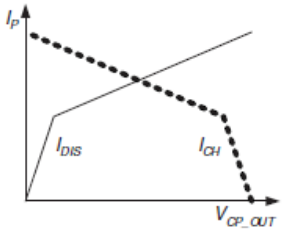

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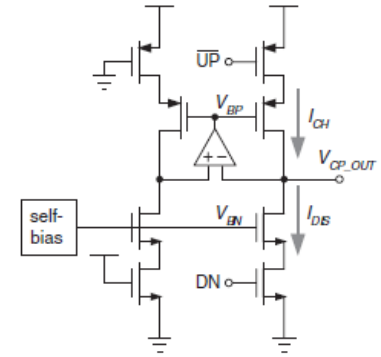

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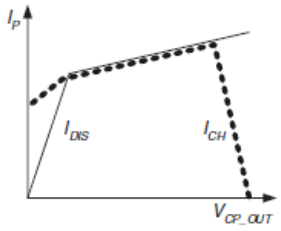

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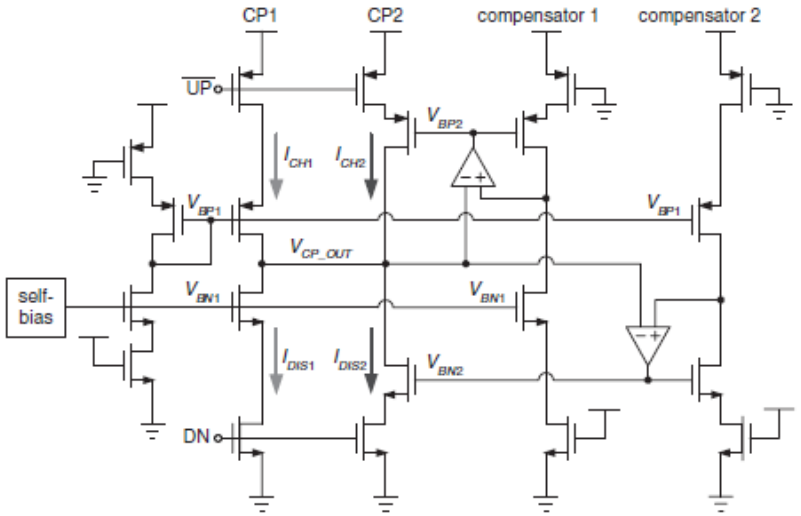
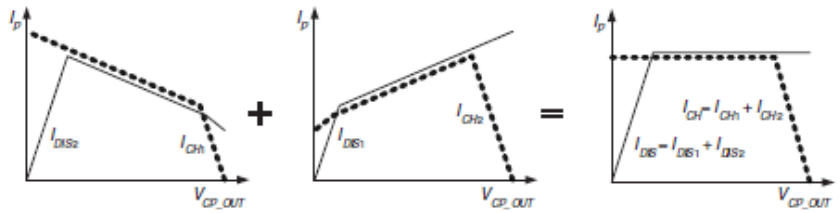
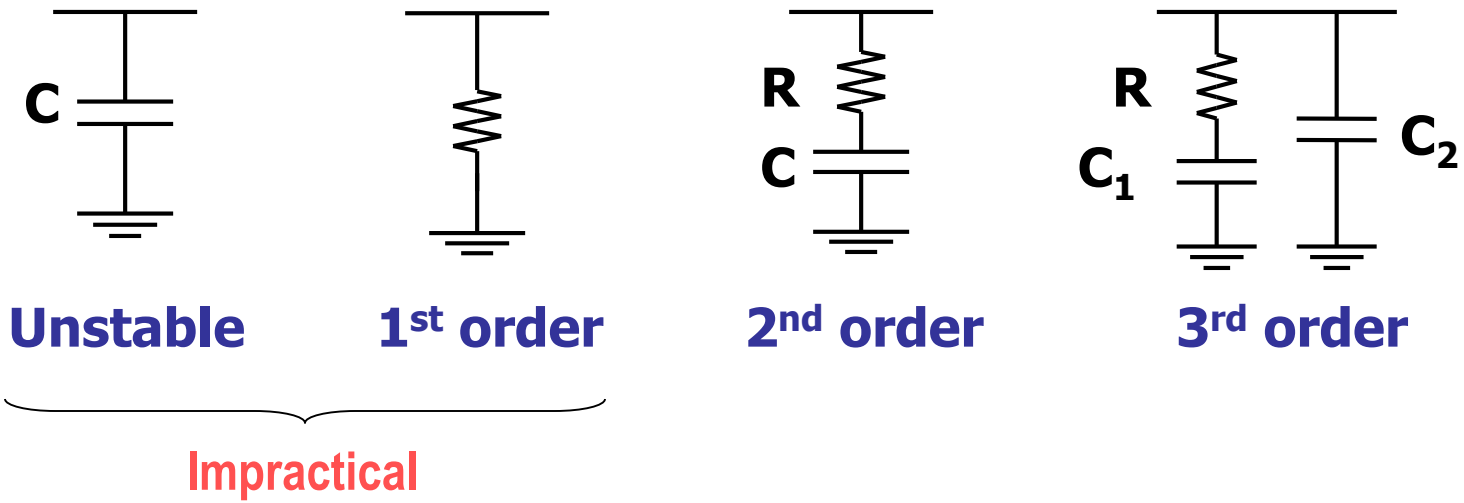




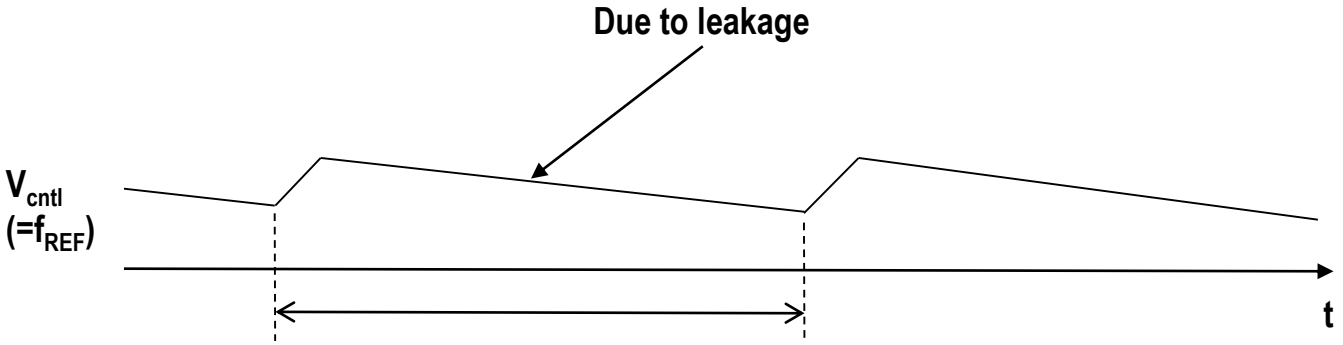
Loop Filter

- Low pass filter composed in passive RC network
- Type
  - ✓ Capacitor only – Unstable
  - ✓ Resistor only – Stable, but lock range is very narrow
  - ✓ 2nd order – Integral path (Set average VCO frequency) + proportional path (Instantaneous phase correction)
  - ✓ 3rd order – 2nd order LF + additional cap to smooth large IR ripple on Vctrl



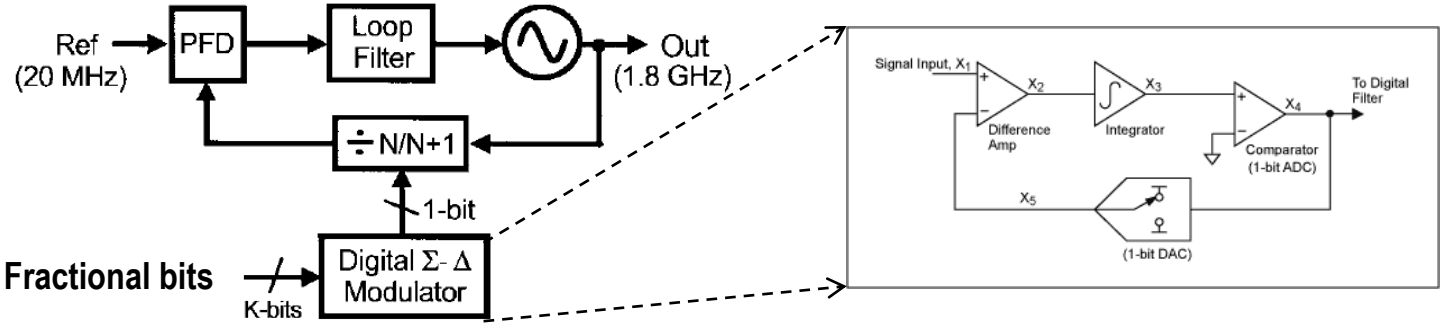
Design tips on Loop Filter

- Main source of reference spur in the frequency multiplier
- Beware the leakage current of the capacitor made with thin oxide of the MOS - Causes spur



Frequency Divider

- Type
  - ✓ Cascade of div-2 – Divide by powers of 2 only
  - ✓ Integer-N divider – Counter-based FSM
  - ✓ Fractional-N divider – Alternates div-N & div-N+1 operation to generate fractional frequency using sigma-delta modulator
  - ✓ Sigma-delta modulator
    - ✓ Keeps the average by dithering
    - ✓ Noise shaping operation moves noise to higher frequency (easily removed)
    - ✓ Prevents spur (only fractional spur present)
    - ✓ Third-order SDM can fully remove fractional spur as well



Design tips on Frequency Divider

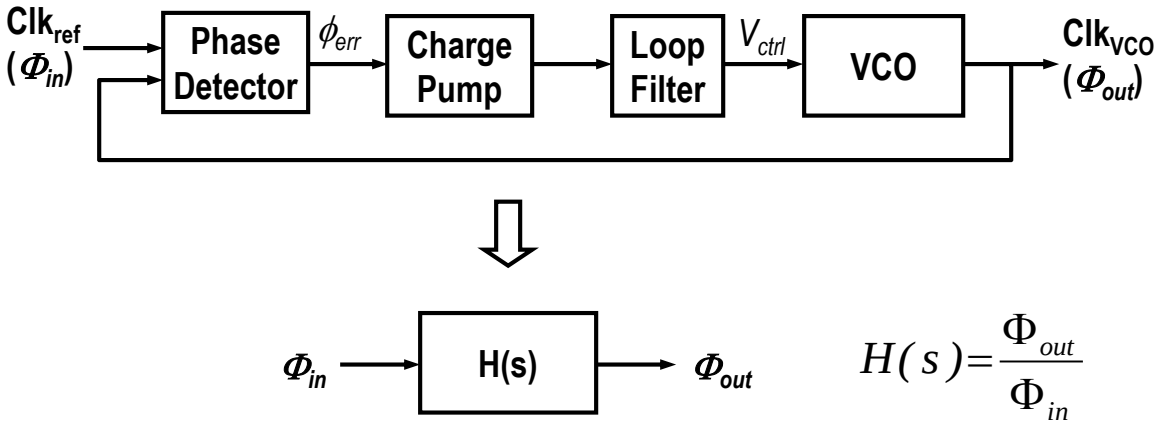
- Divider operating frequency range > entire VCO oscillation frequency range under PVT variation (**NOT** functional operating oscillation frequency)
  - Use dual-modulus prescaler for high frequency division
- Minimum delay – Logic delay degrades PLL loop stability
- Try to reduce jitter with supply variation

PLL Dynamics

- PLL s-domain model
- PLL dynamics analysis using Bode plot
- Jitter in PLL
- PLL design procedure

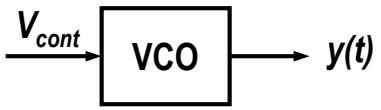
PLL s-domain model

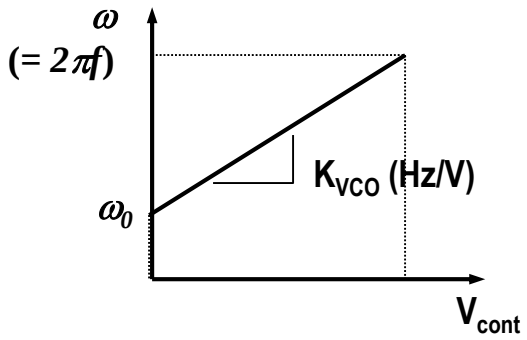
- Assumption – PLL operation frequency is much higher than PLL loop responding speed
  - ✓ Loop bandwidth >> f_0 by the factor of > 10
  - ✓ Can ignore sampling nature of PLL, and consequently, can be modeled in s-domain, not in z-domain
- PLL can be viewed as a linear system with phase-input & phase-output



VCO Model

- Beware the unit –rad/s/V
  - ✓ Multiply by 2π when unit is [Hz/V]





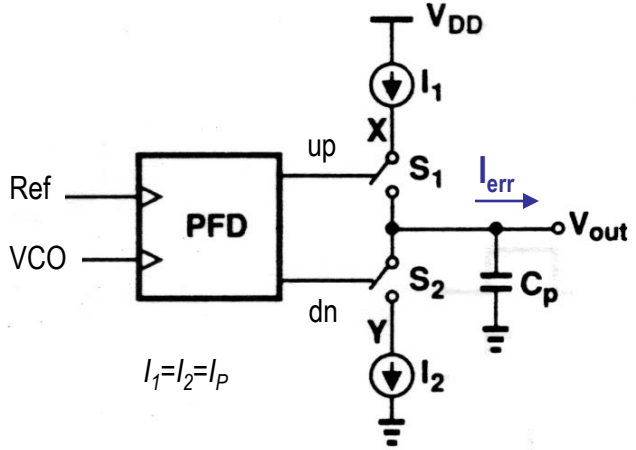
$$\omega_{\text{out}} = \omega_0 + K_{VCO} \cdot v_{\text{cont}}(t)$$

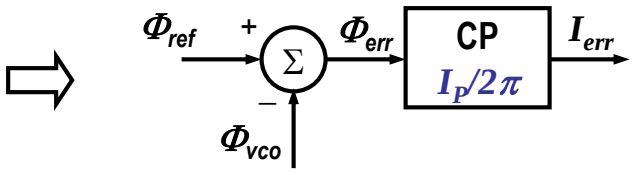
$$y(t) = A_0 \cos\left(\omega_0 t + K_{VCO} \int v_{\text{cont}}(t)dt\right)$$

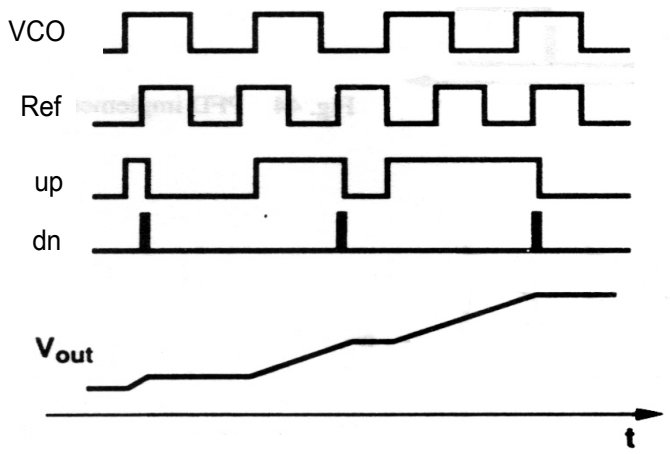
$$\text{Excess phase}: \ \phi_{\text{out}}(t) = K_{VCO} \int v_{\text{cont}}(t)dt$$

$$\text{Transfer function}: \ \frac{\phi_{\text{out}}}{V_{\text{cont}}}(s) = \frac{K_{VCO}}{s}$$

PFD and Charge Pump Model



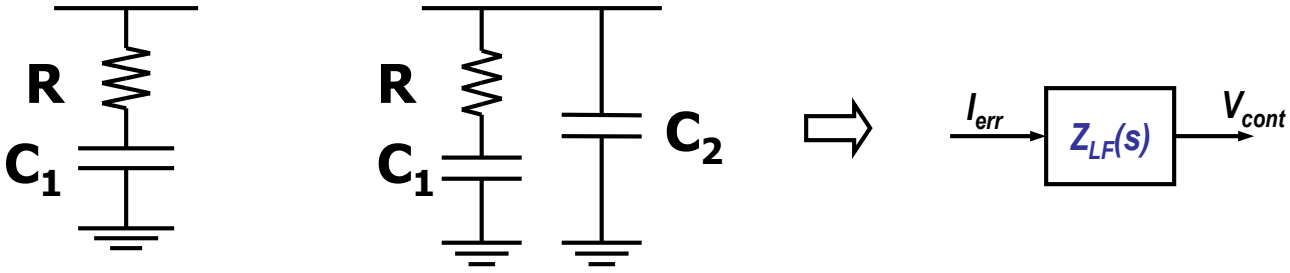




Average error current over a reference cycle: I_{err}

$$I_{err} = \frac{\Phi_{err}}{2\pi} \times I_P$$

Loop Filter Model



2nd order 3rd order

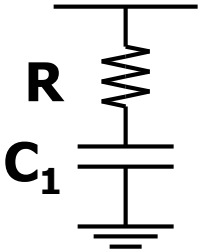
2nd order $$Z_{LF}(s)=\left(R+\frac{1}{sC_1}\right)=\frac{s/\omega_z+1}{sC_1}$$

3rd order $$Z_{LF}(s)=\left(R+\frac{1}{sC_1}\right)\Big\|\frac{1}{sC_2}=\frac{RC_1s+1}{RC_1C_2s^2+(C_1+C_2)s}=\frac{1}{(C_1+C_2)s}\,\frac{s/\omega_z+1}{s/\omega_p+1}$$

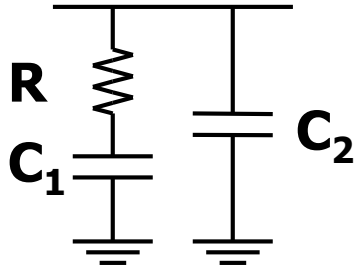
$$\left(\omega_z=\frac{1}{RC_1}\ ,\quad \omega_p=\frac{C_1+C_2}{RC_1C_2}\right)$$ Usually $C_1 > 10C_2$

Loop Filter Model

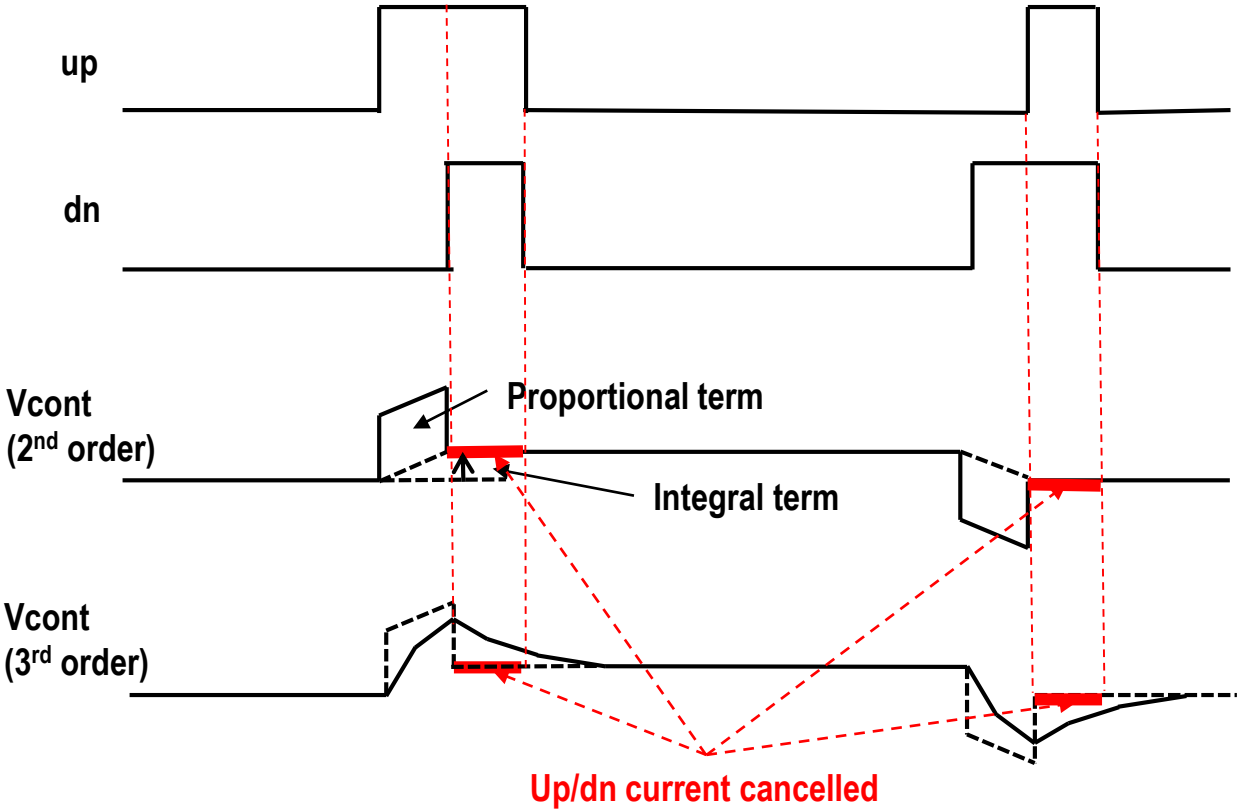
- Second order loop filter causes ripple on the Vcont



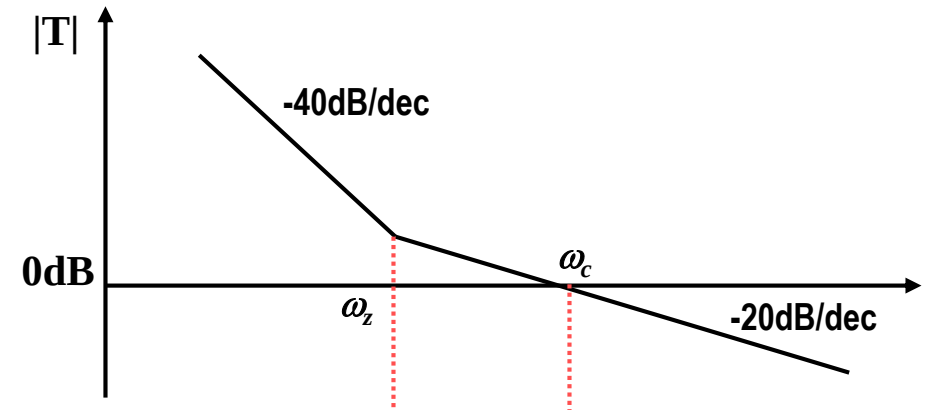
2nd order



3rd order



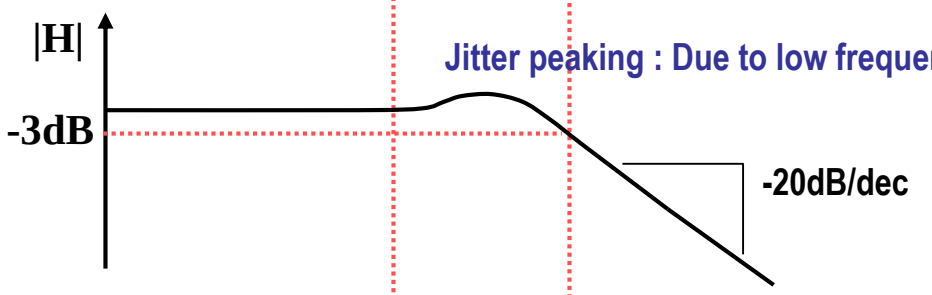
Bode Plot Premier – 2nd Order PLL



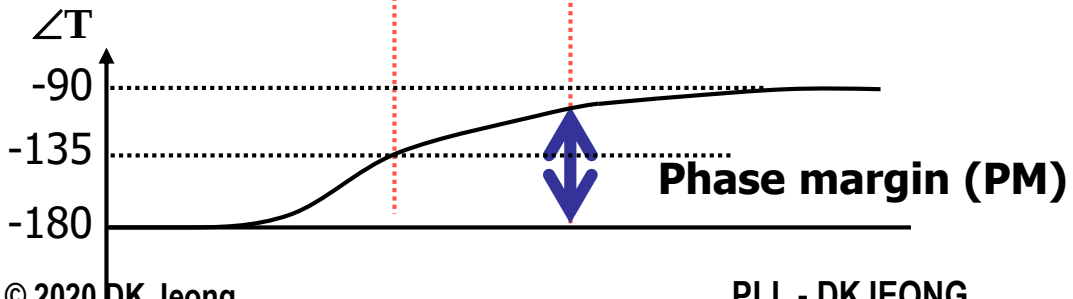
$$T(s) = K\frac{s/\omega_z + 1}{s^2},\ K = \frac{K_{VCO} I_p}{2\pi C_1}$$

$$|T(j\omega_c)| = 1 \Rightarrow$$

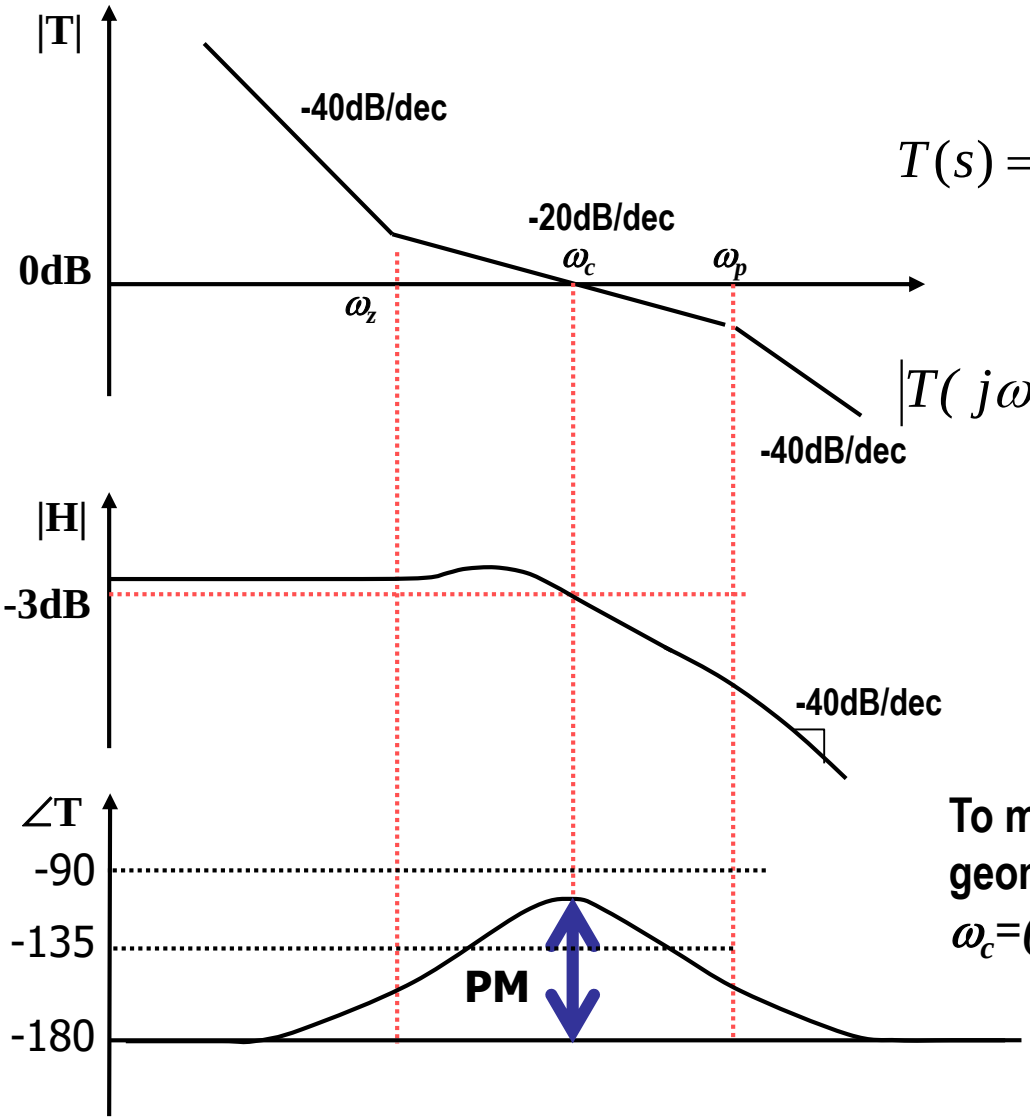
$$\omega_c = \frac{I_p K_{VCO} R}{2\pi} \text{ if } \omega_z << \omega_c$$



Jitter peaking : Due to low frequency zero



Bode Plot Premier – 3rd Order PLL



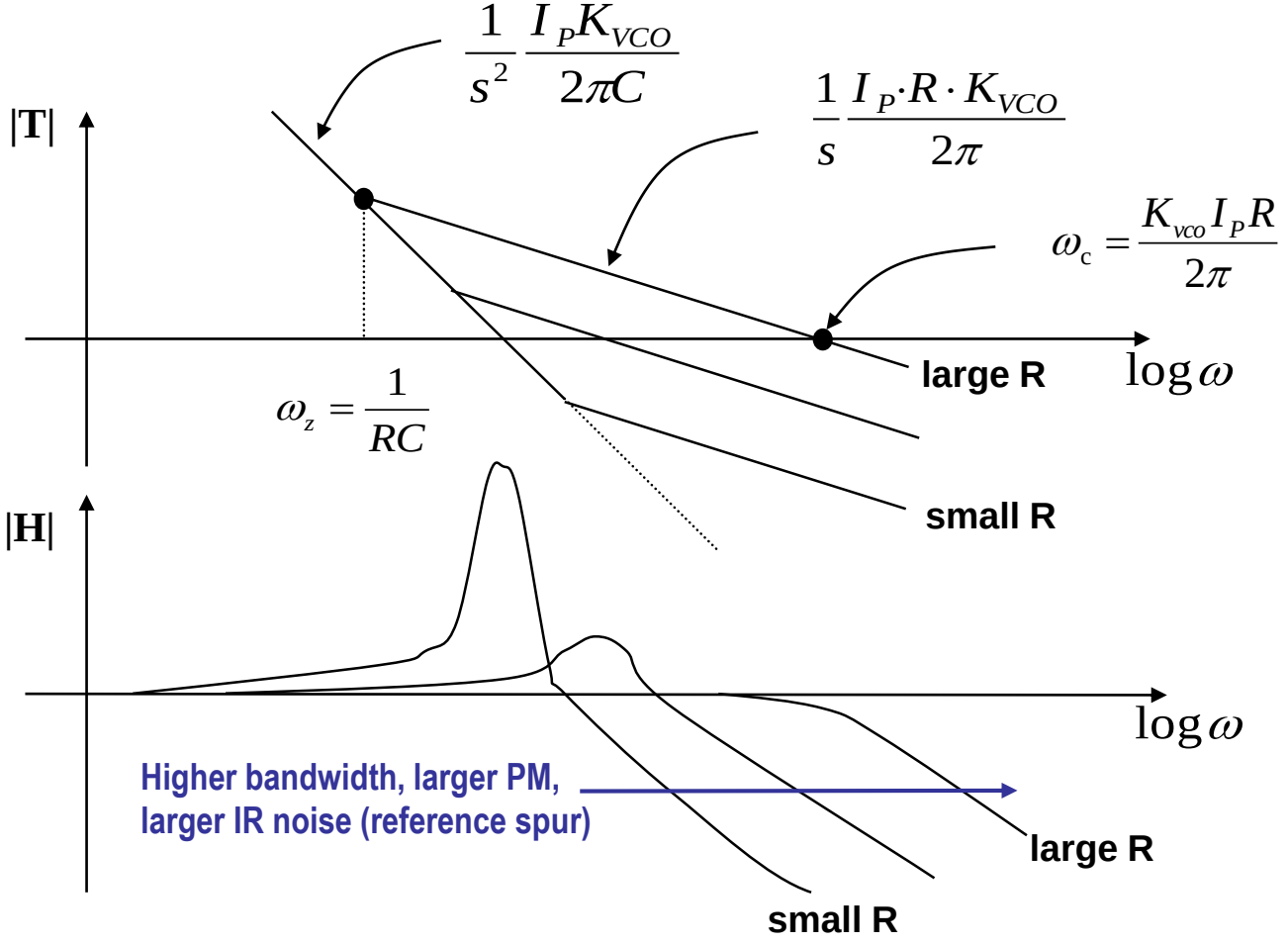
$$T(s) = K\frac{1}{s^2}\frac{s/\omega_z + 1}{s/\omega_p + 1},\ K = \frac{K_{VCO} I_p}{2\pi(C_1 + C_2)}$$

$$|T(j\omega_c)| = 1 \quad \Rightarrow \quad \omega_c = \frac{I_p K_{VCO} R}{2\pi(1 + C_2/C_1)}$$

To maximize PM, ω_c must be located at geometric mean of ω_z and ω_p , *i.e.*, $\omega_c=(\omega_z\omega_p)^{1/2}$

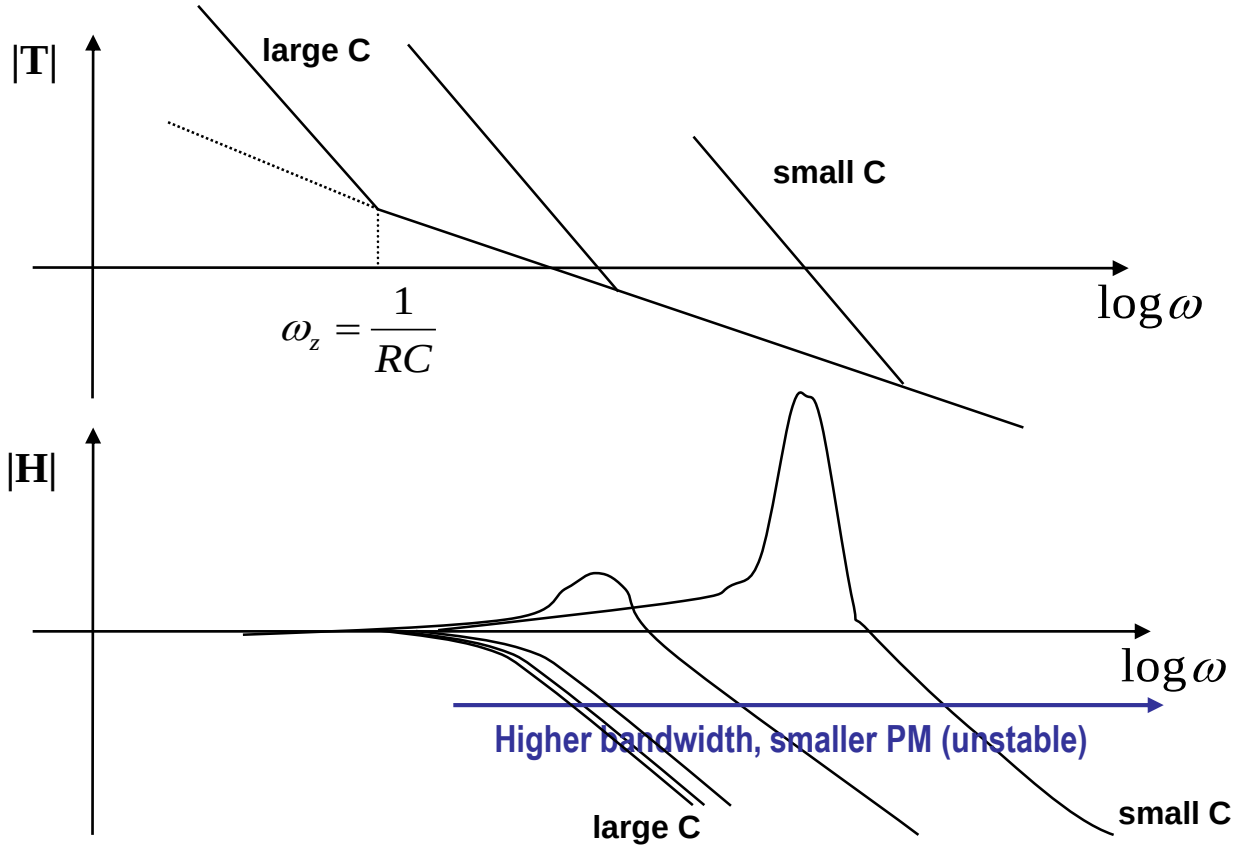
Tuning Design Parameters

- Tuning of R



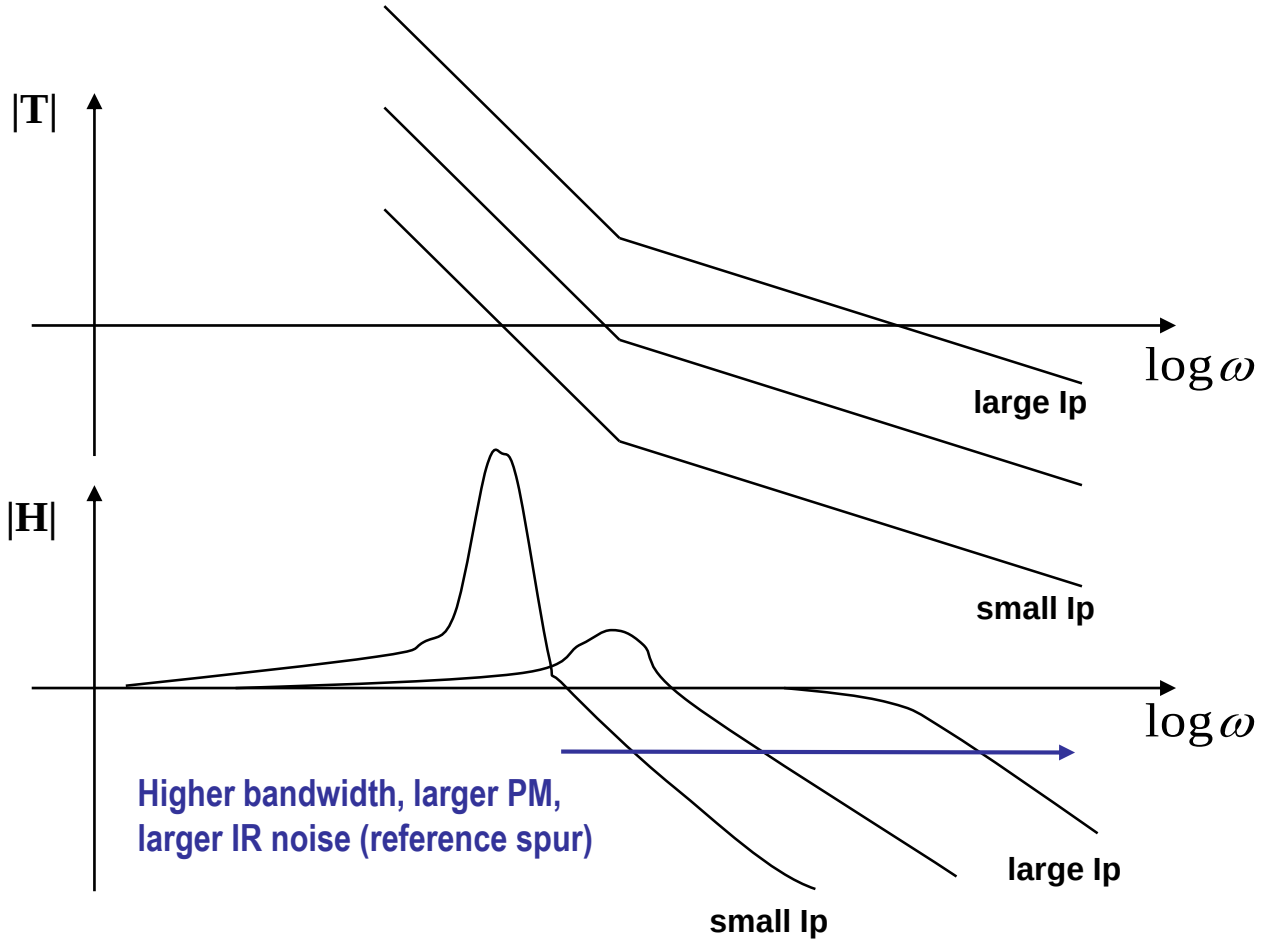
Tuning Design Parameters

- Tuning of C



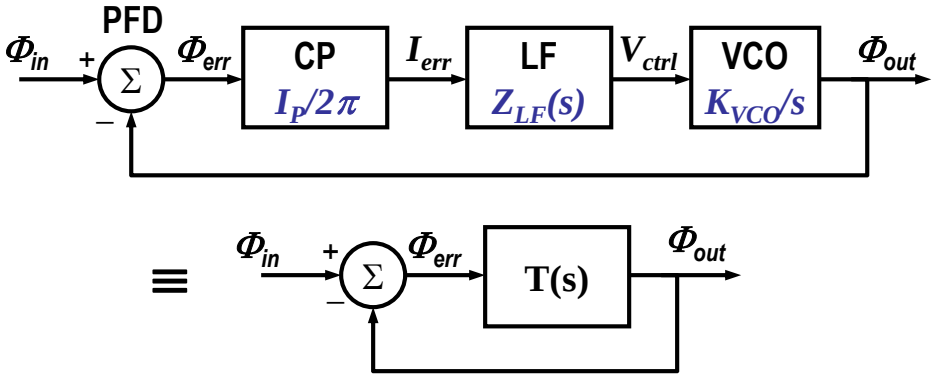
Tuning Design Parameters

- Tuning of I_P



PLL Linear Model

- PLL linear model in s-domain



- Open loop transfer function T(s) = Φ_{out}/Φ_{err}

$$T(s)=\frac{I_P}{2\pi}\cdot Z_{LF}(s)\cdot\frac{K_{VCO}}{s}$$

- Closed loop transfer function H(s) = Φ_{out}/Φ_{in}

$$H(s)=\frac{T(s)}{1+T(s)}$$

PLL Transfer Function of 2nd-order PLL

- Closed loop transfer function H(s)

$$H(s) = \frac{s\frac{I_p K_{VCO} R}{2\pi} + \frac{I_p K_{VCO}}{2\pi C}}{s^2 + s\frac{I_p K_{VCO} R}{2\pi} + \frac{I_p K_{VCO}}{2\pi C}} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C}} \qquad \zeta = \frac{\sqrt{I_p K_{VCO} C}R}{2\sqrt{2\pi}}$$

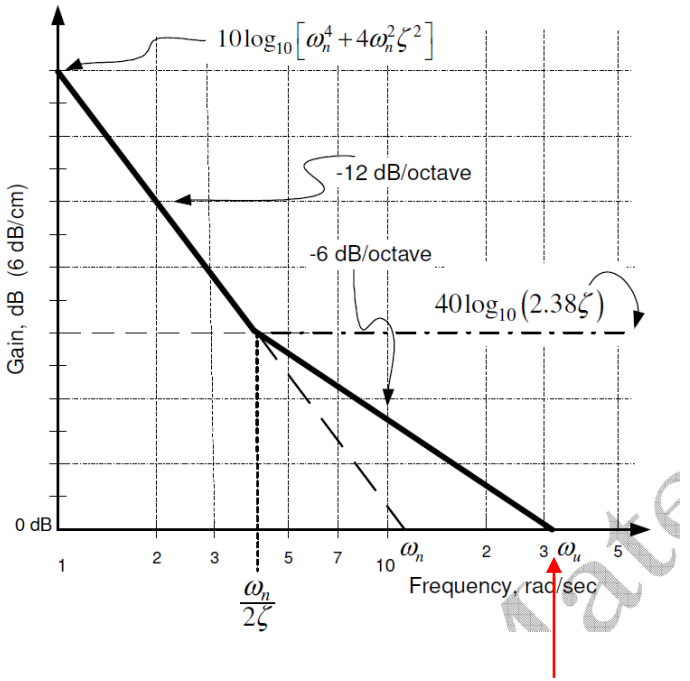
Open-loop Transfer Function

- **Open-loop unit gain frequency**
  ≅ Closed-loop bandwidth

$$\omega_u = \omega_n \sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}}$$

$$\cong \; 2\zeta\omega_n$$

- **Phase Margin?**



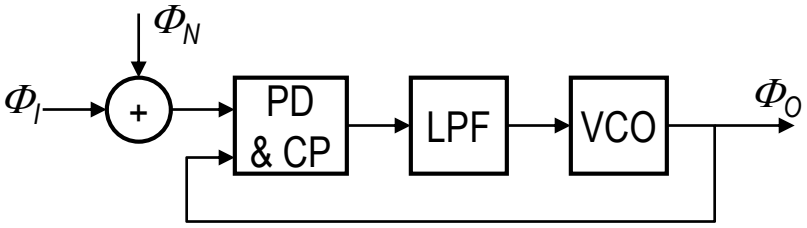
[Crawford - Advanced Phase-Lock Techniques]

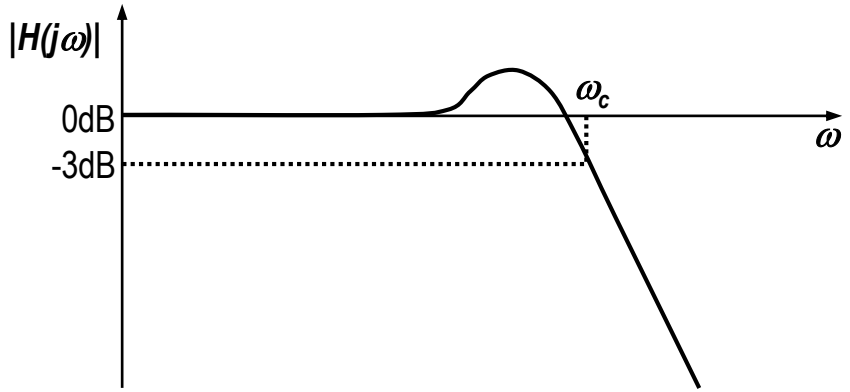
PLL Jitter

- All the loop components may contribute jitter
  - ✓ PLL output jitter can be reduced through proper bandwidth selection
- Two important cases
  - ✓ When input noise is dominant
  - ✓ When VCO noise is dominant

PLL Jitter Transfer

- Input noise
  - ✓ $\Phi_O/\Phi_N = H(s) \rightarrow$ Low pass filter!!
  - ✓ Bandwidth should be lower for noise rejection





Closed-Loop Transfer Function

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

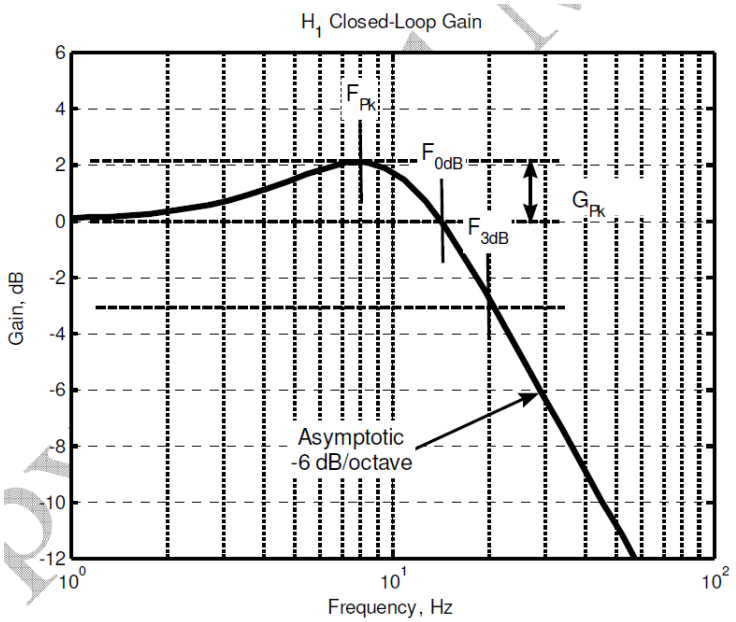
$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C}} \qquad \zeta = \frac{\sqrt{I_p K_{VCO} C}R}{2\sqrt{2\pi}}$$

$$F_{Pk} = \frac{1}{2\pi}\frac{\omega_n}{2\zeta}\sqrt{\sqrt{1+8\zeta^2}-1}\ \text{Hz}$$

$$F_{0dB} = \frac{1}{2\pi}\sqrt{2}\omega_n\ \text{Hz}$$

$$F_{3dB} = \frac{\omega_n}{2\pi}\sqrt{1+2\zeta^2+2\sqrt{\zeta^4+\zeta^2+\frac{1}{2}}}\ \text{Hz}$$

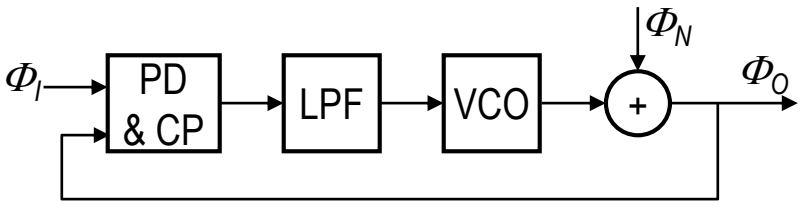
$$G_{Pk} = 10\log_{10}\left(\frac{8\zeta^4}{8\zeta^4-4\zeta^2-1+\sqrt{1+8\zeta^2}}\right)\text{dB}$$

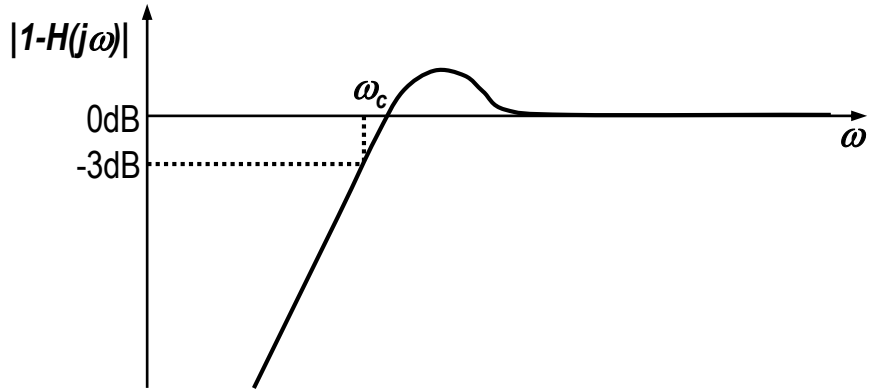


[Crawford - Advanced Phase-Lock Techniques]

PLL Jitter Transfer

- VCO noise
  - ✓ $\Phi_O/\Phi_N = 1 - H(s) \rightarrow$ High pass filter!!
  - ✓ Bandwidth should be higher for noise rejection
  - ✓ Same ω_c





Closed-Loop Transfer Function

- **VCO jitter transfer function**

$$H_2(s) = 1 - H(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

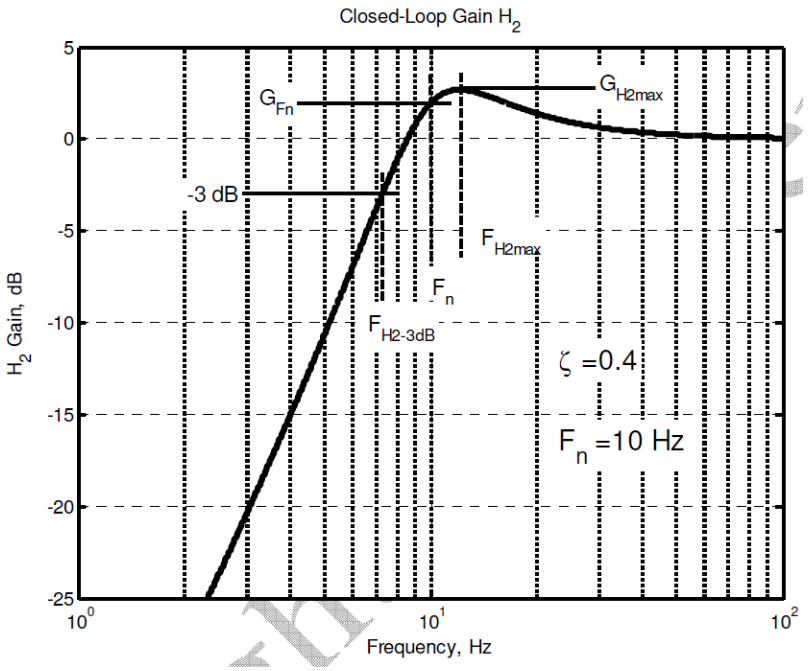
$$F_{H_2-3dB} = \frac{\omega_n}{2\pi}\left[2\zeta^2 - 1 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right]^{1/2}$$

$$G_{H_2-\omega_n} = -10\log_{10}\left(4\zeta^2\right)$$

- **If** $\zeta < \frac{\sqrt{2}}{2}$ **, peaking occurs**

$$F_{H_2-\max} = \frac{1}{2\pi}\frac{\omega_n}{\sqrt{1-2\zeta^2}}$$

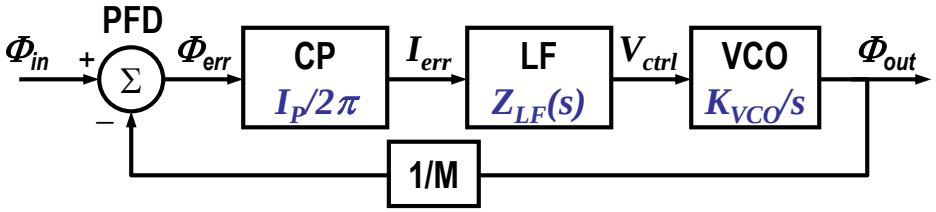
$$G_{H_2-\max} = -10\log_{10}\left(4\zeta^2 - 4\zeta^4\right)$$



[Crawford - Advanced Phase-Lock Techniques]

PLL Linear Model with FB Divider

- PLL linear model in s-domain



- Open loop transfer function T(s) = Φ_{out}/Φ_{err}

$$T(s) = \frac{I_P}{2\pi} \cdot Z_{LF}(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{M}$$

- Closed loop transfer function H(s) = Φ_{out}/Φ_{in}

$$H(s) = M \cdot \frac{T(s)}{1+T(s)}$$

All the stability analysis is on the modified T(s)
Loop gain is reduced by M
Phase is multiplied by M – Frequency as well

PLL Design Procedure

- Determine PLL spec
  - ✓ Operation range, bandwidth, power budget, jitter peaking …
- Design VCO
  - ✓ Should have the proper operation range over PVT variation
  - ✓ Determine K_{VCO}
- Design loop filter
  - ✓ Determine proper pole-zero location
  - ✓ Determine RC values – Should be practical (R=100 ~ 10kΩ, C_{max} = 200pF)
- Determine charge pump current
  - ✓ PM should be considered – More than 60°
  - ✓ Several μA ~ 1mA

Topics in IC Design

2.2 Fractional-N FS

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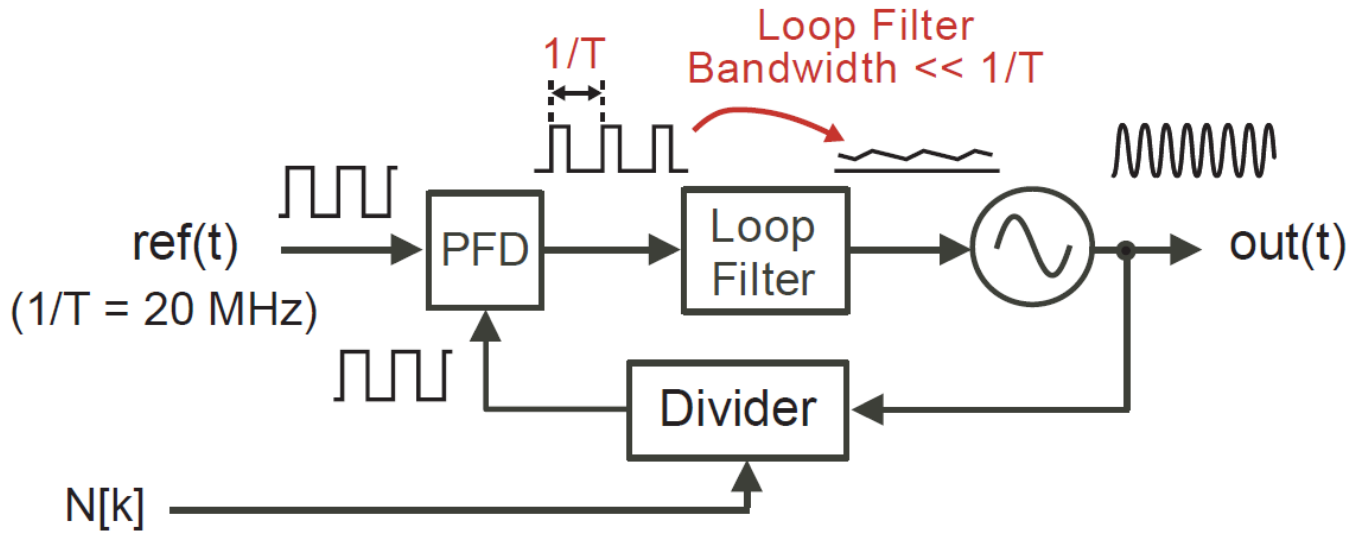
Seoul National University
2020 Fall

Issues

- Background
- Architecture
- Spurious Tone
- SDM and Dithering
- Quantization Noise Analysis

Background

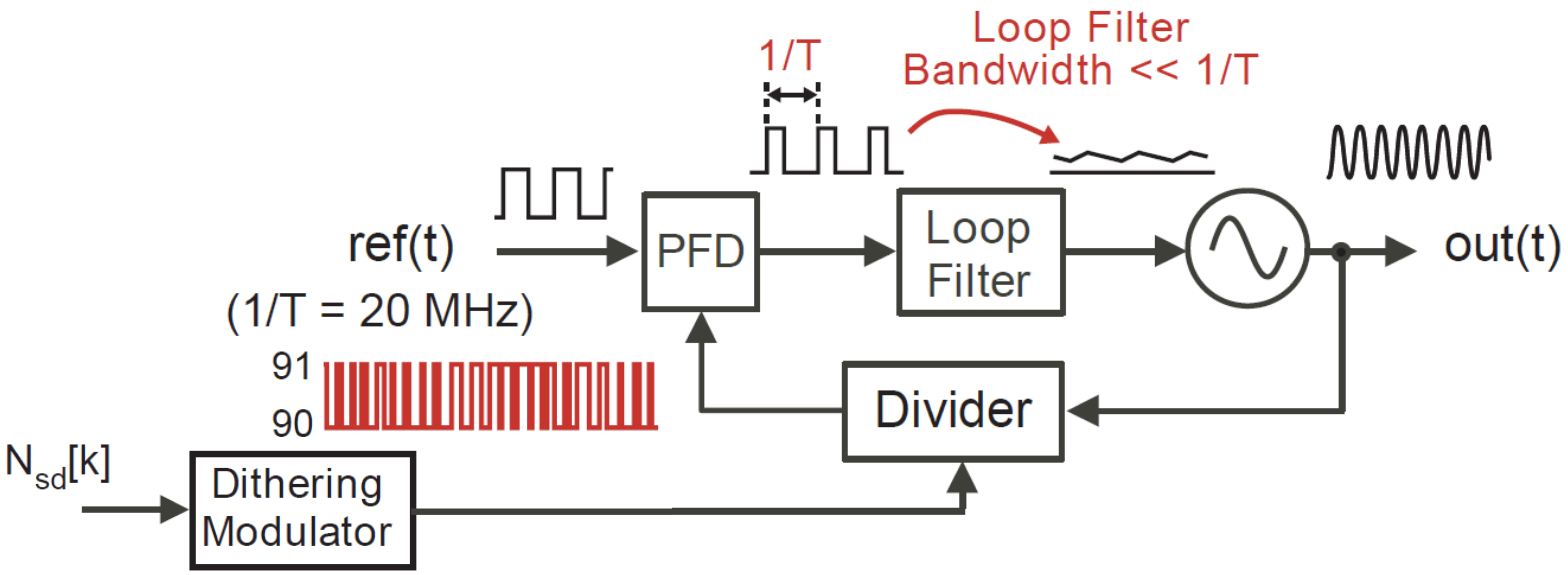
- Integer PLL gives integer * f_{REF}
- Frequency resolution = $f_{REF,}$ too coarse.
- What if we want to have 1 MHz resolution when f_{REF}=20 MHz?
- Fractional divide factor is required.



[MIT Courseware: Perrott]

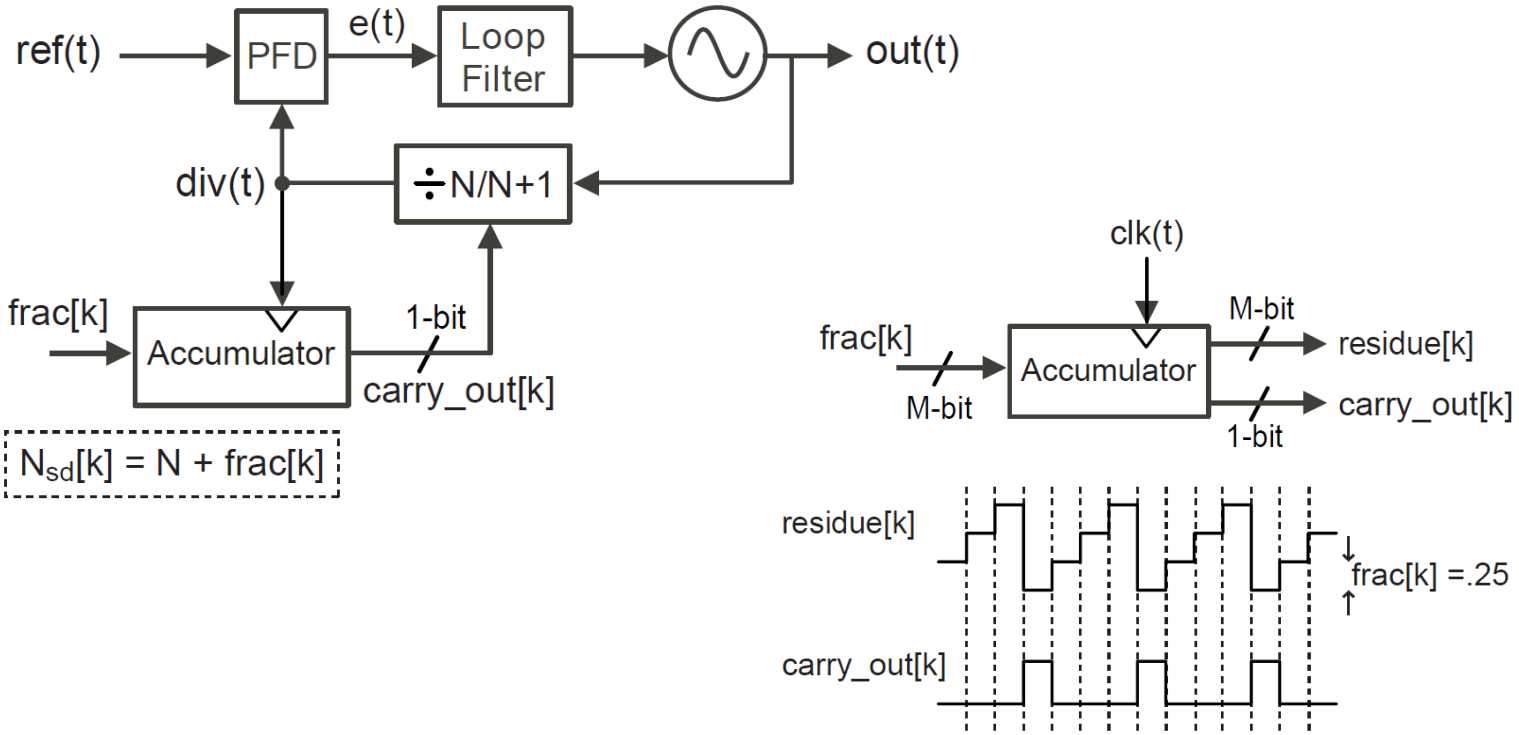
Fractional-N PLL Architecture

- Alternating divide factors are used



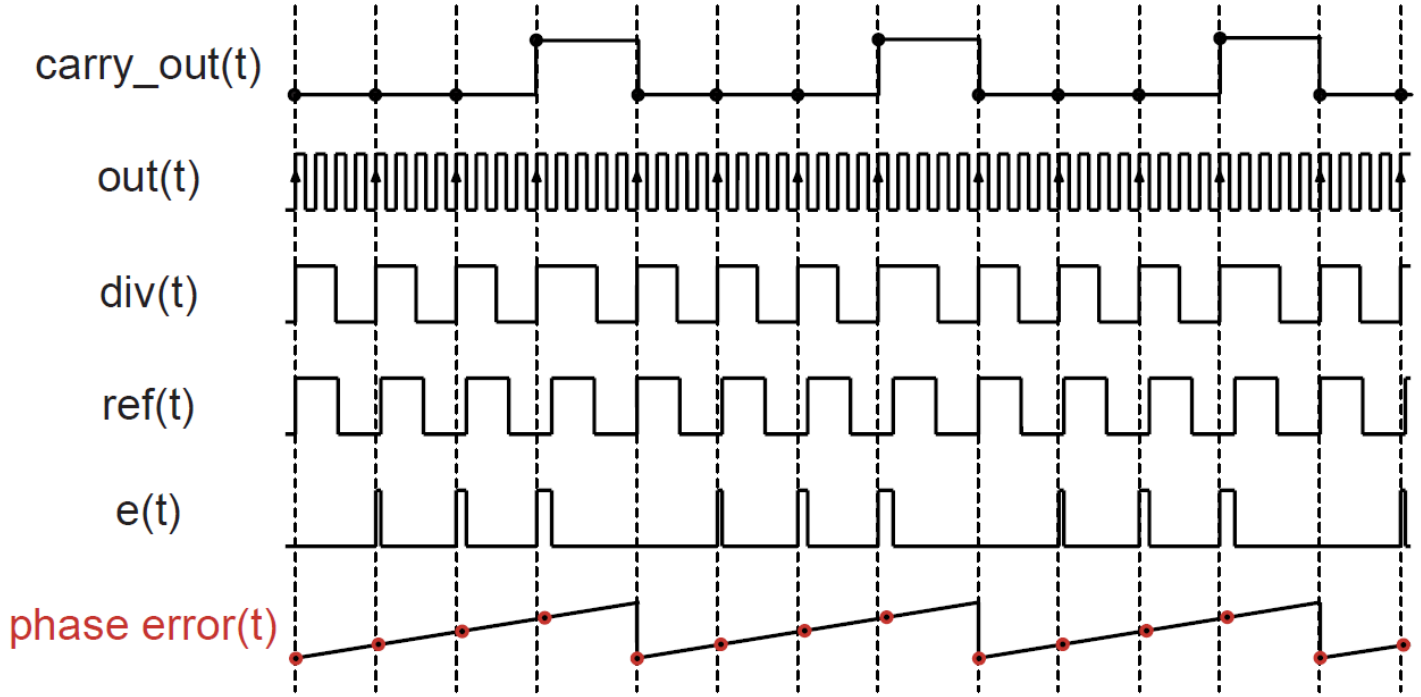
Fractional-N PLL Architecture

- Accumulator is used for generating alternating divide factors
- Accumulator adds a fraction every cycle and carry overflow is the output



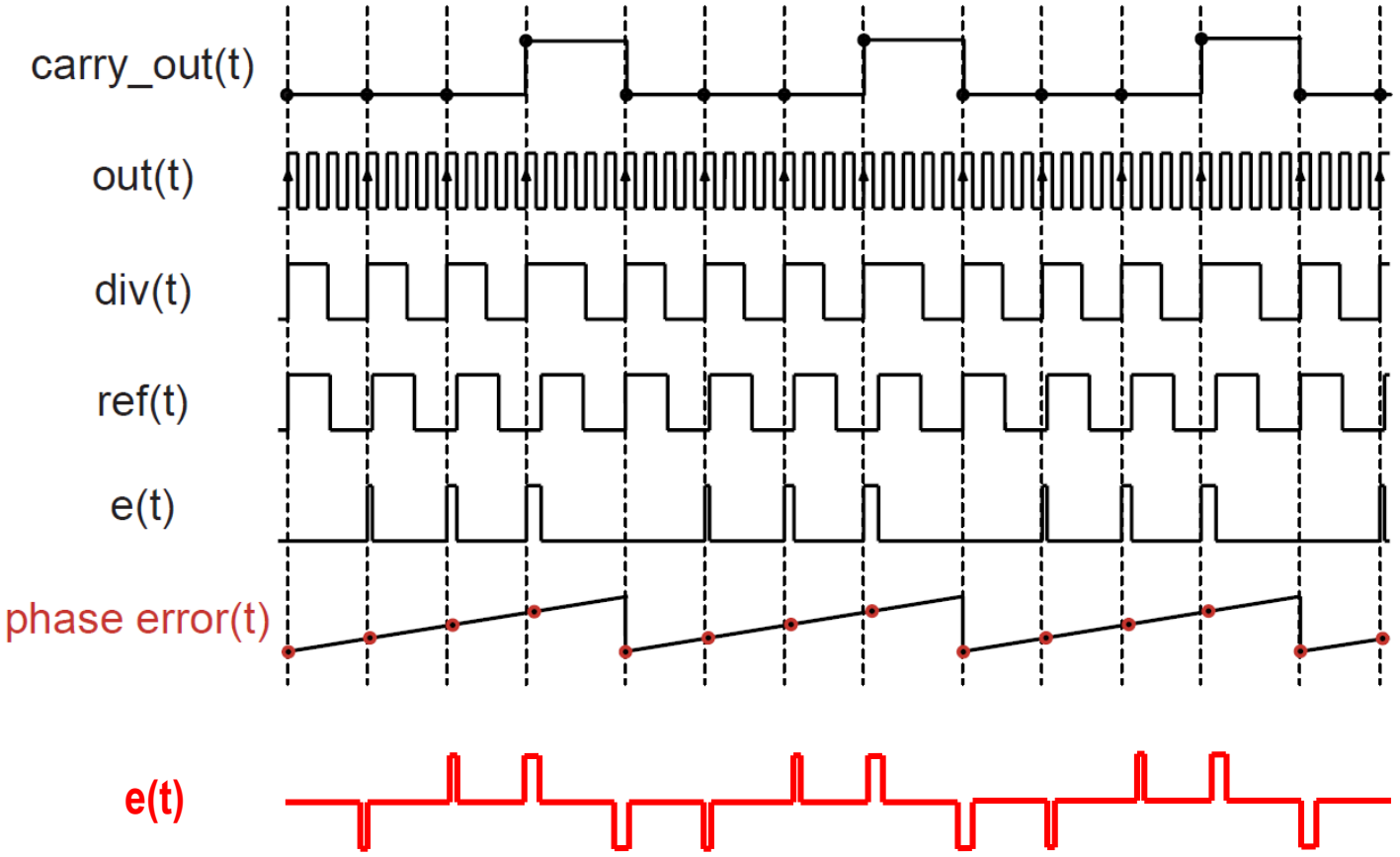
Timing Diagram

- For fractional divide of 4.25, divide value = 4, 3 times and divide value = 5, 1 time.



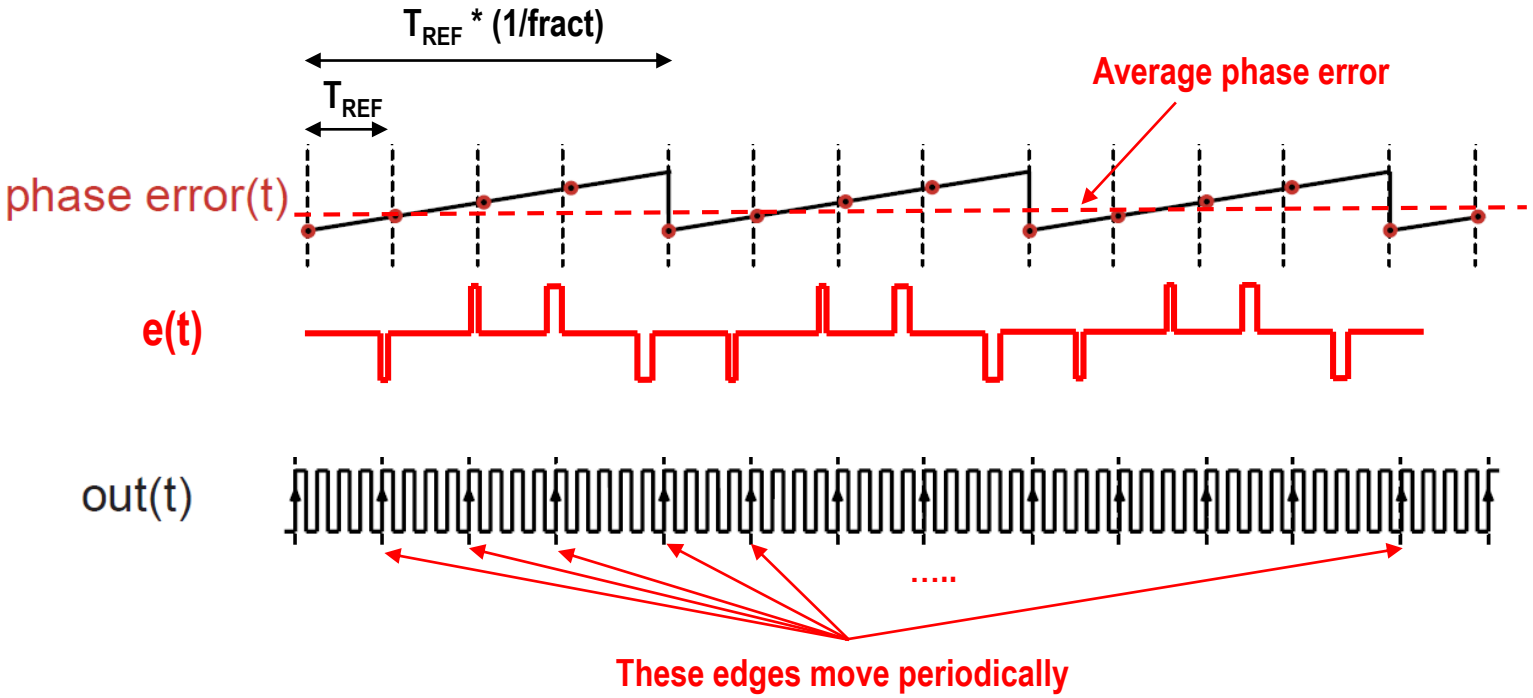
Timing Diagram (corrected)

- In fact, in steady state, average value of e(t)=0.
- All signals except ref(t) must be shifted.



Spurious Tone

- Periodic phase error appears if averaging is not perfect.
- The spurious tone frequency is about f_{REF} and f_{REF} * fract

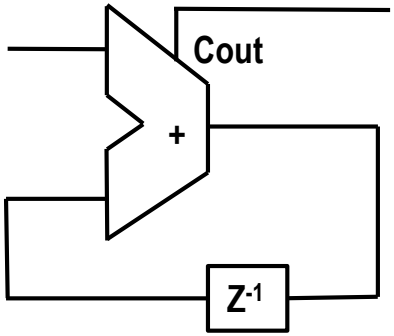


Reducing Spurious Tone

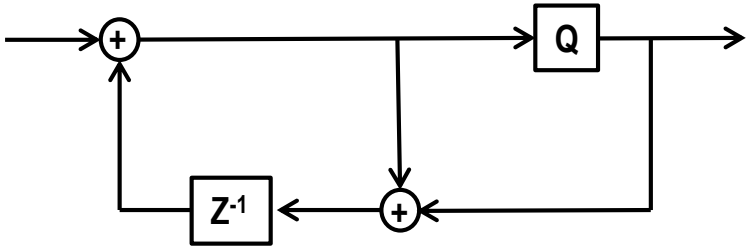
- Instead of periodically alternating at 3:1 ratio, dither the ratio at random, with long-term average of 3:1.
- Fractional spur is spread (f_{REF} * fract)
- How? Use the Sigma-Delta Modulator
- Accumulator is the 1st order SDM
  - Output (carry) is periodically generated, no dithering (1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 …)
- What is the 2nd order SDM?
  - Output is dithered. (1 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0 0 1 …)

1st Order SDM

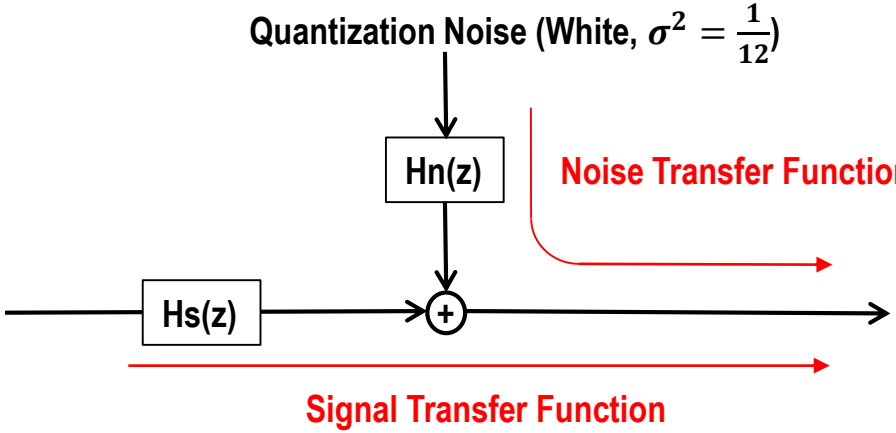
- **Same as accumulator**



Digital Implementation

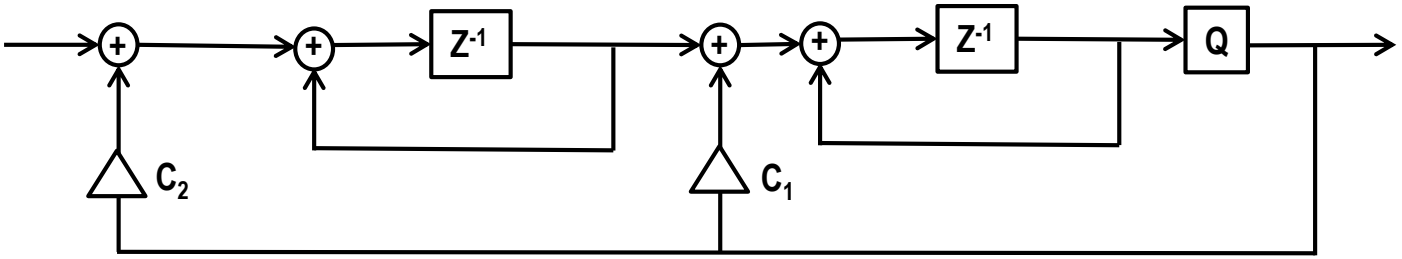


1st order DSM Model



2nd Order SDM

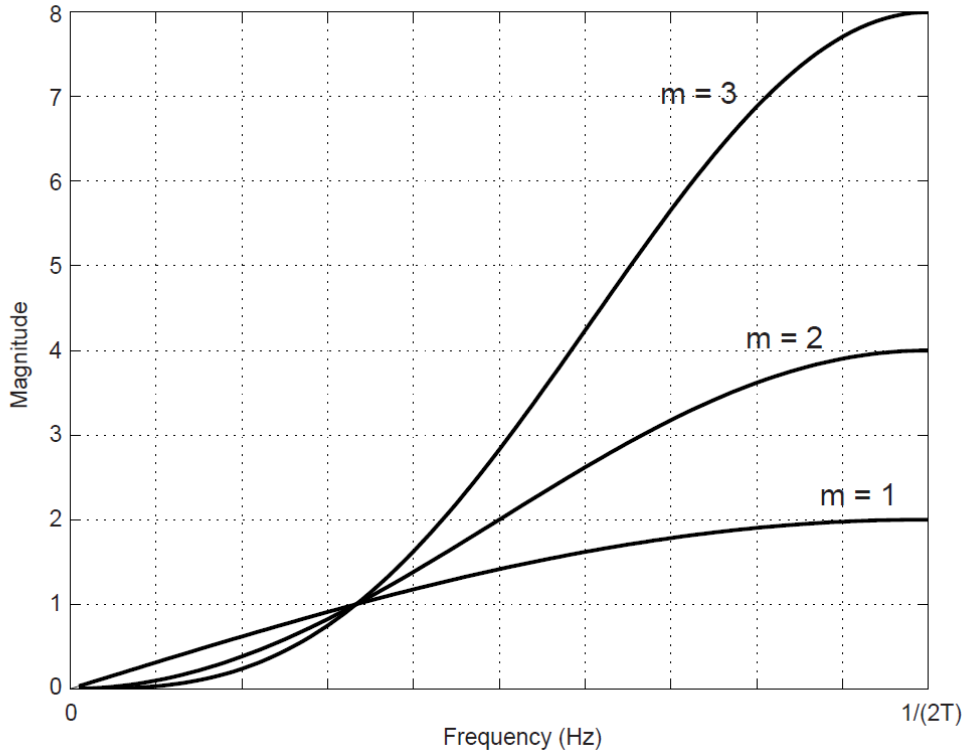
- **Noise is shaped**
- **Dithering added**



2nd order DSM Model

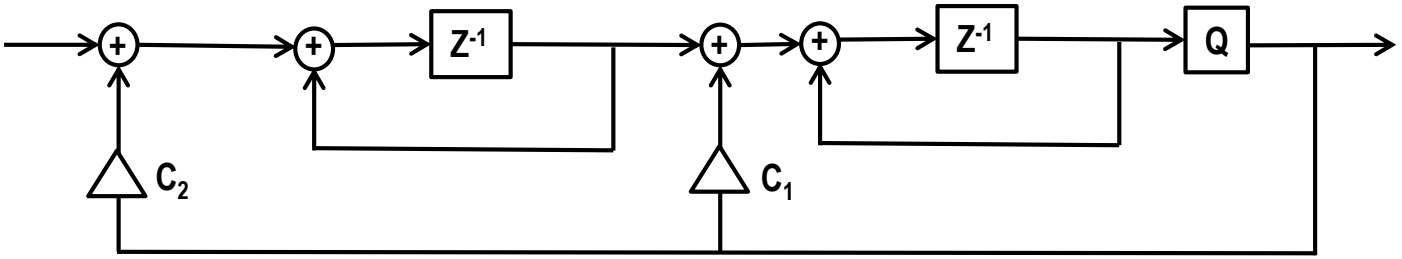
Noise Shaping

- **Signal Transfer function Hs(z) = 1**
- **Noise Transfer Function $Hn(z)=(1-z^{-1})^m$, m = order of DSM**



2nd Order SDM

- **Noise is shaped**
- **Dithering added**

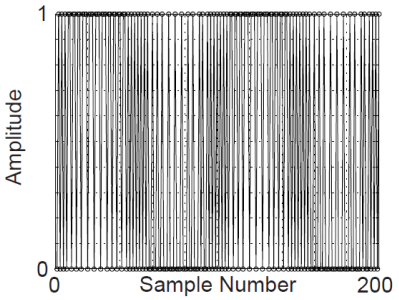


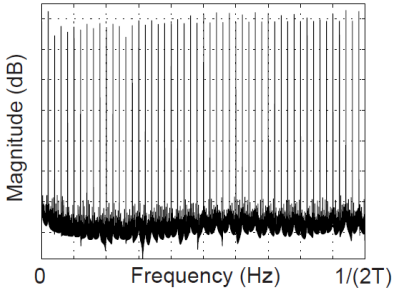
2nd order DSM Model

DSM Outputs

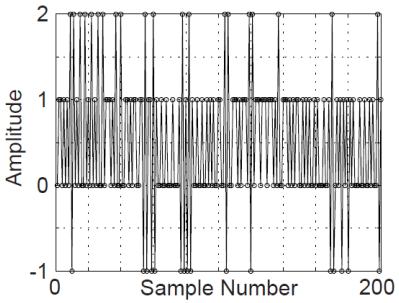
- **For sinusoidal input** $x[k] = 0.5 + 0.25\sin\left(\frac{2\pi}{100}k\right)$

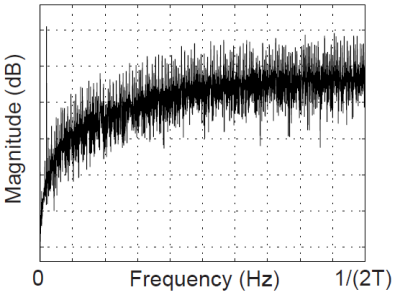
1st order



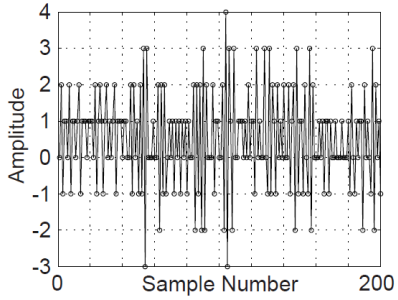


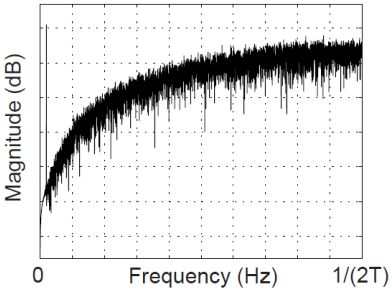
2nd order





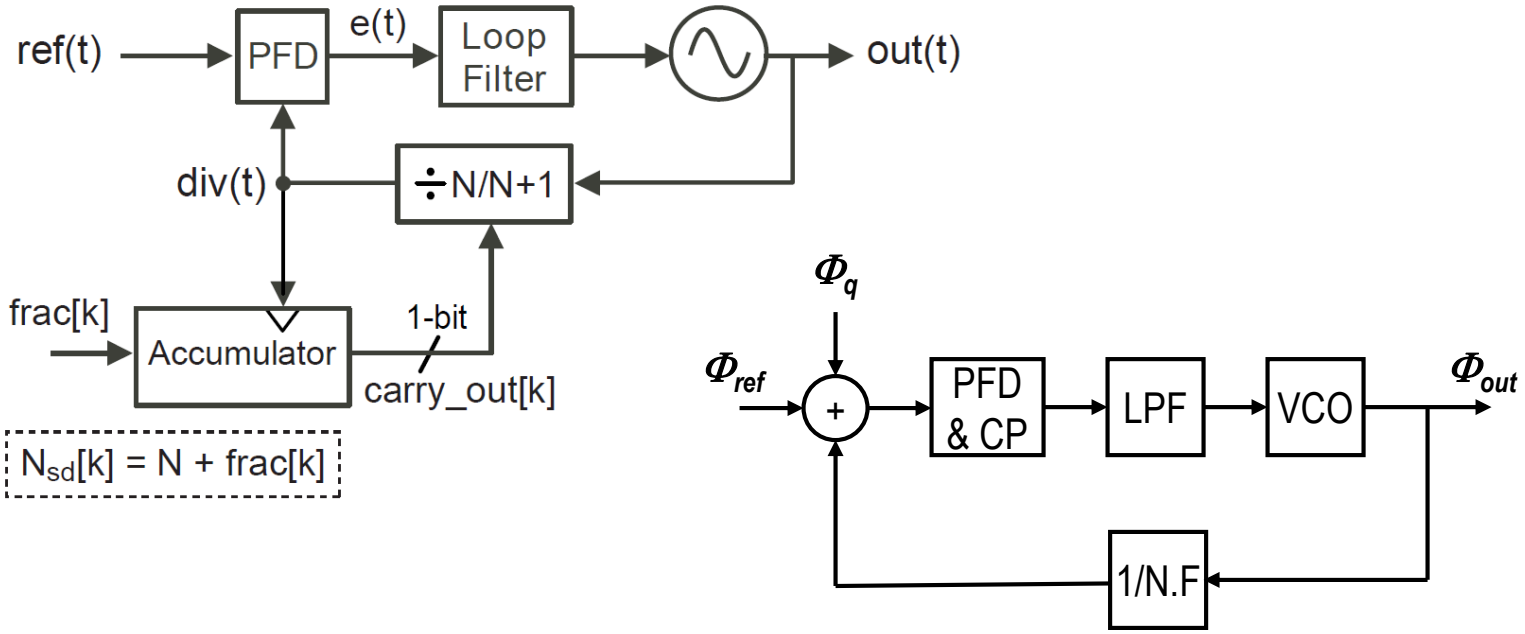
3rd order





Quantization Noise in F-N FS

- **Phase Noise injected at input of PFD**

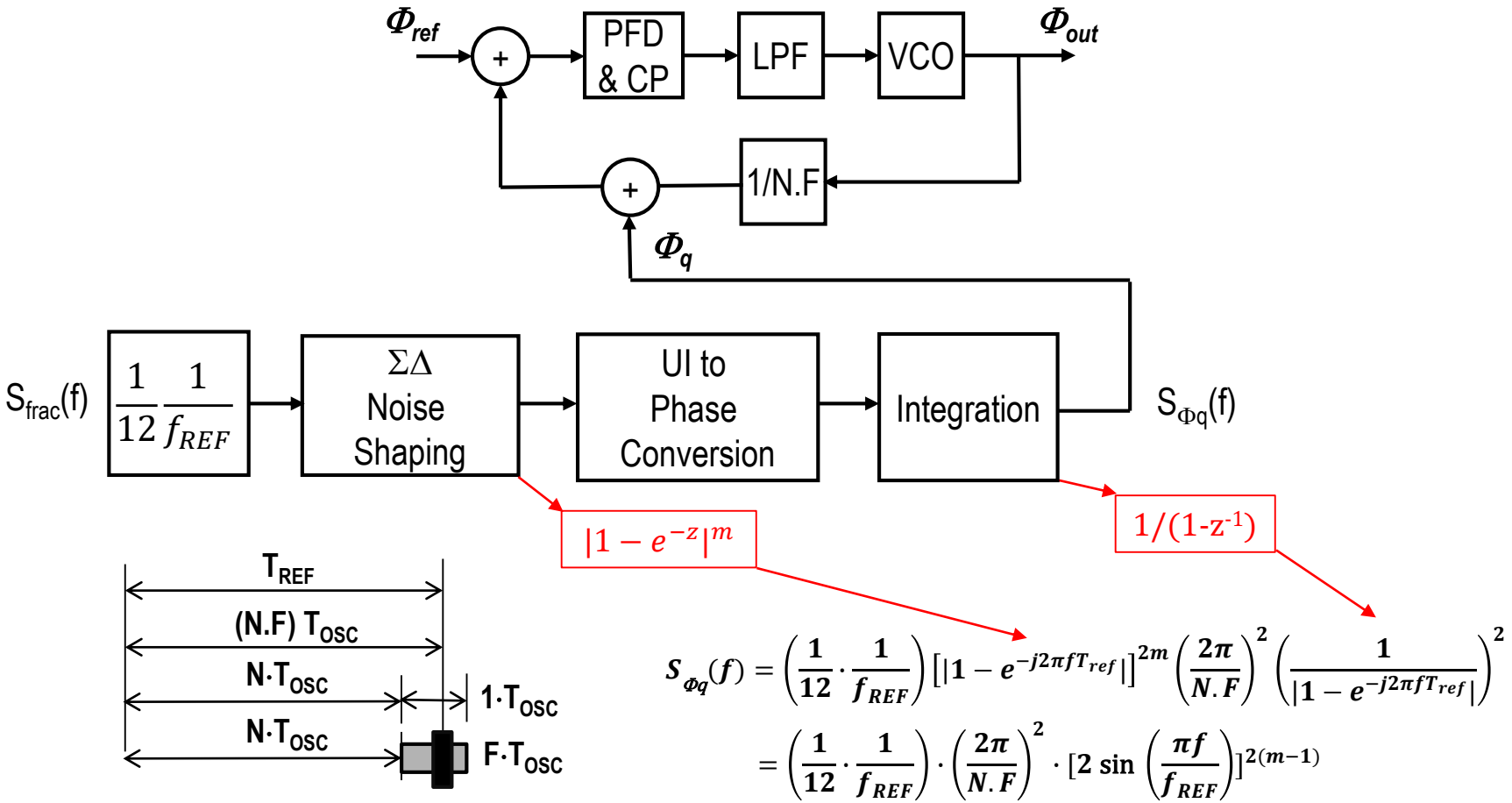


$$S_q(f) = \frac{1}{12} \cdot \frac{(2\pi)^2}{(N.F)^2 \cdot fR_{EF}} \cdot [2 \sin\left(\frac{\pi f}{f_{REF}}\right)]^{2(m-1)}$$

$$S_{qOUT}(f) = S_q(f) \cdot |\, \mathrm{H}(j2\pi f)|^2$$

Phase Noise in Fractional-N FS

- Quantization noise is shaped.



$$S_{\Phi q}(f) = \left(\frac{1}{12}\cdot\frac{1}{f_{REF}}\right)\left[|1-e^{-j2\pi f T_{ref}}|\right]^{2m}\left(\frac{2\pi}{N.F}\right)^2\left(\frac{1}{|1-e^{-j2\pi f T_{ref}}|}\right)^2$$

$$= \left(\frac{1}{12}\cdot\frac{1}{f_{REF}}\right)\cdot\left(\frac{2\pi}{N.F}\right)^2\cdot\left[2\sin\left(\frac{\pi f}{f_{REF}}\right)\right]^{2(m-1)}$$

Topics in IC Design

2.3. Spread-Spectrum Frequency Synthesizer

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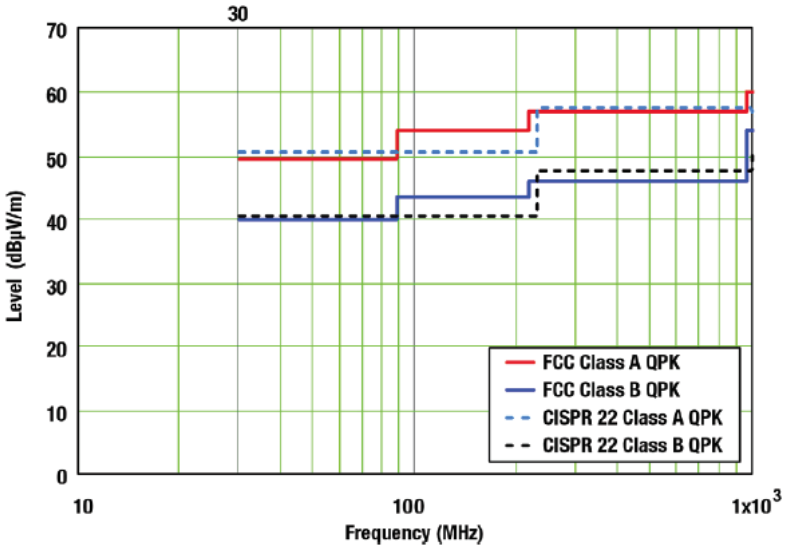
School of Electrical and Computer Engineering
Seoul National University
2020 Fall

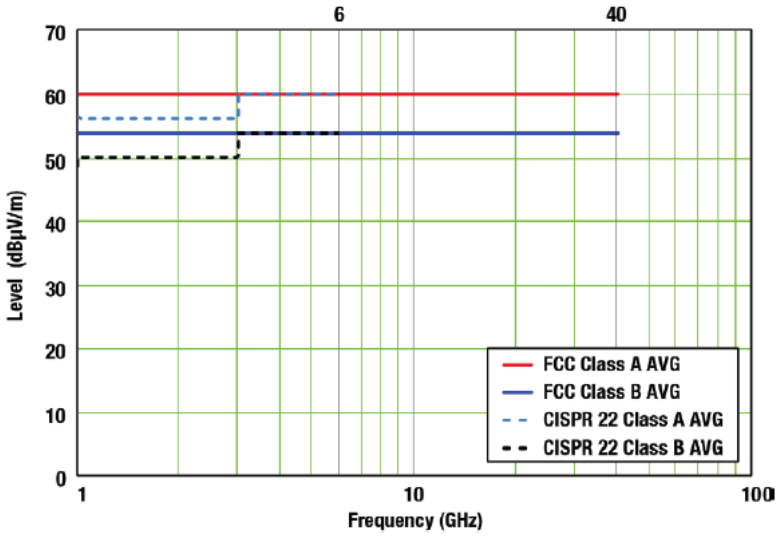
Outline

- EMI issues
- Frequency Spectrum
- Architectures

Background

- Electromagnetic Interference
- Many standards to comply
  - FCC Class A, Class B
  - CISPR

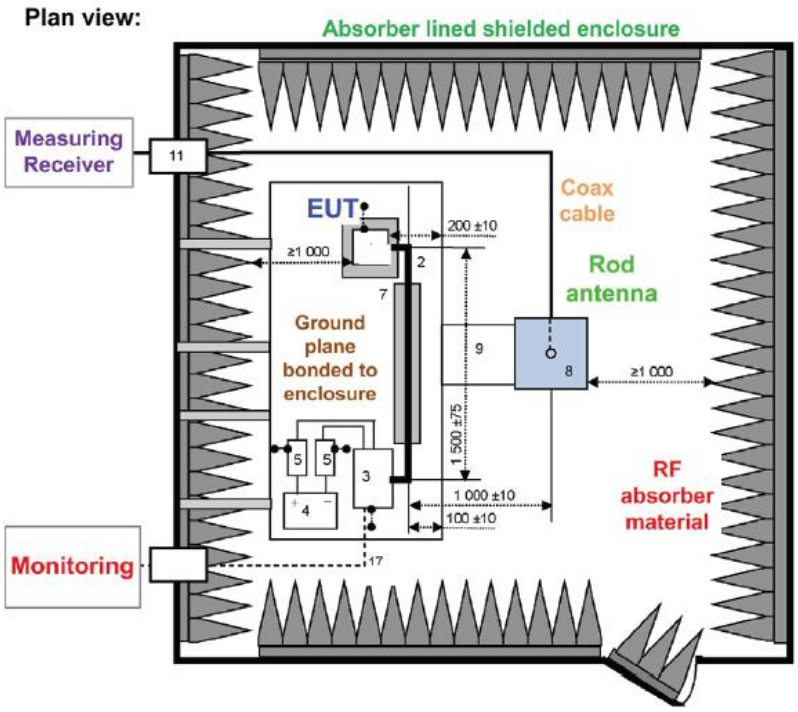


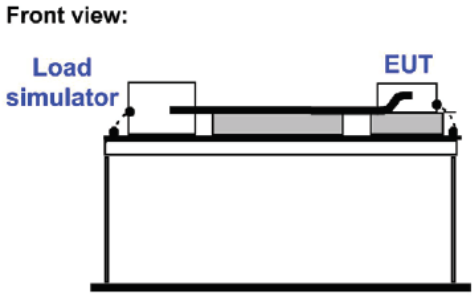


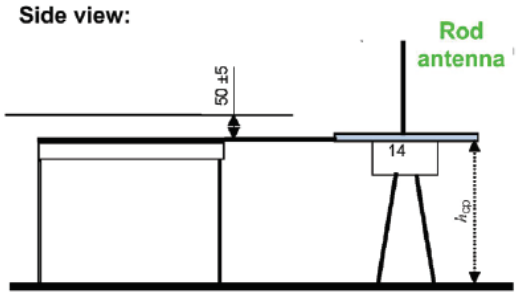
[TI: Overview of Radiated EMI]

Background

- Shield Room Test



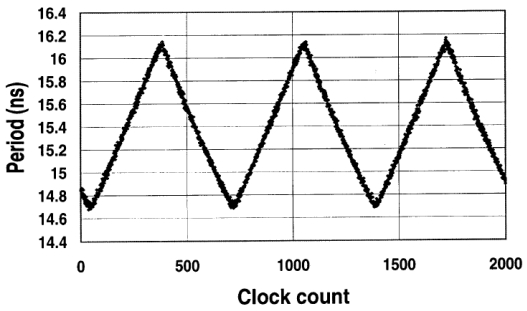


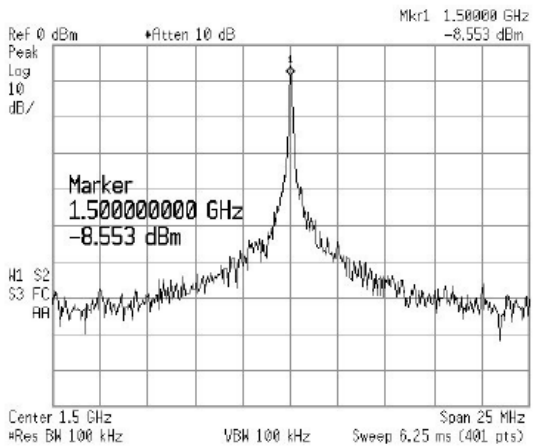


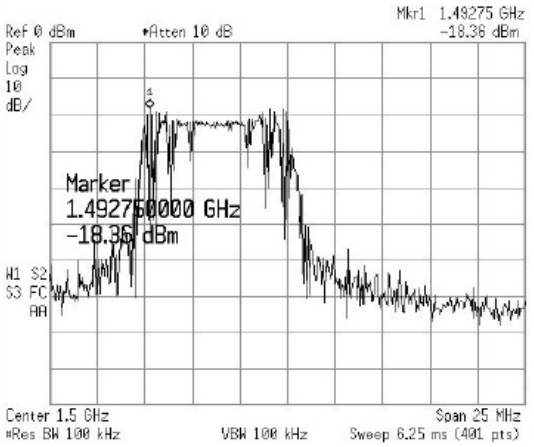
[TI: Overview of Radiated EMI]

EMI Reduction Techniques

- Shielding
- Edge rate reduction
- Low voltage differential signaling
- Spread-spectrum clocking
  - FM modulation of clock with triangular/Hersey-Kiss waveform
  - 30-33kHz (inaudible to human ear)
  - Down spread not to shorten clock period

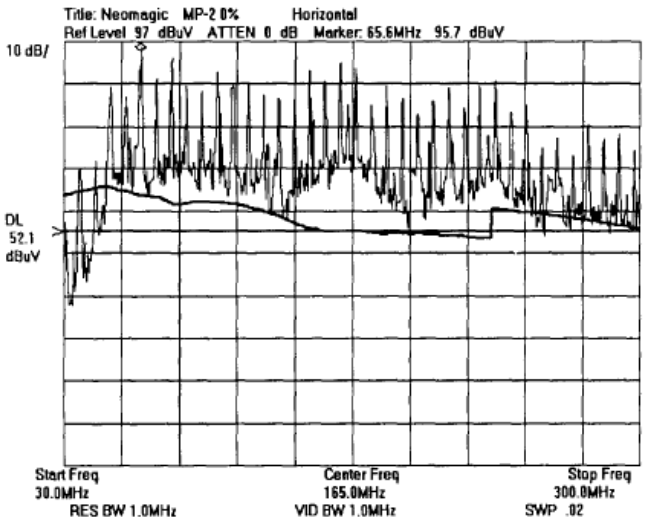




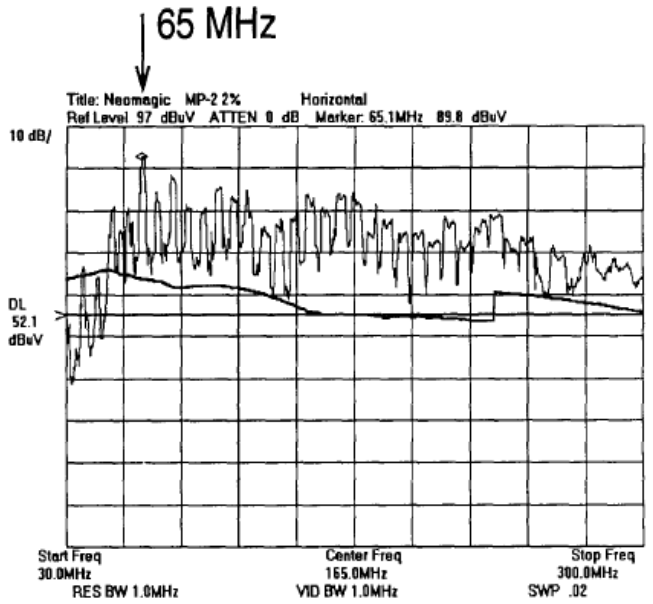


Spectral Peak Reduction

- Spectral peak is reduced by 5.9dB



unmodulated

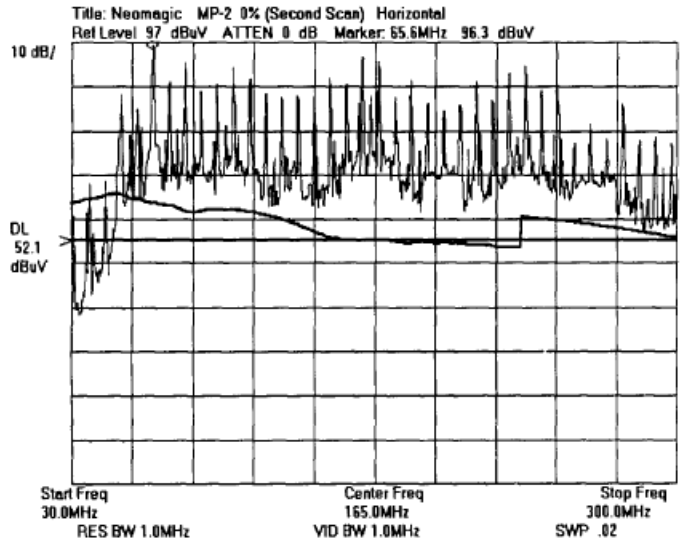


+/- 1 % modulation

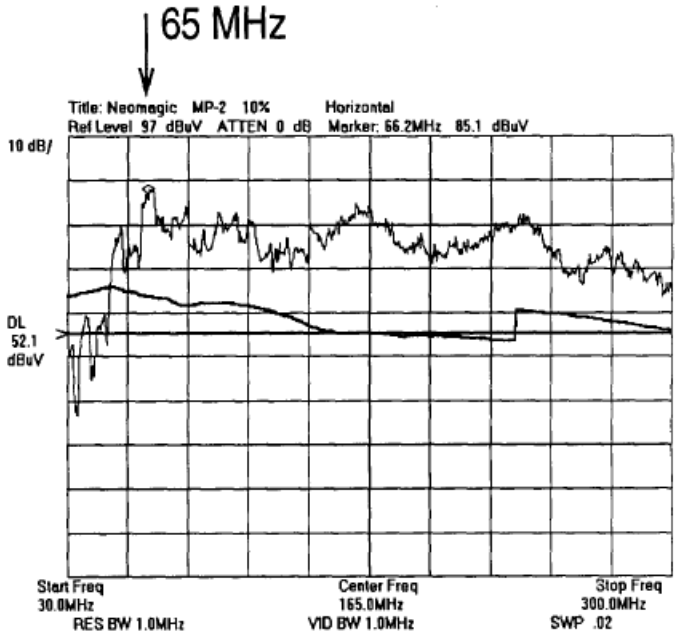
[Li: ISSCC 1999: Dual-Loop SSCG]

Spectral Peak Reduction

- Spectral peak is reduced by 11.2dB



unmodulated

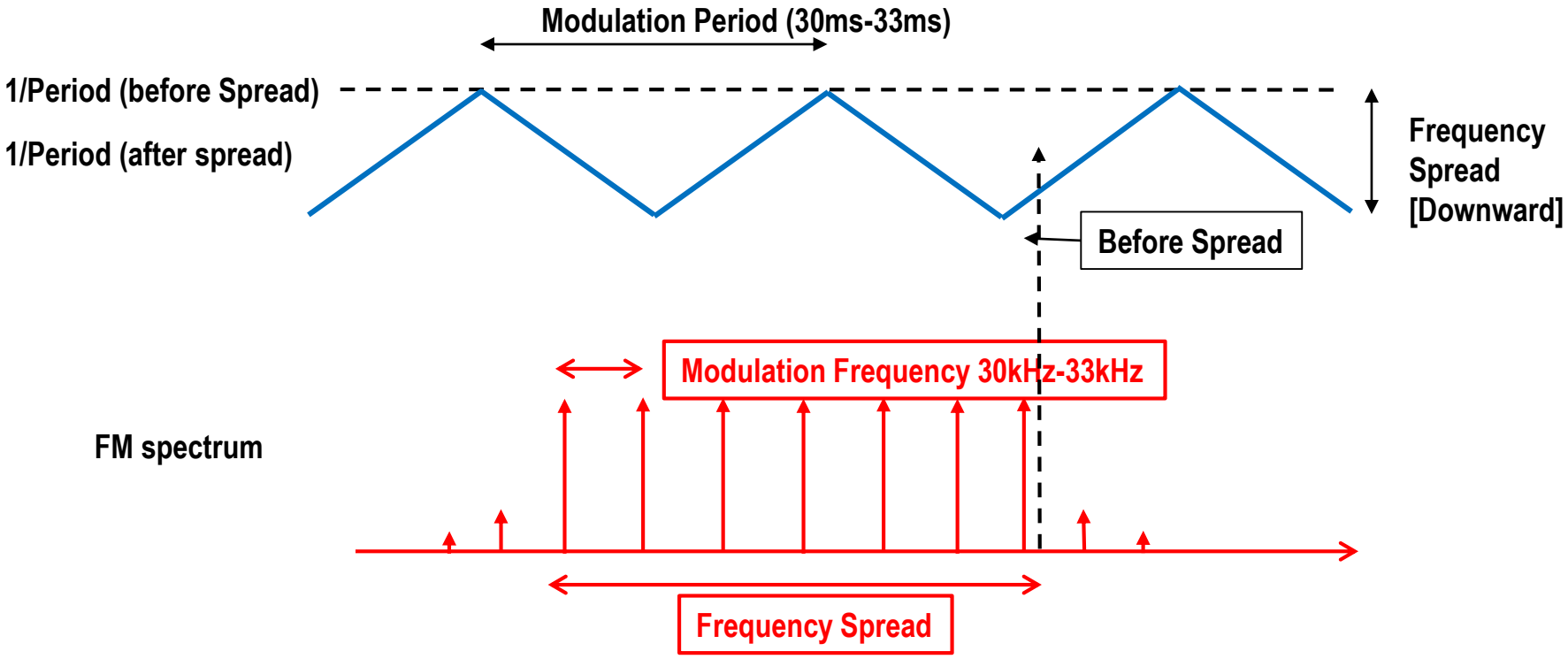


+/- 5 % modulation

[Li: ISSCC 1999: Dual-Loop SSCG]

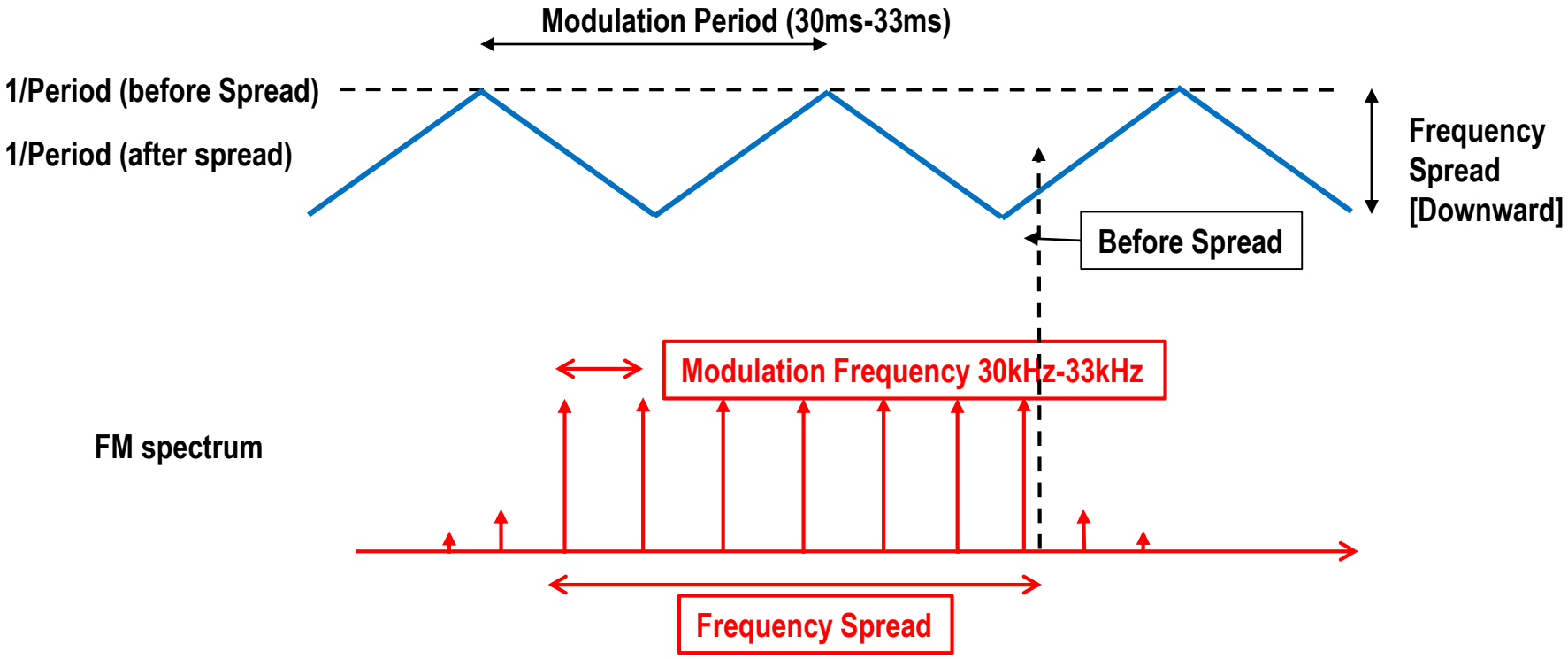
Spectral Peak Reduction

- Peak reduction factor
- 10 log [(Frequency Spread)/(Resolution Bandwidth, 100kHz)]



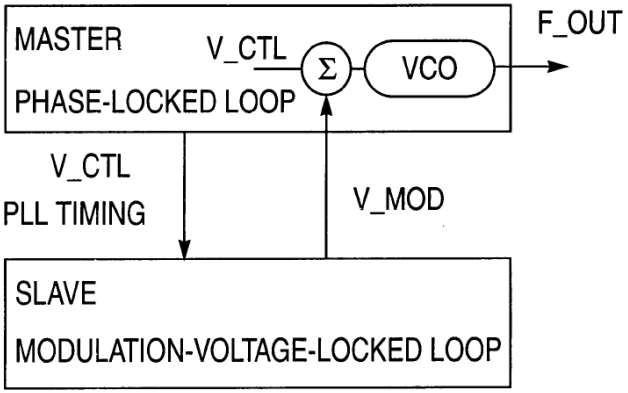
Spectral Peak Reduction

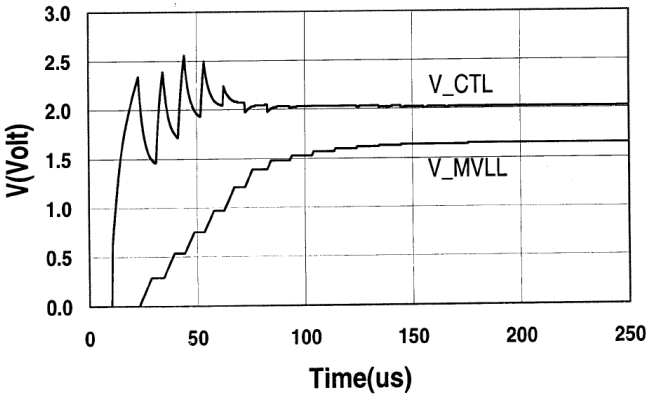
- Peak EMI reduction [dB] =
  10 log [(Frequency Spread)/(Resolution Bandwidth, 100kHz)]

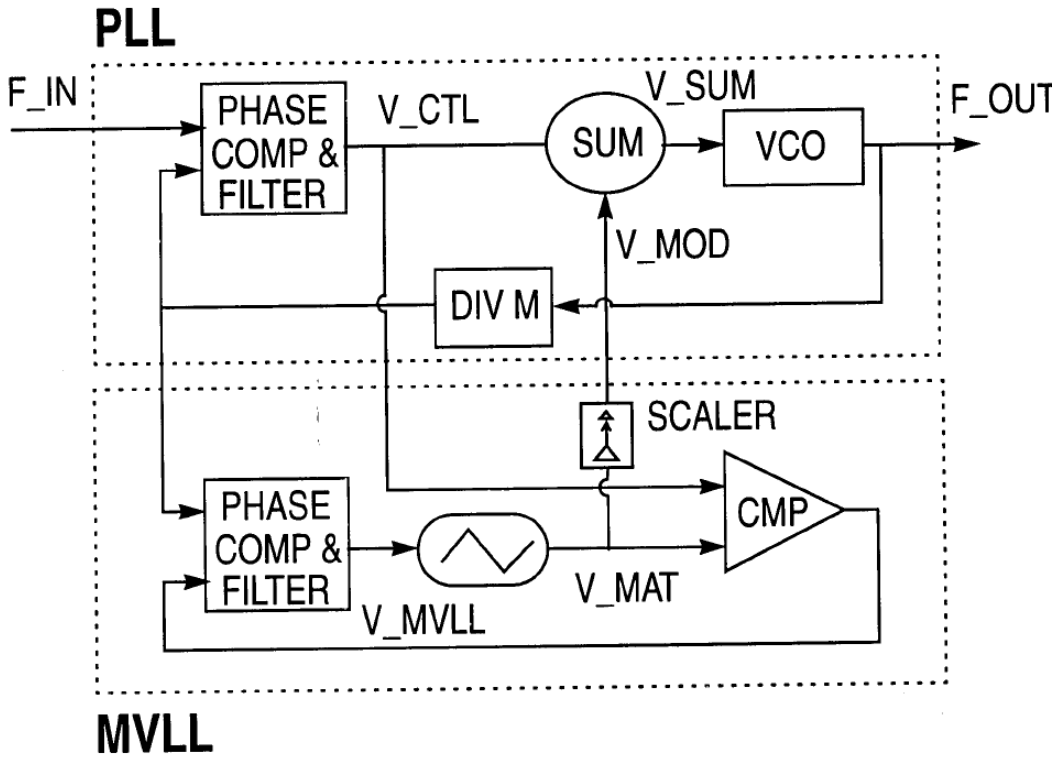


SSCG Architectures

- **Dual Loop**



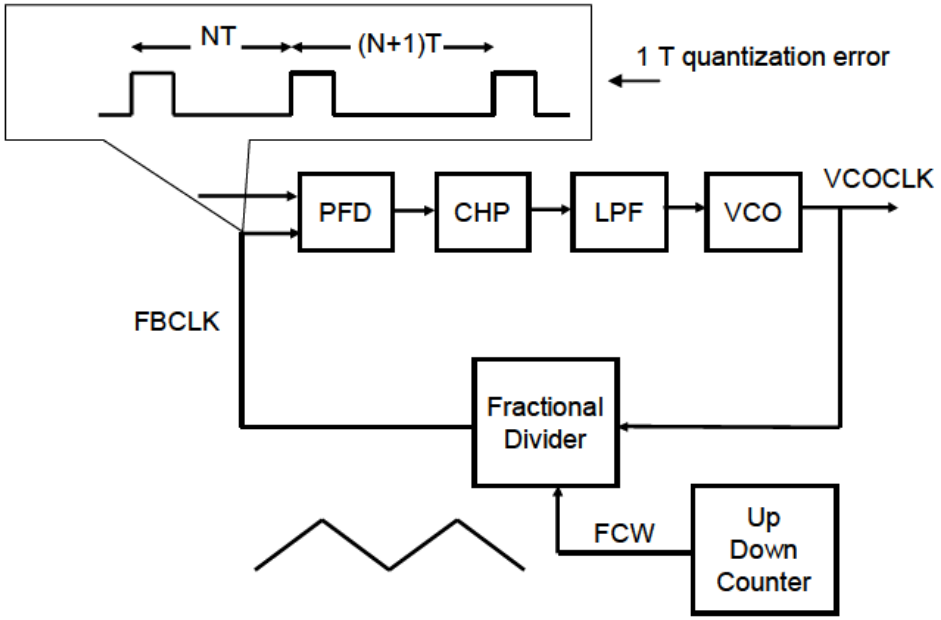




[Li: ISSCC 1999: Dual-Loop SSCG]

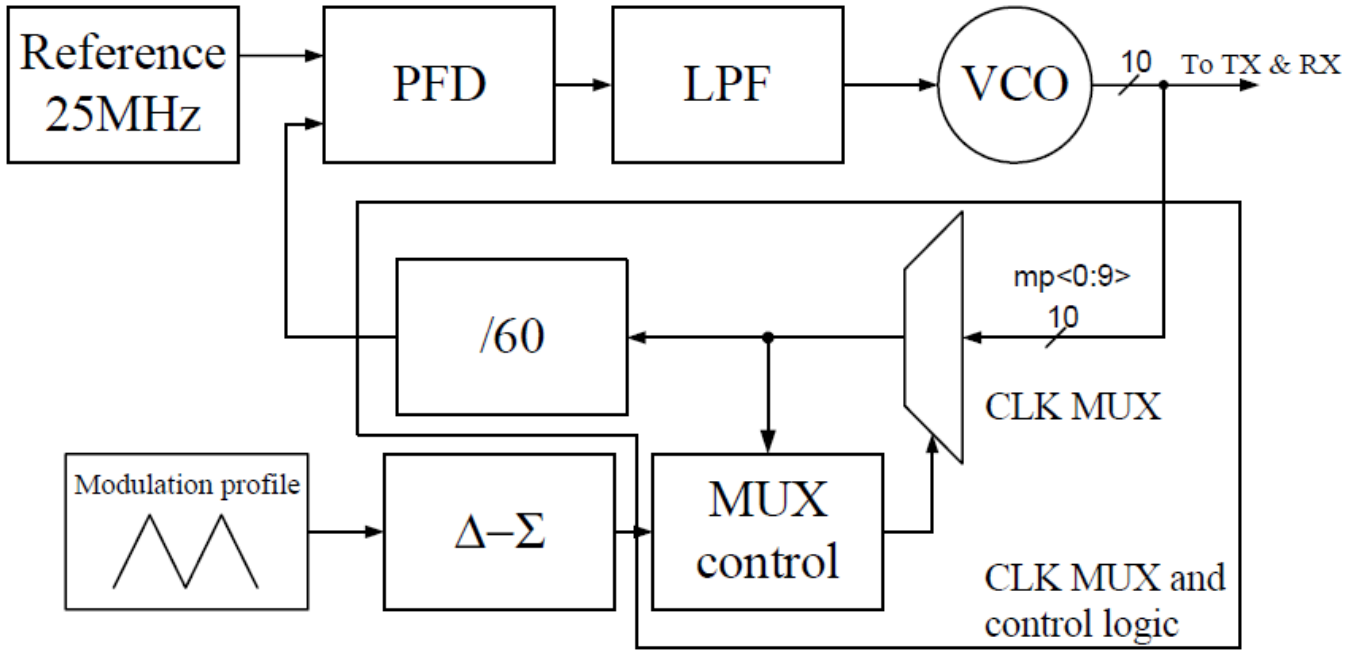
SSCG Architectures

- Integer feedback factor modulation
- Conflict:
  - Low bandwidth to filter quantization noise
  - Harmonic tones of the triangular will be filtered



SSCG Architectures

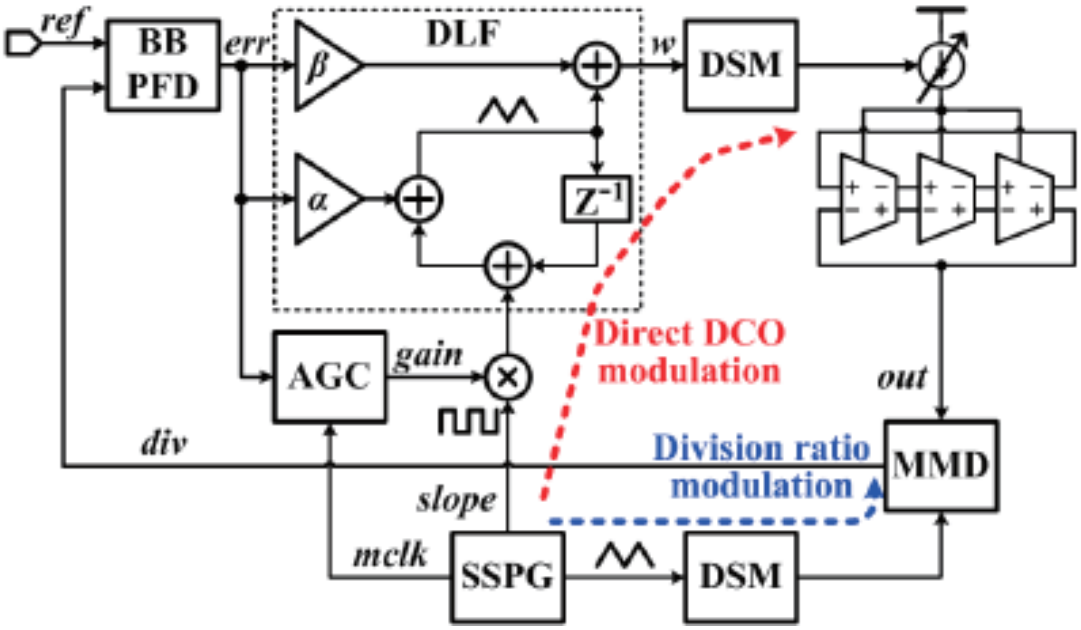
- Feedback factor modulation with fractional phase



[HR Lee: A low jitter 5000 ppm]

SSCG Architectures

- **Two-point modulation**



[2015_SOVC_SCJANG - An All-Digital Bang-Bang PLL Using Two-Point Modulation and Background Gain Calibration for Spread Spectrum Clock Generation]

Modulation Waveform

- **Triangular vs Hersey-Kiss**

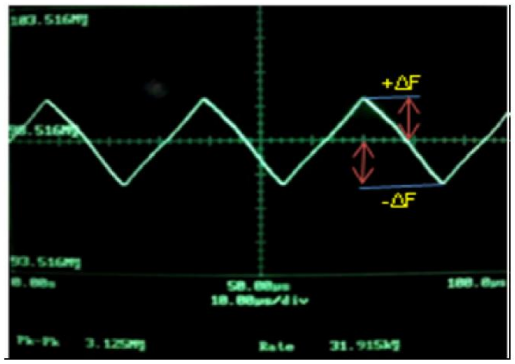


Figure 1. Linear Profile (MDA plot)

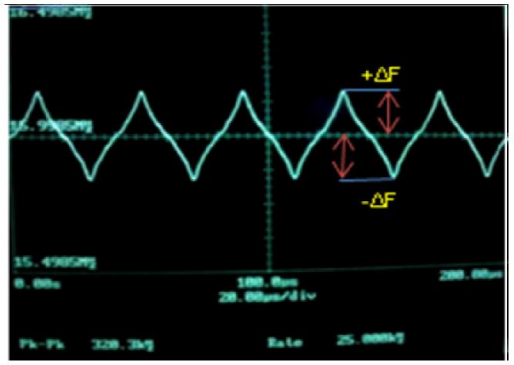


Figure 2. Hershey Kiss Profile (MDA Plot)

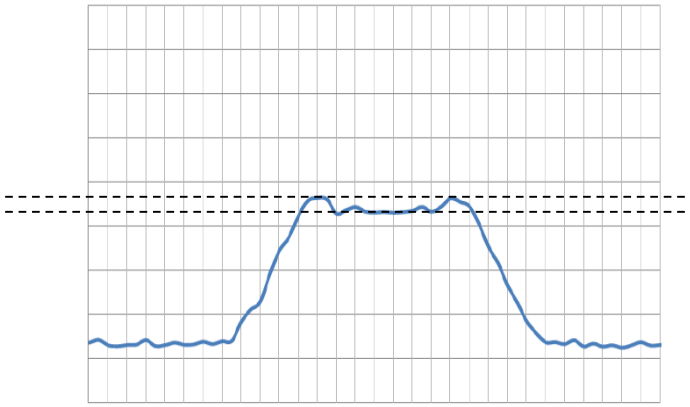


Figure 3. Linear Profile (Spectrum Plot)

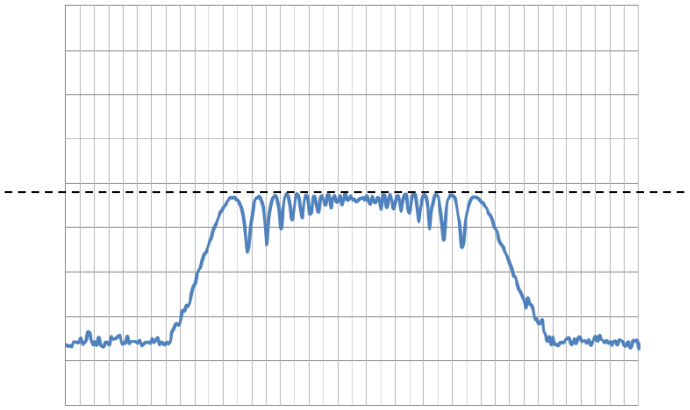


Figure 4. Hershey Kiss Profile (Spectrum Plot)

EMI Reduction at Harmonics

- **EMI Reduction is larger with harmonics**