
3.1. Introduction to All-Digital PLL

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Outline

- **Introduction**
- **ADPLL Building Blocks**
 - Digital Loop Filter
 - Digitally Controlled Oscillator
 - Time-to-Digital Converter
- **Modeling and Analysis**
- **Phase Noise**
- **Summary**

What is an ADPLL?

- **In a broad sense**
 - ADPLL consists of **digital components** and digital equivalents
 - Building blocks have **input/output levels are defined in digital domain**
- **In a strict sense**
 - A PLL exclusively built from digital function blocks and contains **no passive component**
 - All components are synthesizable (Cell-based ADPLL)

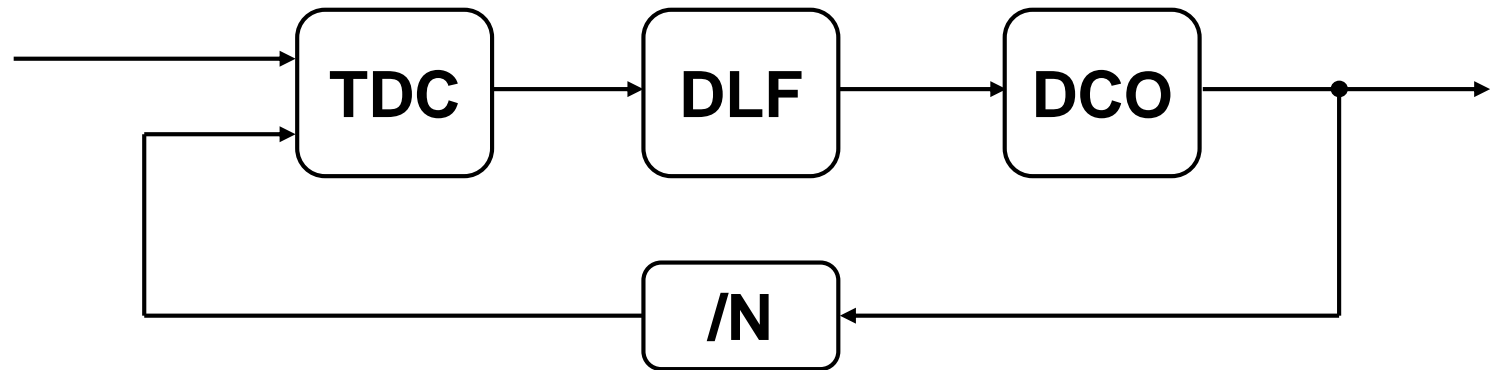
Classification of PLL Types

- **Analog PLL**
 - Analog PD (multiplier), LF built from passive or active RC filter, VCO
- **Digital PLL**
 - Digital PD, charge-pump PLL
- **All-Digital PLL**
 - Built from digital function blocks
 - All components provide **digital interfaces** only

[1] R. E. Best 2003

ADPLL Block Diagram

- **Digital loop filter**
- **Time-to-digital converter (TDC)**
 - Linear
 - Bang-bang
- **Digitally controlled oscillator (DCO)**
 - Explicit DAC + VCO
 - Embedded DAC



Advantages of ADPLL

- **No analog tuning voltage**
 - Suitable for deep-submicron tech using low supply voltage
- **PVT variation can be compensated more easily**
 - Stable transfer characteristic
- **Digital filter**
 - Passive components are not necessary
 - Less sensitive to gate leakage
 - Easily benefit from technology shrink
 - Small area → cost reduction
- **Information can be processed more flexibly**
 - More portability and testability
 - Most function blocks are synthesizable

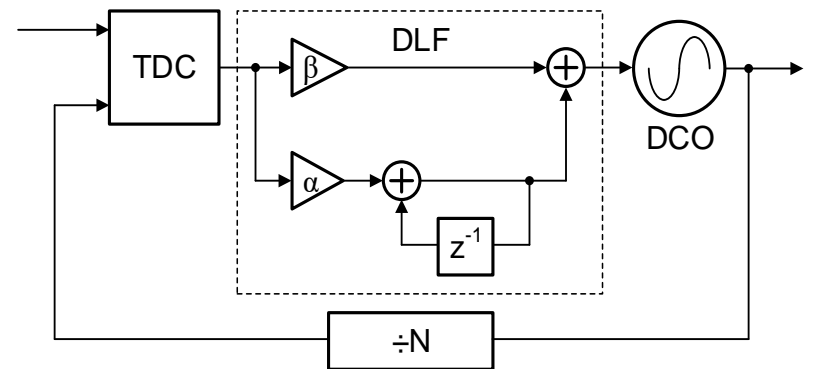
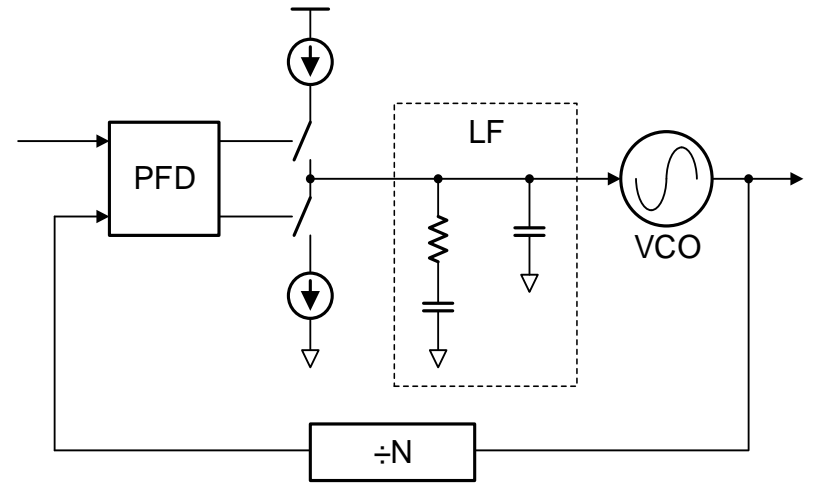
Advantages of Digital Loop Filter

- **Small area**
- **No leakage current**
- **PVT independent**
- **Easy to design**
 - **DLF can be constructed simply by transformation from s-domain to z-domain**
 - **DLF can be expanded to higher-order filter readily**
- **Coefficients can be changed adaptively**
 - **Preset initialization on power-up**
 - **Adaptation during operation for fast locking or low jitter**

Comparison with Typical DPLL

- Almost the same structure as a charge-pump PLL
 - PFD & CP → TDC
 - VCO → DCO

| | CPPLL | ADPLL |
|-------------------------|-------------------------------|--------------------------------------|
| Phase error information | Pump Current | Quantized digital |
| Loop filter | RC filter (passive or active) | Digital filter (IIR or FIR) |
| Oscillator control | Analog (voltage or current) | Digital code (binary or thermometer) |



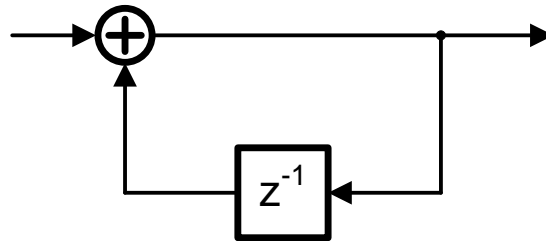
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DLF Examples

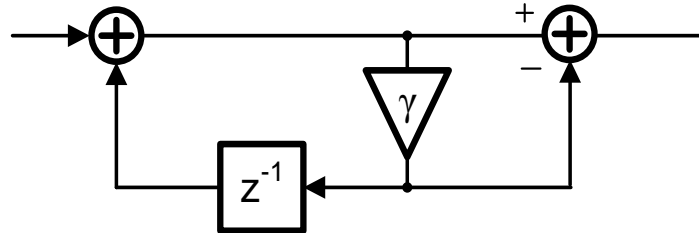
- Simple z-domain IIR filters

Integrator



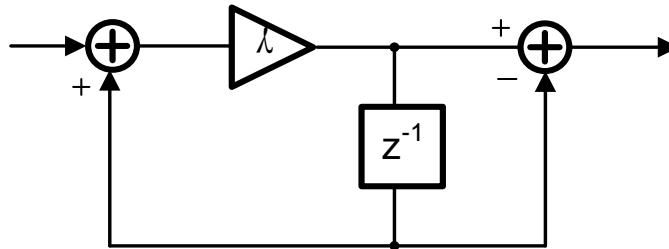
$$H(z) = \frac{1}{1 - z^{-1}}$$

Low pass



$$H(z) = \frac{1 - \gamma}{1 - \gamma z^{-1}}$$

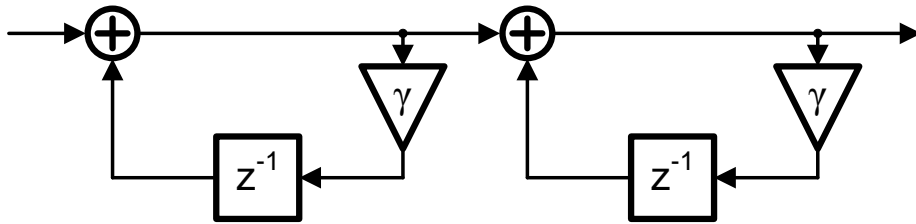
High pass



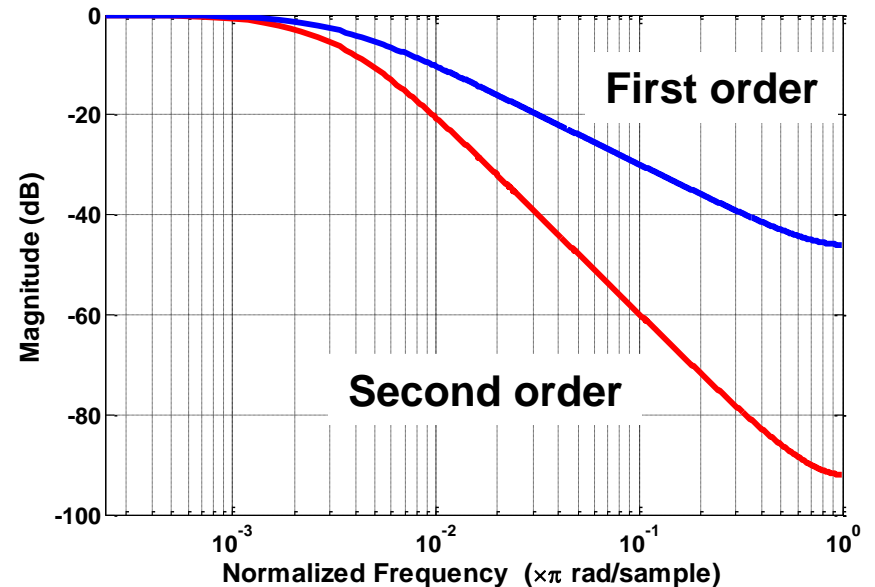
$$H(z) = \frac{\gamma(1 - z^{-1})}{1 - \gamma z^{-1}}$$

Higher Order DLF Example

- **Cascaded IIR low pass filter**
 - Easily expanded to higher order

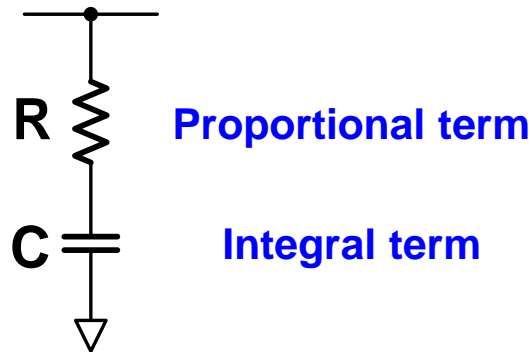


$$H(z) = \left(\frac{1}{1 - \gamma z^{-1}} \right) \cdot \left(\frac{1}{1 - \gamma z^{-1}} \right)$$



Analogy to Analog Filter (1)

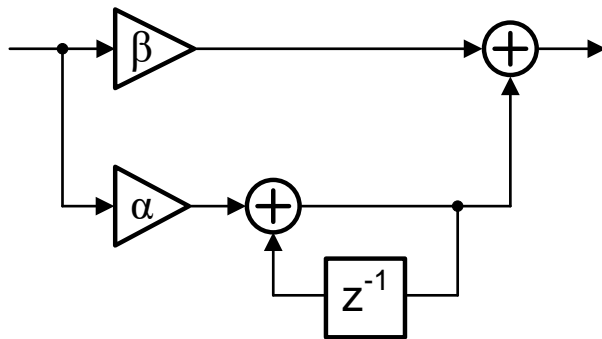
- 1st order passive loop filter



$$H(s) = \left(R + \frac{1}{sC} \right) = \frac{(s/\omega_z + 1)}{sC}$$

$$\omega_z = \frac{1}{RC}$$

- z-domain model



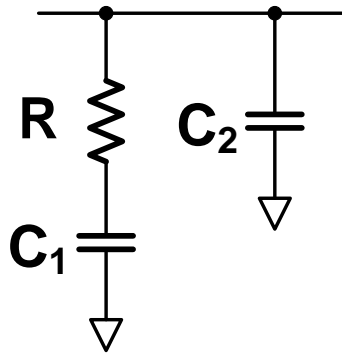
$$H(z) = \left(\beta + \frac{\alpha}{1 - z^{-1}} \right)$$

Integral gain

Proportional gain

Analogy to Analog Filter (2)

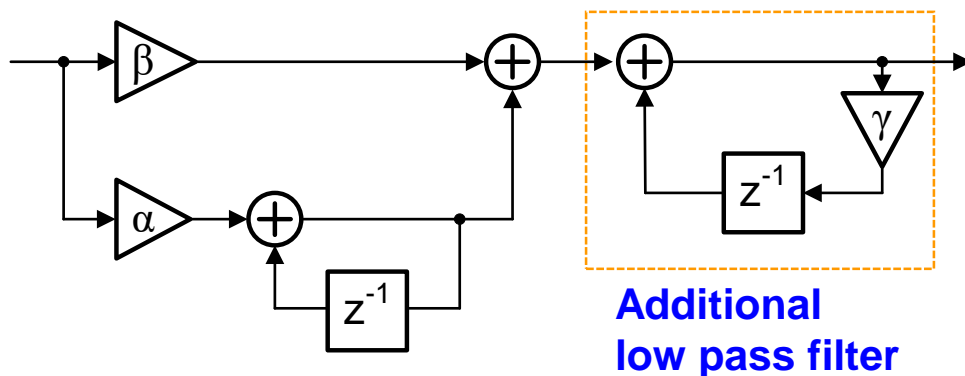
- 2nd order passive loop filter



$$H(s) = \frac{(s/\omega_z + 1)}{(C_1 + C_2)s} \cdot \frac{1}{(s/\omega_p + 1)}$$

$$\omega_z = \frac{1}{RC_1}, \omega_p = \frac{C_1 + C_2}{RC_1 C_2}$$

- z-domain model



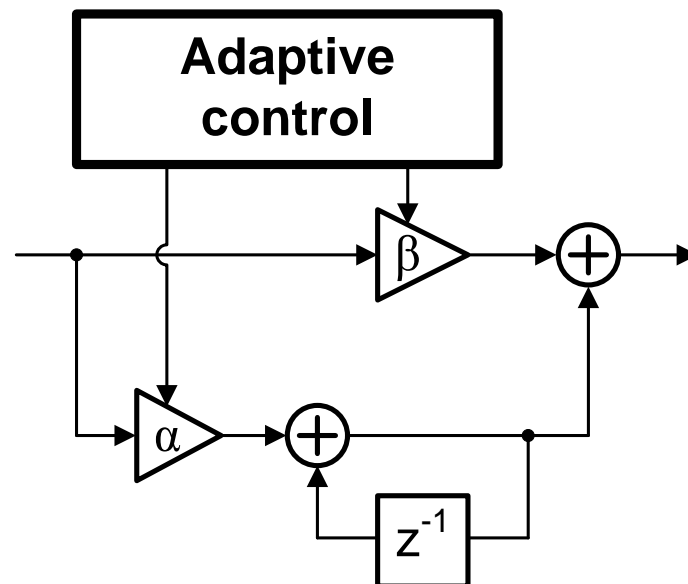
$$H(z) = \left(\beta + \frac{\alpha}{1 - z^{-1}} \right) \cdot \frac{1}{1 - \gamma z^{-1}}$$

With gain normalization

$$H(z) = \left(\beta + \frac{\alpha}{1 - z^{-1}} \right) \cdot \frac{(1 - \gamma)}{1 - \gamma z^{-1}}$$

Adaptive Digital Loop Filter

- **Lock-time control, frequency locking range enhancement**
- **Find the optimum performance point**
 - Input noise filtering vs. lock-time
- **Utilize software or hardware**
 - Gain estimation
 - Noise cancellation



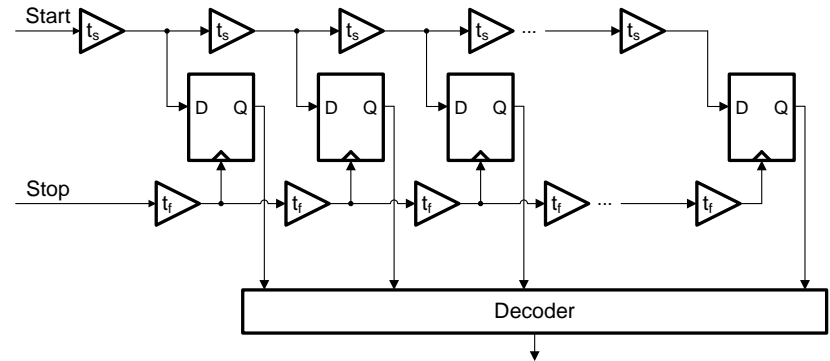
TDC Classification

- **Linear TDC**
 - Delay line based
 - Fine resolution
 - Consumes large hardware and power
 - Process dependent and less reusable

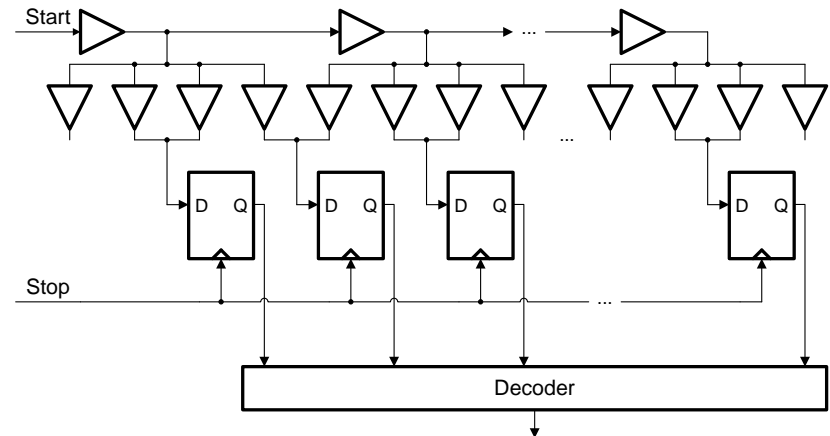
- **Bang-bang TDC**
 - Simple structure
 - Highly nonlinear but can be controlled
 - More reusable

Linear TDC

- **Converts time difference to digital value**
- **Important design factors: resolution, linearity, power, area**
- **Conventional TDC**
 - Delay chain and samplers
 - Minimum delay is restricted by intrinsic gate delay \rightarrow Vernier TDC, interpolative TDC
 - Large size, small dynamic range



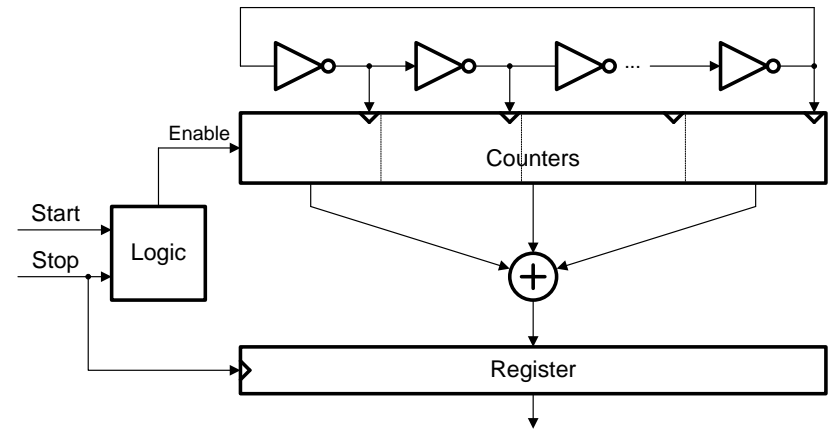
[2] P. Dudek JSSC 2000



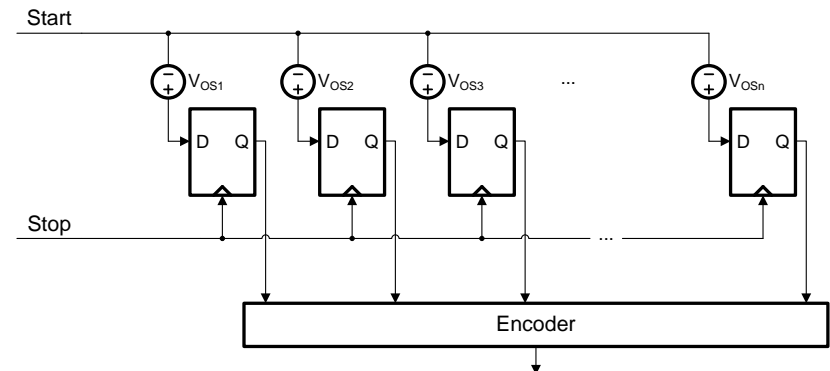
[3] S. Henzler JSSC 2008

Linear TDC

- **To increase dynamic range**
 - Ring oscillator-based TDC
 - Large power consumption due to the free running oscillator
- **Stochastic TDC**
 - Exploits mismatch between samplers and random variation of the offset voltage
 - Very fine resolution
 - Narrow range



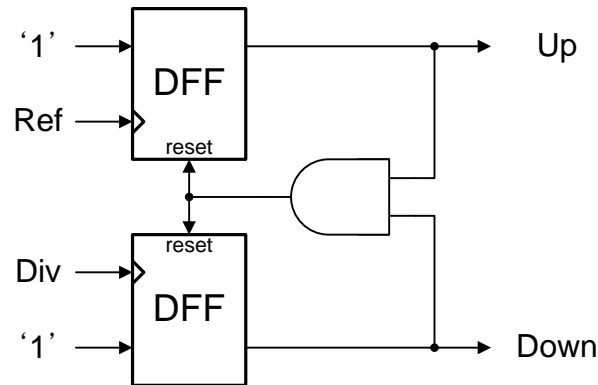
[4] J. Yu JSSC 2010



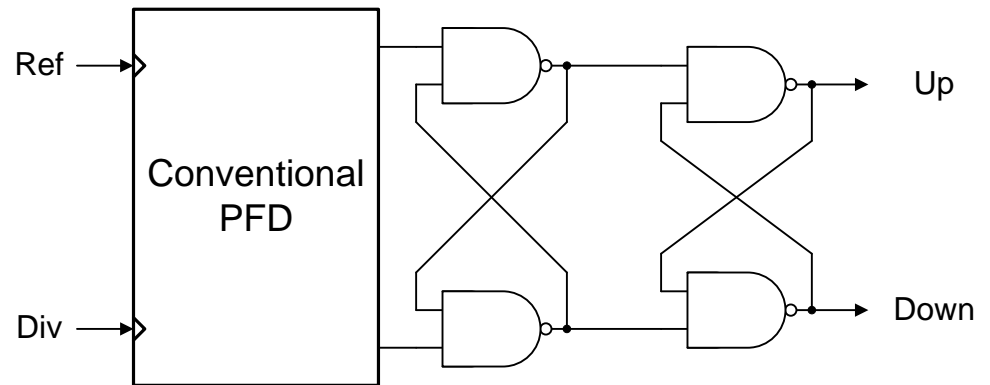
[5] V. Kratyuk TCASI 2009

Bang-Bang TDC

- **Easily achievable and suitable for digital implementation**
 - e.g. bang-bang PFD



Conventional PFD

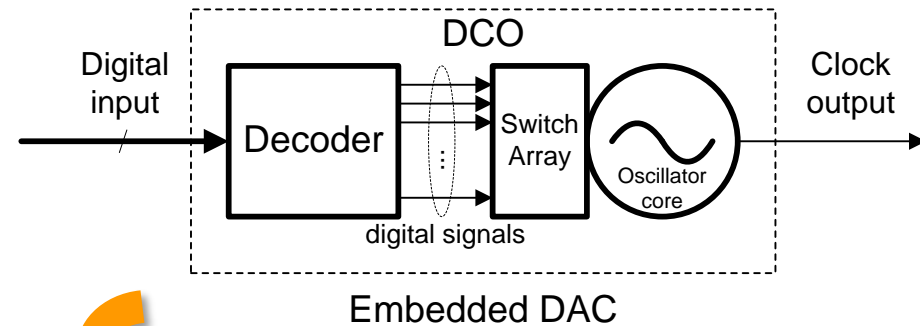
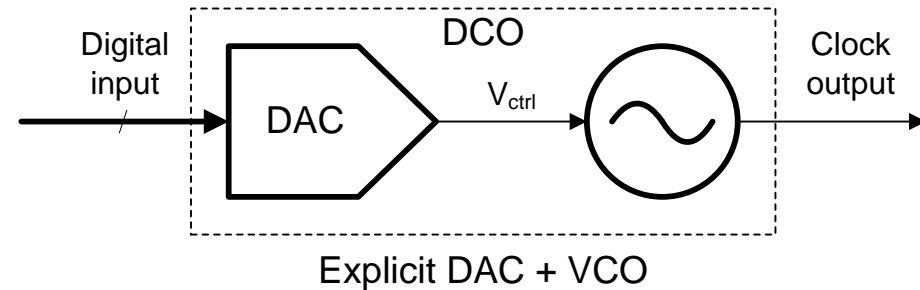


Bang-bang PFD

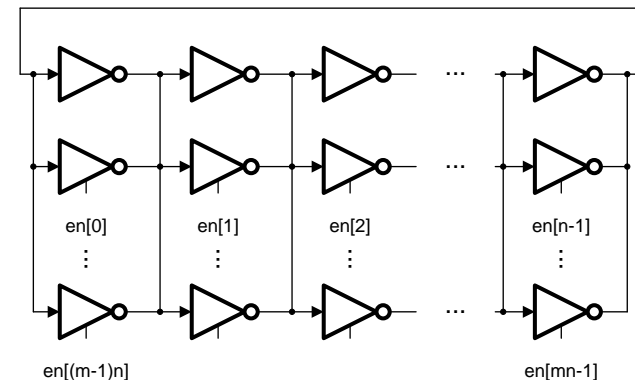
[6] T. Olsson JSSC 2004

Digitally Controlled Oscillator

- **Most Critical component in ADPLL implementation**
- **Digital-to-frequency conversion**
 - Underlying functionality is analog
 - Supports digital interface
 - Analog nature doesn't propagate
- **Implementation method**
 - **Explicit DAC + VCO**
 - **Embedded DAC (turning on/off each unit cell)**

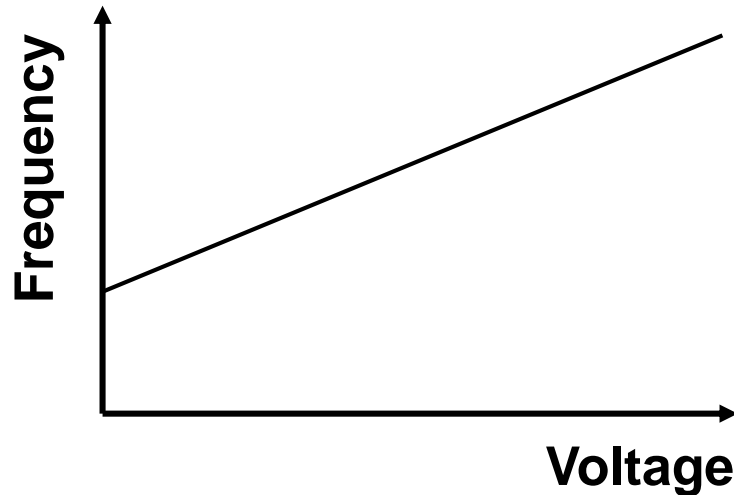


e.g. ring DCO

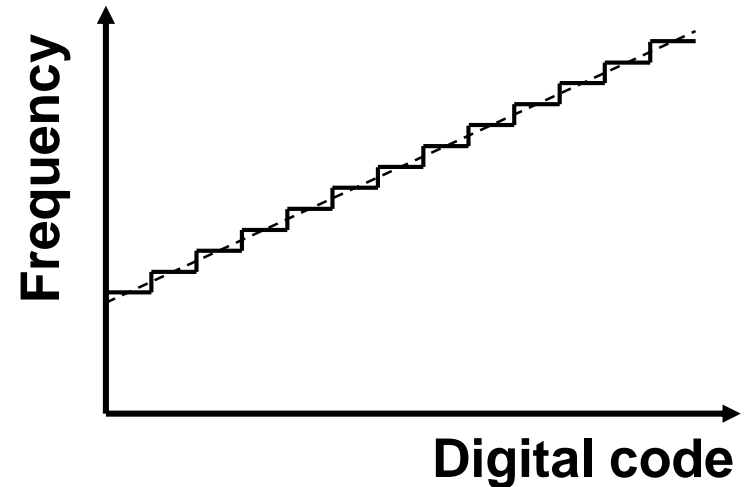


Problem of Limited DCO Resolution

VCO: Continuous output

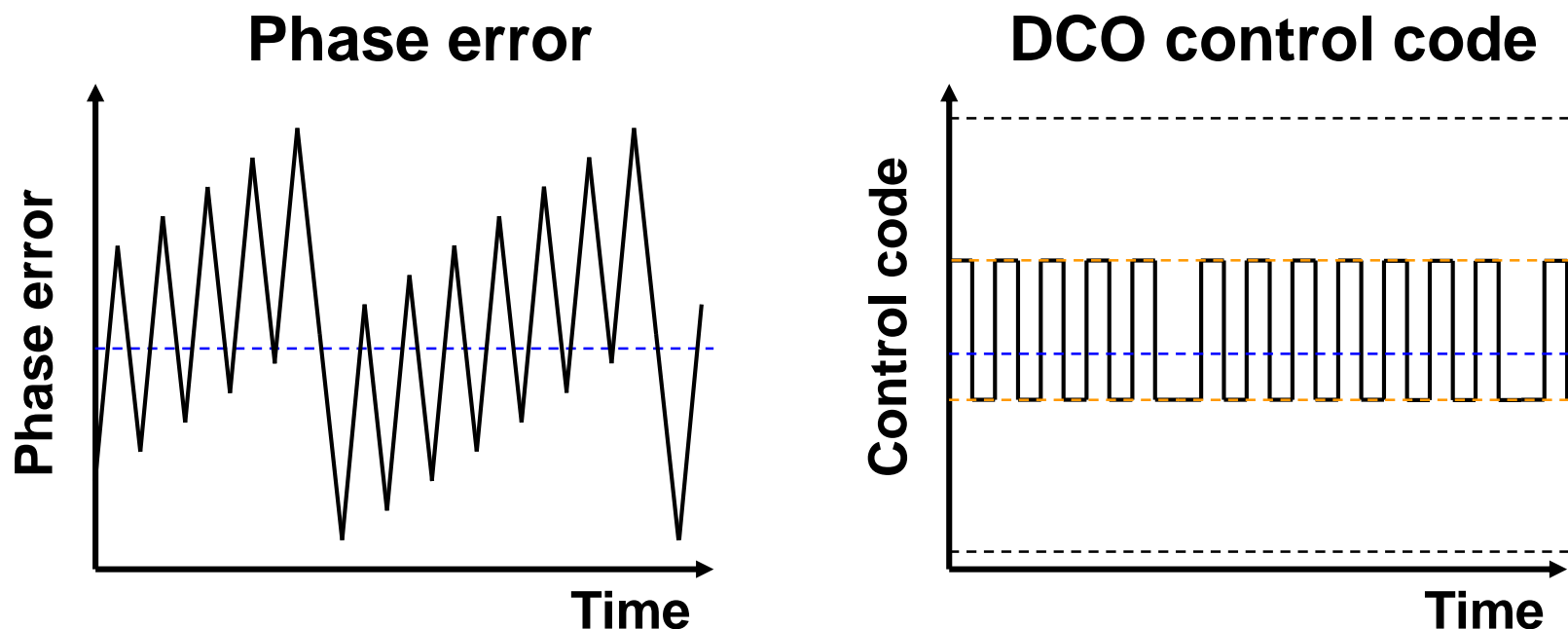


DCO: Quantized output



- Quantized frequency control causes a limit cycle – cycling around the intended frequency

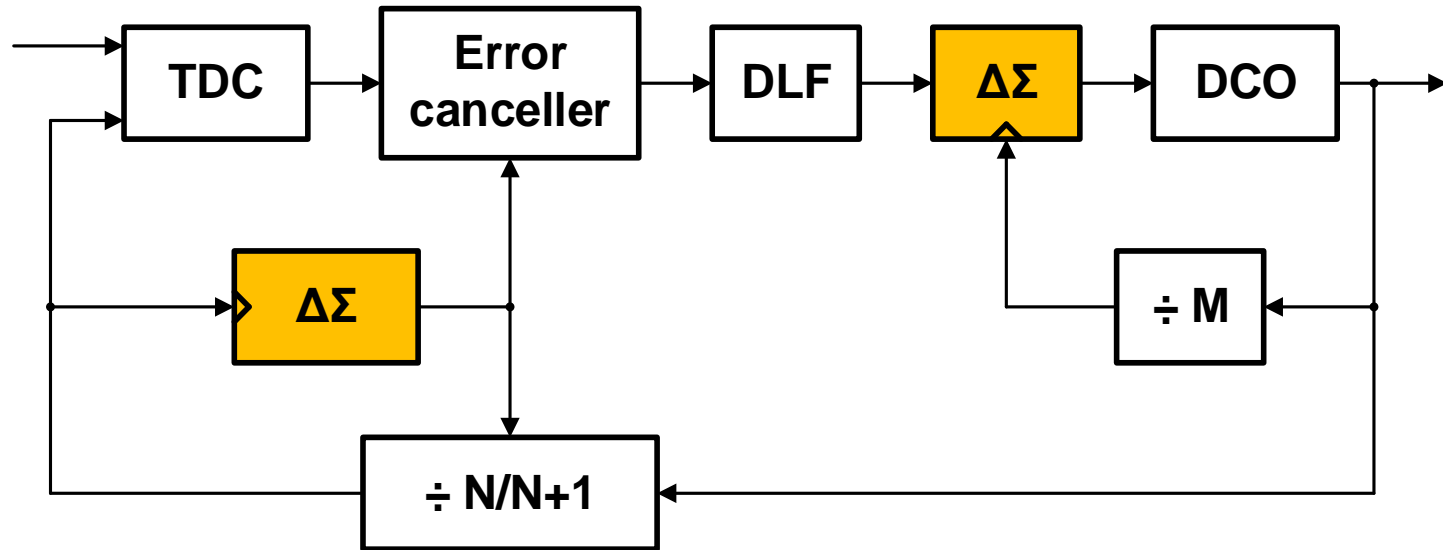
Typical Locked Behavior of ADPLL



- Periodic or pseudo-periodic (peak-to-peak jitter is bounded)
- $\Delta\Sigma$ -modulator can be used to alleviate this problem

ADPLL Architecture

- $\Delta\Sigma$ -modulator ($\Delta\Sigma$) is used to increase the effective resolution of the DCO
- Fractional spur can be reduced by using cancellation techniques

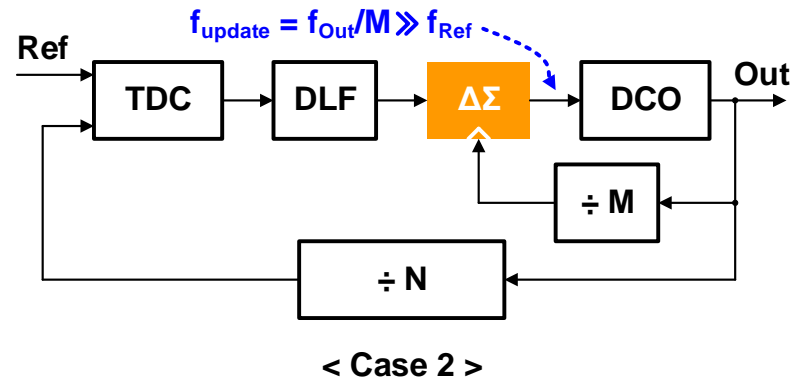
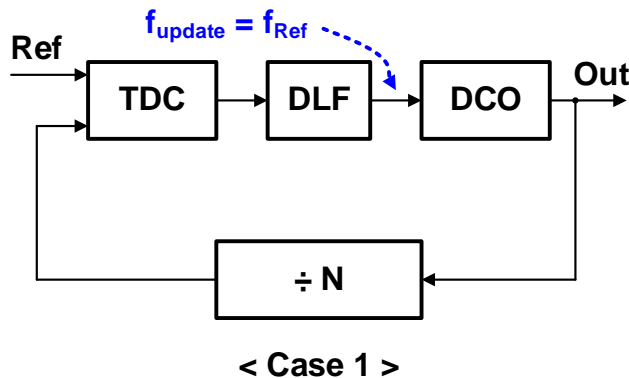


[7] C.-M. Hsu JSSC 2008

[8] R. B. Staszewski JSSC 2005

Low Jitter DCO Using $\Delta\Sigma$ -Modulator

- Effective frequency resolution is improved by high-speed $\Delta\Sigma$ -dithering
- Higher update rate of DCO is important
 - Phase error accumulates for dithering cycles
 - Peak-to-peak jitter is inversely proportional to update frequency



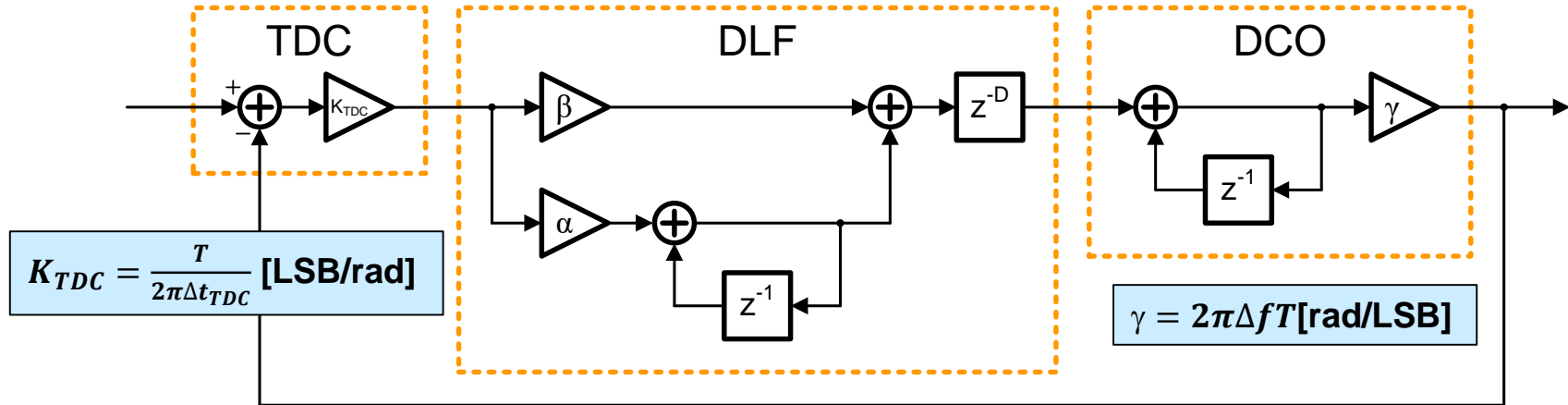
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Analysis methods

- **z-domain analysis**
 - Models discrete-time behavior
 - Can exploit intuitive CPPLL analogy
 - Quick and simple
- **s-domain analysis**
 - z-to-s domain transformation
 - Simple approximation ($z \rightarrow 1+sT$)
 - Bilinear-z transformation ($z \rightarrow (1+sT/2)/(1-sT/2)$)
 - CPPLL analogy can be used
 - Many s-domain analysis techniques reused
 - Phase Margin
 - Bandwidth

Simple z-domain Model



$$L(z) = K_{TDC} \cdot H_{DLF}(z) \cdot H_{DCO}(z) = K_{TDC} \cdot \left(\beta + \frac{\alpha}{1 - z^{-1}} \right) \cdot z^{-D} \cdot \left(\frac{\gamma}{1 - z^{-1}} \right)$$

$$C(z) = \frac{L(z)}{1 + L(z)} = \frac{K_{TDC}(\alpha + \beta)\gamma z - K_{TDC}\beta\gamma}{z^{D+1} - 2z^D + z^{D-1} + K_{TDC}(\alpha + \beta)\gamma z - K_{TDC}\beta\gamma}$$

- **Stability check in z-domain**

- **Unit circle criterion: all poles should be inside the unit circle**
- **Jury's stability criterion**

Steady-State Phase Error

- **Step input:** $p(t) = p \times u(t) \rightarrow P(z) = \frac{p}{1-z^{-1}} = \frac{pz}{(z-1)}$
- **Error function:**

$$\begin{aligned} E_p(z) &= P(z) - P(z)C(z) = \frac{P(z)}{1+L(z)} \\ &= \frac{pz}{(z-1)} \cdot \frac{z^{D-1}(z-1)^2}{z^{D-1}(z-1)^2 + K_{TDC}(\alpha + \beta)\gamma z - K_{TDC}\beta\gamma} \end{aligned}$$

- **Using final value theorem:**

$$\begin{aligned} e_p(\infty) &= \lim_{z \rightarrow 1} (z-1)E_p(z) \\ &= \lim_{z \rightarrow 1} \frac{pz}{(z-1)} \cdot \frac{z^{D-1}(z-1)^3}{z^{D-1}(z-1)^2 + K_{TDC}(\alpha + \beta)\gamma z - K_{TDC}\beta\gamma} = 0 \end{aligned}$$

Phase error is eventually eliminated

Steady-State Frequency Error

- **Ramp input:** $f(t) = wt \times u(t) \rightarrow F(z) = \frac{wTz}{(z-1)^2}$
- **Error function:**

$$\begin{aligned} E_f(z) &= F(z) - F(z)C(z) = \frac{F(z)}{1+L(z)} \\ &= \frac{wTz}{(z-1)^2} \cdot \frac{z^{D-1}(z-1)^2}{z^{D-1}(z-1)^2 + K_{TDC}(\alpha + \beta)\gamma z - K_{TDC}\beta\gamma} \end{aligned}$$

- **Using final value theorem:**

$$\begin{aligned} e_f(\infty) &= \lim_{z \rightarrow 1} (z-1)E_f(z) \\ &= \lim_{z \rightarrow 1} \frac{wTz}{(z-1)^2} \cdot \frac{z^{D-1}(z-1)^3}{z^{D-1}(z-1)^2 + K_{TDC}(\alpha + \beta)\gamma z - K_{TDC}\beta\gamma} = 0 \end{aligned}$$

Frequency error is eventually eliminated

Analysis Using CPPLL Analogy

- **DLF coefficients selection**
 - **Apply bilinear transform to s-domain filter**
 - T_s : sampling time of digital system

$$H(s) = \left(R + \frac{1}{sC} \right) \xrightarrow{s = \frac{2}{T_s} \cdot \frac{1-z^{-1}}{1+z^{-1}}} H(z) = \frac{\left(\frac{T_s}{2C} + R \right) + \left(\frac{T_s}{2C} - R \right) z^{-1}}{1 - z^{-1}}$$

- **Compare coefficients**

$$H(z) = \left(\beta + \frac{\alpha}{1 - z^{-1}} \right) = \frac{(\alpha + \beta) - \beta z^{-1}}{1 - z^{-1}} \longrightarrow \begin{array}{l} \alpha = \frac{T_s}{C} \\ \beta = R - \frac{T_s}{2C} \end{array}$$

[10] V. Kratyuk TCASII 2007

Analysis Using CPPLL Analogy

- Use stability analysis method of CPPLL

$$\alpha = \frac{T_s}{T_{REF}} \cdot \frac{\Delta t_{TDC} \cdot N}{K_{DCO}} \cdot \frac{\omega_{UGBW}^2}{\sqrt{1 + \tan^2(\text{PM})}}$$
$$\beta = \alpha \cdot \left(\frac{\tan(\text{PM})}{T_s \cdot \omega_{UGBW}} - \frac{1}{2} \right)$$

- T_s : Sampling period [s]
- T_{REF} : Reference period (usually $T_{REF} = T_s$)
- K_{DCO} : DCO gain [Hz/LSB]
- Δt_{TDC} : Resolutions of TDC [s/LSB]
- PM : Phase Margin
- ω_{UGBW} : Unit gain bandwidth [rad/s]

[10] V. Kratyuk TCASII 2007

Analysis Using CPPLL Analogy

- Use stability analysis using simple approximation ($z \rightarrow 1+sT$)

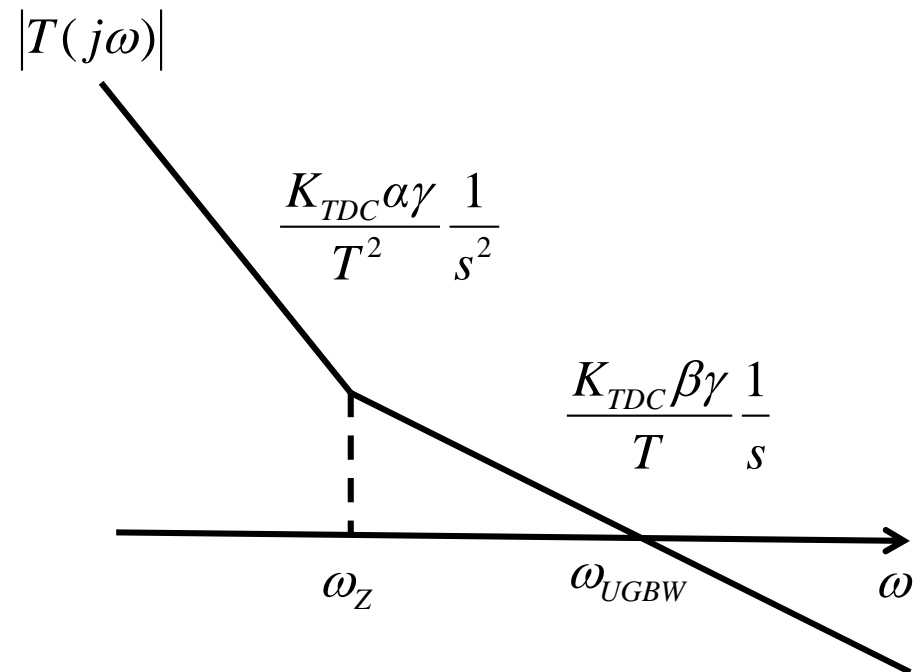
$$T(s) = K_{TDC} \cdot \left(\beta + \frac{\alpha}{sT} \right) \cdot \frac{\gamma}{sT}$$

$$\omega_Z = \frac{\alpha}{\beta T}$$

$$\omega_{UGBW} = \frac{K_{TDC} \beta \gamma}{T}$$

$$PM = \angle T(j\omega_{UGBW}) + 180^\circ$$

$$= \tan^{-1} \left(\frac{K_{TDC} \beta^2 \gamma}{\alpha} \right)$$



$$\alpha = \frac{T^2 \cdot \omega_{UGBW}^2}{\tan(PM) \cdot K_{TDC} \cdot \gamma} = \frac{\omega_{UGBW}^2 \cdot \Delta t_{TDC}}{\tan(PM) \cdot K_{VCO}}$$

$$\beta = \frac{T \cdot \omega_{UGBW}}{K_{TDC} \beta \gamma} = \frac{\omega_{UGBW} \cdot \Delta t_{TDC}}{T \cdot K_{VCO}}$$

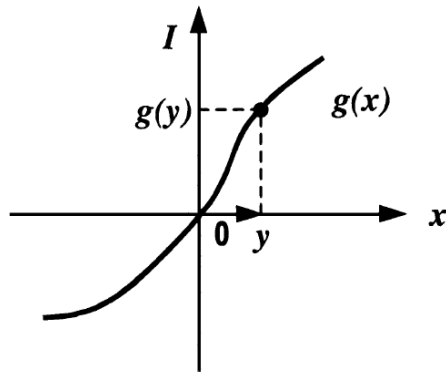
$$K_{TDC} = \frac{T}{2\pi \cdot \Delta t_{TDC}} \text{ [LSB / rad]}$$

$$\begin{aligned} \gamma &= 2\pi \cdot \Delta f_{DCO} \cdot T \\ &= 2\pi \cdot K_{DCO} \cdot T \text{ [rad/LSB]} \end{aligned}$$

$$K_{DCO} : \text{[Hz/LSB]}$$

PD Gain in Presence of Jitter

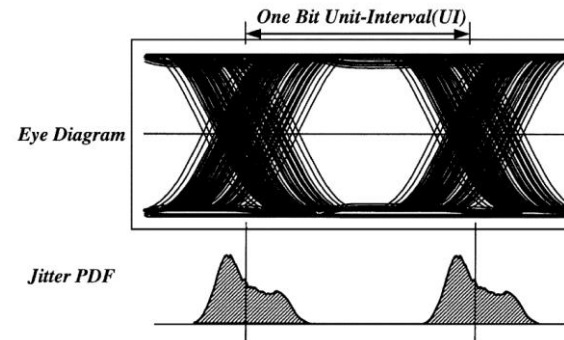
- PD inputs contain jitter from input and VCO



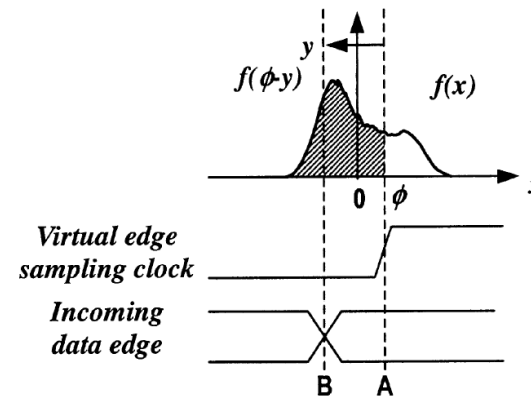
General phase detector gain curve.

$$I_{\text{avg}}(\phi) = \alpha_T \int_{-\infty}^{+\infty} f(\phi - y)g(y)dy = \alpha_T \int_{-\infty}^{+\infty} f(y)g(\phi - y)dy$$

$$K_{\text{PD}}(\phi)|_{\phi=\phi_{\text{Lock}}} = \left. \frac{\partial I_{\text{avg}}(\phi)}{\partial \phi} \right|_{\phi=\phi_{\text{Lock}}}$$



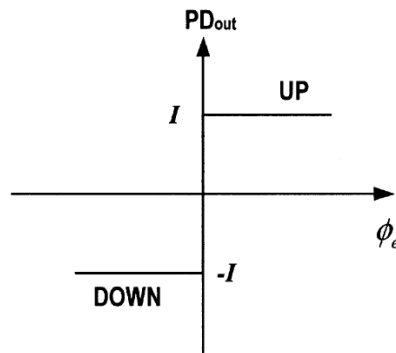
Eye diagram and jitter pdf.



[TCASII_YDCHOI - Jitter transfer analysis of tracked oversampling techniques for multigigabit clock and data recovery]

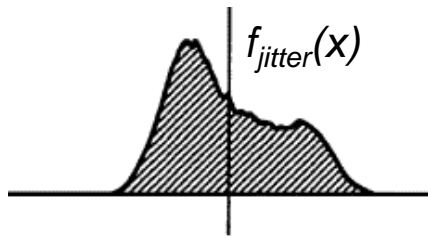
BBPD Gain in Presence of Jitter

- Highly nonlinear characteristics of BBPD (one-bit TDC)



BBPD gain curve

⊗ (convolution)

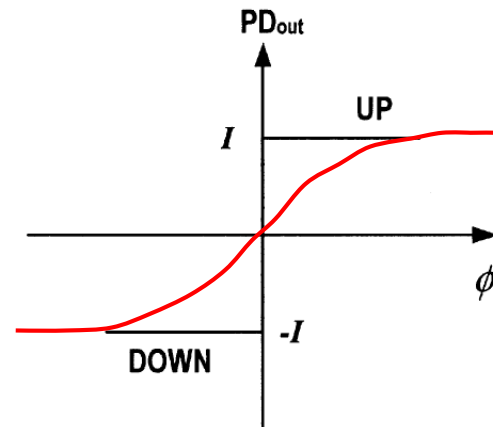


$$I_{avg}(\phi) = \alpha_T \int_{-\infty}^{+\infty} f(\phi-y)g(y)dy = \alpha_T \int_{-\infty}^{+\infty} f(y)g(\phi-y)dy$$

$$PD_{out}(\phi_e) = \alpha_T \int_{-\infty}^{\phi_e} f(y) \cdot I dy + \alpha_T \int_{\phi_e}^{\infty} f(y) \cdot (-I) dy$$

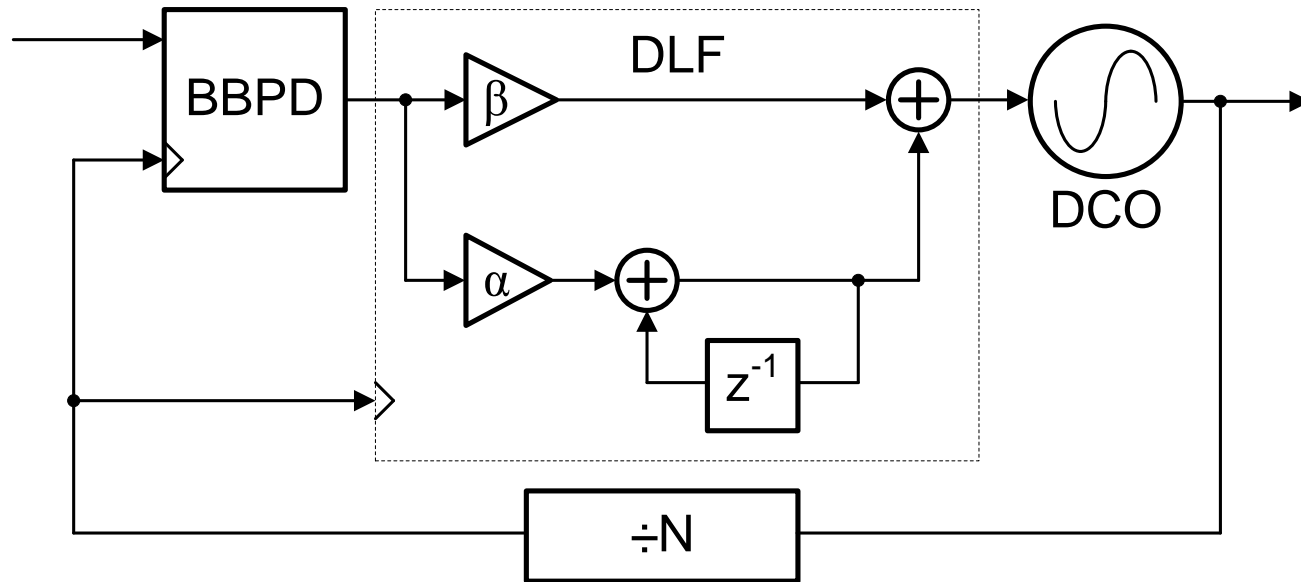
$$= \alpha_T \cdot I \cdot \left(2 \cdot \int_{-\infty}^{\phi} f(y) dy - 1 \right)$$

=



[TCASII_YDCHOI - Jitter transfer analysis of tracked oversampling techniques for multigigabit clock and data recovery]

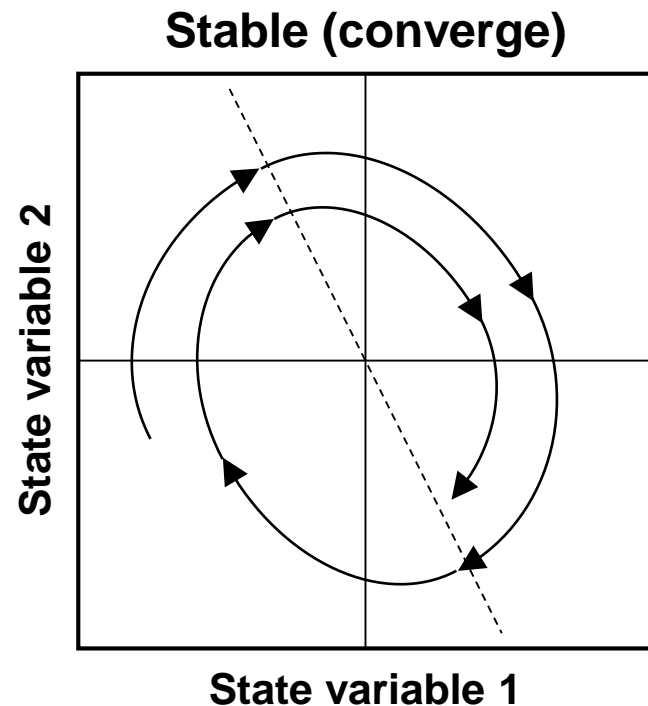
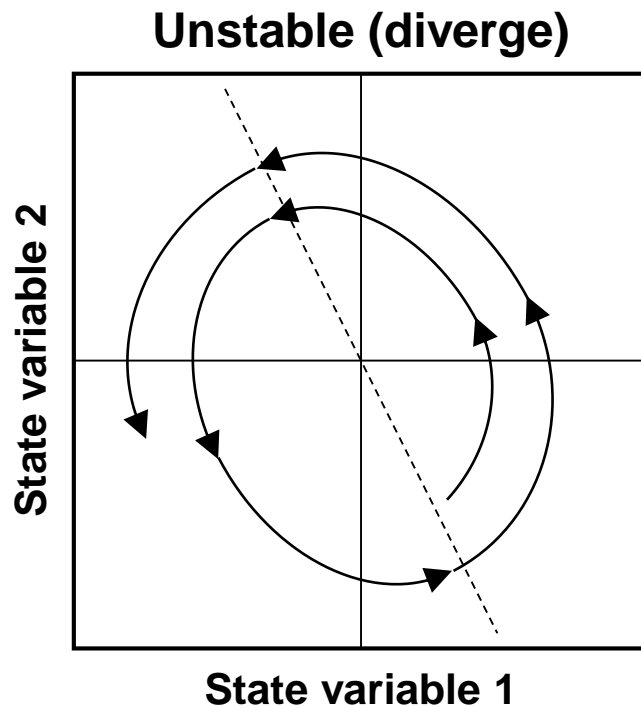
ADPLL with BBPD (1)



- **Loop dynamic of ADPLL with BBPD**
 - Highly nonlinear characteristics of BBPD (one-bit TDC)
Described by time-domain difference equation
 - Refer to [11]–[15] for more details

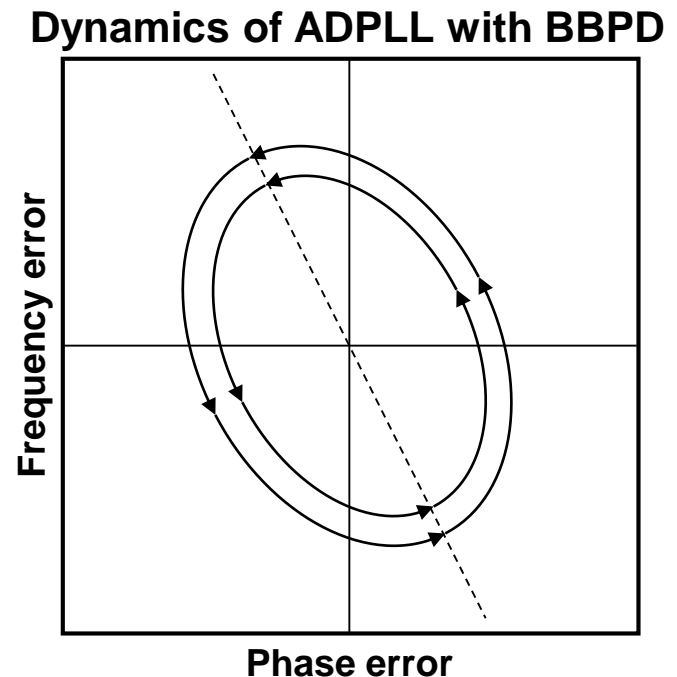
Nonlinear Loop Dynamics

- Nonlinear dynamics are illustrated by trajectories in the phase space
- Behavior: equilibrium point or periodic orbit



ADPLL with BBPD (2)

- **Stability condition: Existence of limit-cycle**
 - Phase and frequency errors never converge to zero concurrently
- **Long pipeline stages increase loop latency**
 - Enlarge the size of orbit
 - Degrade jitter performance
- **Small loop latency is important**



ADPLL with BBPD (3)

- 1st order BBPLL loop dynamics (initial error = 0)
 - Peak-to-peak jitter is directly proportional to loop latency

| Latency = 0, $J_{pp} = \Delta$ | | | | | |
|--------------------------------|-------|----------------|-------|----------------|-------|
| Phase | P_0 | $P_0 - \Delta$ | P_0 | $P_0 - \Delta$ | P_0 |
| PD _{OUT} | DN | UP | DN | UP | DN |
| | ↓ | ↓ | ↓ | ↓ | ↓ |
| DCO _{in} | DN | UP | DN | UP | DN |

| Latency = 1, $J_{pp} = 3\Delta$ | | | | | | | | |
|---------------------------------|-------|----------------|-------|----------------|-----------------|----------------|-------|----------------|
| Phase | P_0 | $P_0 + \Delta$ | P_0 | $P_0 - \Delta$ | $P_0 - 2\Delta$ | $P_0 - \Delta$ | P_0 | $P_0 + \Delta$ |
| PD _{OUT} | DN | DN | DN | UP | UP | UP | DN | DN |
| | | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ |
| DCO _{in} | UP | DN | DN | DN | UP | UP | UP | DN |

Latency = D, $J_{pp} = (1 + 2D) \times \Delta$

[11] N. D. Dalt TCASI 2005

ADPLL with BBPD (4)

- **1st order BBPLL loop dynamics**

- Initial error $\neq 0$, $J_{pp} = 2(1+D)\Delta$
- For uniform distribution

$$\sigma_J^2 = \frac{(1+D)^2}{3} \Delta^2$$

$\sigma_J^2 =$ Jitter variance

$D =$ Delay

$\Delta =$ Quantized Step of DCO

- **2nd order BBPLL loop dynamics**

$$\begin{cases} \tau_{k+1} = \tau_k - R \cdot \varphi_{k-D} - \text{sgn}(\tau_{k-D}) \\ \varphi_{k+1} = \varphi_k + \text{sgn}(\tau_{k+1}) \end{cases}$$

- Size of orbit (stability) depends on D and $R = \alpha(\text{int})/\beta(\text{prop})$
- For small R, $J_{pp} \approx 2(1+D)\Delta$
- For uniform distribution and small orbit

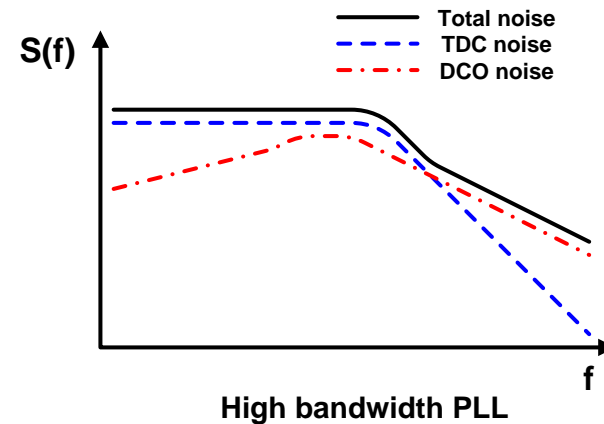
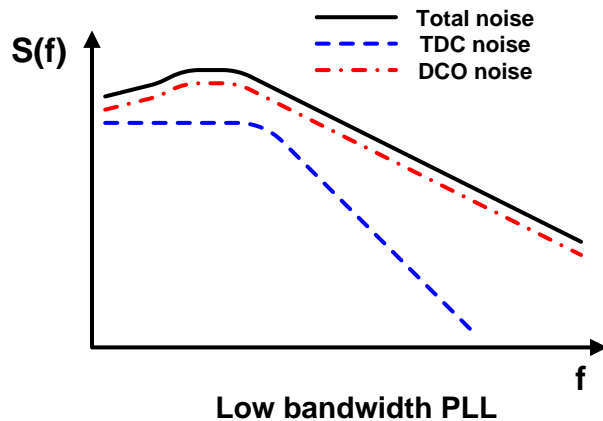
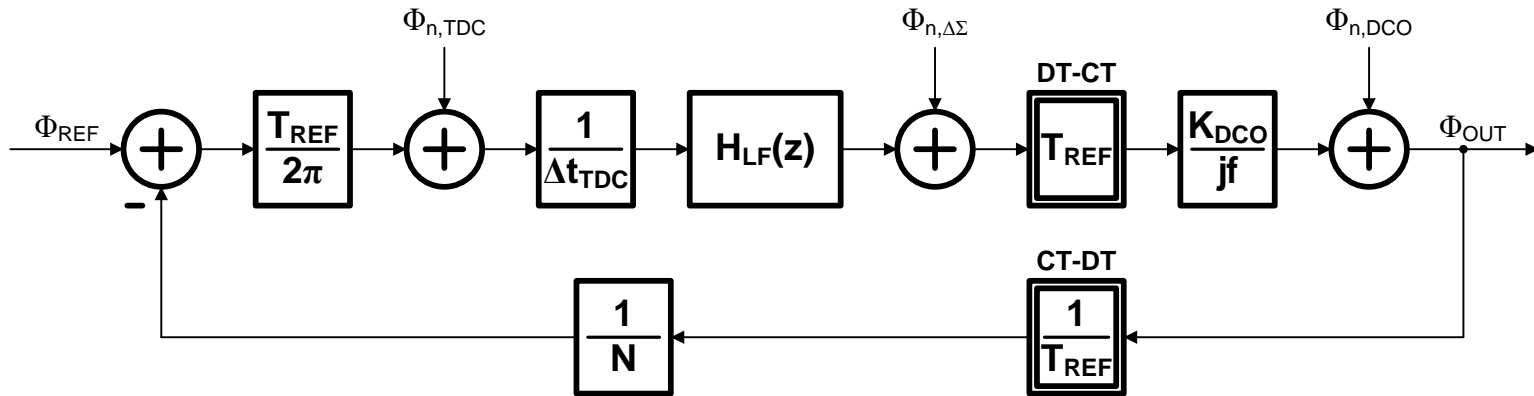
$$\sigma_J^2 = \frac{(1+D)^2}{3} \Delta^2$$

[11] N. D. Dalt TCASI 2005

Outline

- Introduction
- **ADPLL Building Blocks**
 - Digital Loop Filter
 - Digitally Controlled Oscillator
 - Time-to-Digital Converter
- Modeling and Analysis
- **Phase Noise**
- Summary

General Linearized s-domain Model



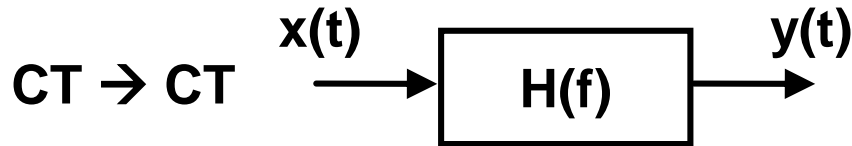
$$A(f) = \frac{T_{REF}}{2\pi} \cdot \frac{1}{\Delta t_{TDC}} \cdot H(f) \cdot \left(\frac{K_{DCO}}{jf} \right) \cdot \left(\frac{1}{N} \right)$$

$$G(f) = \frac{A(f)}{1 + A(f)}$$

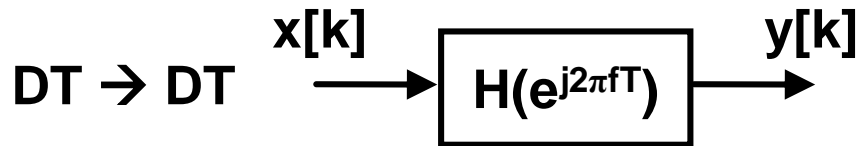
$$\text{DCO gain} = \frac{\gamma}{1-z^{-1}} = \frac{2\pi\Delta f T}{j2\pi f T} = \frac{K_{DCO}}{jf} \text{ [rad/s/LSB]}$$

[16] M. H. Perrott JSSC 2002

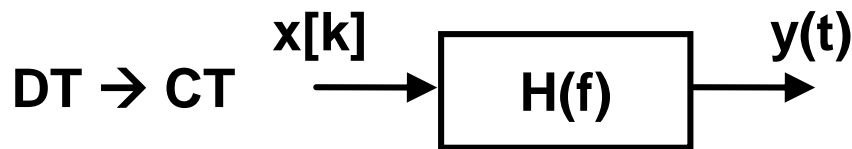
Spectral Density Conversion



$$S_y(f) = |H(f)|^2 S_x(f)$$



$$S_y(e^{j2\pi fT}) = |H(e^{j2\pi fT})|^2 S_x(e^{j2\pi fT})$$



$$S_y(f) = \frac{1}{T} |H(f)|^2 S_x(e^{j2\pi fT})$$

[16] M. H. Perrott JSSC 2002

Quantization Noise of TDC

- Modeled as an additive random variable with white spectral density

$$\sigma_{\Phi_{n,TDC}}^2 = \frac{(\Delta t_{TDC})^2}{12}$$

$$S_{\Phi_{n,TDC}}(f) = \frac{\sigma_{\Phi_{n,TDC}}^2}{f_{REF}} = \frac{(\Delta t_{TDC})^2}{12} \cdot \frac{1}{f_{REF}}$$

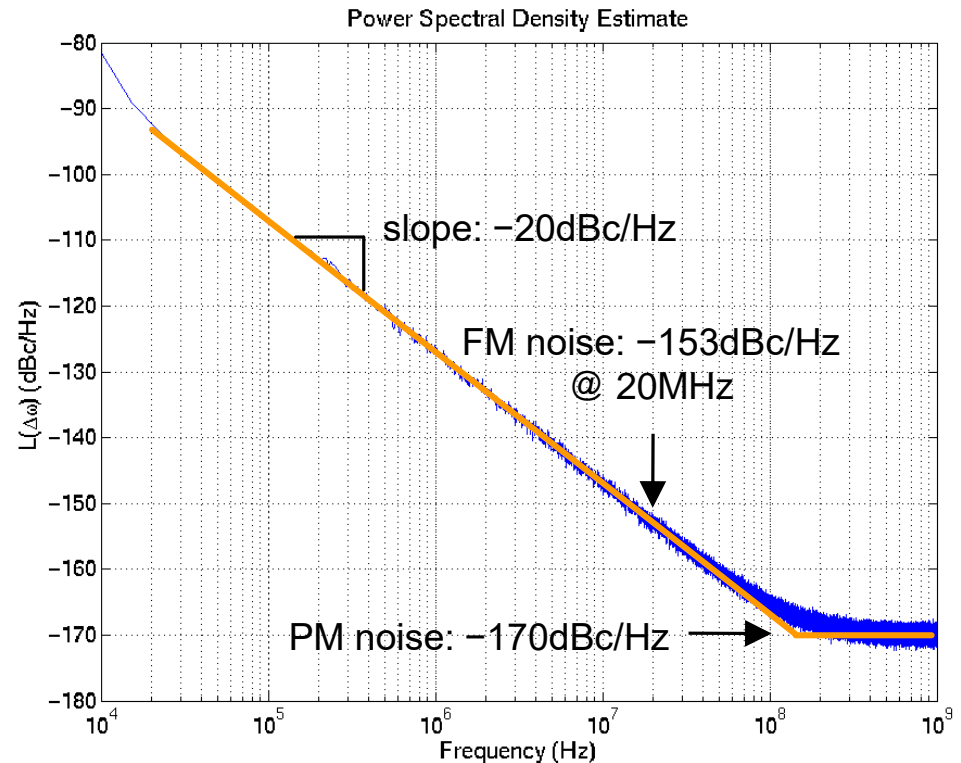
- Output noise is low pass filtered by the loop
 - Small Δt_{TDC} and large f_{REF} is advantageous

$$\begin{aligned} S_{\Phi_{OUT,TDC}}(f) &= \left| \frac{2\pi}{T_{REF}} \cdot N \cdot G(f) \right|^2 \cdot S_{\Phi_{n,TDC}}(f) \\ &= \frac{(2\pi)^2}{12} \cdot \left(\frac{\Delta t_{TDC}}{T_{OUT}} \right)^2 \cdot \frac{1}{f_{REF}} \cdot |G(f)|^2 \end{aligned}$$

[17] R. B. Staszewski JSSC 2005

Noises in Oscillator

- **FM noise**
 - Up-converted flicker noise ($1/f^3$)
 - Up-converted thermal noise ($1/f^2$)
- **PM noise**
 - Thermal electronic noise added from outside of the oscillator core (e.g. output buffer)
 - High pass filtered by the loop



$$S_{\Phi_{OUT,DCO}}(f) = |1 - G(f)|^2 \cdot S_{\Phi_{n,DCO}}(f)$$

Quantization Noise of DCO (1)

- Modeled as an additive random variable with white spectral density accounting for the effect of zero-order hold

$$\sigma_{\Phi_{n,q}}^2 = \frac{1}{12}$$

$$S_{\Phi_{n,q}}(e^{j2\pi f T}) = \sigma_{\Phi_{n,q}}^2 \left(\frac{\sin(\pi f T_{REF})}{\pi f T_{REF}} \right)^2 = \frac{1}{12} \left(\text{sinc} \frac{f}{f_{REF}} \right)^2$$

- Output noise is high pass filtered by the loop
 - Small Δf_{DCO} and large f_{REF} is advantageous

$$\begin{aligned} S_{\Phi_{OUT,q}}(f) &= \frac{1}{T_{REF}} \left| \left(\frac{T_{REF} \cdot \Delta f_{DCO}}{jf} \right) (1 - G(f)) \right|^2 \cdot S_{\Phi_{n,q}}(e^{j2\pi f T_{REF}}) \\ &= \frac{1}{12} \cdot \left(\frac{\Delta f_{DCO}}{f} \right)^2 \cdot \frac{1}{f_{REF}} \cdot \left(\text{sinc} \frac{f}{f_{REF}} \right)^2 \cdot |1 - G(f)|^2 \end{aligned}$$

[8] R. B. Staszewski JSSC 2005

DCO Dithering

- **Discrete frequency level**
 - **Frequency error always occurs**
 - **DCO resolution is the limiting factor of the phase noise performance**
 - **Dithering by using $\Delta\Sigma$ modulation to enhance resolution**
 - **Dithering noise should be less than the natural phase noise of the oscillator**
 - **Caution: dithering increases high frequency noise**

Quantization Noise of DCO (2)

- **Power spectral density of quantization noise of n^{th} order $\Delta\Sigma$ dithering ($f_{\text{dth}} = M \cdot f_{\text{REF}}$)**
 - High frequency noise increases

$$S_{\Phi_{n,\Delta\Sigma}}(e^{j2\pi f T}) = \frac{\sigma_{\Phi_{n,q}}^2}{M} \left(2 \sin \frac{\pi f T_{\text{REF}}}{M} \right)^{2n} = \frac{1}{12M} \left(2 \sin \frac{\pi f}{M f_{\text{REF}}} \right)^{2n}$$

- **Output noise is high pass filtered by the loop**

$$\begin{aligned} S_{\Phi_{\text{OUT},\Delta\Sigma}}(f) &= \frac{1}{T_{\text{REF}}} \left| \left(\frac{T_{\text{REF}} \cdot \Delta f_{\text{DCO}}}{j f} \right) (1 - G(f)) \right|^2 \cdot S_{\Phi_{n,\Delta\Sigma}}(e^{j2\pi f T_{\text{REF}}}) \\ &= \frac{1}{12} \cdot \left(\frac{\Delta f_{\text{DCO}}}{f} \right)^2 \cdot \frac{1}{f_{\text{dth}}} \cdot \left(2 \sin \frac{\pi f}{f_{\text{dth}}} \right)^{2n} \cdot |1 - G(f)|^2 \end{aligned}$$

[8] R. B. Staszewski JSSC 2005

Quantization Noise of DCO (3)

- **Noise shaping**
 - Performance bottleneck in some RF application
 - Fine resolution is important even if dithering is used

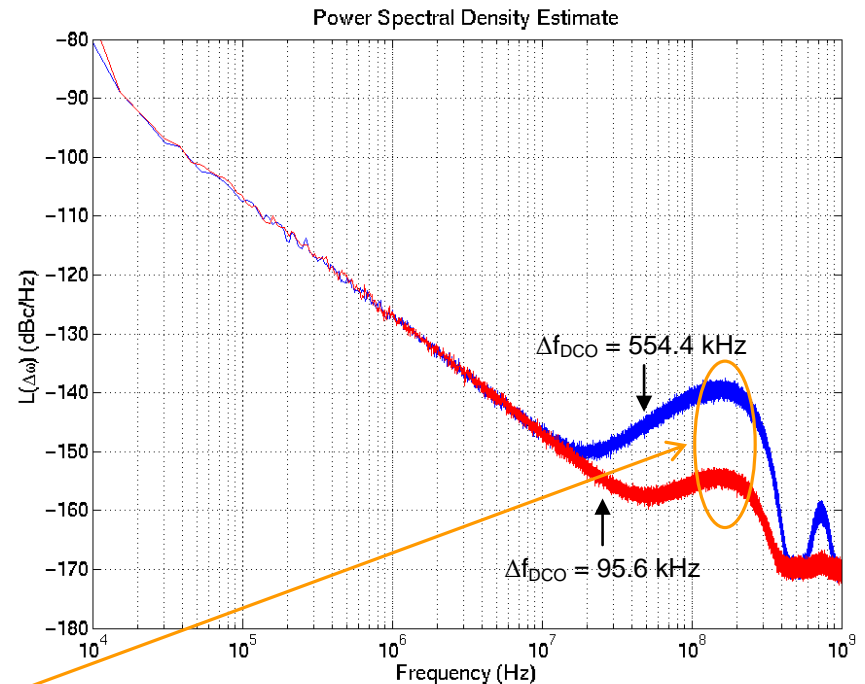
- **Peak value**

$$\max\{S_{\Phi_{OUT,\Delta\Sigma}}(f)\} = \frac{1}{12} \cdot \left(\frac{\Delta f_{DCO}}{f}\right)^2 \cdot \frac{1}{f_{dth}} \cdot \left(\frac{4(rn)^2}{(rn)^2 + 1}\right)^n$$

for $n = \frac{\tan r}{r}$ and $r = \frac{\pi f}{f_{dth}}$

- **For 2nd order dithering**

$$\max\{S_{\Phi_{OUT,\Delta\Sigma}}(f)\} = 0.95 \left(\frac{\Delta f_{DCO}}{f}\right)^2 \cdot \frac{1}{f_{dth}} \quad \text{for } f = \frac{f_{dth}}{2.7}$$



2nd order dithering,
 $f_0 = 4$ GHz, $f_{dth} = 500$ MHz

Time-Domain Noise (Jitter)

- **Jitter**
 - Uncertainty or randomness in the timing of events
- **Phase modulation jitter (PM jitter)**
 - Non-accumulative jitter
 - Random fluctuation in the delay between input and output event with zero mean and bounded variation
- **Frequency modulation jitter (FM jitter)**
 - Accumulative jitter
 - Uncertainty of when a transition occurs accumulates with every transition
 - Modeled as a random walk that is not bounded

[18] K. Kundert 2001

Time-domain Simulation Method

- **Oversampling simulation**
 - Spice, Simulink (matlab), etc.
 - Transverse all the equally spaced time-stamps
 - Inefficient due to the high oversampling ratio
- **Event-driven simulation**
 - VHDL or Verilog
 - Proceed to the time-stamp at which the next event occurs
 - Fast and efficient
 - More useful in ADPLL design

Basic Time-Domain Equation

- For nominal frequency f_0 and nominal period T_0

$$f_0 + \Delta f = \frac{1}{T_0 - \Delta T}$$

- For small $\Delta T/T_0$

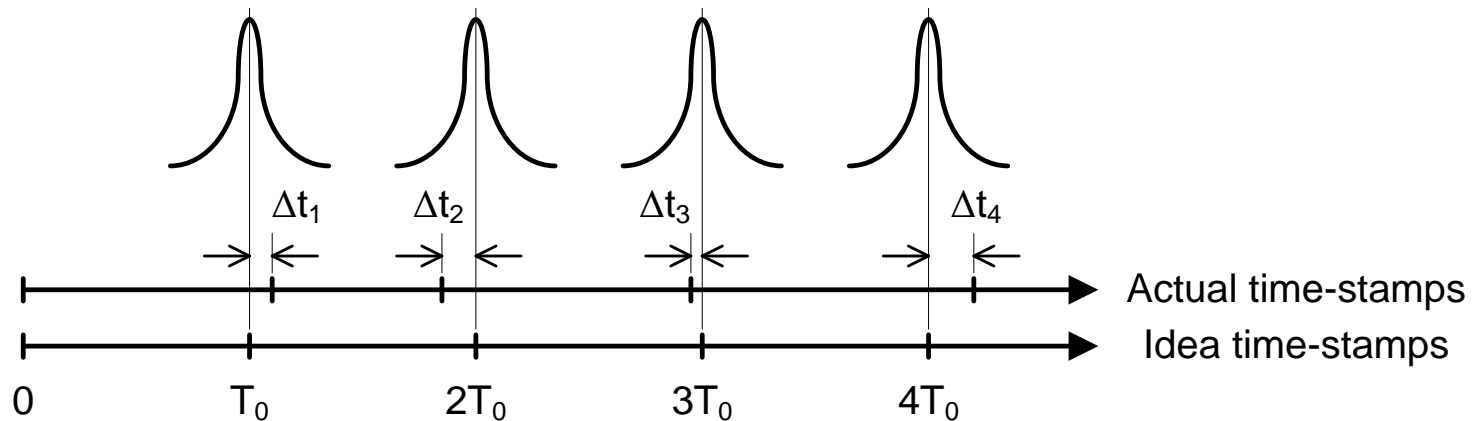
$$\Delta f \approx f_0 \frac{\Delta T}{T_0} = f_0^2 \Delta T = \frac{\Delta T}{T_0^2}$$

- **Timing deviation (TDEV)**
 - The difference between actual and ideal timing

$$TDEV[i] = \sum_{l=1}^i \Delta T[l] = \sum_{l=1}^i \frac{\Delta f[l]}{f_0^2}$$

[19] R. B. Staszewski TCASI 2005

Oscillator PM Jitter



- **Non accumulative additive random error**
- **Timing errors do not influence one another**

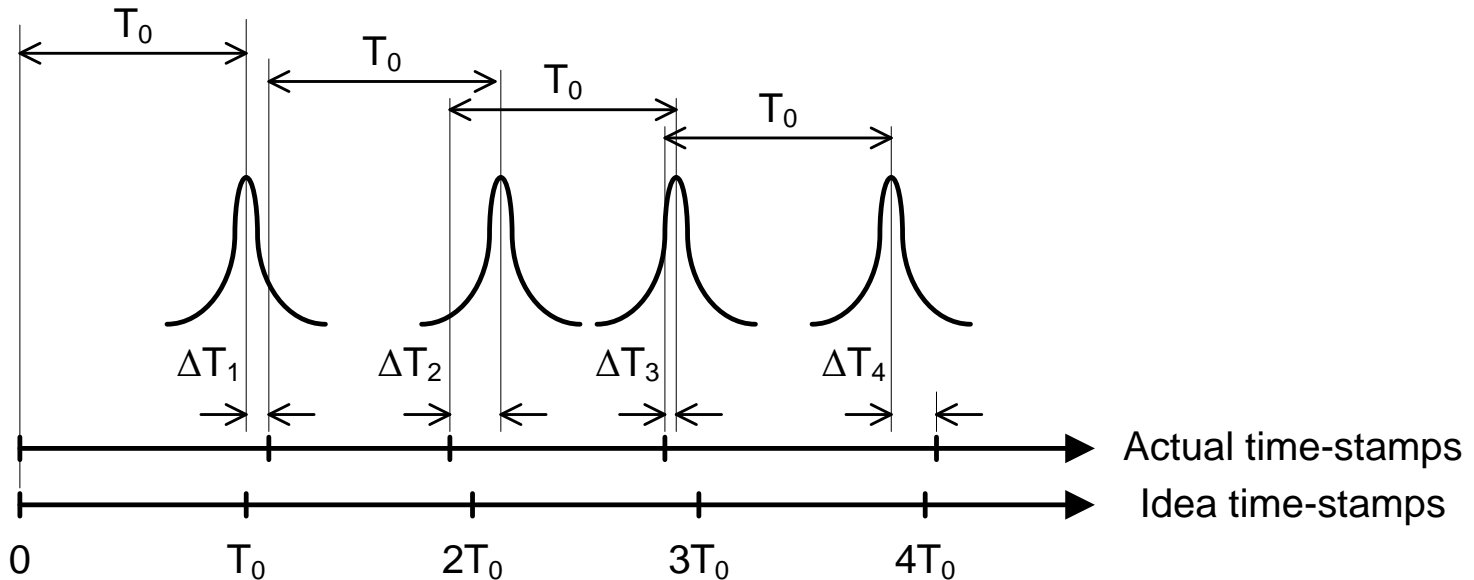
$$TDEV_{PM}[i] = t[i] - i \cdot T_0 = (i \cdot T_0 + \Delta t[i]) - i \cdot T_0 = \Delta t[i]$$

- **Relation between time and frequency domains**

$$\sigma_{\Delta t} = \frac{T_0}{2\pi} \sqrt{L \cdot f_0} \quad (L: \text{noise floor})$$

[19] R. B. Staszewski TCASI 2005

Oscillator FM Jitter



- **Accumulative jitter**
- **Each transition depends on all previous deviation**

$$TDEV_{FM}[i] = t[i] - i \cdot T_0 = (i \cdot T_0 + \sum_{l=1}^i \Delta T[l]) - i \cdot T_0 = \sum_{l=1}^i \Delta T[l]$$

- **Relation between time and frequency domains**

$$\sigma_{\Delta T} = \frac{\Delta f}{f_0} \sqrt{T_0} \sqrt{L\{\Delta f\}}$$

[19] R. B. Staszewski TCASI 2005

Jitter and Phase Noise

- **Convert phase noise specification into time-domain constraints**

- **FM jitter**

$$\sigma_{\Delta T} = \frac{\Delta f}{f_0} \sqrt{T_0} \sqrt{L\{\Delta f\}}$$

- e.g. to meet **-153 dBc/Hz @ 20 MHz for 1.9 GHz**
 - **20 MHz/1.9 GHz x (0.53 ns x 10^{-15.3} /Hz)^{0.5} = 5.4 fs_{RMS}**

- **PM jitter**

$$\sigma_{\Delta t} = \frac{T_0}{2\pi} \sqrt{L \cdot f_0}$$

- e.g. to meet **-170 dBc/Hz for 1.9 GHz**
 - **0.53 ns x (1.9 GHz x 10⁻¹⁷ /Hz)^{0.5} / 2π = 11.6 fs_{RMS}**

[22] <http://www.jittertime.com/resources/pncalc.shtml>

Summary

- **ADPLLs are similar to DSP systems**
- **ADPLL will be dominantly used in deep-submicron technology**
- **DLF offers more flexibility in design**
- **TDC and DCO dominate overall performance**
- **Various techniques can be exploited to analyze the ADPLL in both frequency and time domain**

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- [5] V. Kratyuk, et al., “A digital PLL with a stochastic time-to-digital converter,” *IEEE Trans. Circuits and Syst. I: Regular Papers*, vol. 56, no. 8, pp. 1612-1621, Aug. 2009.
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References (2)

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- [11] N. D. Dalt, “A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs,” *IEEE Trans. Circuits and Syst. I: Regular Papers*, vol. 52, no. 1, pp. 21-31, Jan. 2005.

References (3)

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- [22] <http://www.jittertime.com/resources/pncalc.shtml>
- [23] YDCHOI - TCASII - Jitter transfer analysis of tracked oversampling techniques for multigigabit clock and data recovery," *IEEE Trans. Circuits and Syst. II: Analog and Digital Signal Processing*, VOL 50, No 11, Nov 2003, pp. 775-783.

3.2. Digitally Controlled Oscillator

Deog-Kyoon Jeong

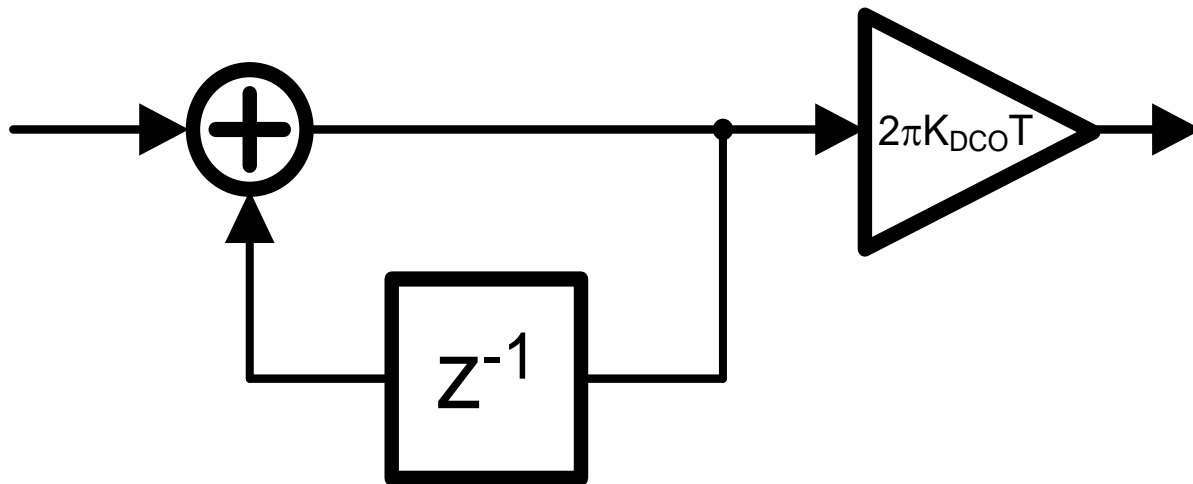
***Integrated Systems Design Laboratory
Seoul National University***

Outline

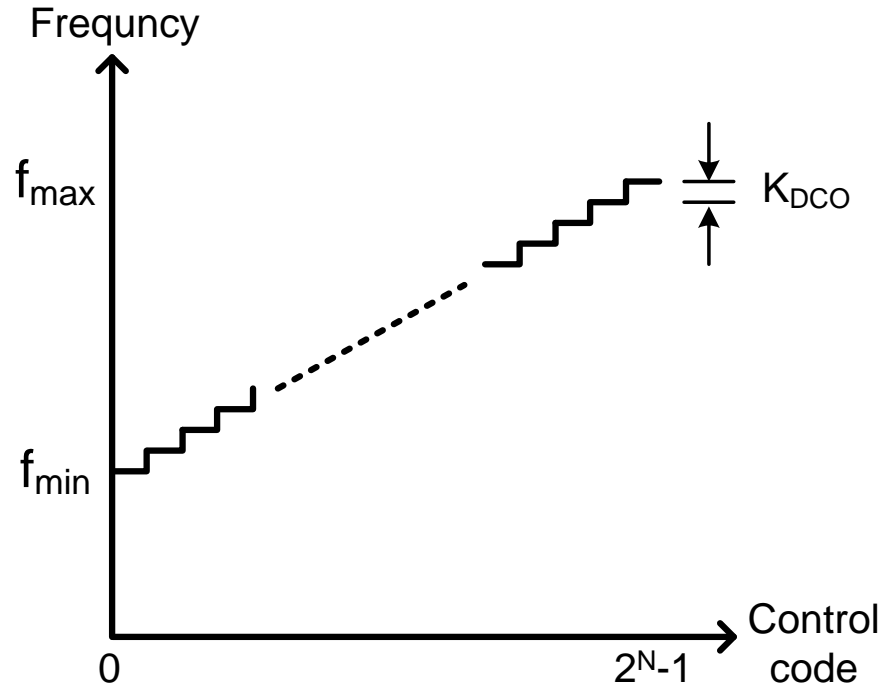
- **Basic Operation**
- Requirements
- Classification
- Design Example
- Issues on DCO design
- Case Studies

Basic Operation (1)

- A digital controlled oscillator (DCO) is the digital counterpart of voltage controlled oscillator (VCO) in an all digital phase locked loop (ADPLL).
- Z-domain modeling



Basic Operation (2)



- **Input : N-bit digital code**
- **Output : periodic clock signal with frequency range ($f_{\min} \sim f_{\max}$)**
- **$K_{\text{DCO}} : \Delta f$ (Hz/bit)**

Outline

- **Basic Operation**
- **Requirements**
- **Classification**
- **Design Example**
- **Issues on DCO design**
- **Case Studies**

DCO Requirements

- **Fine frequency resolution (low K_{DCO})**
- **Wide range**
 - (Fine resolution + wide range) require larger N
- **Linearity (constant $\Delta f/f$)**
- **Low phase noise**
- **Low power consumption**
- **Small active area**

DCO Classification (1)

- **Analog approach**
 - DAC + VCO
 - DAC + ICO
 - DAC + Varactor in LC tank
- **Digital approach**
 - Control the number of inverter stages
 - Control the number of drivers(variable inverter strength)
 - Control the C value in LC tank
 - Control the divider with high freq. oscillator

DCO Classification (2)

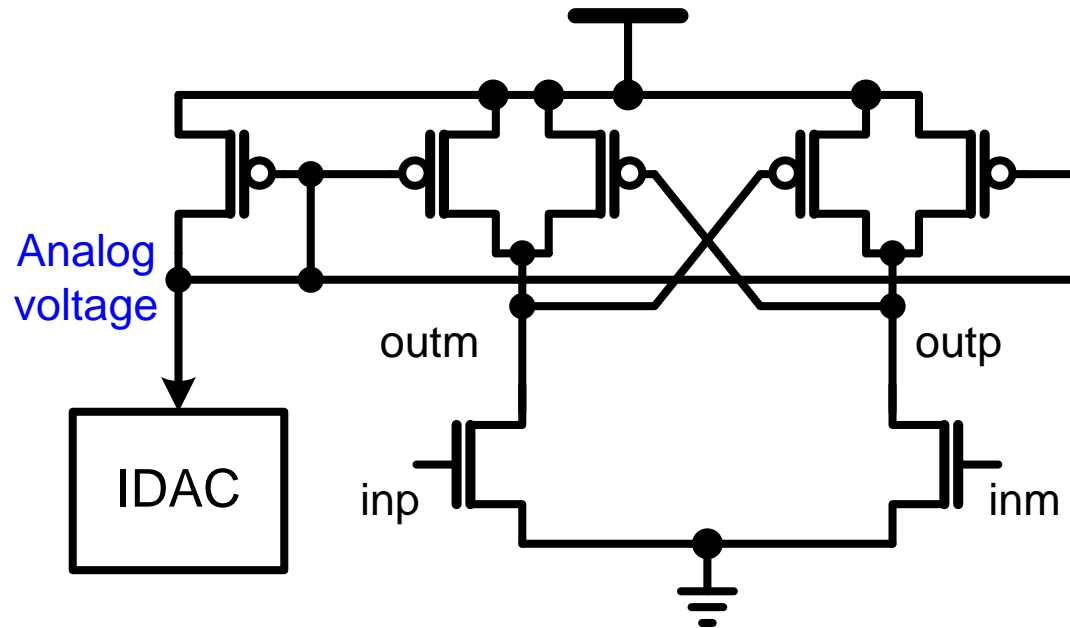
- **Ring oscillator**
 - Simple to design, small area
 - Relatively low maximum frequency
 - Poor phase noise
 - Control # of stages, strength, supply voltage, load capacitor.
- **LC oscillator**
 - Large area due to an inductor
 - Relatively high maximum frequency
 - Good phase noise, fine resolution
 - Control C value

Outline

- Basic Operation
- Requirements
- Classification
- **Design Example**
- Issues on DCO design
- Case Studies

Analog approach (1)

- IDAC + analog VCO
 - Control the R value

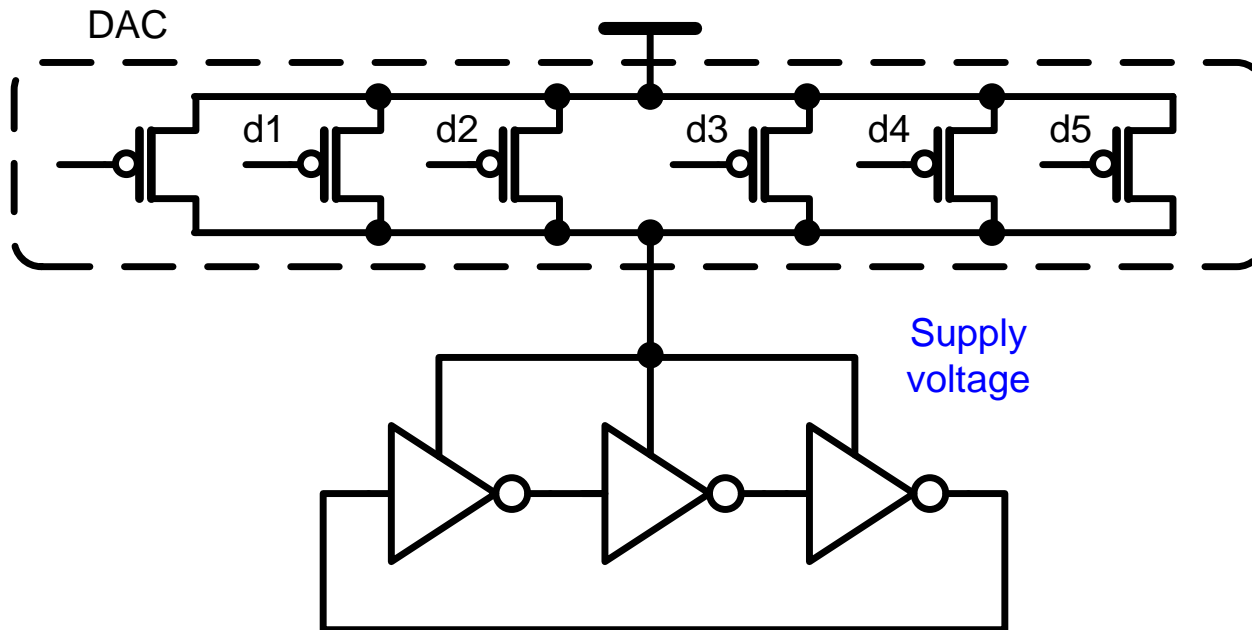


$$T_d = \frac{C_{load} V_{swing}}{I} = R_{eq} C_{load}$$

[1] V. Kratyuk, SOVC, 2006

Analog approach (3)

- **DAC + analog VCO**
 - **Control the voltage**

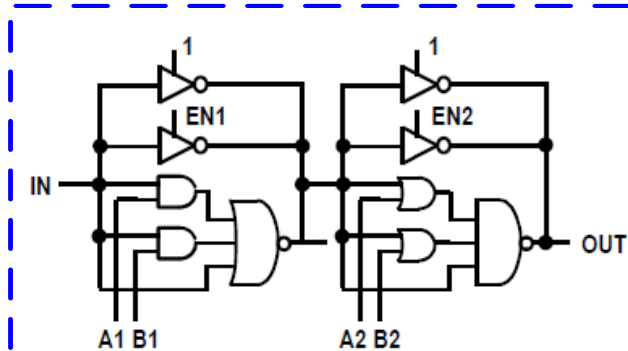
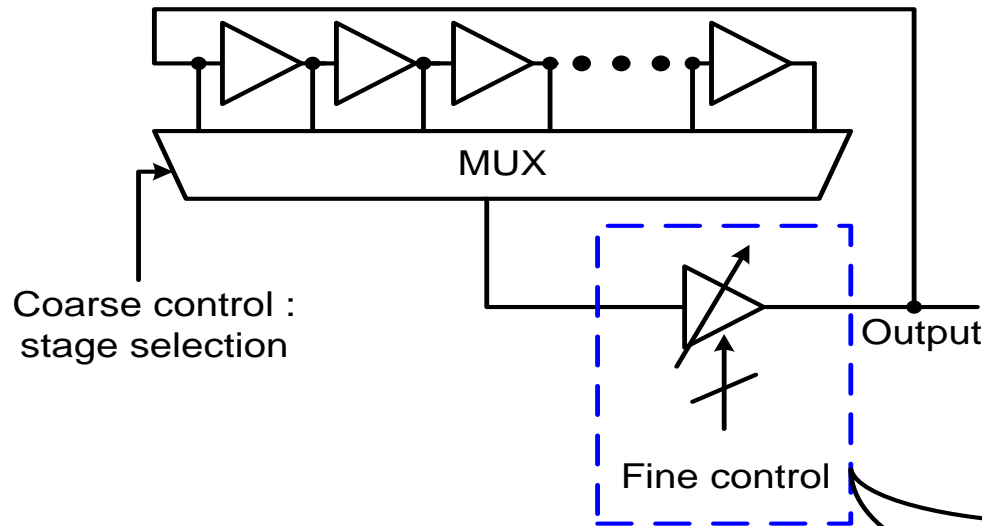


$$T_d = \frac{C_{load} V_{swing}}{I} = R_{eq} C_{load}$$

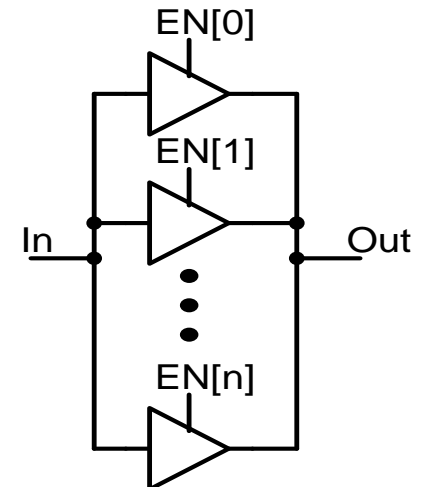
[2] D.Oh, ISSCC, 2007

Digital approach (1)

- **Stage selection + strength control**
 - All components are cell-based



Fine control :
Combination delay path



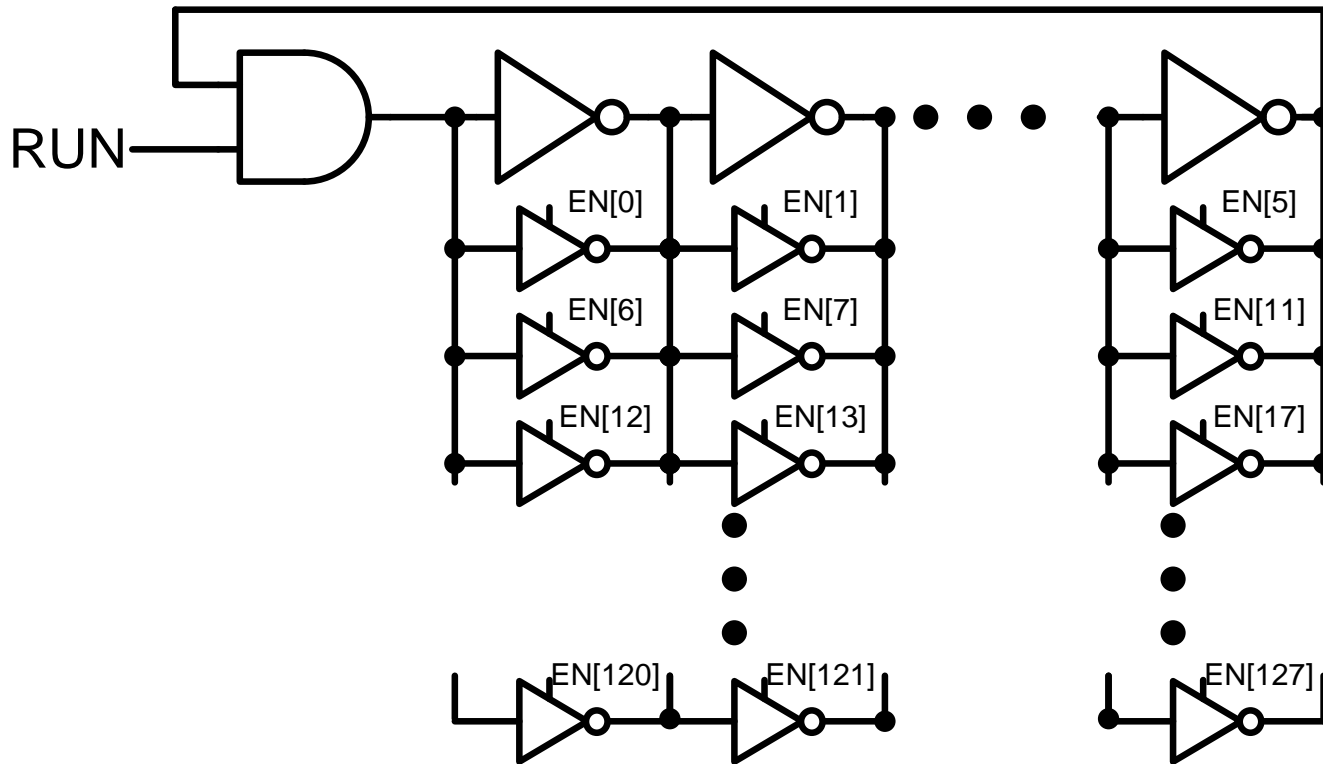
Fine control :
Strength selection

[3] T.-Y.Hsu, TCAS II, 2001

[4] Ching-Che Chung, JSSC, 2003

Digital approach (2)

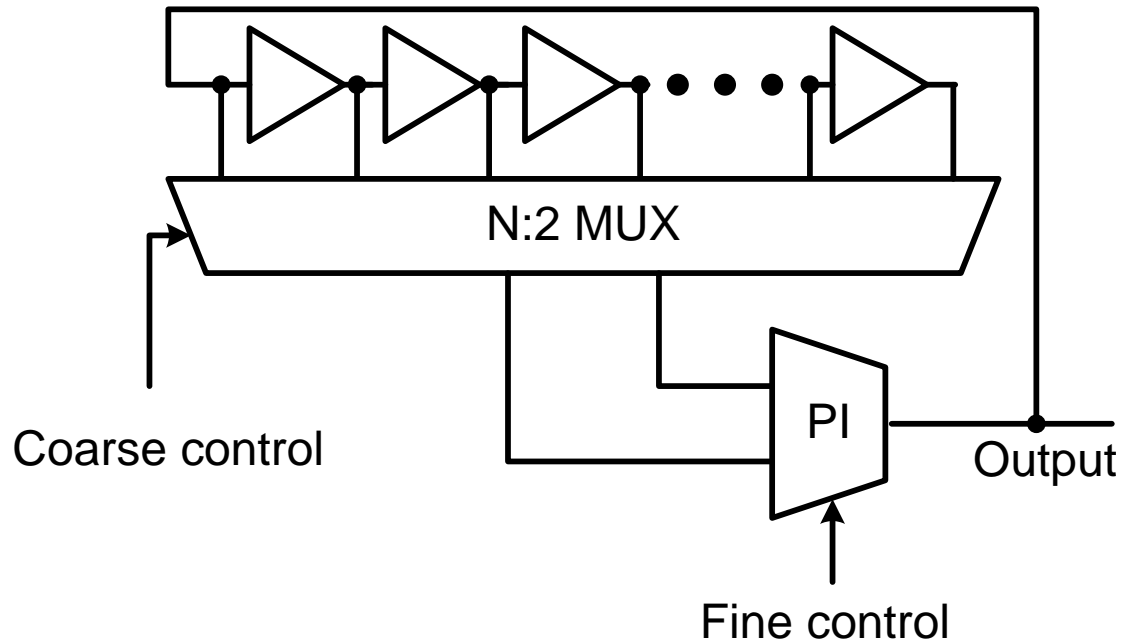
- Strength control



[5] T. Olsson, JSSC, 2004

Digital approach (3)

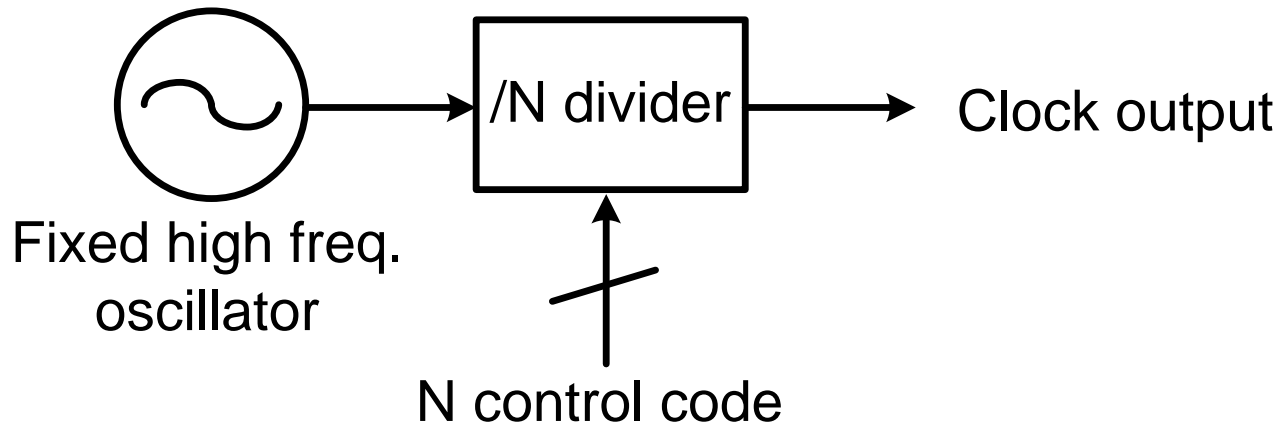
- **2-phase selection + phase interpolating**
 - **Control logic includes a FSM**



[6] S. Sidiropoulos, JSSC, 1997

Digital approach (4)

- **High freq. oscillator + integer freq. divider**
 - Low resolution
 - Used for wide-range applications



LC DCOs (1)

- **Frequency tuning scheme**

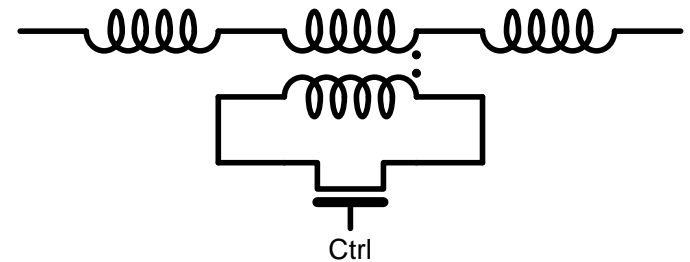
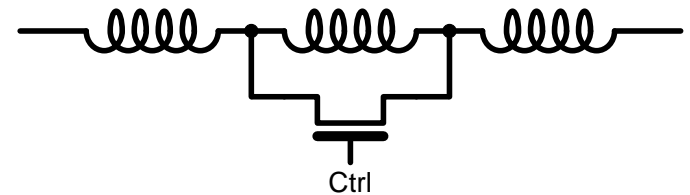
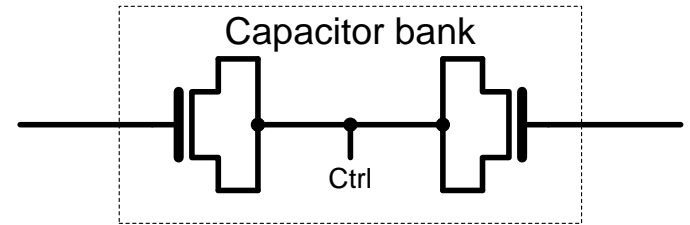
$$\omega_0 = \frac{1}{\sqrt{LC}}$$

- **Capacitance tuning**

- **MOS capacitance tuning**
- **For coarse/fine control**

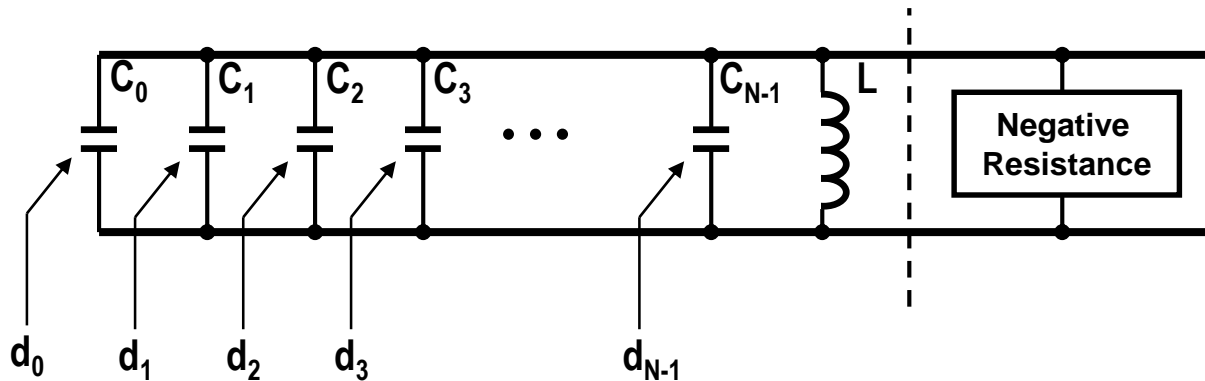
- **Inductance tuning**

- **Self/mutual inductance tuning**
- **For band selection or coarse control**
- **Suitable for dual mode operation**

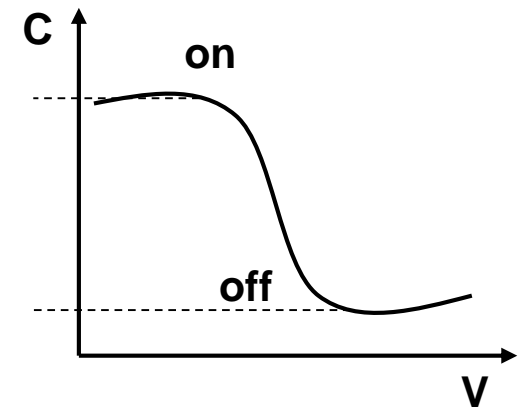


LC DCOs (2)

- **Segmented LC-VCO**
 - Change frequency by turning on/off binary- or equally-weighted small capacitances



$$\omega_0 = \frac{1}{\sqrt{LC}}$$



C-V curve of MOS capacitor in deep-submicron process

[7] R. B. Staszewski, TMTT, 2003

Outline

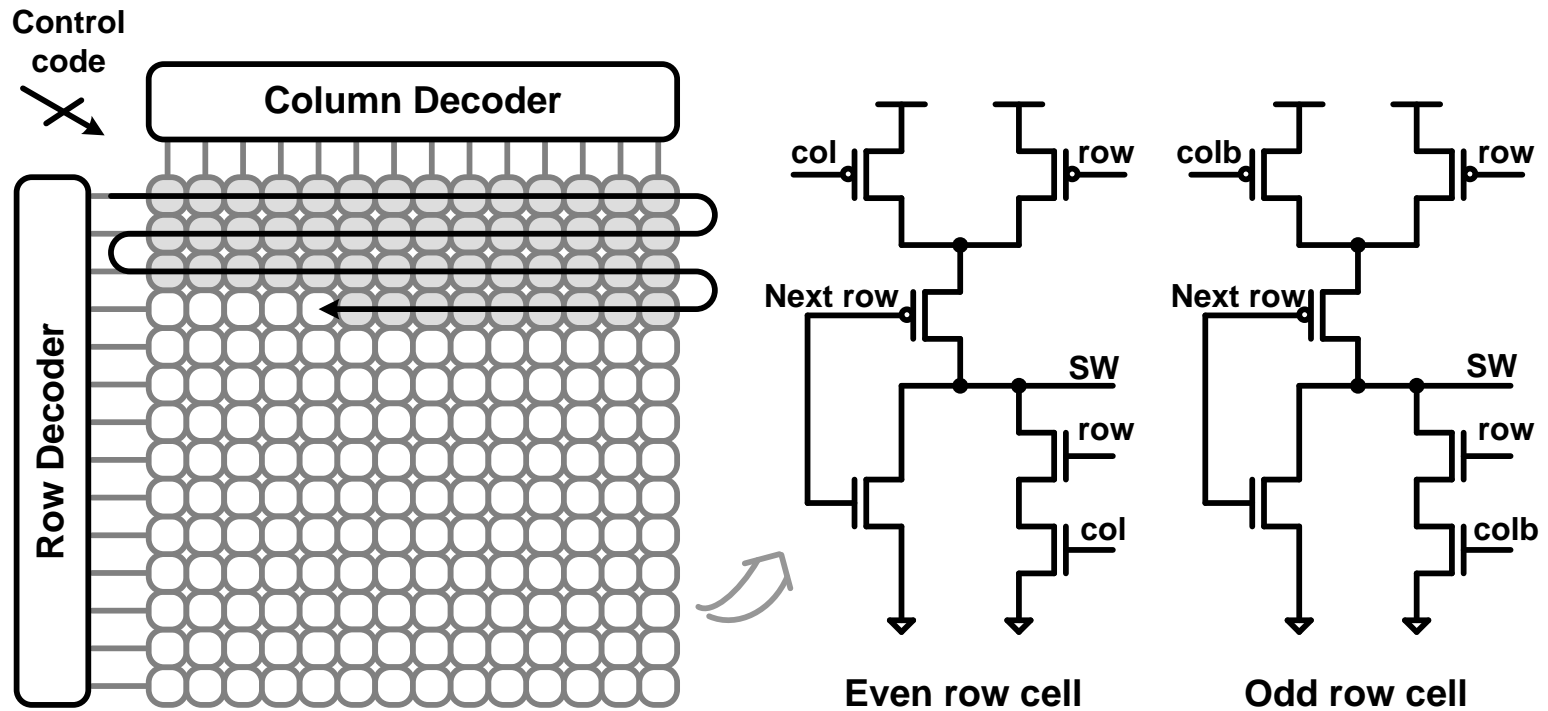
- Basic Operation
- Requirements
- Classification
- Design Example
- **Issues on DCO design**
- Case Studies

Trade-offs in LCDCOs

- **Capacitive tuning:** $\frac{\Delta f}{f_0} \approx \frac{1}{2} \frac{\Delta C}{C}$
 - **To enhance frequency resolution**
 - Increase capacitance
 - Low LC-tank Q due to the parasitic capacitance
 - Phase noise performance degradation
 - Increased power consumption due to large load capacitance
 - **Trade-off between frequency resolution, output frequency, tuning range, and power consumption**

Design Issues (1)

- **Reducing switching noise**
 - **Minimizing on/off switching**
 - **Only one column bit state changes**



[2] D. Oh, ISSCC, 2007

Design Issues (2)

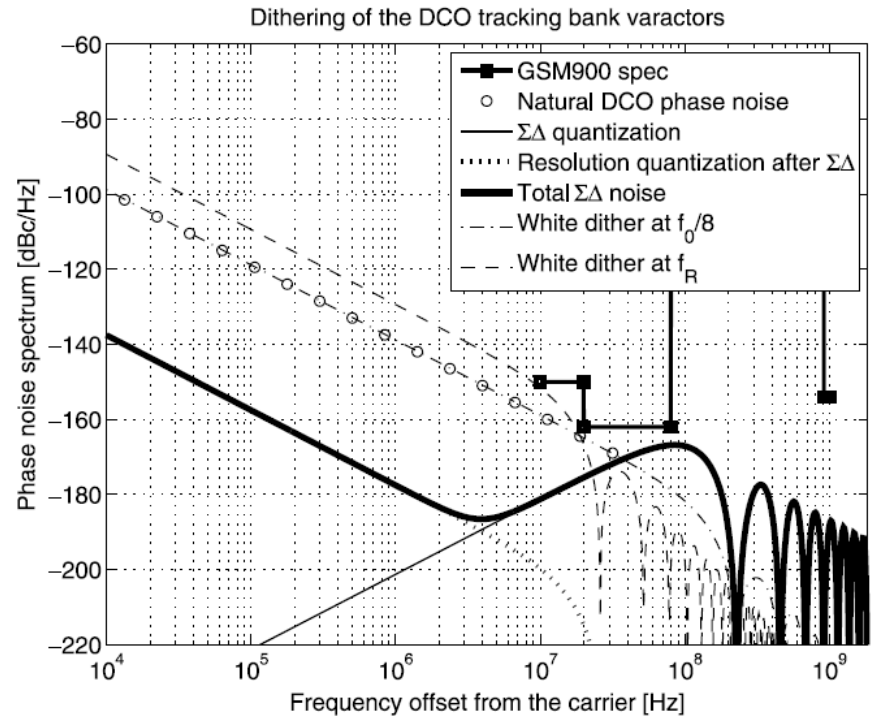
- **Frequency resolution**
 - **Quantization noise due to uniform dithering**

$$S_{\Phi}(f) = \frac{1}{12} \cdot \left(\frac{\Delta f_{res}}{f} \right)^2 \cdot \frac{1}{f_{dth}} \cdot \left(\text{sinc} \frac{f}{f_{dth}} \right)^2$$

- **Quantization noise due to $\Sigma\Delta$ modulation**

$$S_{\Phi_{\Sigma\Delta}}(f) = \frac{1}{12} \cdot \left(\frac{\Delta f_{res}}{f} \right)^2 \cdot \frac{1}{f_{dth}} \cdot \left(2 \sin \frac{\pi f}{f_{dth}} \right)^{2n}$$

- **Directly affect phase noise performance**
- **Performance bottleneck in some application**



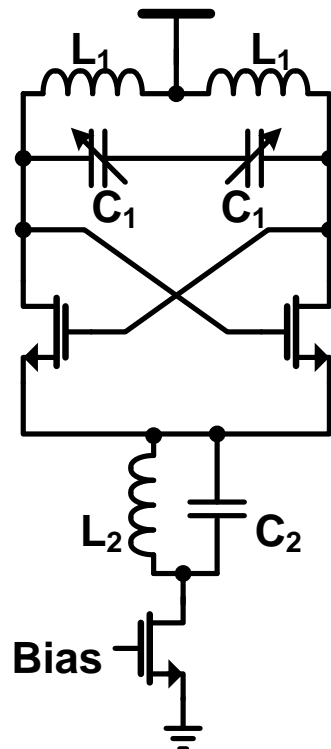
[9] R. B. Staszewski, JSSC, 2005

Design Issues (3)

- **Choice for negative g_m device**
 - **NMOS**
 - Smallest parasitic capacitance for same g_m
 - Output swing exceeds the supply voltage
 - **PMOS**
 - Lower 1/f noise in most process(not always)
 - **CMOS**
 - Large parasitic capacitance
 - Low signal distortion
 - Min. & Max. output voltage is fixed

Design Issues (4)

- **Noise on current source**
 - The drain node of the current source has a ripple of 2x output frequency
 - Additional LC for high Z to the current source



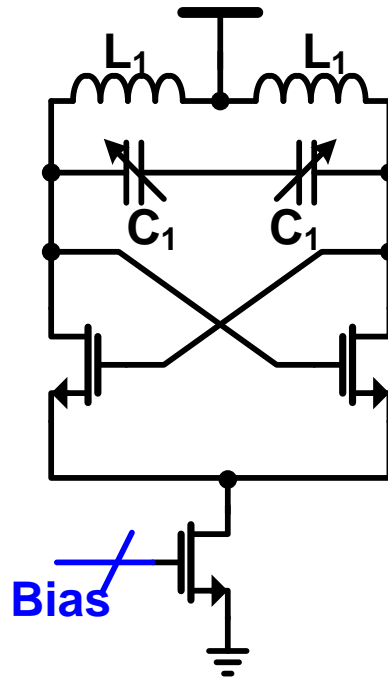
$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$$

$$2\omega_0 = \frac{1}{\sqrt{L_2 C_2}}$$

[9] R. B. Staszewski, JSSC, 2005

Design Issues (5)

- **Current source sizing**
 - According to the operating frequency, the optimum size changes
 - Digital code controls the current source

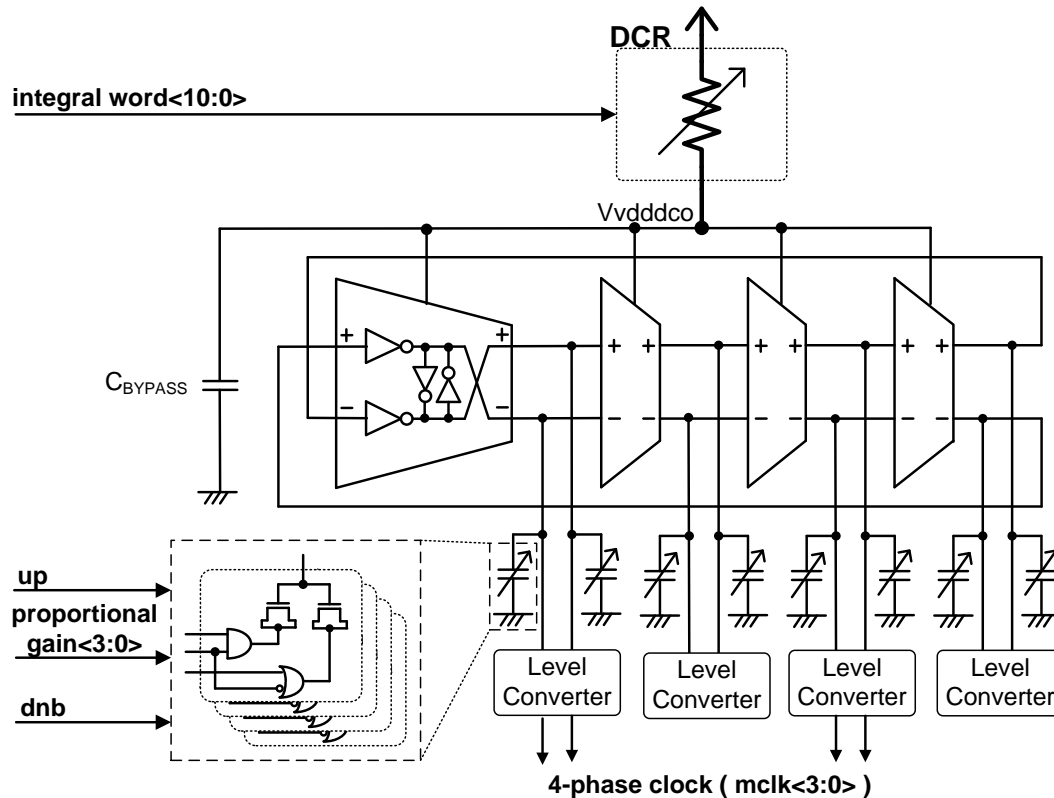


[8] R. B. Staszewski, JSSC, 2005

Outline

- Basic Operation
- Requirements
- Classification
- Design Example
- Issues on DCO design
- **Case Studies**

Monotonic DCO (1)

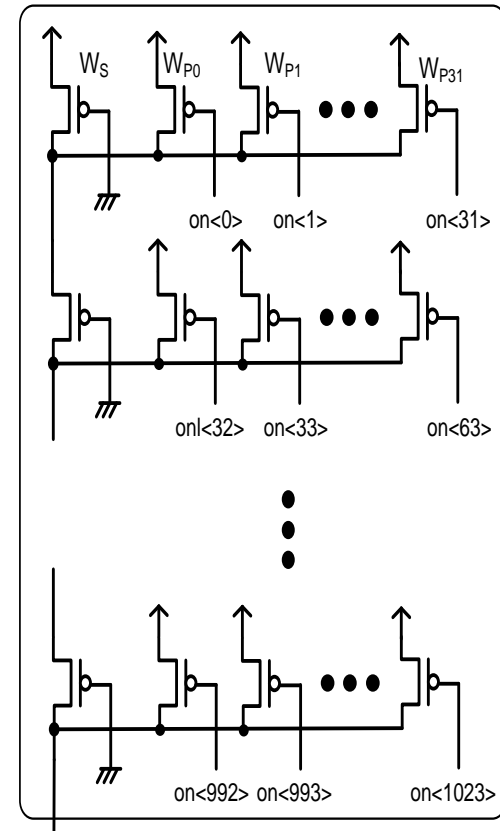


- **Core oscillator : inverter-based 4-stage delay element**
 - Integral word \rightarrow control supply of the core oscillator
 - PD outputs \rightarrow altering load capacitor

[16] H. Song, JSSC

Monotonic DCO (2)

- **Digitally controlled resistor (DCR)**
 - Stacked row cells of PMOS array
 - monotonic characteristics
- **Linear characteristics by non-uniformly sizing of $W_{P1}, W_{P2}, \dots, W_{P31}$**

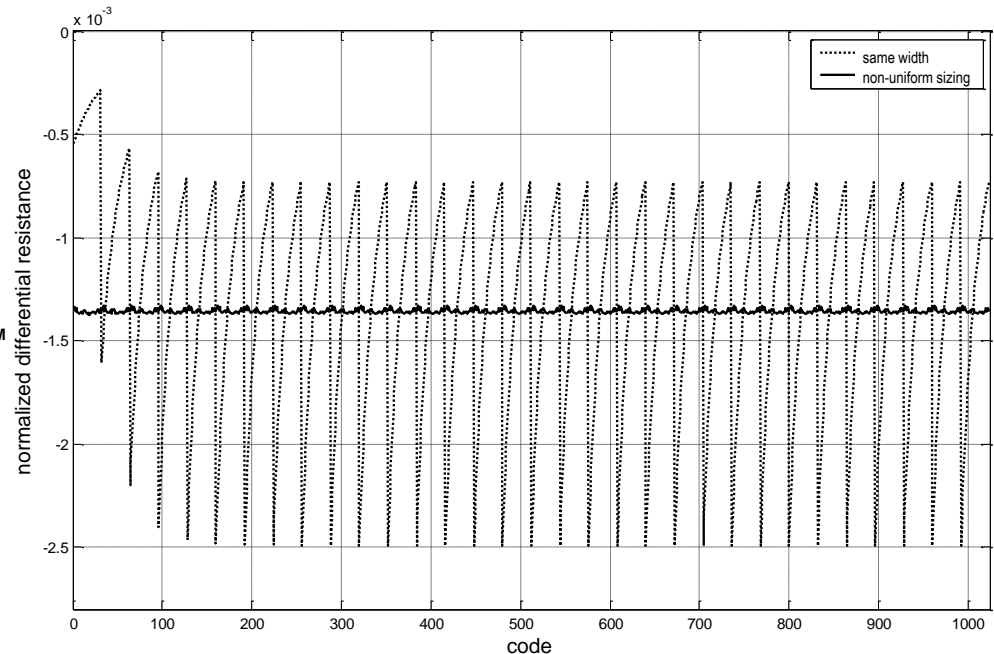
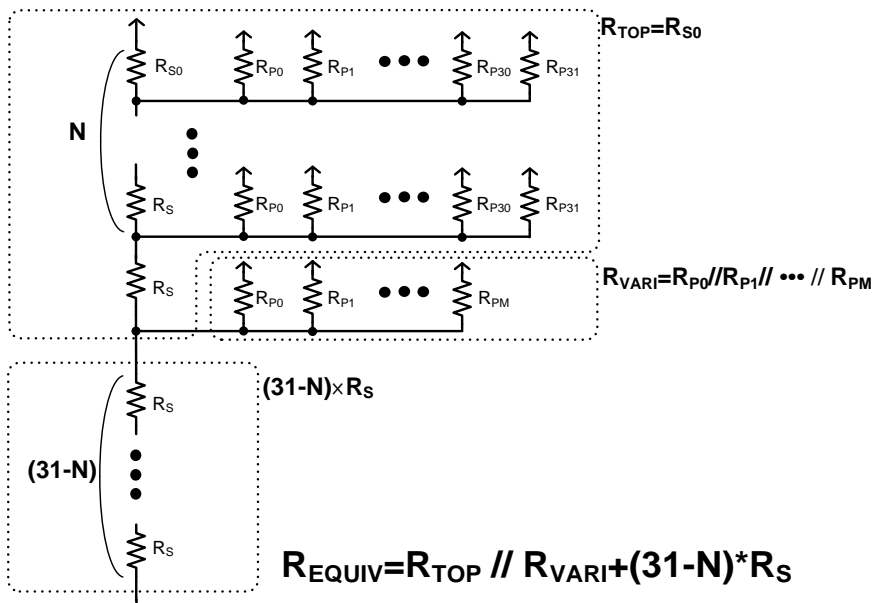


[16] H. Song, JSSC

Monotonic DCO (3)

- Simulation results of the DCR with non-uniformly sized parallel PMOSs
 - Resistance range : 330 Ω ~ 3.3 k Ω

integral word = $2^5 * N + M$ ($N, M = 0 \sim 31$)

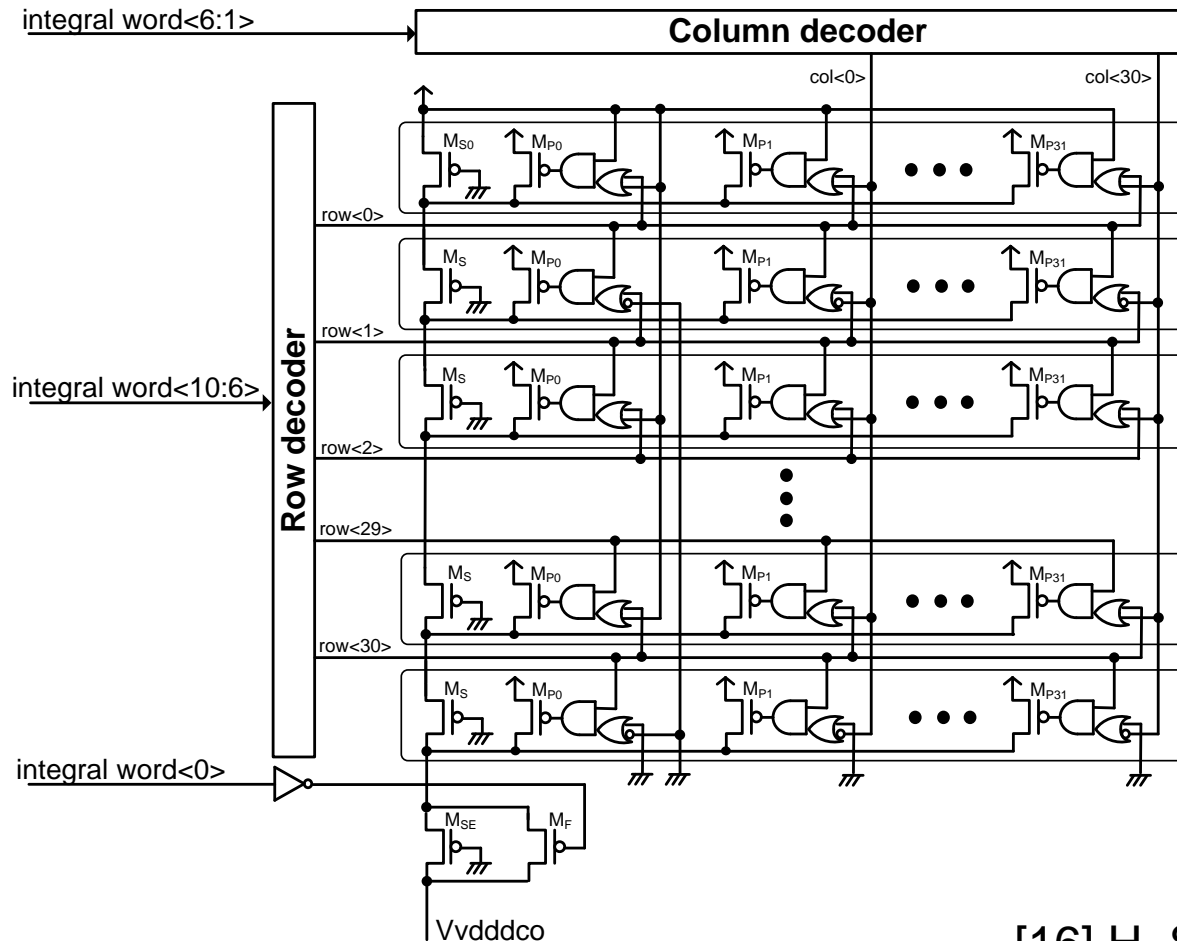


same width: $R_{S0} = R_S, R_{P0} = R_{P1} = \dots = R_{P31}$
 Non-uniform sizing: $R_{S0} > R_S, R_{P0} > R_{P1} > \dots > R_{P31}$

[16] H. Song, JSSC

Monotonic DCO (4)

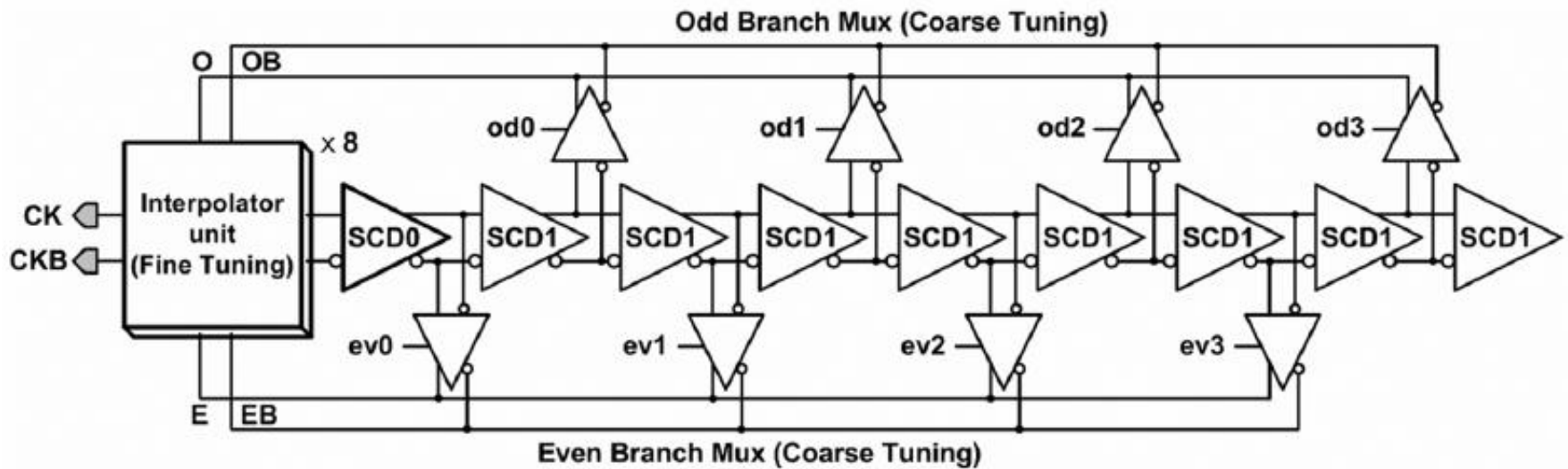
- Implementation of the DCR



[16] H. Song, JSSC

V-Tolerant DCO (1)

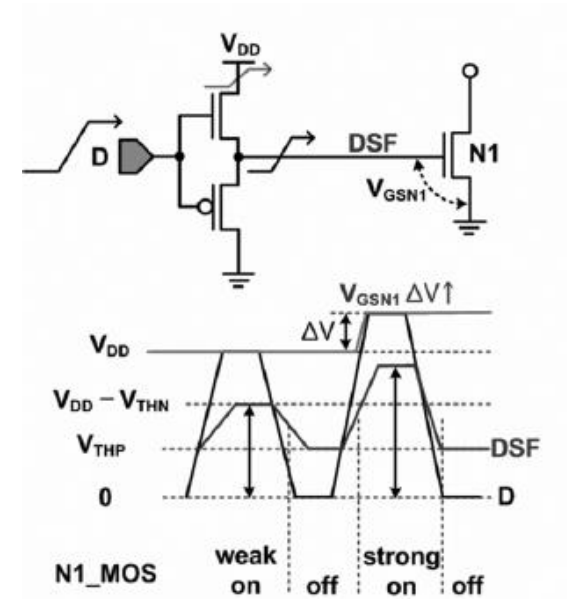
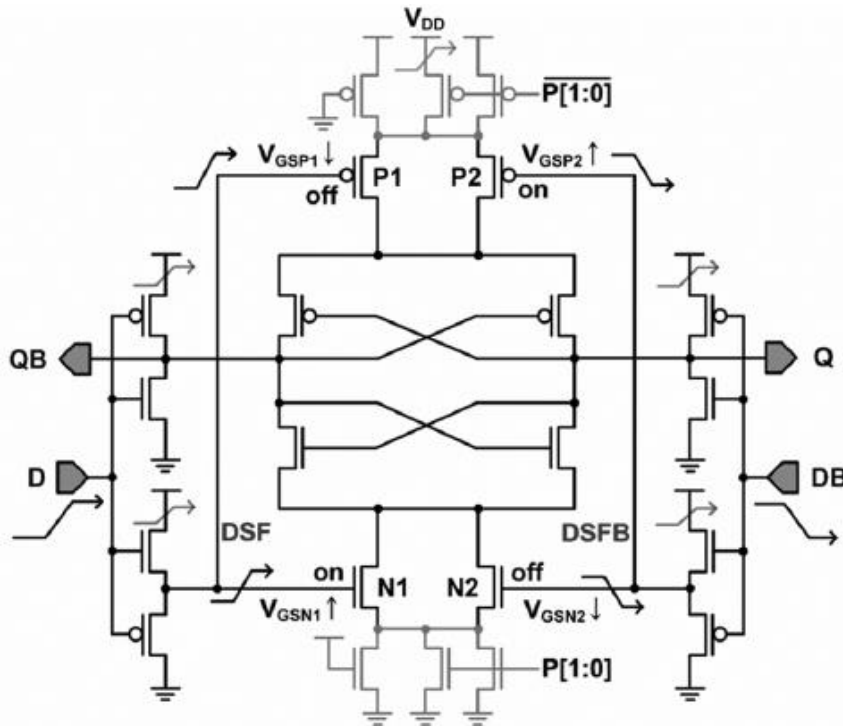
- **Supply-compensated delay cell**
 - Coarse : stage selector
 - Fine : phase interpolator



[14] B. M. Moon, TCAS II, 2008

V-Tolerant DCO (2)

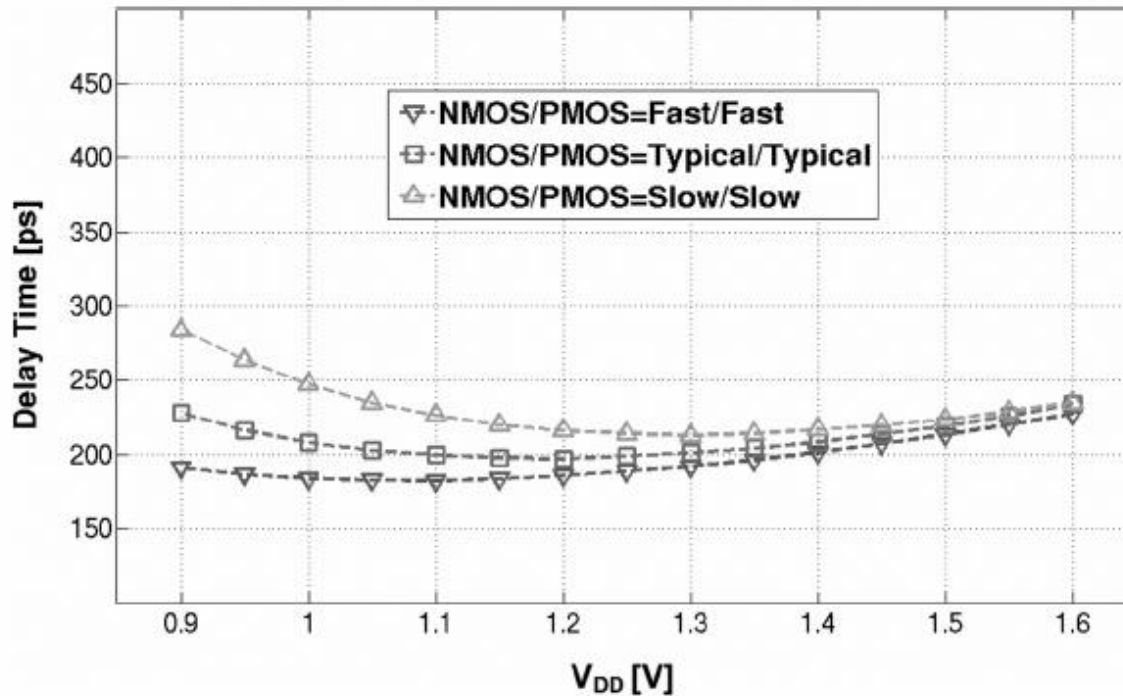
- **Supply-compensated delay cell**
 - The strength of the latch is controlled by V_{th} (PMOS) and $V_{DD} - V_{th}$ (NMOS).



[14] B. M. Moon, TCAS II, 2008

V-Tolerant DCO (3)

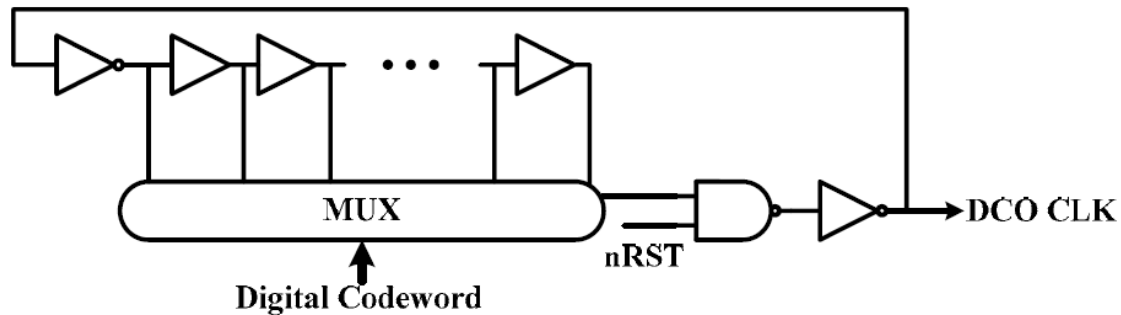
- **Supply-compensated delay cell**
 - Delay time is insensitive to the supply voltage.



[14] B. M. Moon, TCAS II, 2008

Fast locking ADPLL (1)

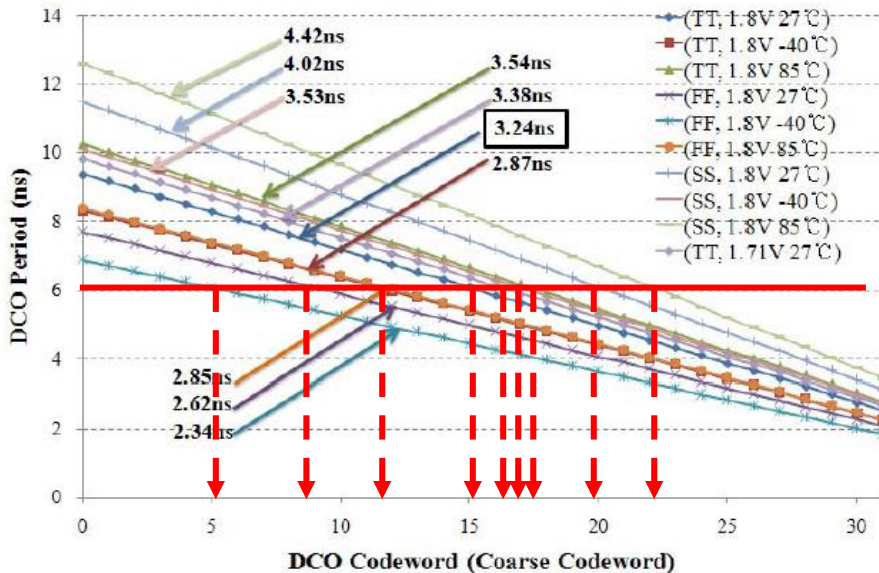
- **DCO code prediction for fast locking**
 - Using reference clock, PVT sensor detects current condition.
 - DCO code prediction makes a fast locking



[15] H. S. Jeon, ISCAS, 2008

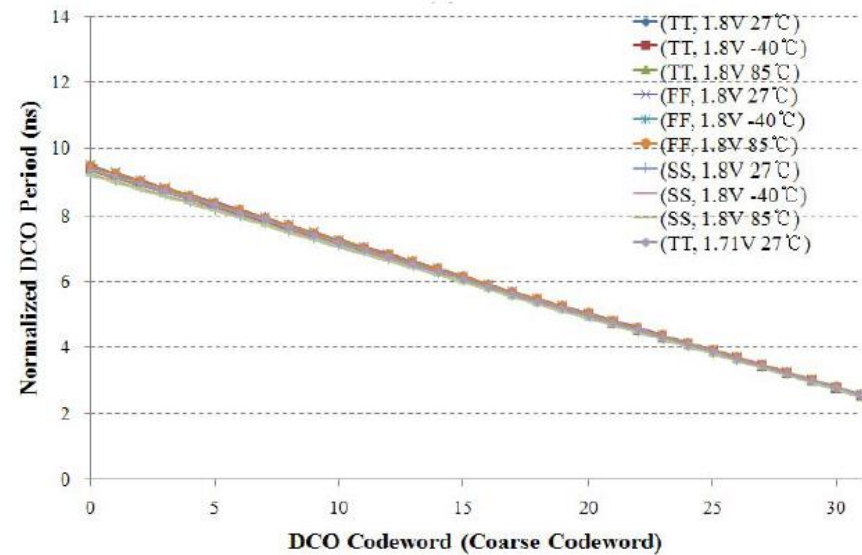
Fast locking ADPLL (2)

- DCO code prediction for fast locking
 - By normalizing, PVT variation can be cancelled



(a) DCO period

Predicted codeword for 6ns period



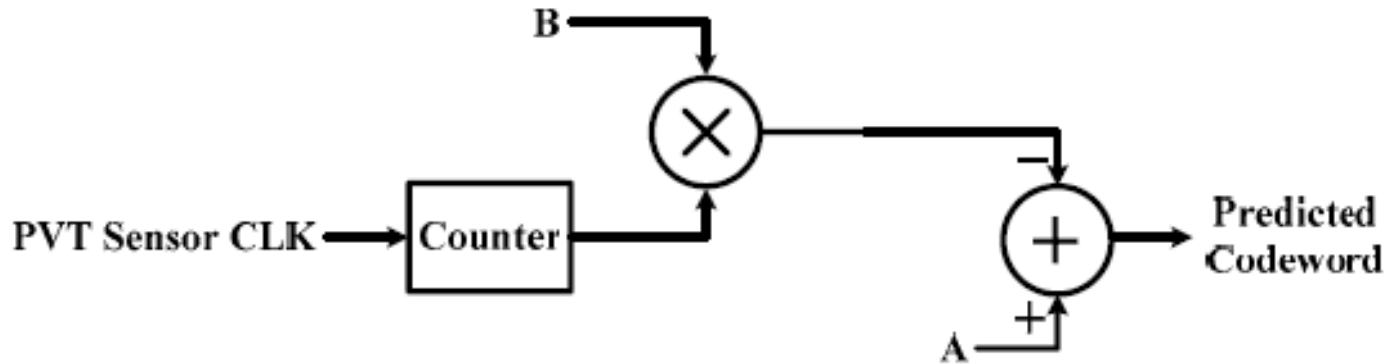
(b) DCO normalized period

$$T_{DCO}^{Norm} = T_{DCO}^C \times (T_{Sen}^R / T_{Sen}^C)$$

[15] H. S. Jeon, ISCAS, 2008

Fast locking ADPLL (3)

- DCO code calculation
 - DCO code predictor



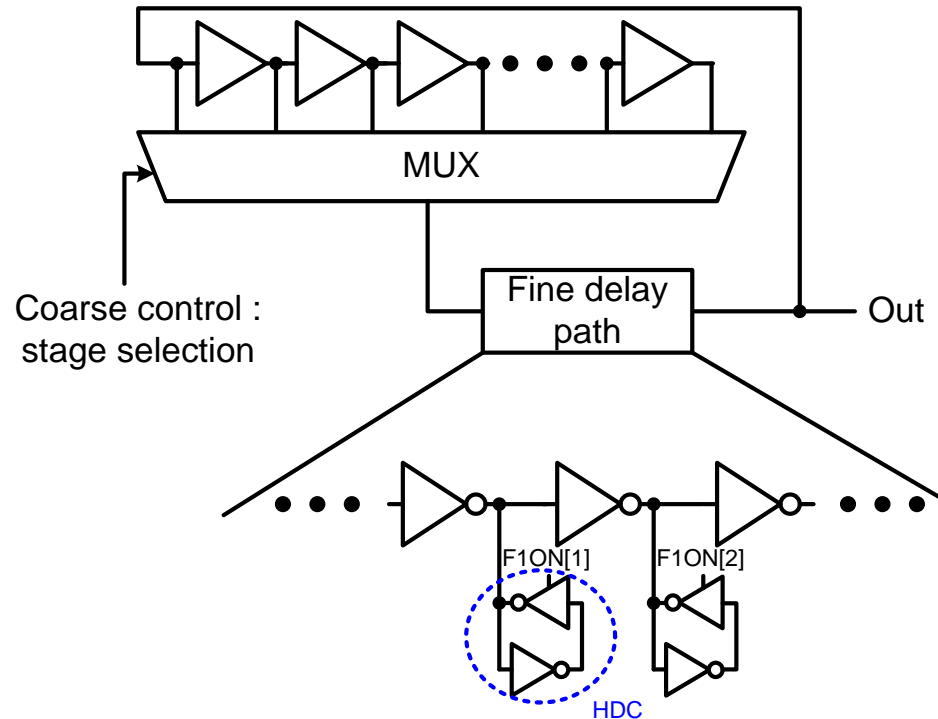
$$\begin{aligned}
 \text{codeword} &= \frac{T_{DCO}^{R,Max} \times (F_{Sen}^R / F_{Sen}^C) - T_{desired}}{T_{DCO}^{R,Max} \times (F_{Sen}^R / F_{Sen}^C) - T_{DCO}^{R,Min} \times (F_{Sen}^R / F_{Sen}^C)} \\
 &= \left(\frac{T_{DCO}^{R,Max}}{T_{DCO}^{R,Max} - T_{DCO}^{R,Min}} \right) - \left(\frac{T_{Sen}^R}{T_{DCO}^{R,Max} - T_{DCO}^{R,Min}} \times T_{desired} \times F_{Sen}^C \right) \\
 &= A - (B \times F_{Sen}^C)
 \end{aligned}$$

Precalculated in simulation

[15] H. S. Jeon, ISCAS, 2008

Fine-Resolution DCO (1)

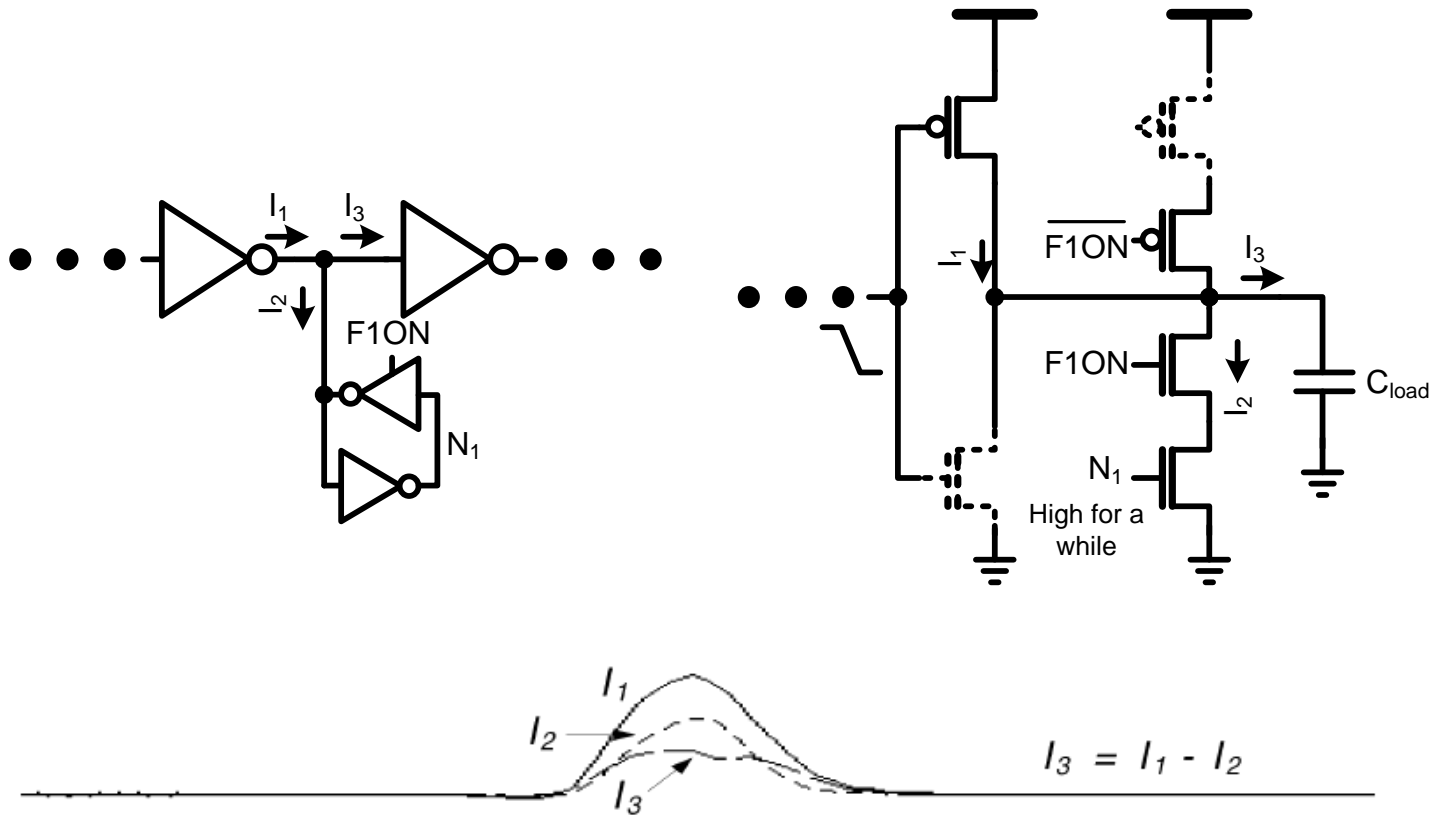
- **Hysteresis delay cell**
 - **Coarse stage : selecting delay path**
 - **Fine stage : hysteresis delay cell**



[13] D. Sheng, TCAS II, 2007

Fine-Resolution DCO (2)

- Hysteresis delay cell



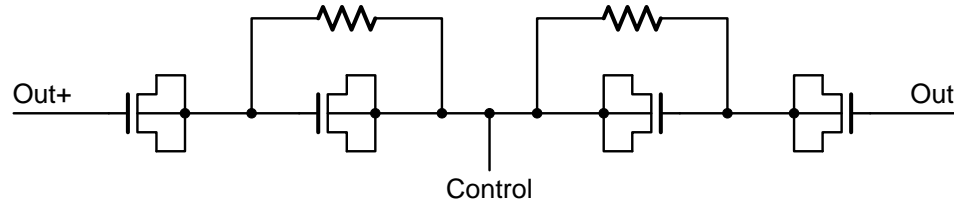
[13] D. Sheng, TCAS II, 2007

Frequency Resolution

- **Phase noise of LC DCO is affected by the frequency resolution**
- **Δf is linearly proportional to ΔC**
- **Output frequency: ~ GHz**
 - **Required Δf : ~ kHz**
 - **Required minimum ΔC : ~ aF**
 - **Minimum ΔC depends on the minimum feature size of the process**
 - **Various studies focus on ΔC minimization**

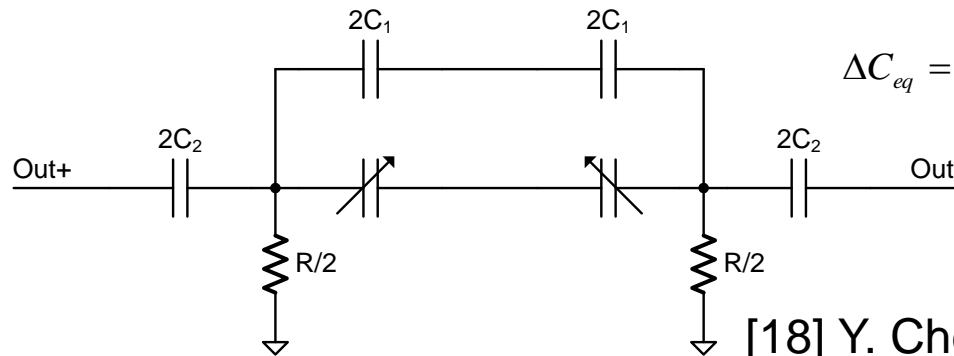
Capacitance Minimization Techniques

- **Capacitors in series**



[17] X. Dai, ISIC, 2009

- **Capacitive divider network**



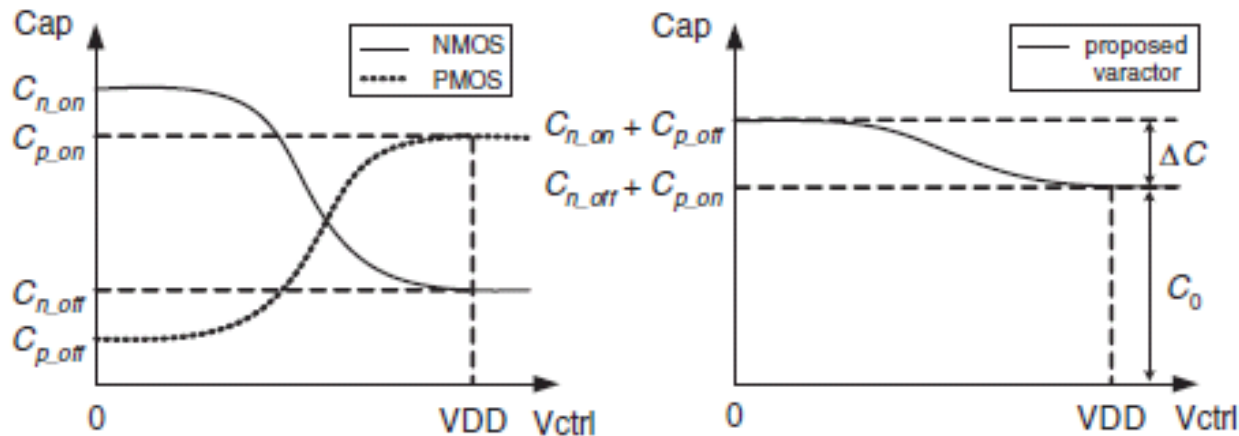
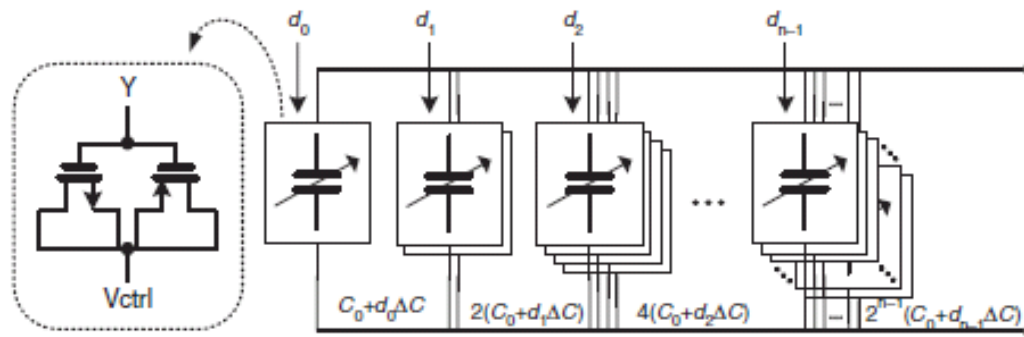
$$\Delta C_{eq} = \left(\frac{C_2}{C_0 + C_1 + C_2} \right)^2 \Delta C$$

[18] Y. Chen, A-SSCC, 2007

- **Vulnerable to process variation, parasitic, and mismatch**

Fine-Resolution LC-DCO (1)

- NMOS-PMOS varactor bank



[11] J. H. Han, EL, 2008

Fine-Resolution LC-DCO (2)

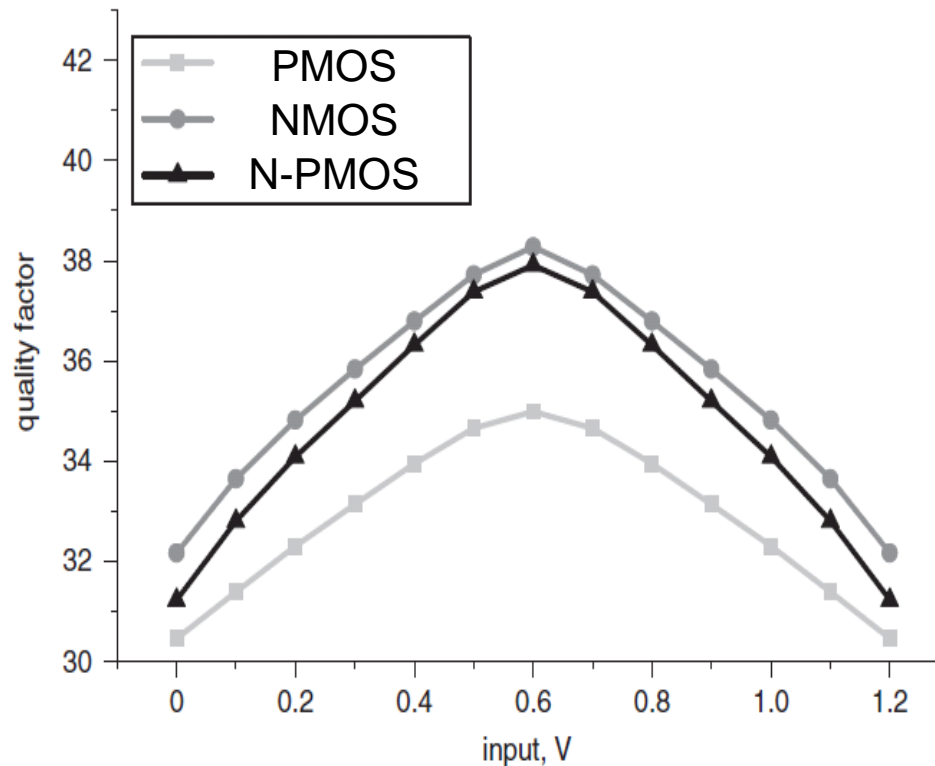
- **NMOS-PMOS varactor bank**
 - **Capacitance of MOSFET in various process**

| Process | NMOS | | | PMOS | | | NMOS-PMOS | | |
|---------|----------|-----------|------------|----------|-----------|------------|-----------|-----------|------------|
| | C_{on} | C_{off} | ΔC | C_{on} | C_{off} | ΔC | C_{on} | C_{off} | ΔC |
| 65nm | 200a | 104a | 96a | 183a | 94a | 89a | 294a | 287a | 7a |
| 90nm | 253a | 143a | 110a | 266a | 159a | 107a | 413a | 409a | 4a |
| 130nm | 3.7f | 2.0f | 1.7f | 3.4f | 1.6f | 1.8f | 5.2f | 5.4f | -0.2f |
| 180nm | 4.2f | 2.2f | 2.0f | 4.6f | 2.5f | 2.1f | 6.7f | 6.8f | -0.1f |

[11] J. H. Han, EL, 2008

Fine-Resolution LC-DCO (3)

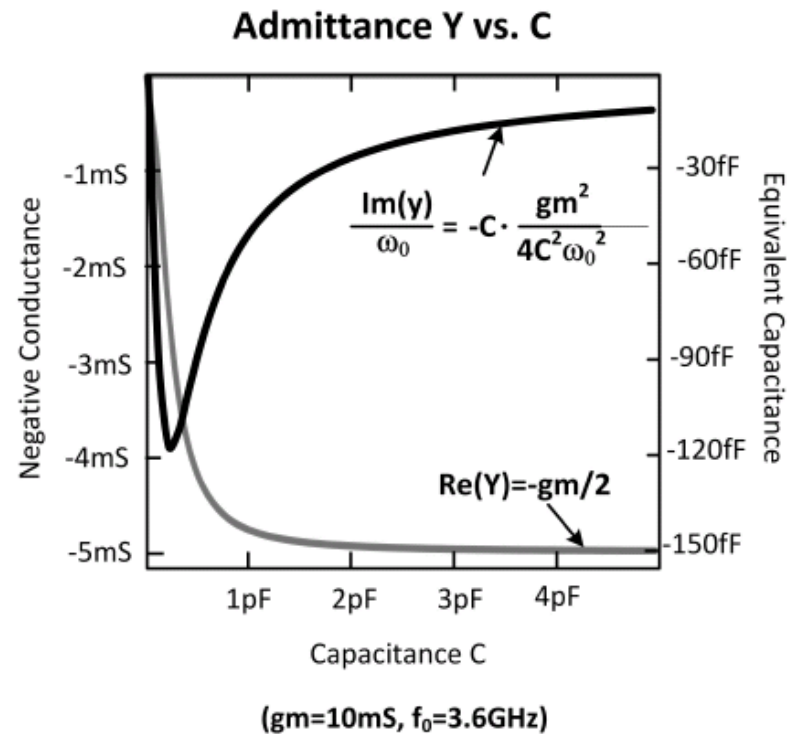
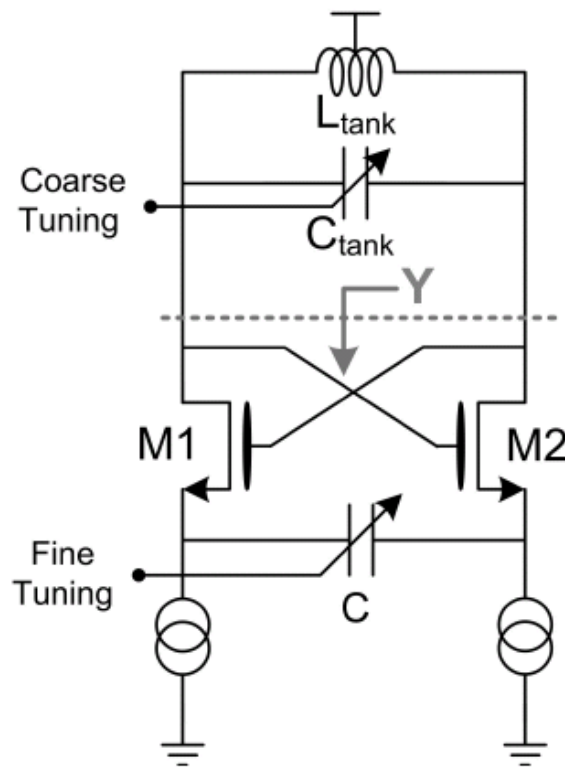
- **NMOS-PMOS varactor bank**
 - **Quality factors of the varactors**



[11] J. H. Han, EL, 2008

Fine-Resolution LC-DCO (4)

- **Source degeneration capacitor**
 - Capacitance shrinking factor ≈ 500 (@ $C=5\text{pF}$)

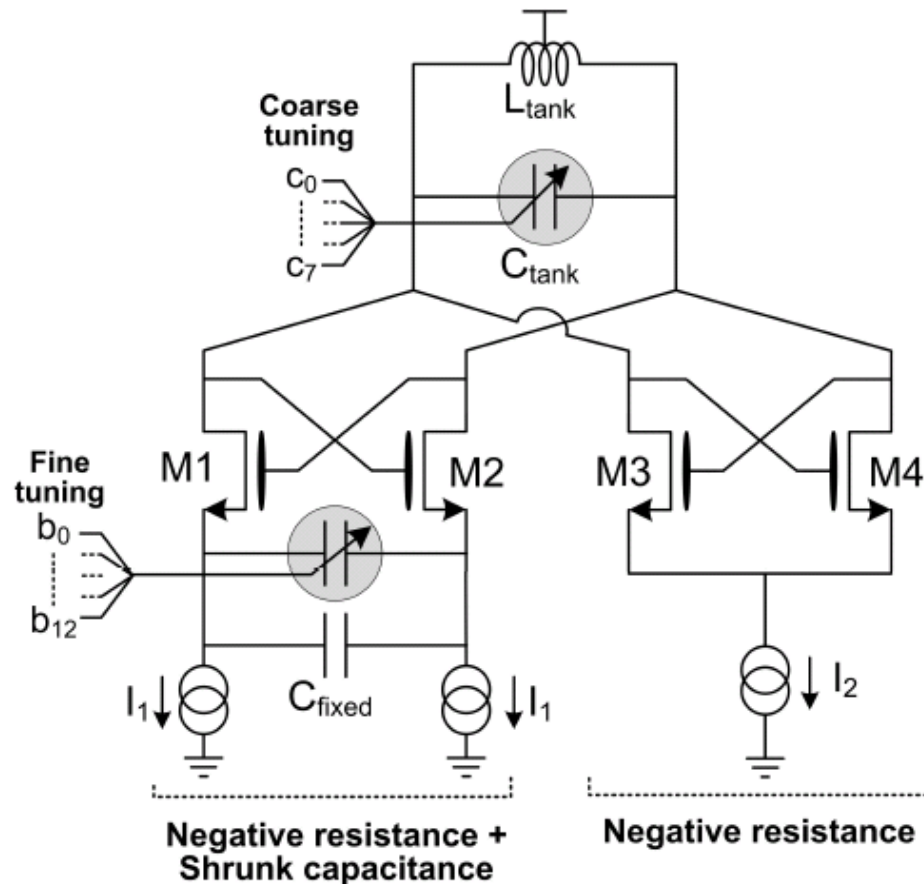


$$Y = -\frac{gm}{2} - j\omega_0 C \frac{g_m^2}{(2\omega_0 C)^2}$$

[12] L. Fanori, ISSCC, 2010

Fine-Resolution LC-DCO (5)

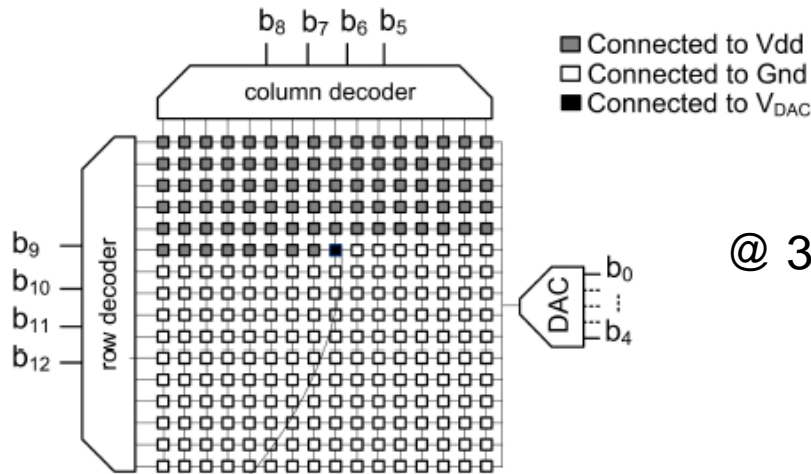
- Source degeneration capacitor



[12] L. Fanori, ISSCC, 2010

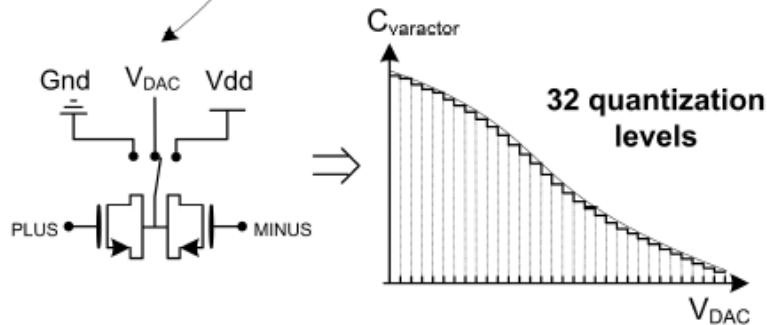
Fine-Resolution LC-DCO (6)

- **Source degeneration capacitor**
 - Adding 4-bit DAC for higher resolution



@ 3.3GHz with shrinking factor of 150

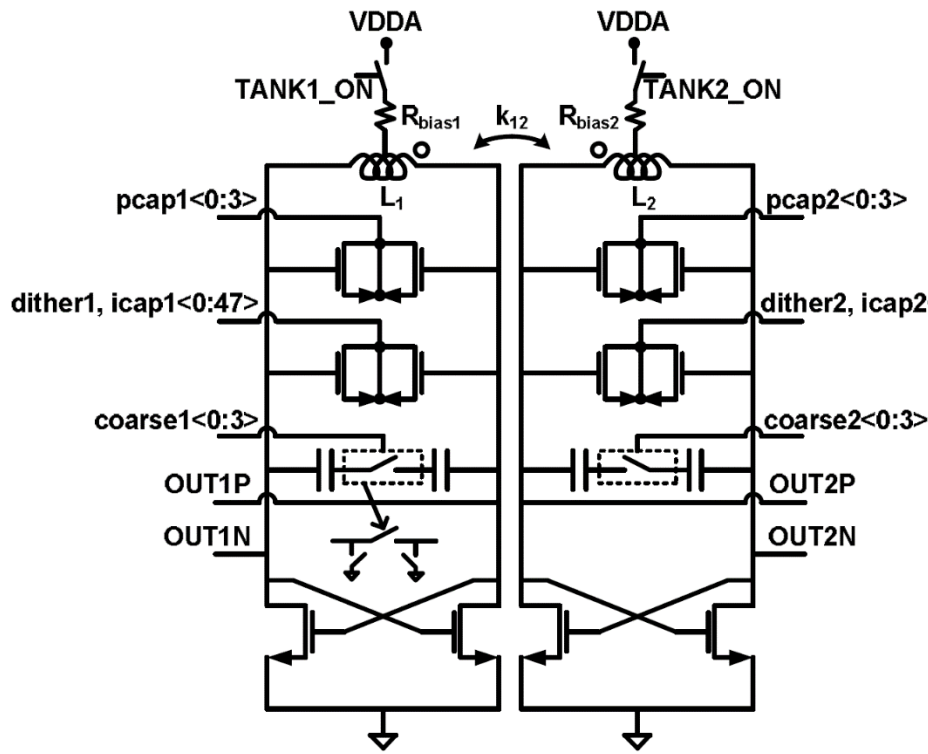
$$\overline{\Delta f} = 300Hz$$



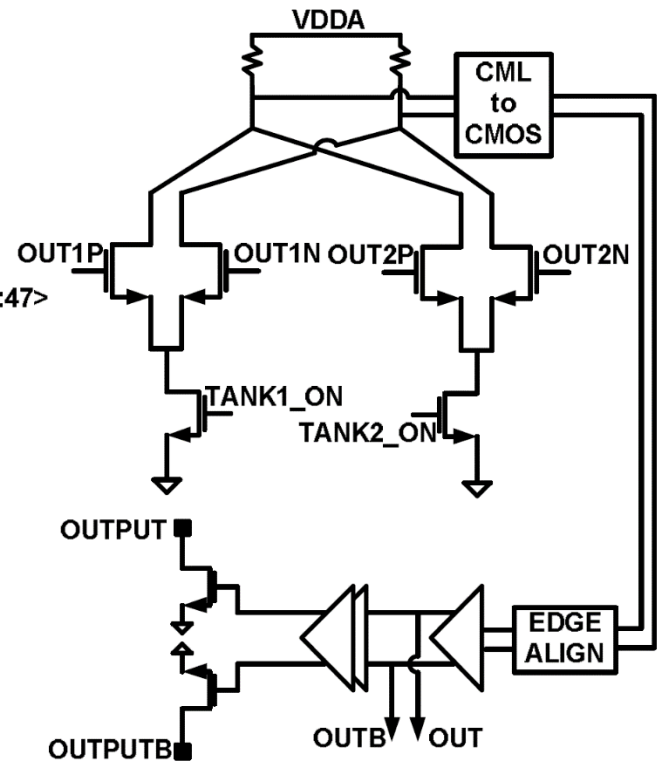
[12] L. Fanori, ISSCC, 2010

Dual-LC Tank DCO (1)

- Dual-LC tank DCO
 - Only one -gm cell is intended to be enabled



$$L_1=2.05\text{nH}, L_2=1.28\text{nH}, k_{12}=0.3$$

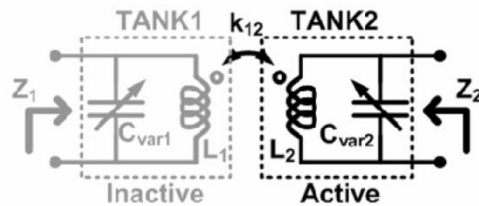


[19] A. Goel, SOVC, 2010

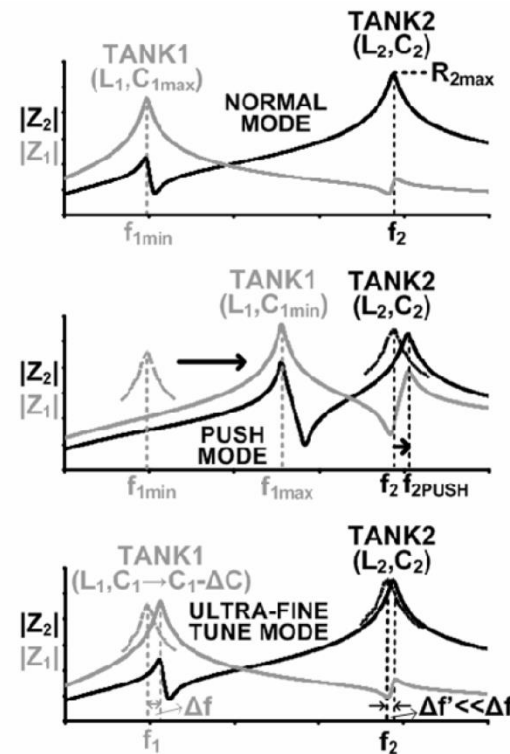
Dual-LC Tank DCO (2)

- **Coupled inductors**

- Behavior of active tank is influenced by the inactive tank
- Adjusting the resonance frequency of inactive tank results in three modes



| TANK2 MODE | C_{var1} | FEATURES |
|-----------------|----------------------------------|---------------------------------|
| Normal | C_{max} | High Q, Good Phase Noise |
| Push | C_{min} | Tuning Range Extension |
| Ultra-fine Tune | $C_1 \rightarrow C_1 - \Delta C$ | Ultra-fine frequency resolution |



[19] A. Goel, SOVC, 2010

Dual-LC Tank DCO (3)

- Performance summary

| DPLL with Dual LC Tank DCO | | |
|---|---|---|
| Technology | 45 nm SOI CMOS | |
| Core Area | 0.111 mm ² | |
| | TANK1 active | TANK2 active |
| Digital Core Power | 2.5 mA (1.0 V, 5.86 GHz) | 4.2 mA (1.0 V, 10.86 GHz) |
| Oscillator Core Power | 2.9 mA (1.0 V, 5.86 GHz) | 3.8 mA (1.0 V, 10.86 GHz) |
| Other DCO Power (Prescaler, Buffers) | 7.0 mA (1.1V, 5.86 GHz) | 11.7 mA (1.1V, 10.86 GHz) |
| Frequency Range | 5.85–8.86 GHz | 7.89–11.64 GHz |
| Push Mode Extension | 5.67–8.86 GHz | 7.89–12.09 GHz |
| RMS Jitter * | 218 fs (5.78 GHz) # 274 fs (5.98 GHz) 267 fs (8.3 GHz) | 227 fs (8 GHz) 295 fs (11.65 GHz) 362f s (12 GHz) # |
| Phase Noise for Free Running Oscillations (TANK1, 1 MHz offset) | -108.8 dBc/Hz (5.78 GHz) # -110.2 dBc/Hz (5.98 GHz) -103 dBc/Hz (8.3 GHz) | |
| Fine Tune Resolution (TANK2 in Band 16) | 20.2 MHz | |
| Ultra-fine Tune Mode Resolution (TANK2 in Band 16) | 0.7 MHz | |

* RMS Jitter is integrated from $f_c/1667$ to $f_c/2$

In Push Mode operation

Low Phase Noise LCVCO Comparisons

| Year | Publish | Title | VDD | power | Pnoise Calculation @20M, 0.9G |
|------|---------|--|----------|----------|----------------------------------|
| | | | [V] | [W] | |
| 2006 | ISSCC | A phase noise reduction technique for quadrature LC-VCO with phase to amplitude noise conversion | 1.8 | 2.77E-02 | -173.7 |
| 2010 | EL | [22]Low-phase-noise LC-VCO using high-Q 8-shaped inductor | 1.8(Reg) | 1.35E-02 | -171.9 |
| 2009 | IEEE MW | A CMOS backgate coupled QVCO based on Back-to-Back series Varactor configuration for minimal AM-to-PM noise conversion | 1.0 | 4.40E-03 | -170.3 |
| 2008 | ISSCC | A 28GHz Low phase Noise CMOS VCO using and amplitude redistribution Technique. | 2.5 | 6.70E-03 | -168.8 |
| 2001 | JSSC | A filtering Technique to lower LC oscillator Phase Noise | 2.5 | 9.25E-03 | -166.2 |
| 2003 | JSSC | A low phase noise 5GHz CMOS quadrature VCO using superharmonic coupling | 1.8 | 2.20E-02 | -165.7 |
| 2001 | JSSC | low-power Low phase Noise Differentially tuned quadrature VCO design in standard CMOS | 2.5 | 2.00E-02 | -165.5 |
| 2001 | JSSC | Low power low phase noise differentially tuned quadrature VCO design in standard CMOS | 2.5 | 2.00E-02 | -165.5 |
| 2010 | IEEE MW | [21]An UMTS and GSM Low Phase Noise Inductively Tuned LC VCO | 1.8 | 1.35E-02 | -165.0 |
| 2007 | IEEE | [18]A Low Phase Noise Quad-Band CMOS VCO with Minimized Gain | 2.6 | 4.42E-02 | -164.8 |
| 2002 | JSSC | Analysis and design of a 1.8 GHz CMOS LC quadrature VCO | 2 | 5.00E-02 | -162.5 |
| 2002 | JSSC | Analysis and design of a 1.8 GHz CMOS LC quadrature VCO | 2 | 5.00E-02 | -162.5 |
| 2007 | JSSC | A 1-V 17GHz 5mW CMOS quadrature VCO based on tranformer coupling | 1 | 5.00E-03 | -161.5 |
| 2002 | JSSC | A Noise shifting Differential Colpitts VCO | 2.5 | 1.00E-02 | -161.5 |
| 2009 | RFIC | Low phase noise gm-boosted differential Colpitts VCO with suppressed AM-to-FM conversion | 0.9V | 1.62E-03 | -160.2 |

Meet
GSM
Spec

Wide Tuning Ranges LCVCO Comparisons

| Year | Publish | Title | Inductor Tuning method | Truning range max/min x100 | Freq [Hz] | | | Process | VDD | power | Pnoise Calculation @20M,0.9G |
|------|---------|--|-------------------------------|----------------------------------|-----------|----------|----------|---------|---------|---------|---------------------------------|
| | | | | | min | center | max | | [V] | W | |
| 2006 | MTT | Switched resonator and Their Application in a dual band monolithic CMOS LC-Tuned VCO | Self 7.9n/3.2n | 110.6 | 1.64E+09 | 1.73E+09 | 1.81E+09 | 0.18u | 3.3~3.6 | 1.6E-02 | -159.5 |
| 2008 | JSSC | Design of wide Tuning-Range CMOS VCOs using switched coupled-inductors | Mutual | 160.1 | 7.34E+09 | 9.55E+09 | 1.18E+10 | 90n | 1.2 | 7.7E-03 | -154.3 |
| 2009 | JSSC | LC PLL with 1.2-Octave Locking Range based on mutual-inductance switching in 45nm SOI CMOS | Mutual k=0.48 0.1n/0.2n | 239.7 | 7.30E+09 | 1.24E+10 | 1.75E+10 | 45n | 1 | 1.4E-02 | -141.7 |
| 2005 | RFIT | Multi-mode wide-band 130 nm CMOS WLAN and GSM-UMTS | Mutual | 334.8 | 3.42E+09 | 7.44E+09 | 1.15E+10 | 0.13u | 1.5 | 3.0E-03 | -163.9 |
| 2007 | MTT | New Frequency Plan and Reconfigurable 6.6- 7.128 GHz CMOS Quadrature VCO for MB OFDM UWB Application | Self | 108.0 | 6.60E+09 | 6.86E+09 | 7.13E+09 | 0.18u | 2 | 2.0E-02 | -159.3 |
| 2000 | CICC | A new approach to fully integrated CMOS LC-oscillators with a very large tuning range | Self | 159.7 | 1.34E+09 | 1.74E+09 | 2.14E+09 | 0.35u | 3 | - | -132.5 |
| 2007 | EL | Wide tuning range LC-oscillator in 65nm SOI CMOS, based on switchable secondary inductor | Mutual 0.6n/0.3n | 176.6 | 6.40E+09 | 8.85E+09 | 1.13E+10 | 65n | 1 | 4.5E-03 | -143.8 |
| 2007 | JSSC | A Magnetically Tuned Quadrature Oscillator | Mutual + K control | 228.1 | 3.20E+09 | 5.25E+09 | 7.30E+09 | 65n | 1.2 | 2.4E-02 | -150.1 |
| 2009 | RFIC | 1.1 to 1.9GHz CMOS VCO for Tuner Application with Resistively Tuned Variable Inductor | Mutual + R | 177.4 | 1.06E+09 | 1.47E+09 | 1.88E+09 | 0.25u | 3 | 2.0E-02 | -148.4 |
| 2005 | ASSCC | A 1V Dual-Band VCO Using an Integrated Variable Inductor | Mutual + C | 513.6 | 2.20E+09 | 6.75E+09 | 1.13E+10 | 0.18u | 1 | 5.0E-03 | -154.5 |
| 2009 | CICC | A CMOS 3.3-8.4 GHz wide tuning range, low phase noise LC VCO | Self | 254.5 | 3.30E+09 | 5.85E+09 | 8.40E+09 | 0.13u | 1.6 | 1.5E-02 | -162.4 |
| 2002 | ESSCIRC | ESSCIRC A CMOS fully integrated 1 GHz and 2 GHz dual band VCO with a voltage controlled inductor | Self | 200.0 | 1.00E+09 | 1.50E+09 | 2.00E+09 | 0.25u | 1.5 | 1.4E-02 | -155.4 |
| 2007 | RFIT | A Dual Band CMOS Quadrature VCO for Low Power and Low Phase Noise Application | Self | 272.2 | 1.80E+09 | 3.35E+09 | 4.90E+09 | 0.18u | 1.7 | 6.8E-03 | -155.0 |

◆None can meet GSM spec.(-165dBc/Hz @ 900MHz freq, 20MHz offset).

◆There is trade-off between tuning range and phase noise.

Reference(1)

- [1] V. Kratyuk, et al. "A digital PLL with a stochastic time-to-digital converter" *IEEE SOVC, Dig. Tech. Paper*, June. 2006.
- [2] D. Oh, et al., "A 2.8Gbs All-Digital CDR with a 10b Monotonic DCO," *IEEE ISSCC Dig. Tech. Papers*, 2007.
- [3] T.-Y. Hsu, et al. "Design and analysis of a portable high-speed clock generator," *IEEE Trans. on Circuits and Systems. II*, Apr. 2001.
- [4] C.-C. Chung, et al. "An all-digital phase-locked loop for high speed clock generation," *IEEE J. Solid-State Circuits*, Feb. 2003.
- [5] T. Olsson, et al. "A Digitally Controlled PLL for SoC Applications," *IEEE J. Solid-State Circuits*, Vol. 39, No. 5, May 2004, pp 751-760, Feb. 2003.
- [6] S. Sidiropoulos, et al., "A semidigital dual delay-locked loop," *IEEE J. Solid-State Circuits*, Nov. 1997.
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- [9] R. B. Staszewski, et al. "A digitally controlled oscillator in a 90nm digital CMOS process for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2203-2211, Nov. 2005.
- [10] H. Shi, et al., "Variable Negative Gm Technique for RF LC VCO with Very Large Tuning Range," in *Electron Devices and Solid-State Circuits, 2005 IEEE Conference on*, pp. 145-148, 2005.
- [11] J. H. Han, et al., "Digitally controlled oscillator with high frequency resolution using novel varactor bank," *IEEE Electronics Letters*, vol. 44, no. 25, pp. 830-842, Dec. 2008.
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3.3. Time-to-Digital Converter

Deog-Kyoon Jeong

***Integrated Systems Design Laboratory
Seoul National University***

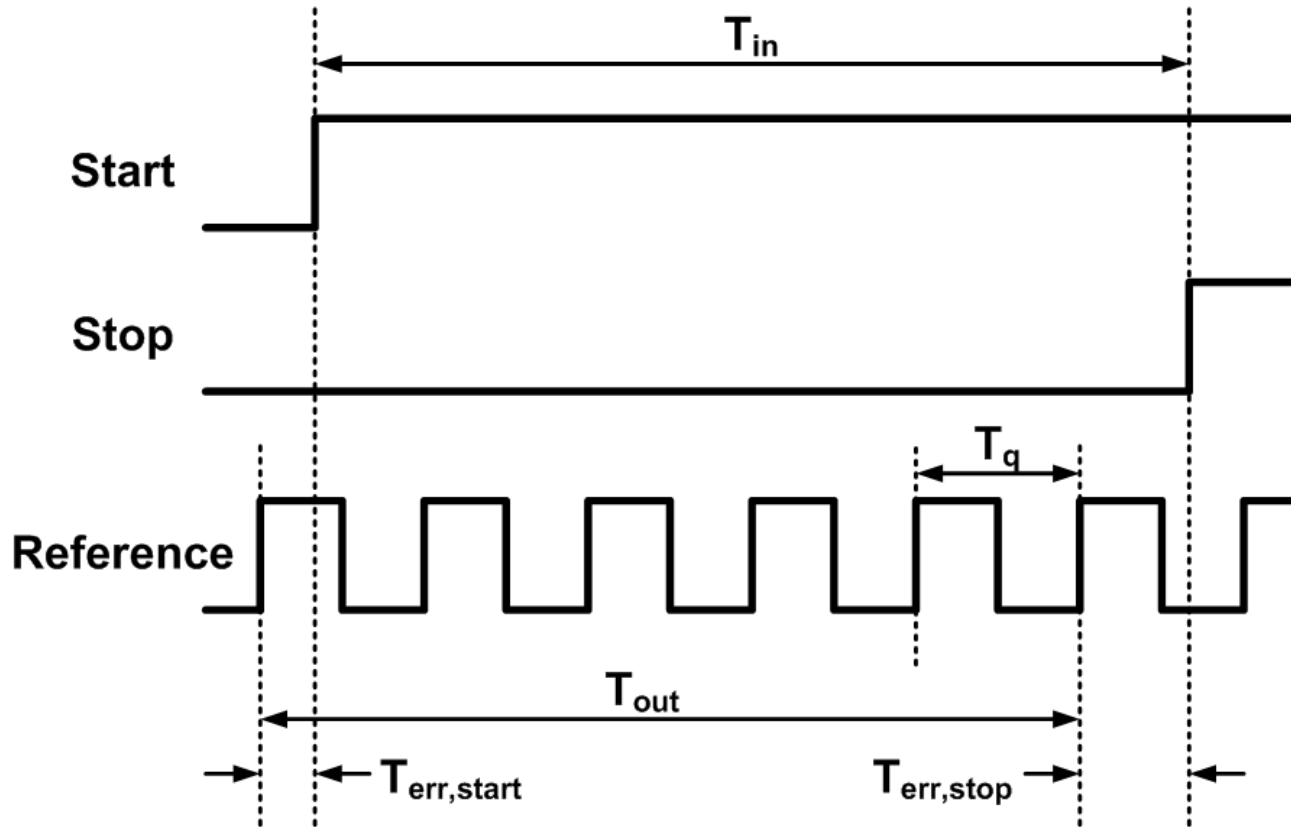
Outline

- **Introduction**
- **Basic Operation**
- **TDC Requirements**
- **TDC Classification**
 - **Short time interval generation**
 - **Time stretching**
 - **Etc**

Introduction

- **Time-to-digital converter(TDC) is a device for converting a time difference between two events into a digital representation of their time indices.**
 - **Time-of-flight(TOF) measurement in high energy particle physics, laser range finding and positive electron tomography(PET) medical imaging technology**
 - **On-chip timing and jitter measurements**
 - **Phase difference measurement in All-digital PLL and All-digital DLL**

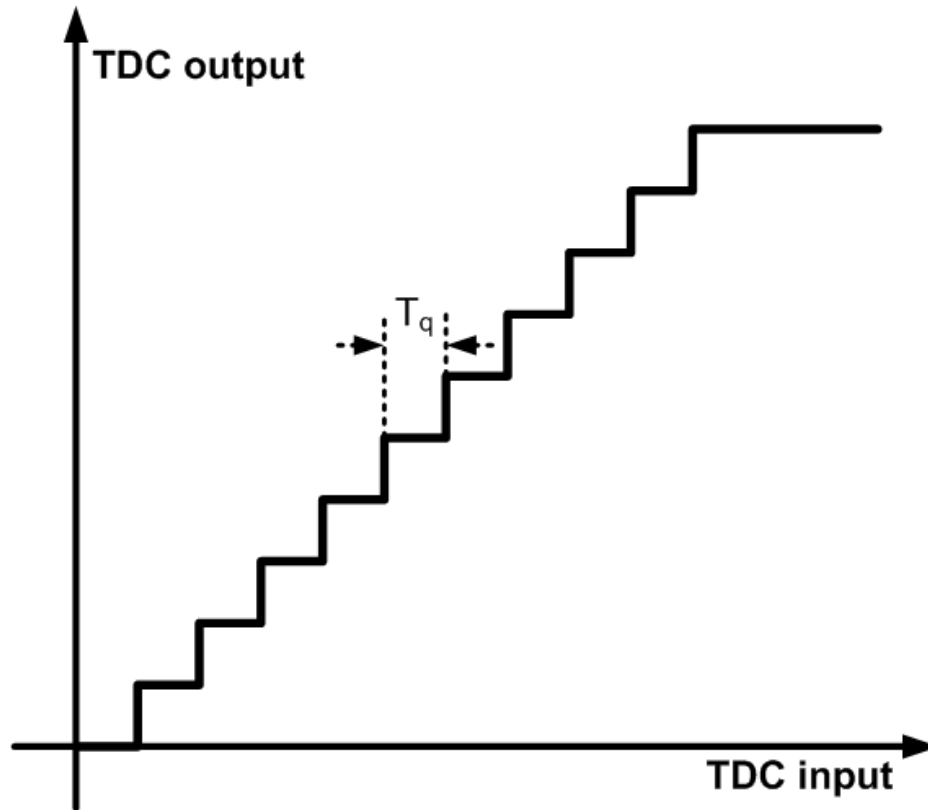
Basic Operation(1)



$$\mathbf{TDC}_{OUT} = \frac{T_{out}}{T_q} = \frac{T_{in} - T_{err}}{T_q}, \quad \mathbf{T_{err}} = T_{err,stop} - T_{err,start}$$

Basic Operation(2)

- TDC transfer curve



TDC Requirements

- **High resolution**
- **Wide range**
- **Linearity(INL, DNL)**
- **Low power**
- **Small area**

Outline

- Introduction
- Basic Operation
- TDC Requirements
- **TDC Classification**
 - Short time interval generation
 - Time stretching
 - Etc

TDC Classification

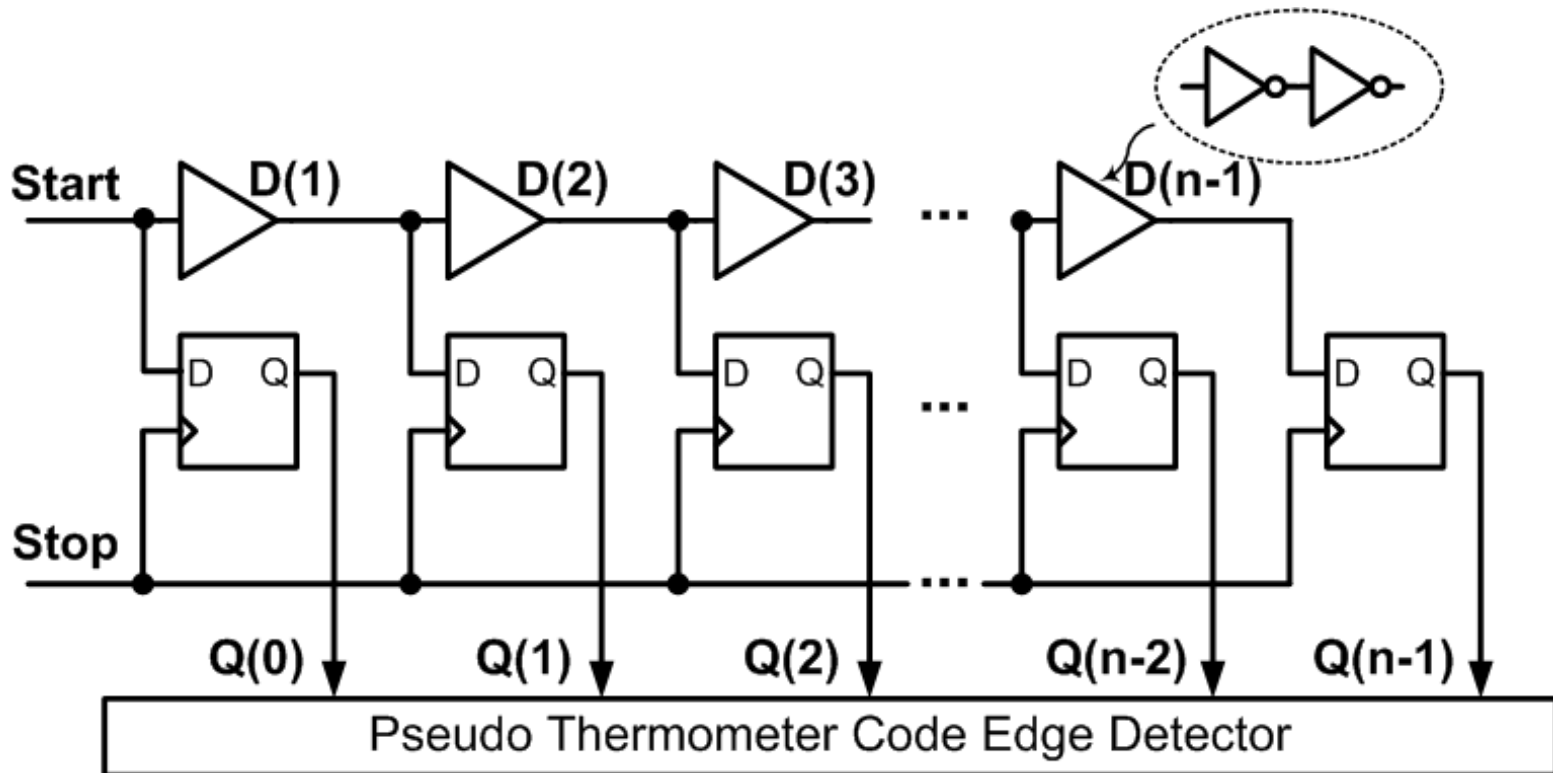
- **Short time interval generation**
- **Time Stretching**
- **Etc**
 - **Gated ring oscillator TDC**
 - **Pulse shrinking TDC**
 - **Stochastic TDC**
 - **Utilizing ADC**

Short Time Interval Generation

- **Generation of the more fine timing signal to enable the more accurate translation of time interval to digital code**
 - **Delay chain TDC**
 - **Differential delay chain TDC**
 - **Vernier TDC**
 - **Interpolation TDC**

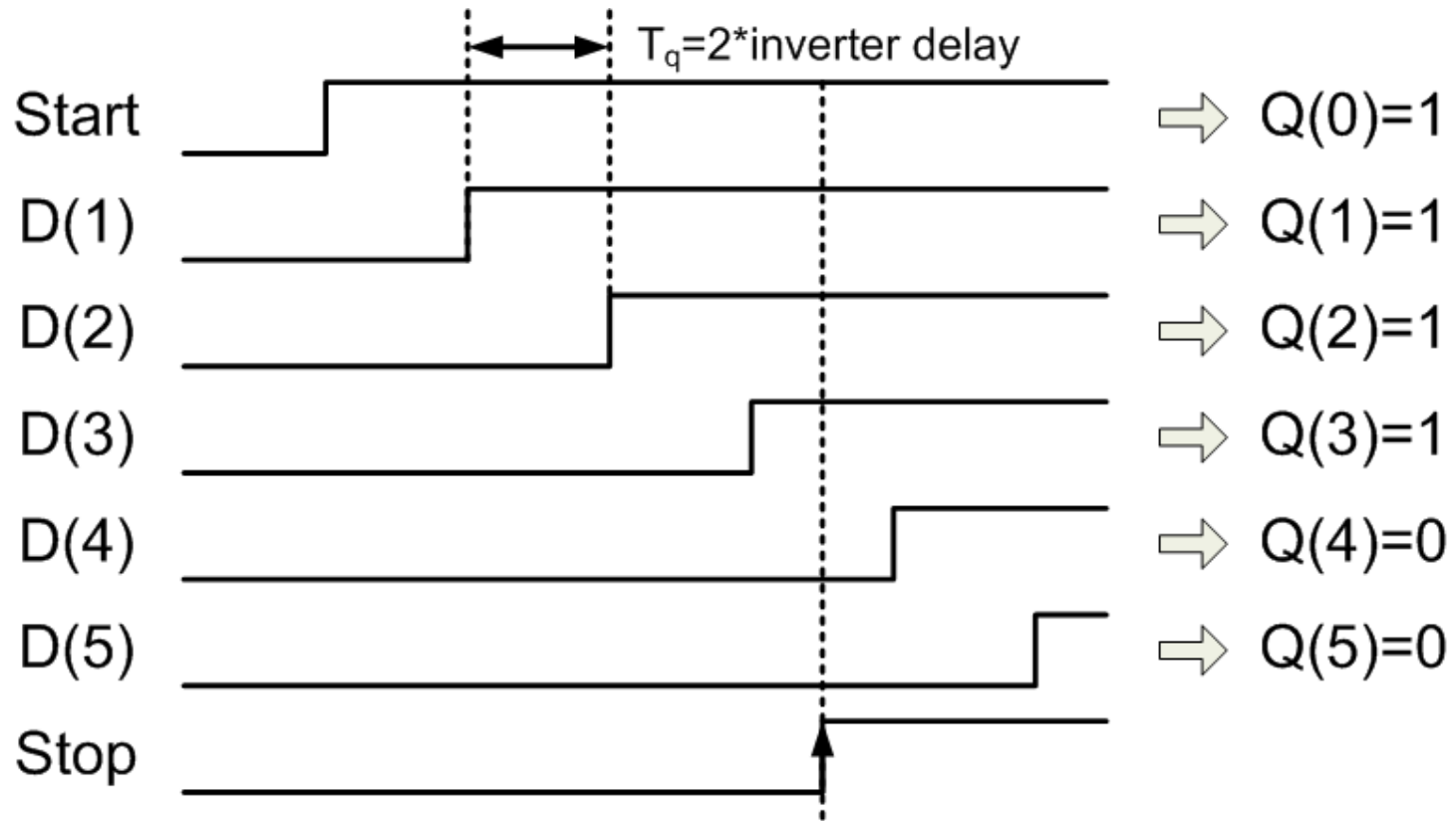
Delay Chain TDC

- Two-inverter delay resolution



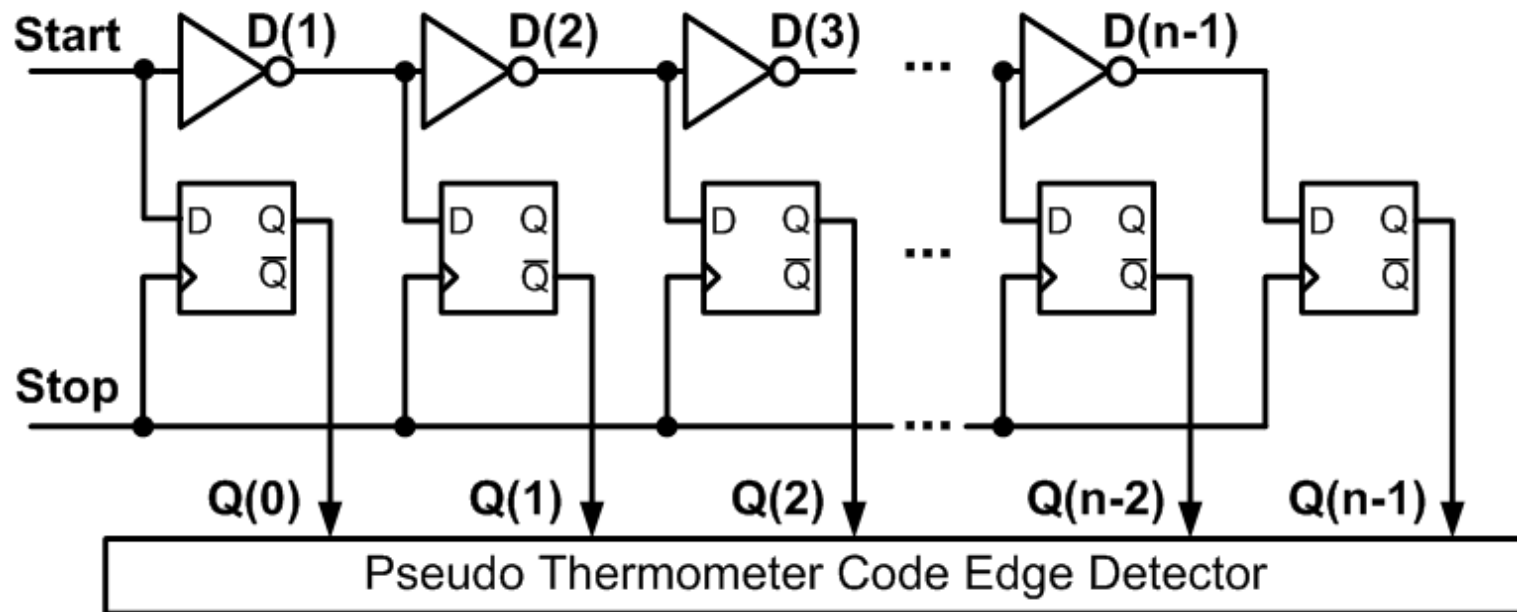
[1] Rahkonen, Circuit and Systems, 1989

Delay Chain TDC



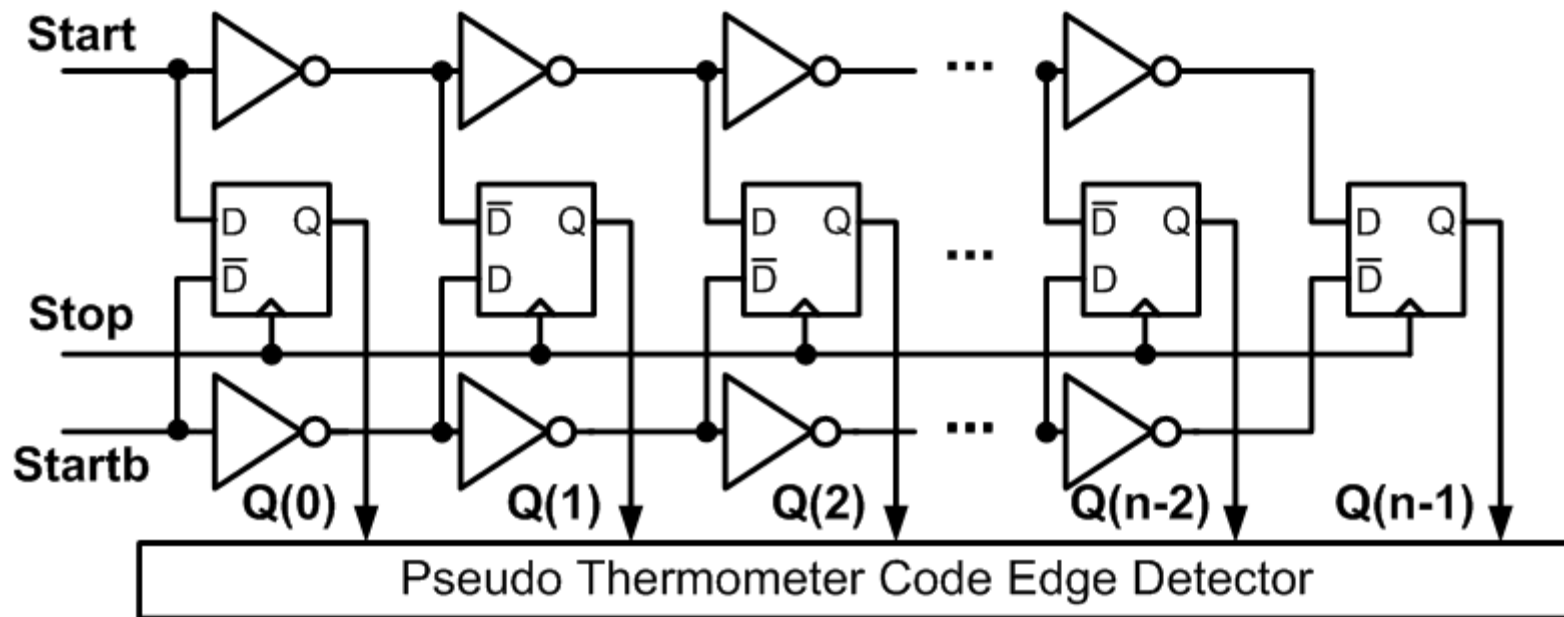
Differential Delay Chain TDC

- One-inverter delay resolution
- Different setup time for data '1' and '0'



Differential Delay Chain TDC

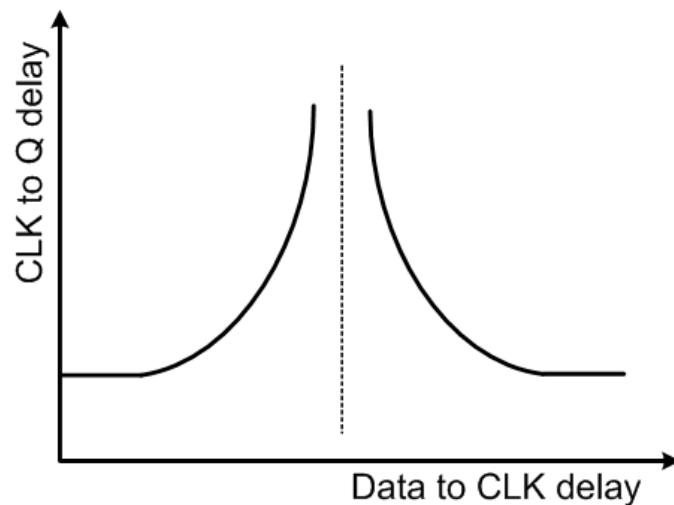
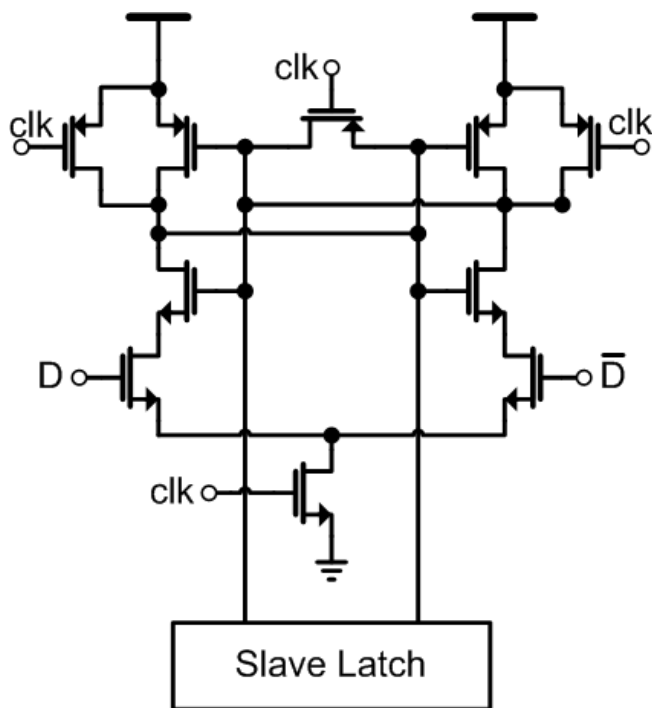
- One-inverter delay resolution
- Using symmetric DFF



[2] Staszewski, TSCASII, 2006

Differential Delay Chain TDC

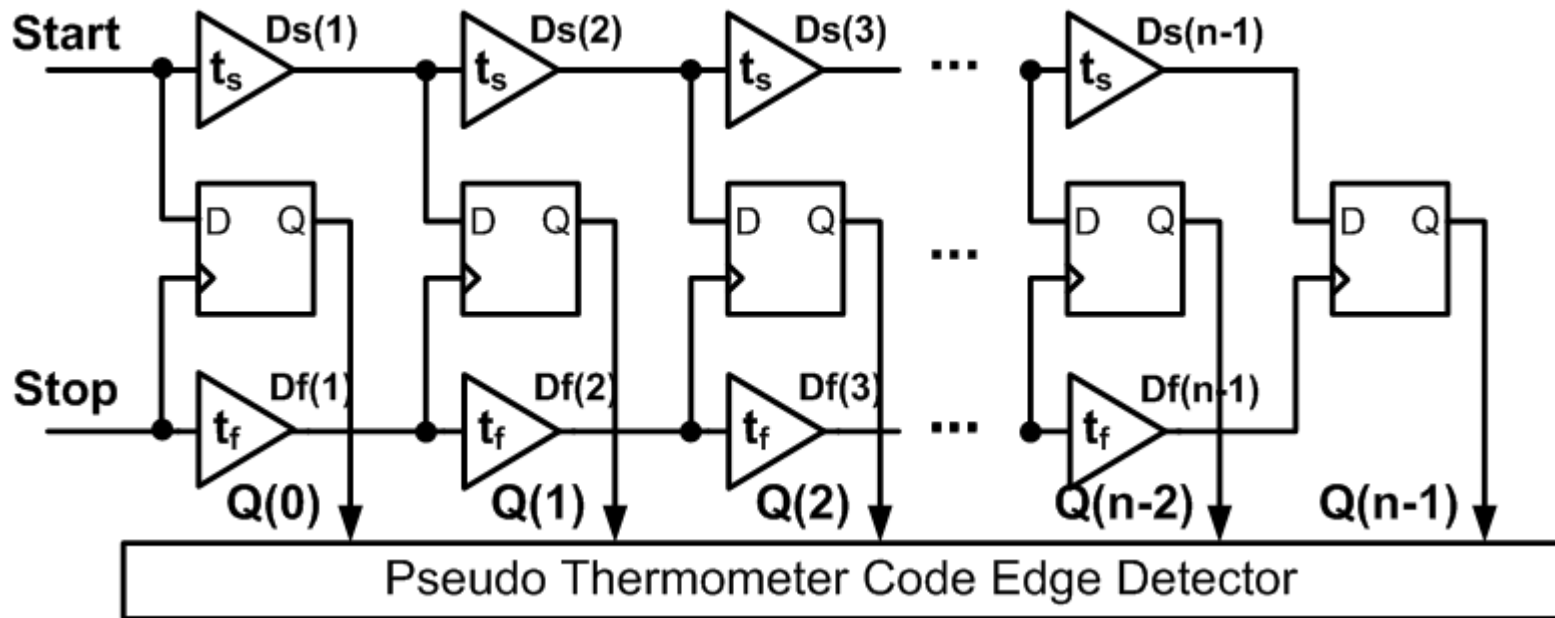
- **Symmetric DFF**
 - Same setup time for data '1' and '0'



[3]Nikolic,JSSC,2000

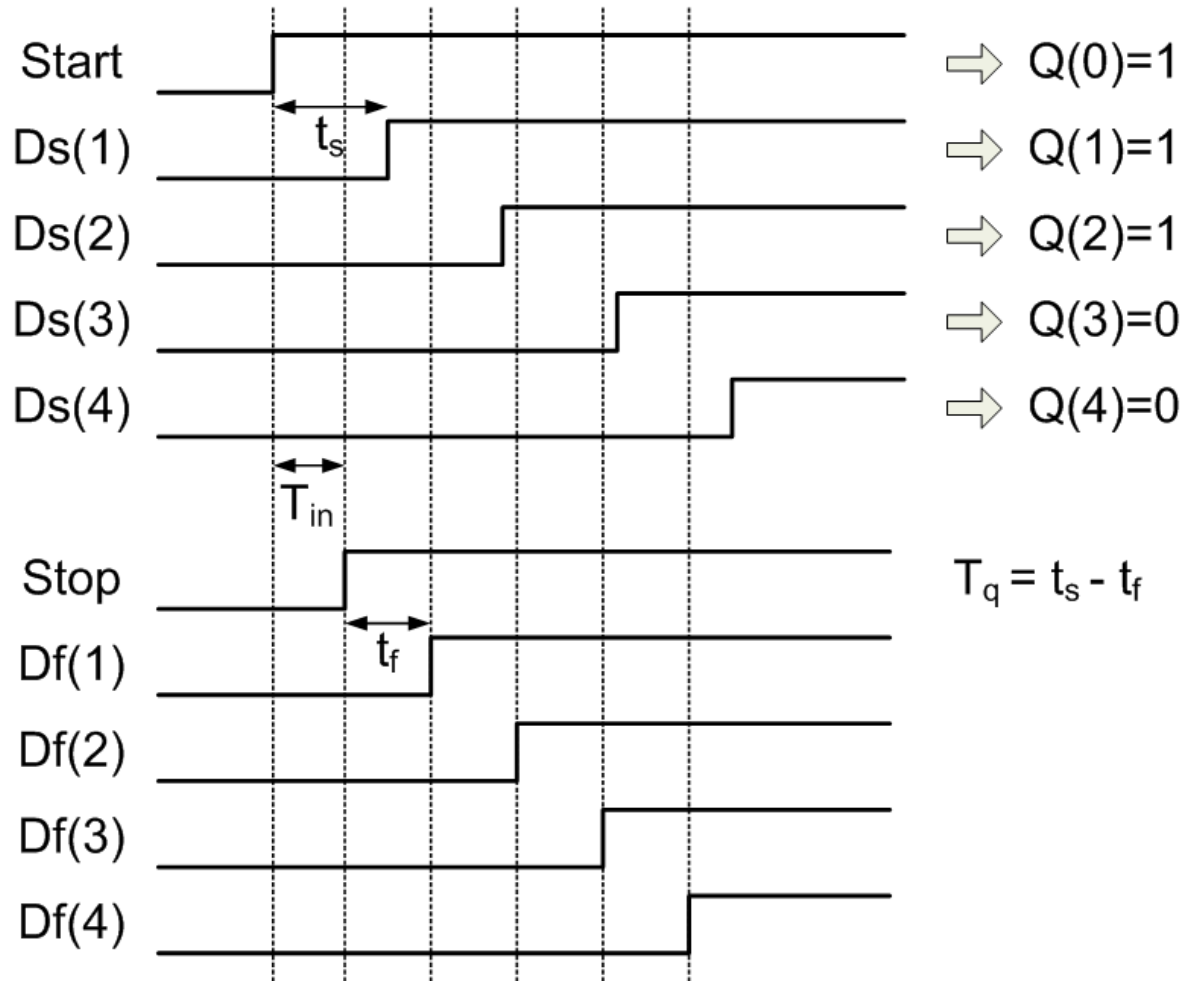
Vernier TDC

- Sub-gate-delay resolution
- TDC resolution = $t_s - t_f$, ($t_s \neq t_f$)

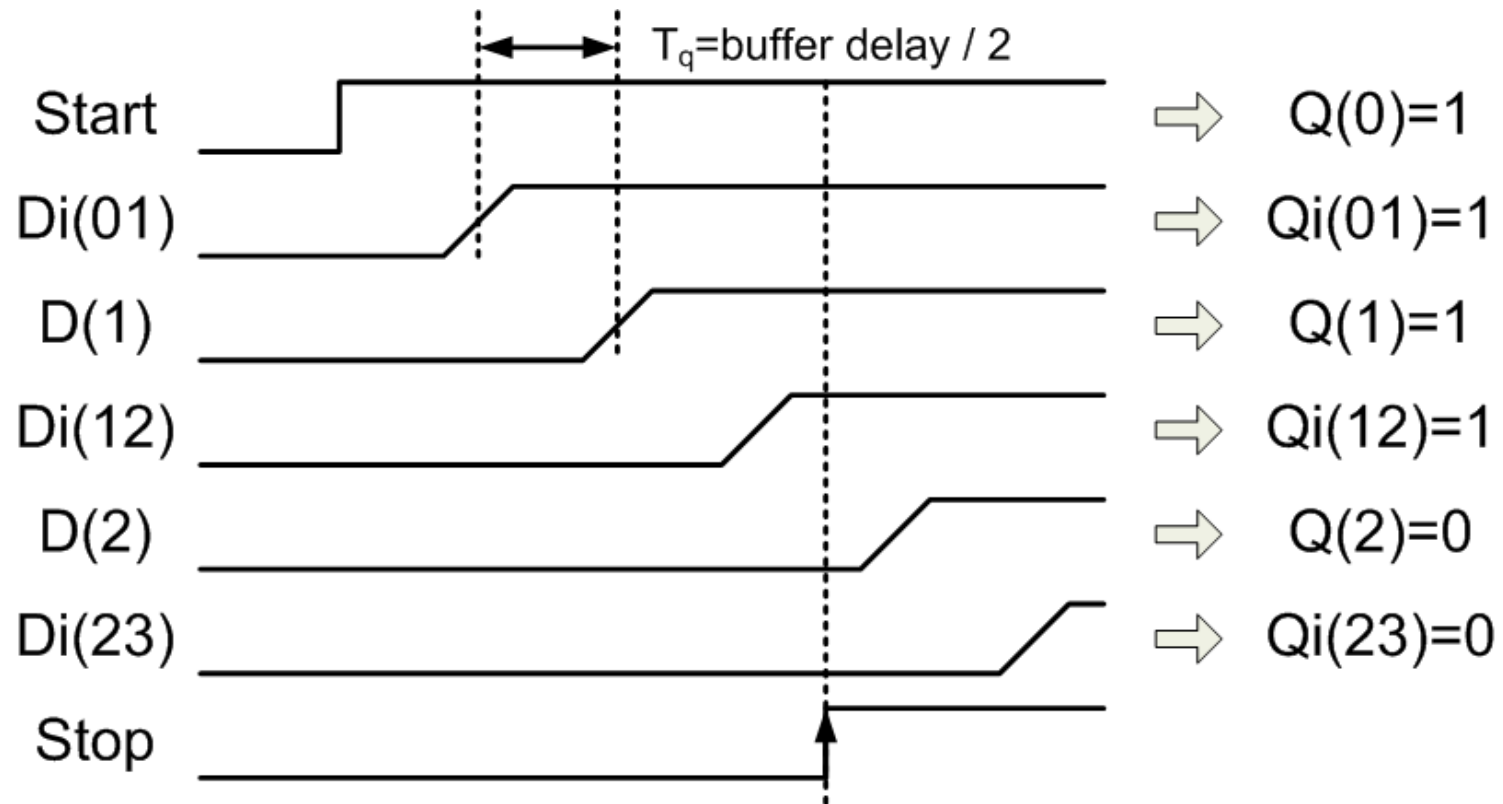


[4]Dudek,JSSC,2000

Vernier TDC



Interpolation TDC

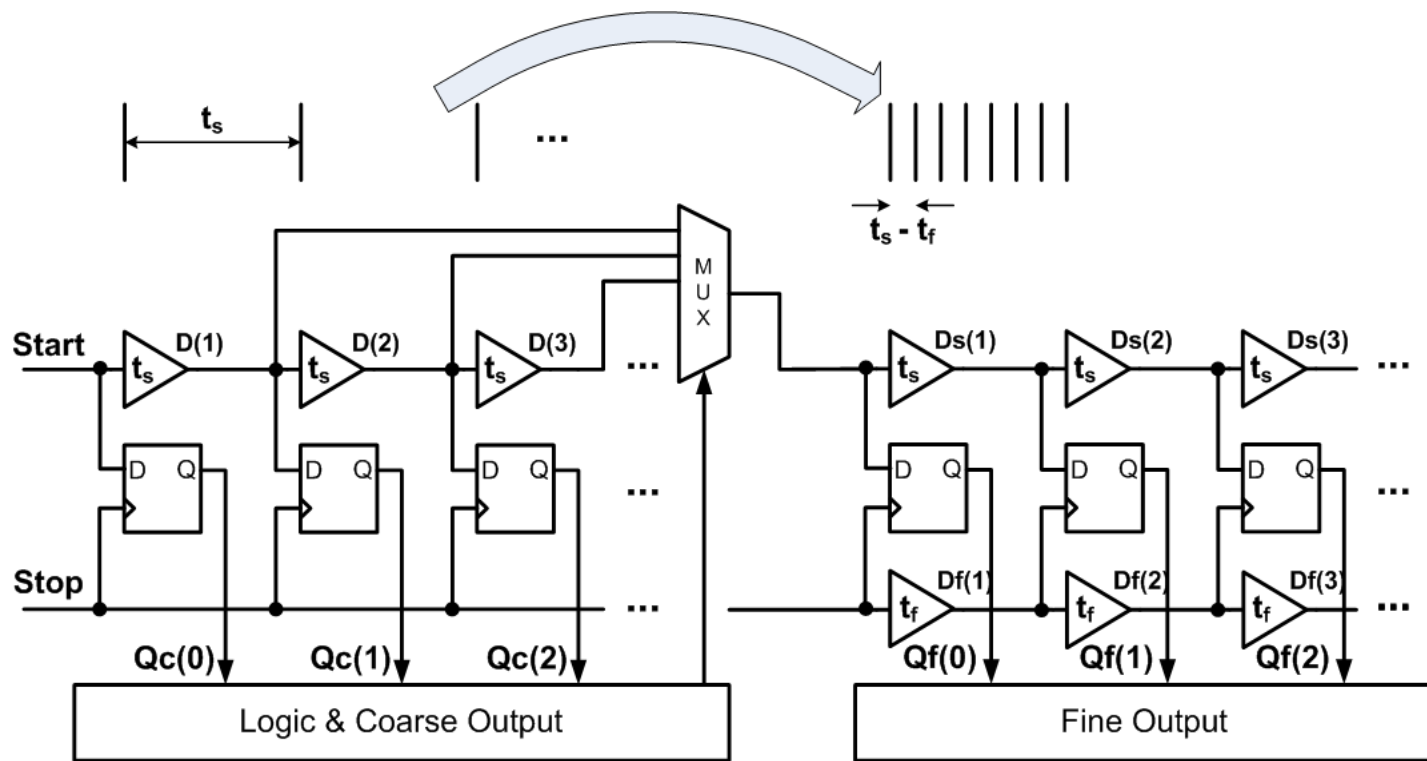


Wide Range TDC

- **TDC range = # of delay cell x resolution**
- **For wide range and high resolution, too many delay cells are needed.**
=> large area and poor linearity.
- **Solutions:**
 - **Two-step TDC**
 - **Logarithmic TDC**
 - **Ring TDC**

Two-Step TDC

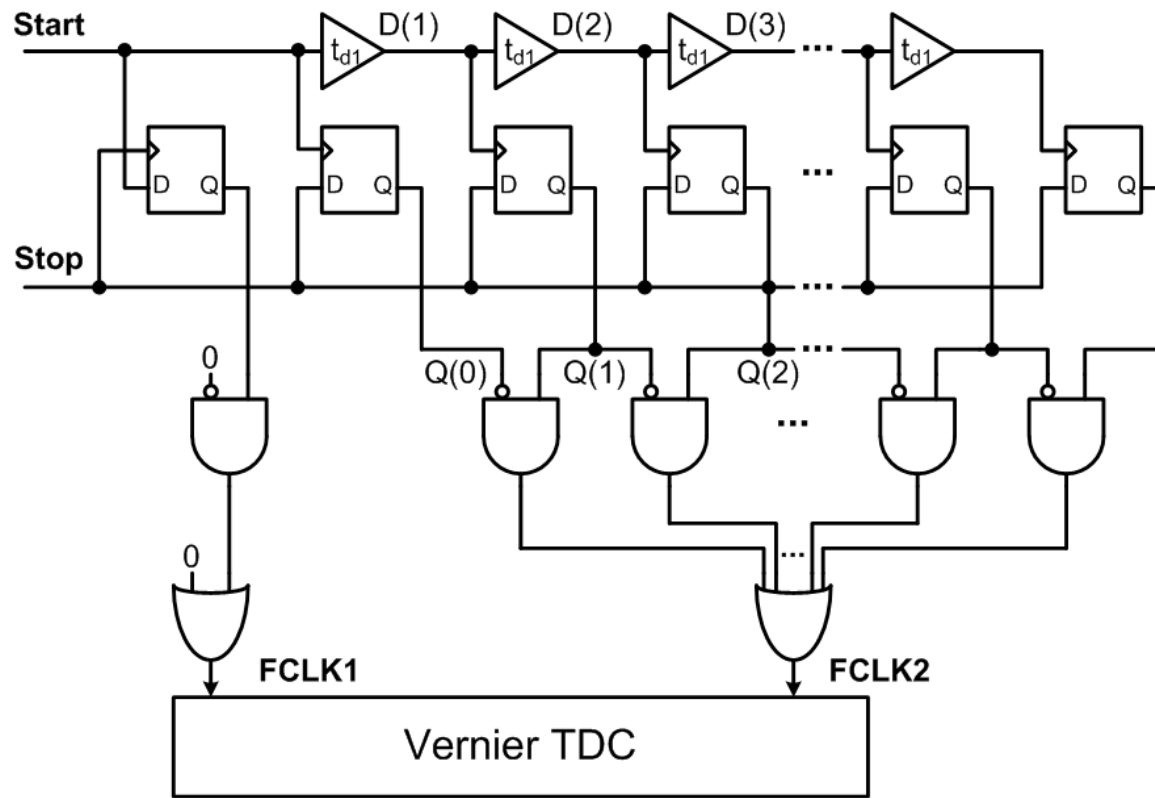
- Incorporates both the delay chain TDC and Vernier TDC



[6]Ramakrishnan, VLSI Design, 2006

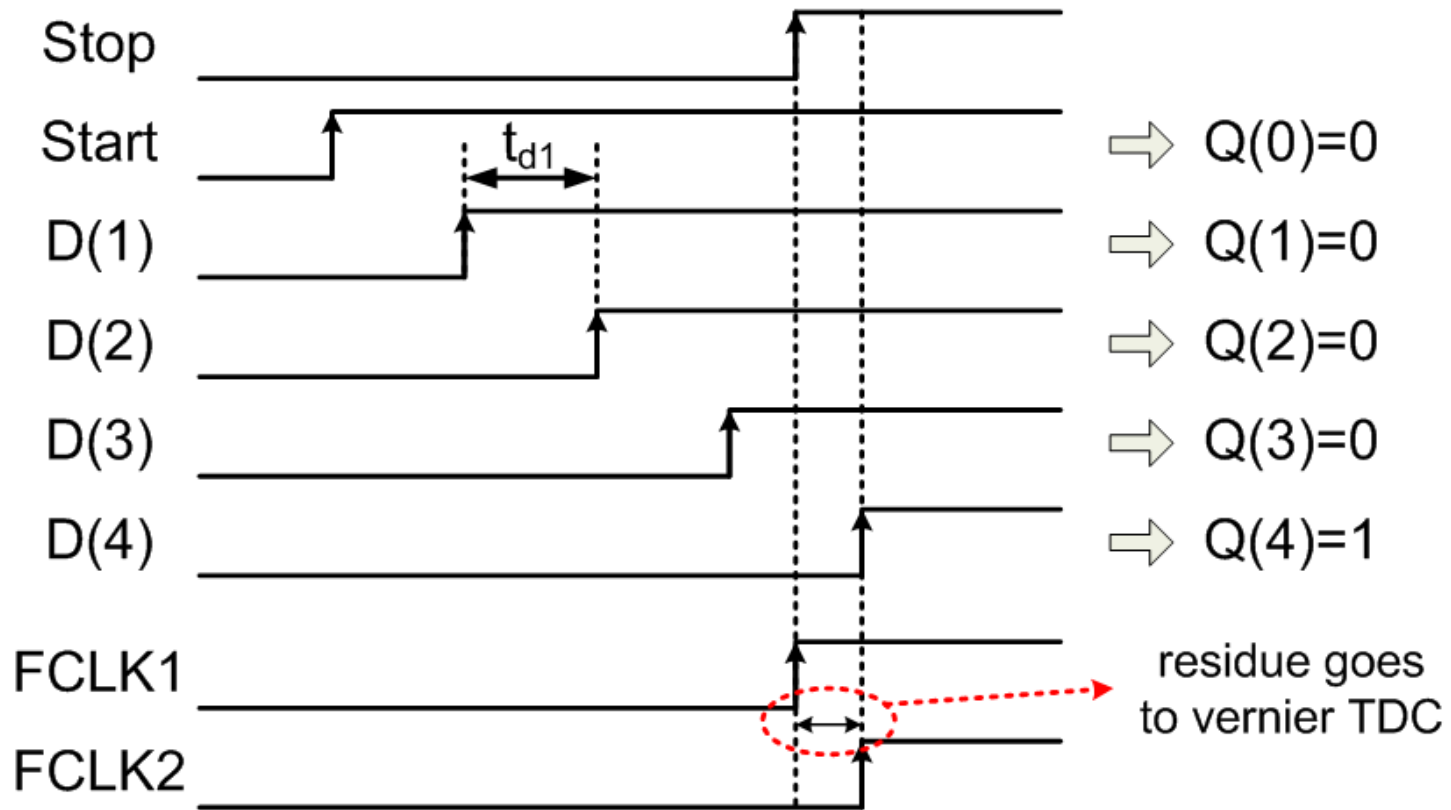
Two-Step TDC (1)

- Incorporates both the delay chain TDC and Vernier TDC



[7]Tokairin,ISSCC,2010

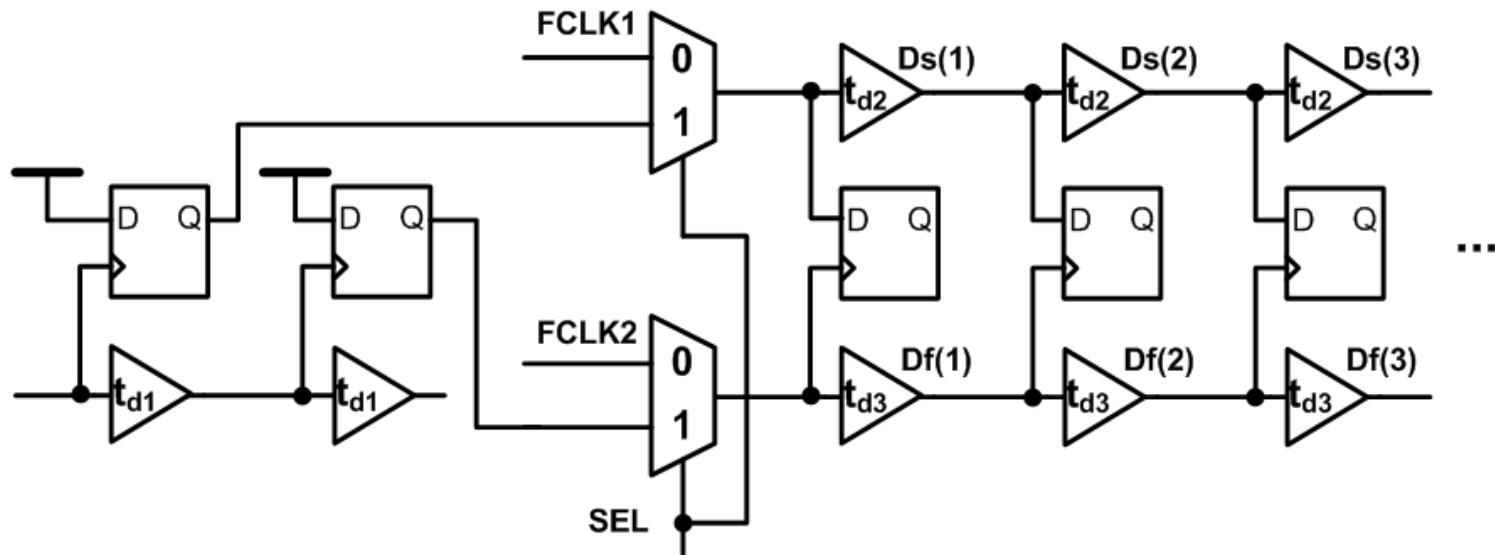
Two-Step TDC (2)



[7]Tokairin,ISSCC,2010

Two-Step TDC (3)

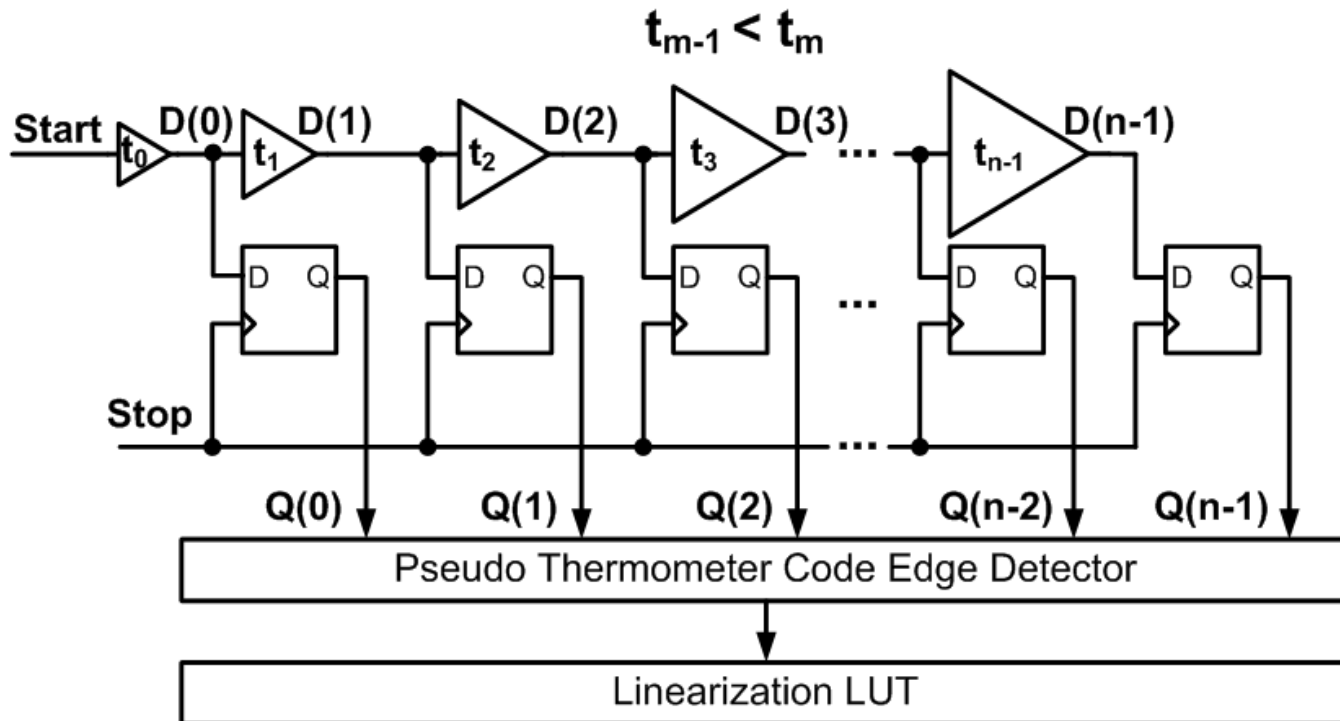
- **SEL=high** => measures t_{d1} for normalization
- **SEL=low** => measures residue from delay chain TDC



[7]Tokairin,ISSCC,2010

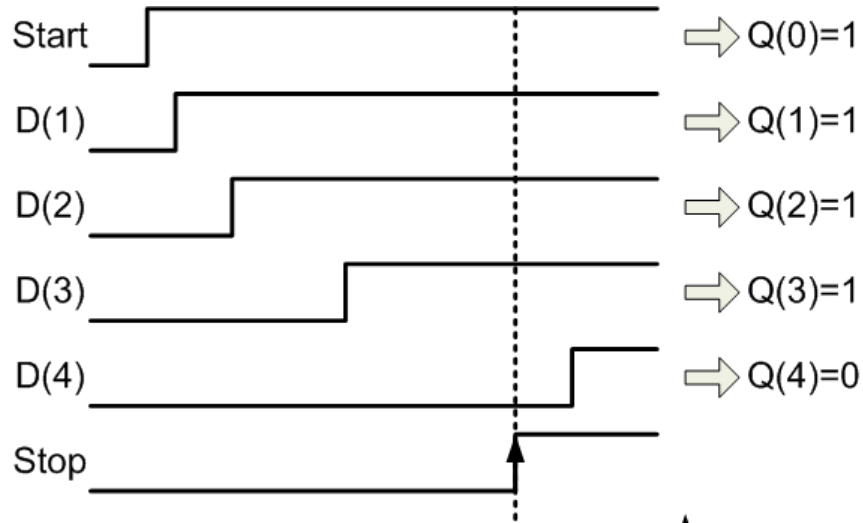
Logarithmic TDC

- Wide range is achieved through logarithmic inverter delay
- Additional logic is required for linearization

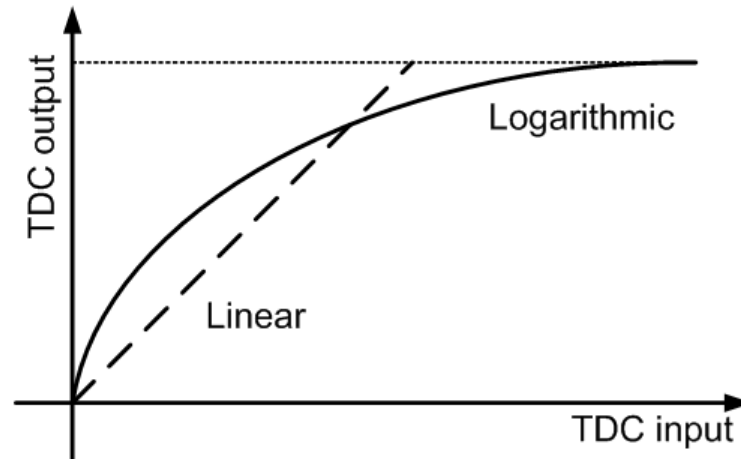


[8]Lin,ISSCC,2004

Logarithmic TDC

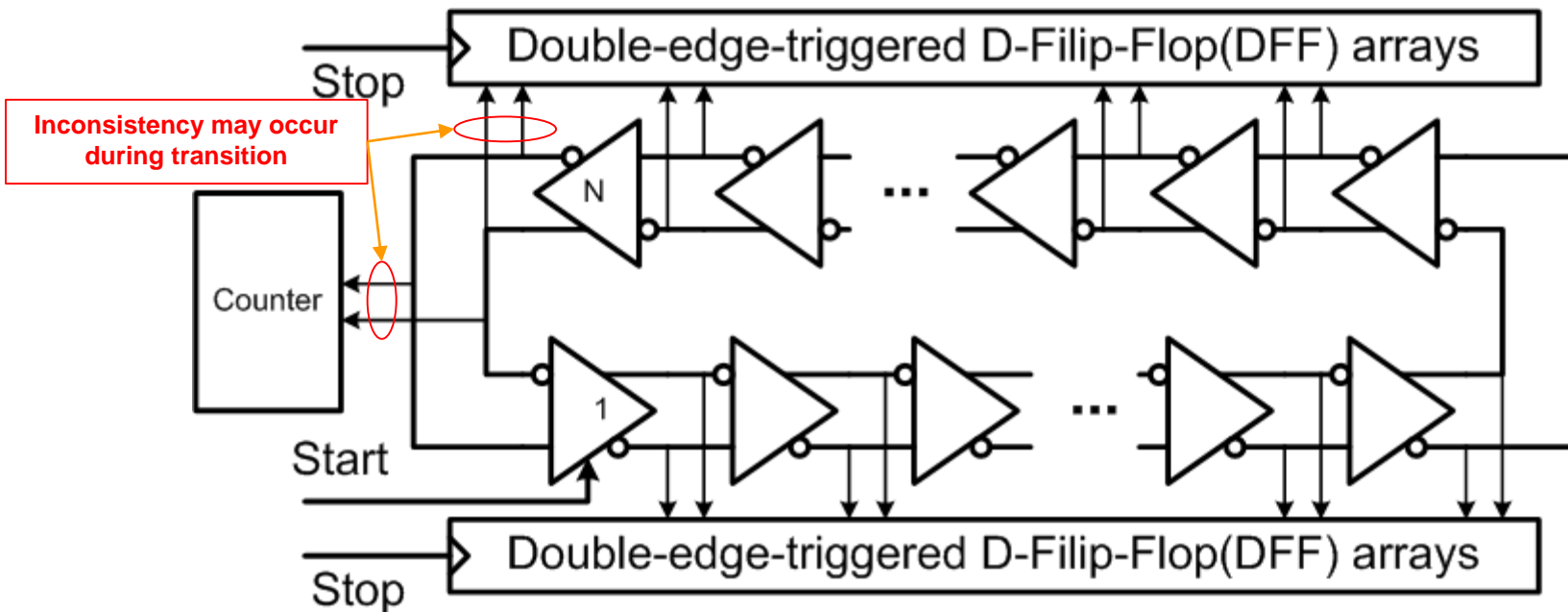


Transfer curve



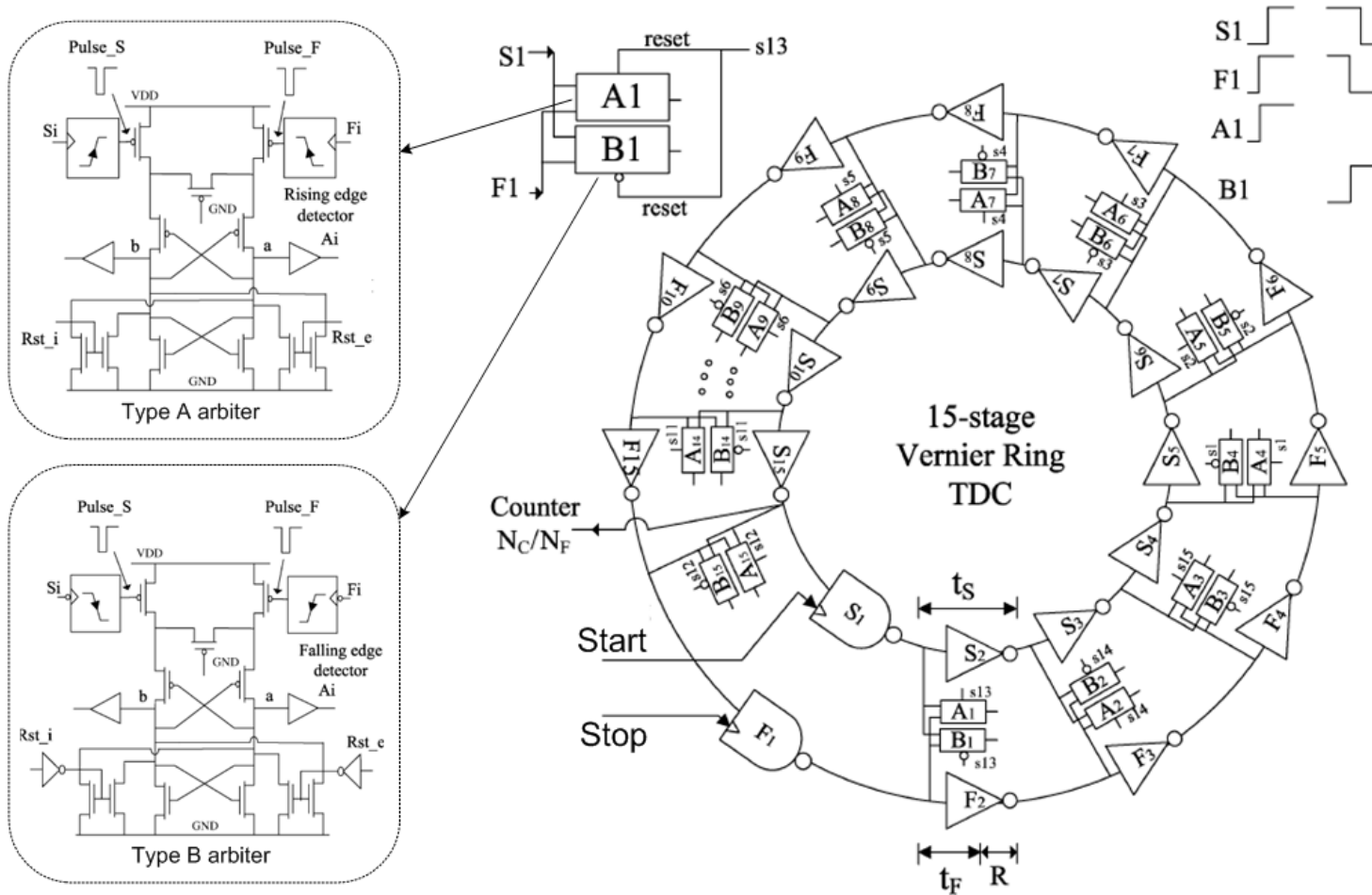
Cyclic TDC

- Reuses the delay elements and increases the detection range
- Better linearity than delay chain TDC



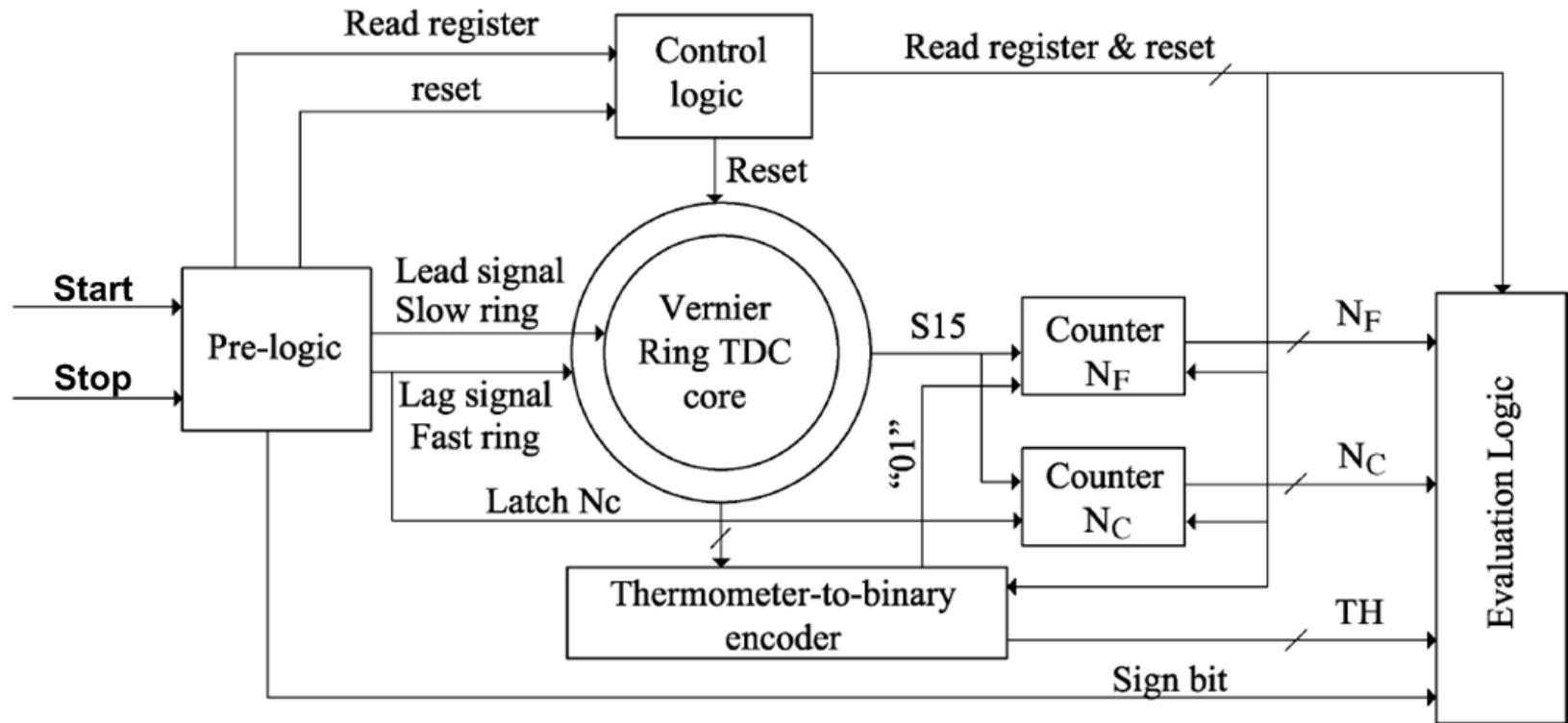
[9]Chang,ISSCC,2008

Vernier Ring TDC



[10]Yu, JSSC, 2010

Vernier Ring TDC

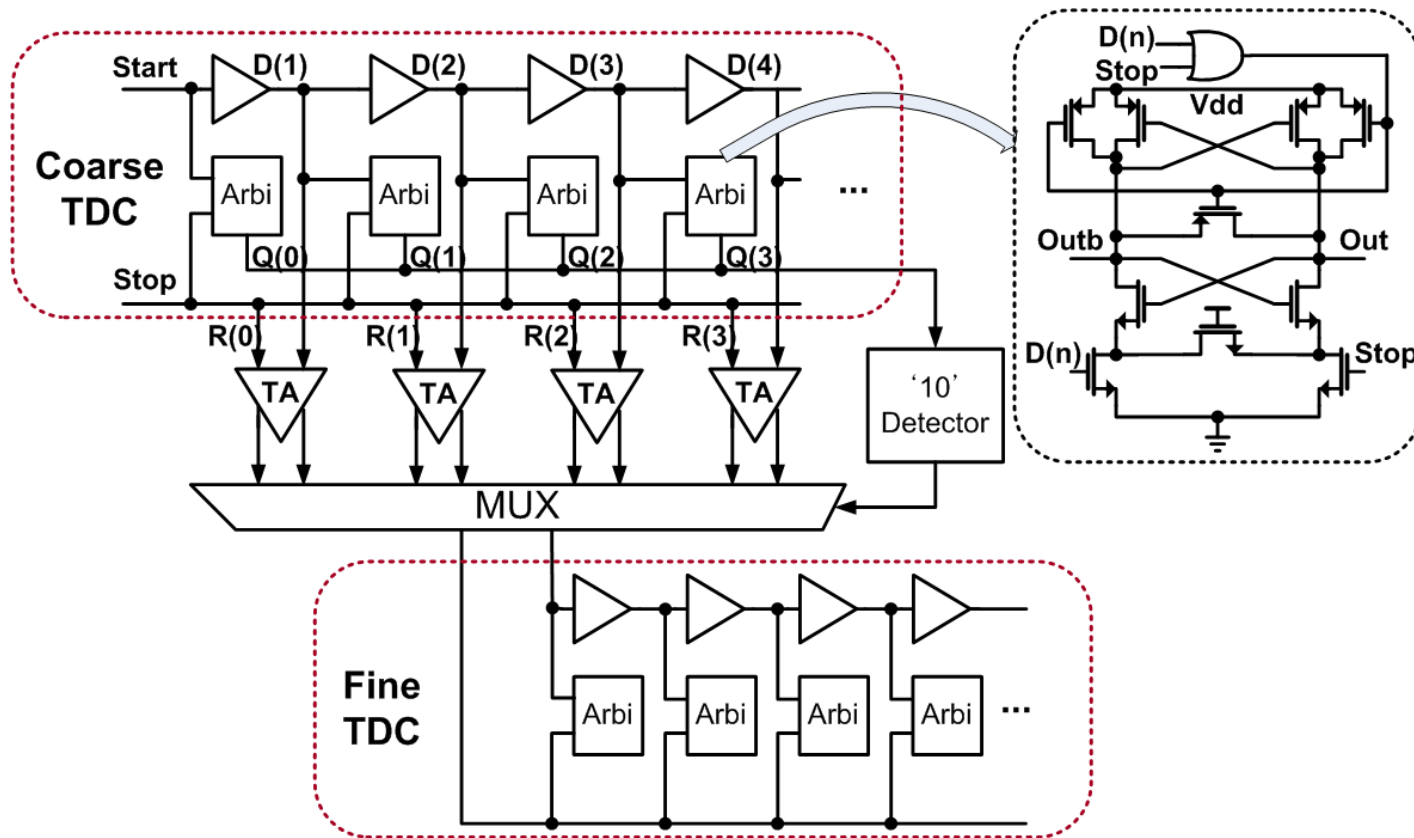


Time Stretching TDC

- **Opposite approach to get high resolution is time stretching**
- **Amplifies input time difference and uses simple delay chain TDC**
- **Amplification greatly relaxes the requirement on device matching in delay line**
 - **Time amplifying TDC**
 - **Sub-exponent TDC**

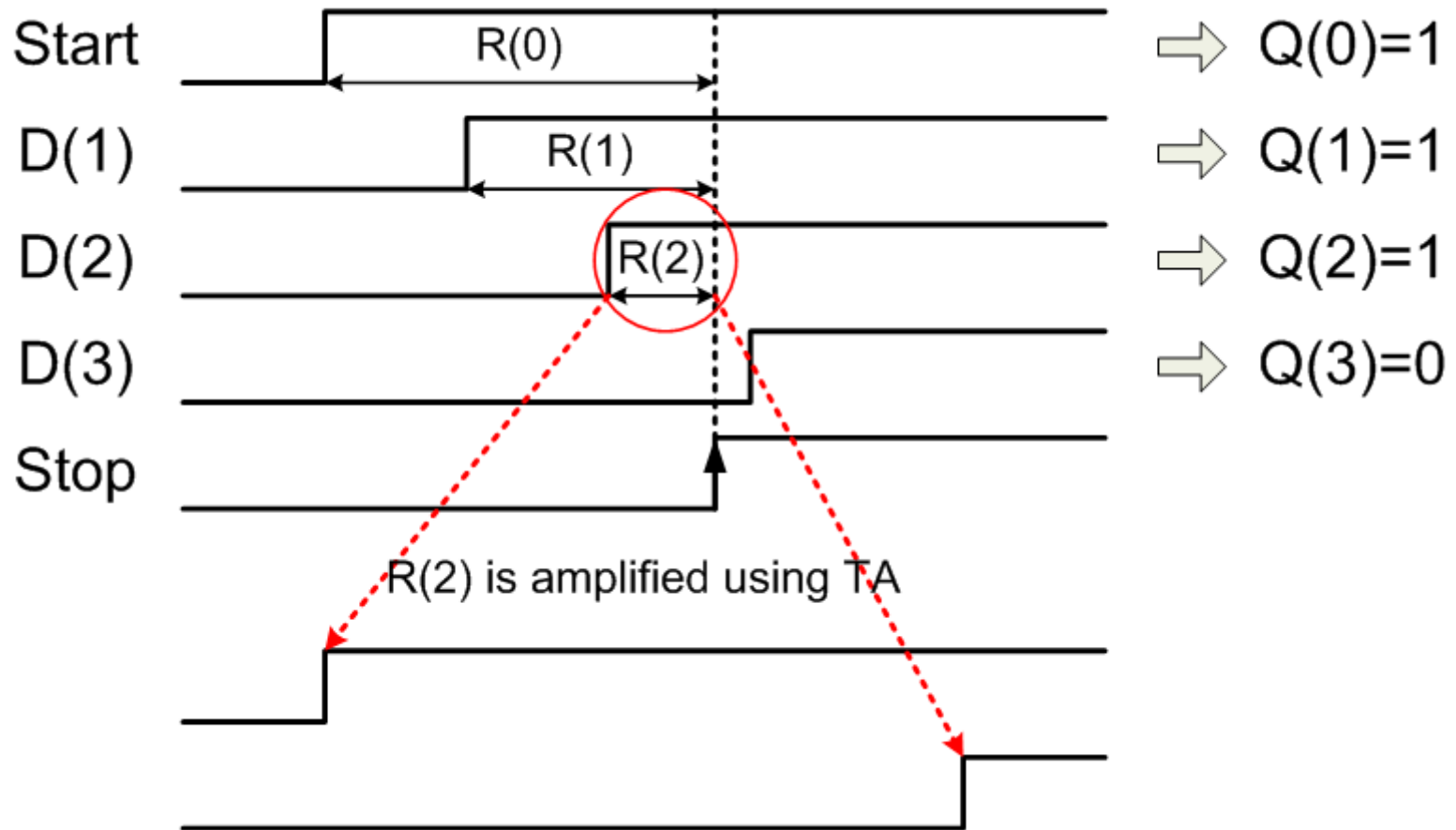
Time Amplifying TDC (1)

- Time residue is amplified by TA(Time Amplifier) and resolved by fine TDC



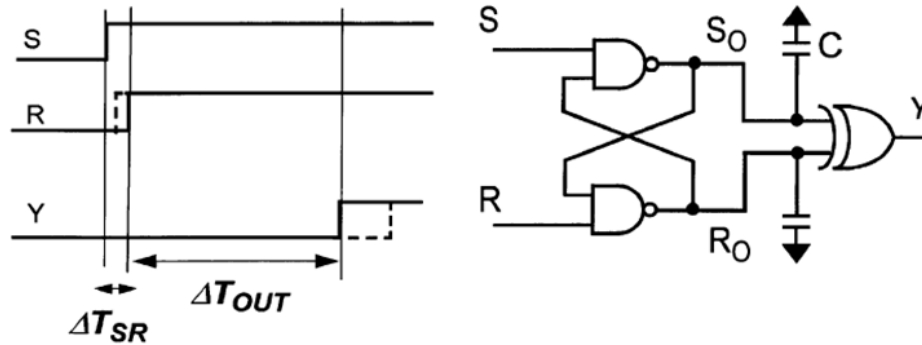
[13]Lee, JSSC 2008

Time Amplifying TDC (2)

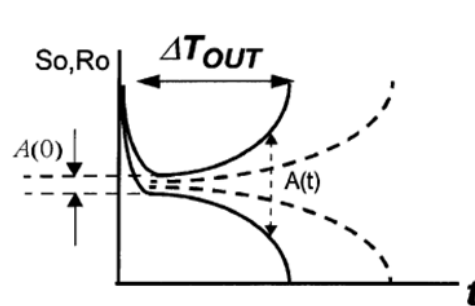


Time Amplifying TDC (3)

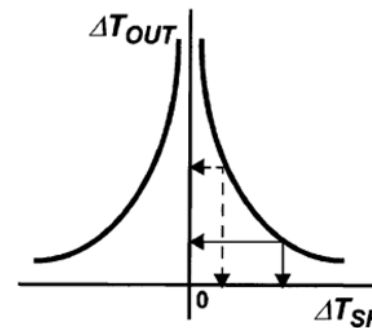
- In SR latch followed by an XOR, the propagation delay varies as an even-symmetric logarithmic function versus input time difference.



(a) SR latch followed by an XOR



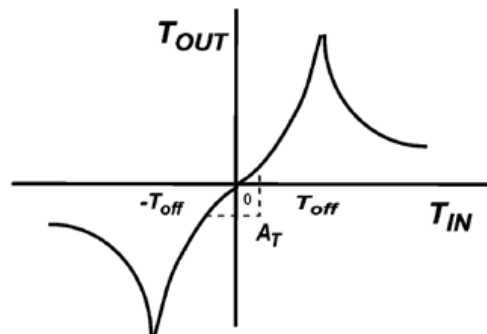
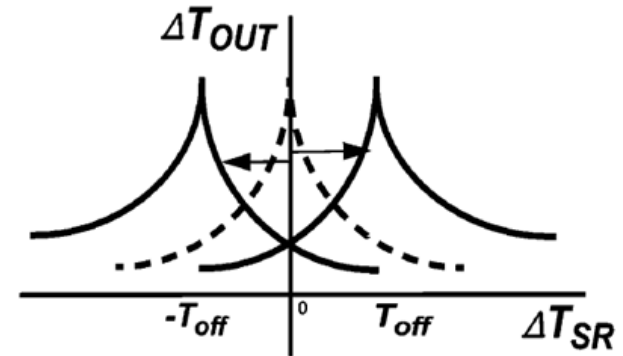
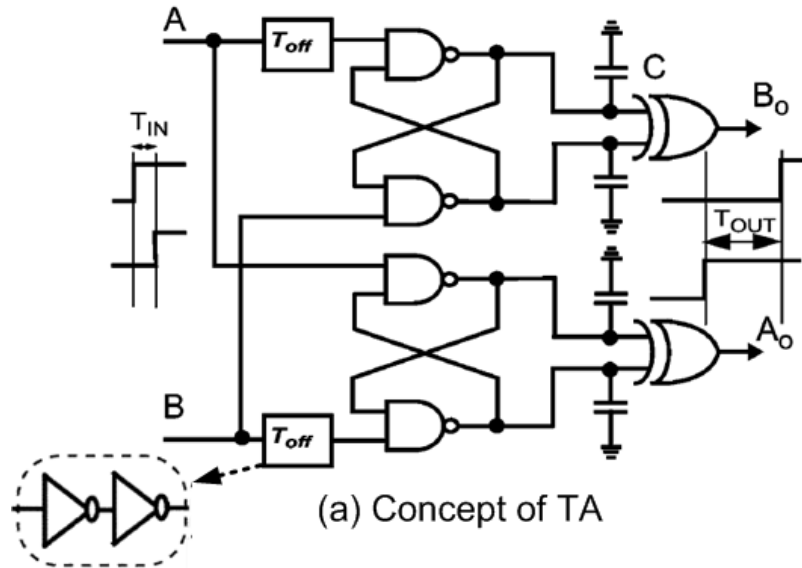
(b) Regeneration process
In SR latch



(c) Relationship between the
regeneration time and the initial time
difference

[13]Lee, JSSC 2008

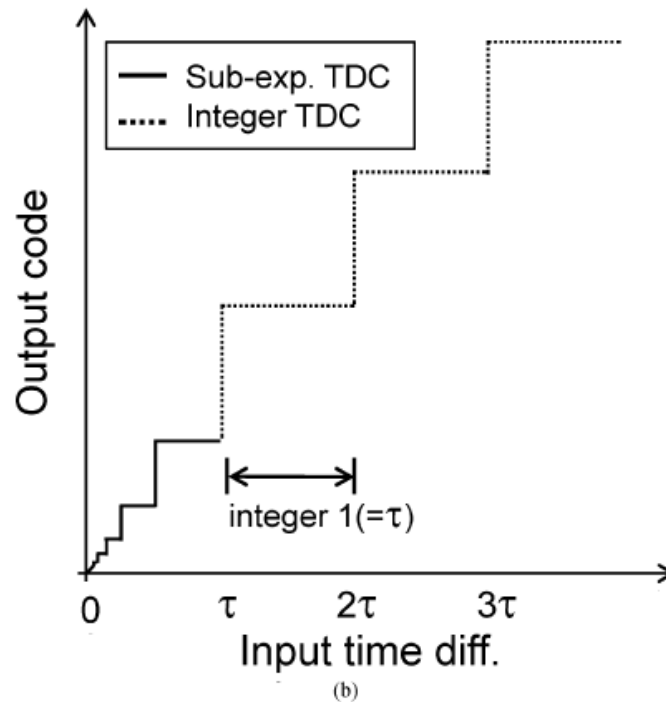
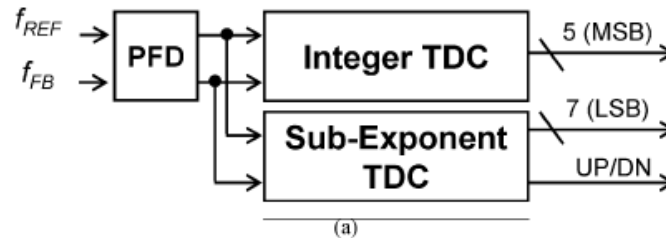
Time Amplifying TDC (4)



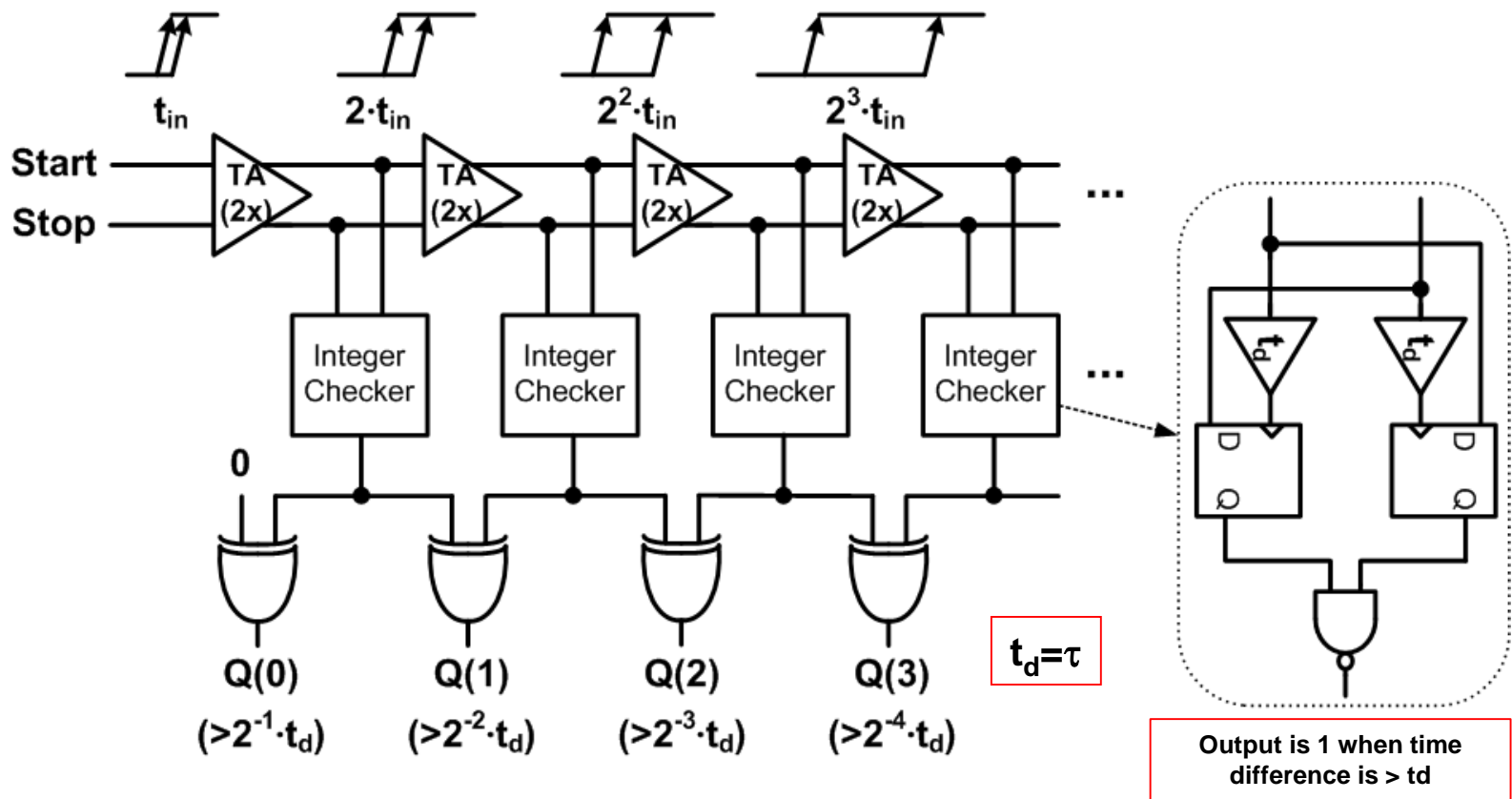
T_{off} controls the linear range
 A_T is a gain of TA around zero input
 $A_T = 2(C/g_m)/T_{off}$
 g_m : transconductance of the NAND
 in metastability

Sub-Exponent TDC (1)

- **Scaling of resolution according to input time difference**



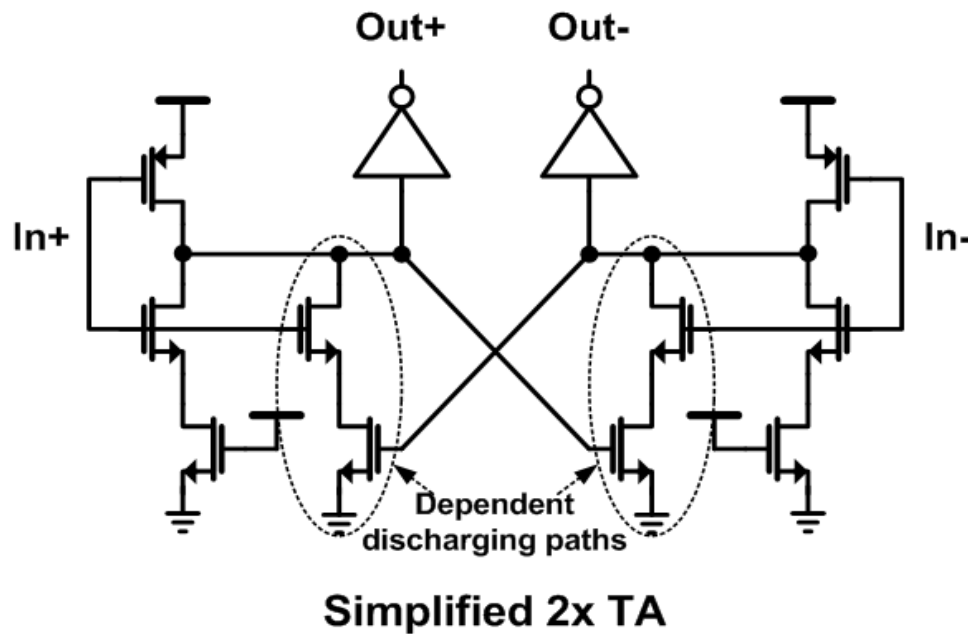
Sub-Exponent TDC (1)



[14]Lee, JSSC 2010

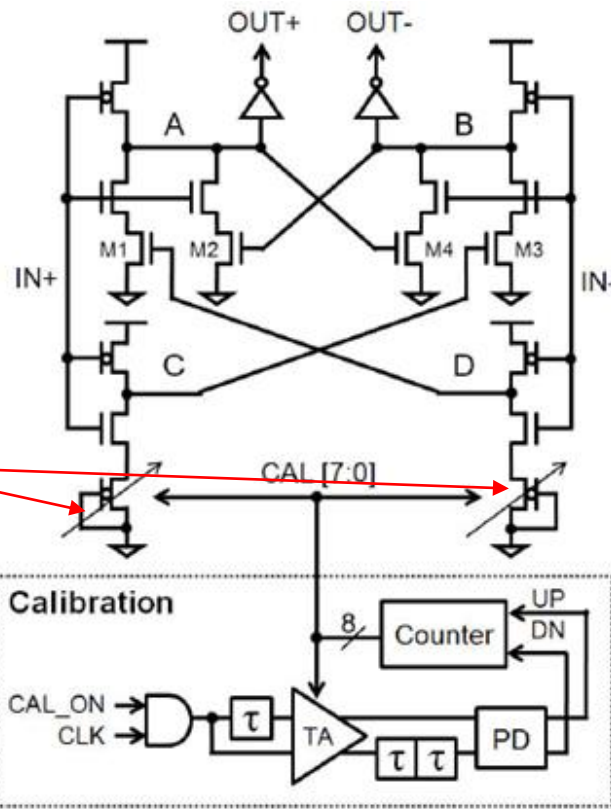
Sub-Exponent TDC (2)

- First discharging is performed by two identical path
 - Second discharging is performed by only one path
- => The gain of TA roughly is twice of the small signal input gain.

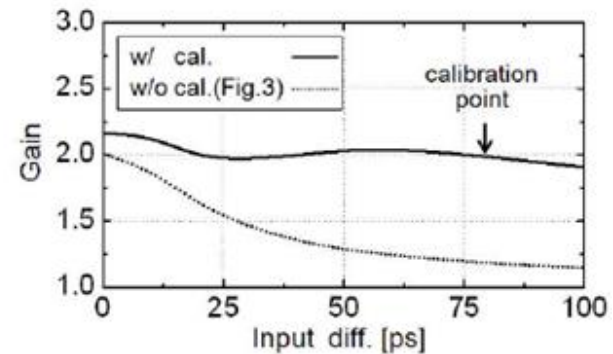
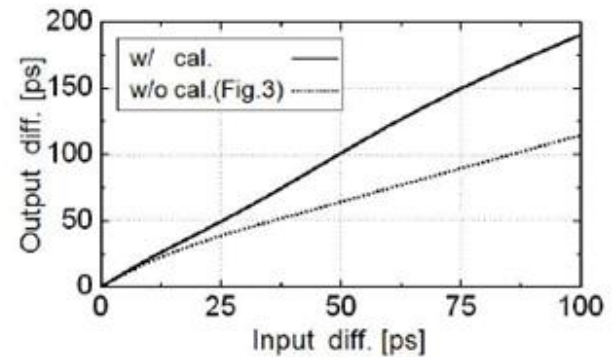


Sub-Exponent TDC (3)

- With large input time diff, output saturated. To get accurate 2x time amplification, TA calibration is necessary



PMOS diodes:
Slow discharge
on C & D
M1 and M3 not
completely
turned off

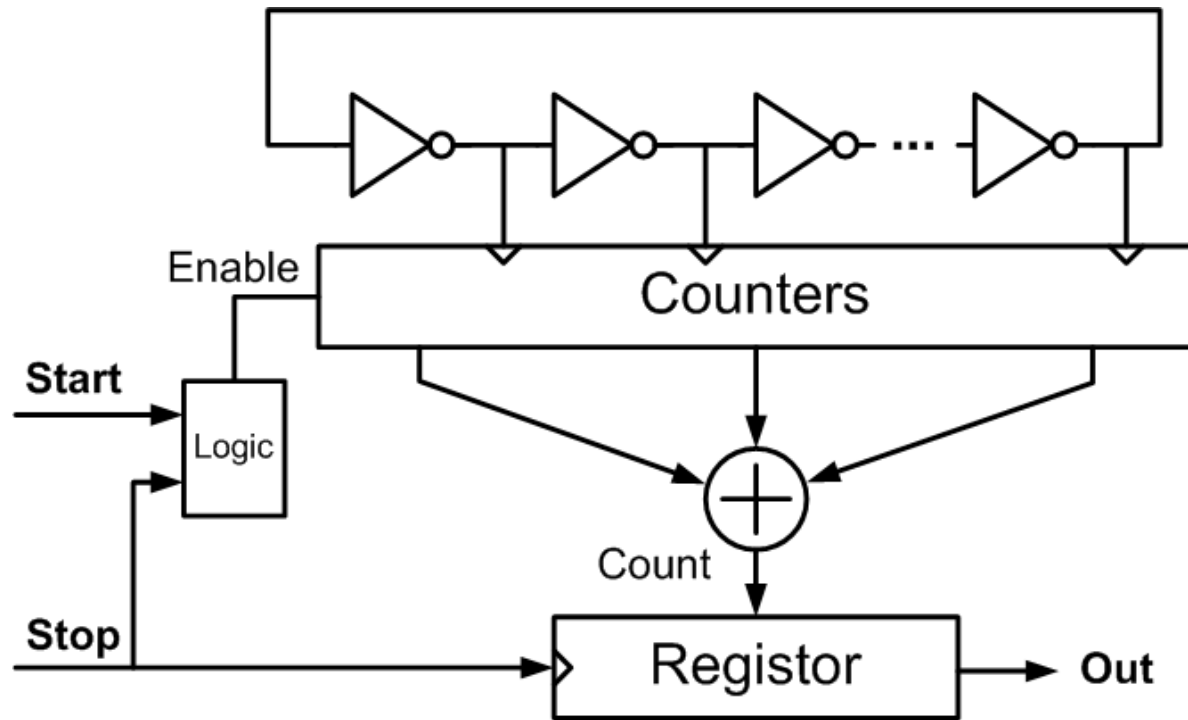


Other TDCs

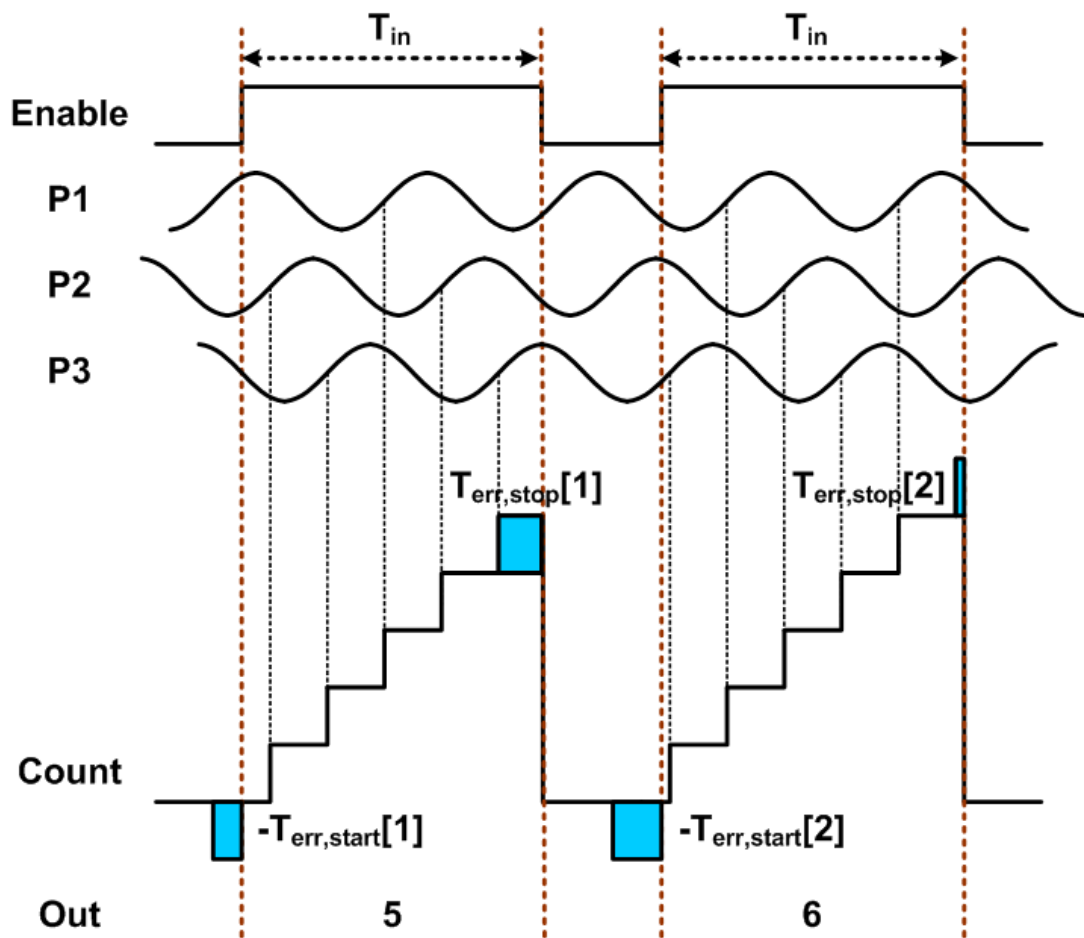
- **Etc**
 - **Gated ring oscillator TDC**
 - **Pulse shrinking TDC**
 - **Stochastic TDC**
 - **Time-to-Voltage followed by ADC**

Oscillator-Based TDC

- **Counters operate when enable signal is high**
- **Oscillator runs freely regardless of input**
=> Large power consumption



Oscillator-Based TDC

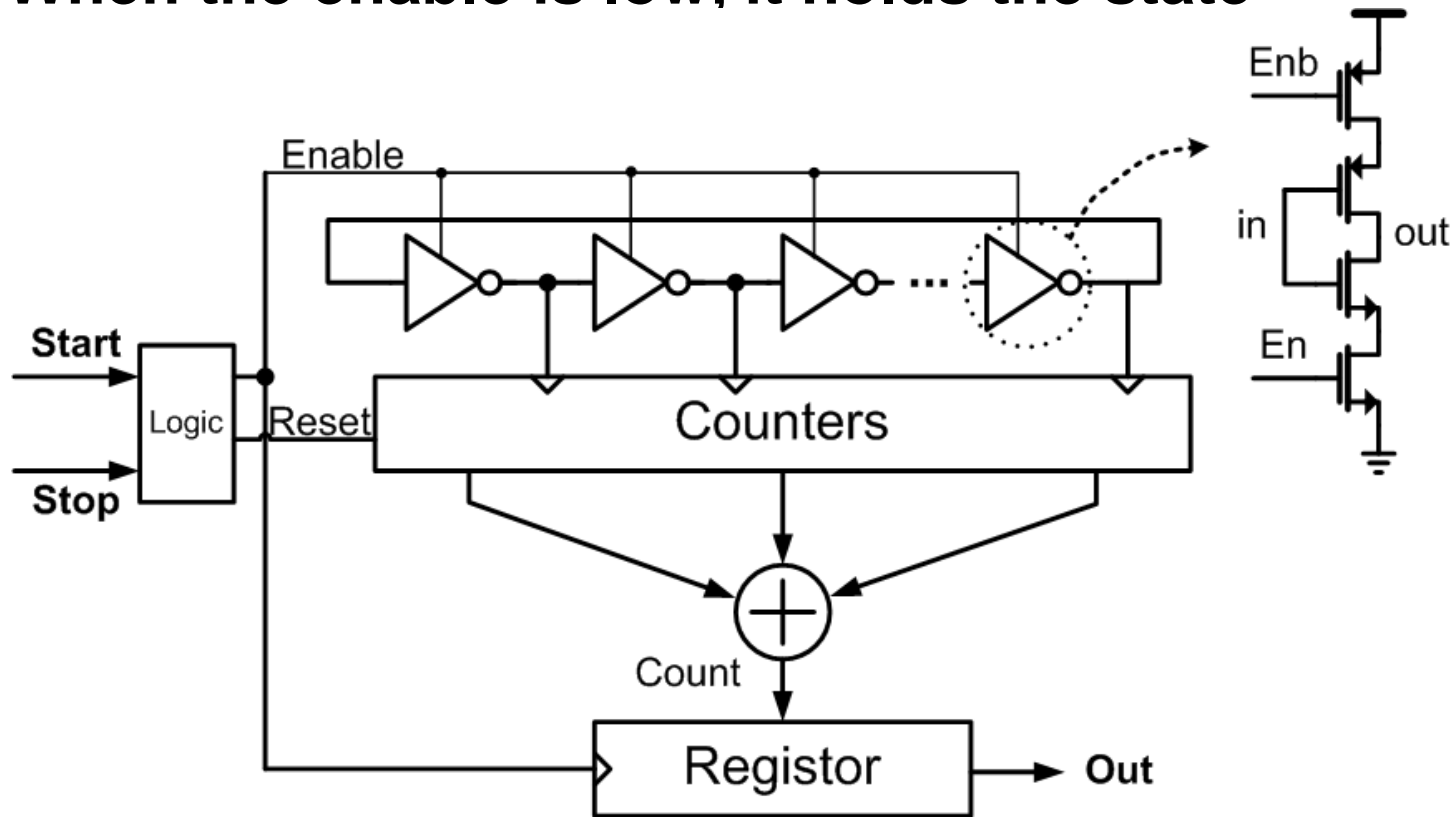


$$T_{err} = T_{err,stop} - T_{err,start}$$

An oscillator-based TDC's $T_{err,start}$ is random, having uniform density on the interval $[0, T_q]$.

Gated Ring Oscillator TDC (1)

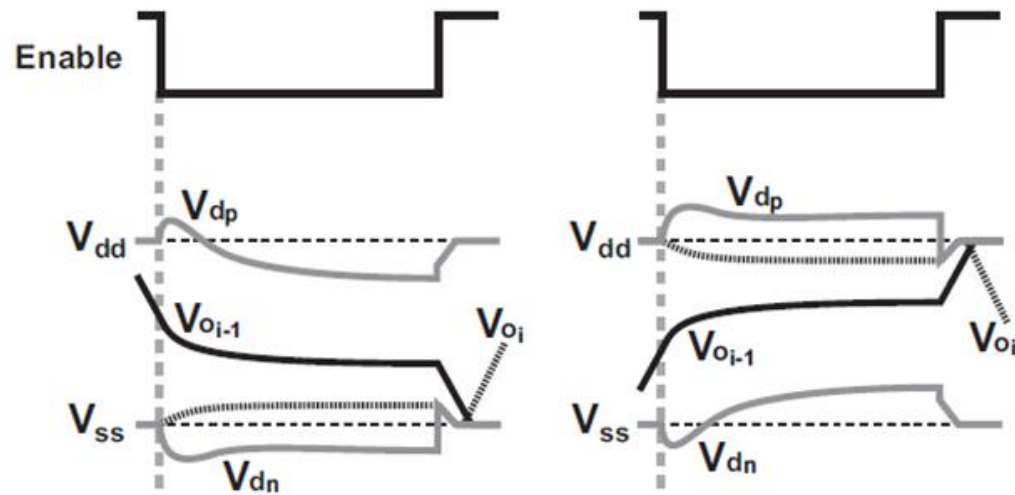
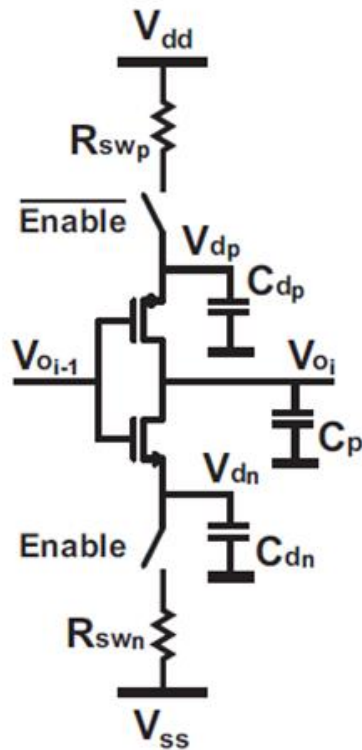
- Oscillator operates only when the enable is high
- When the enable is low, it holds the state



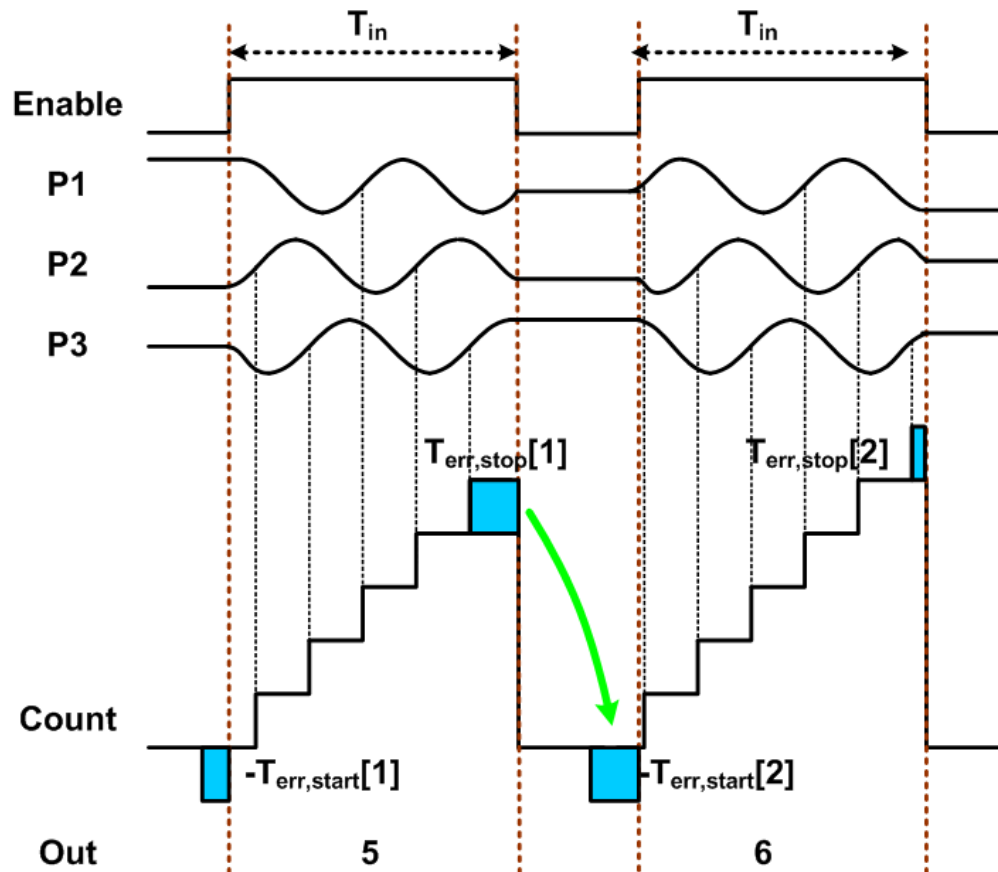
[16]Straayer, JSSC, 2009

Gated Ring Oscillator TDC (2)

- When the enable is low, the time residue is stored in V_{oi} node



Gated Ring Oscillator TDC (3)



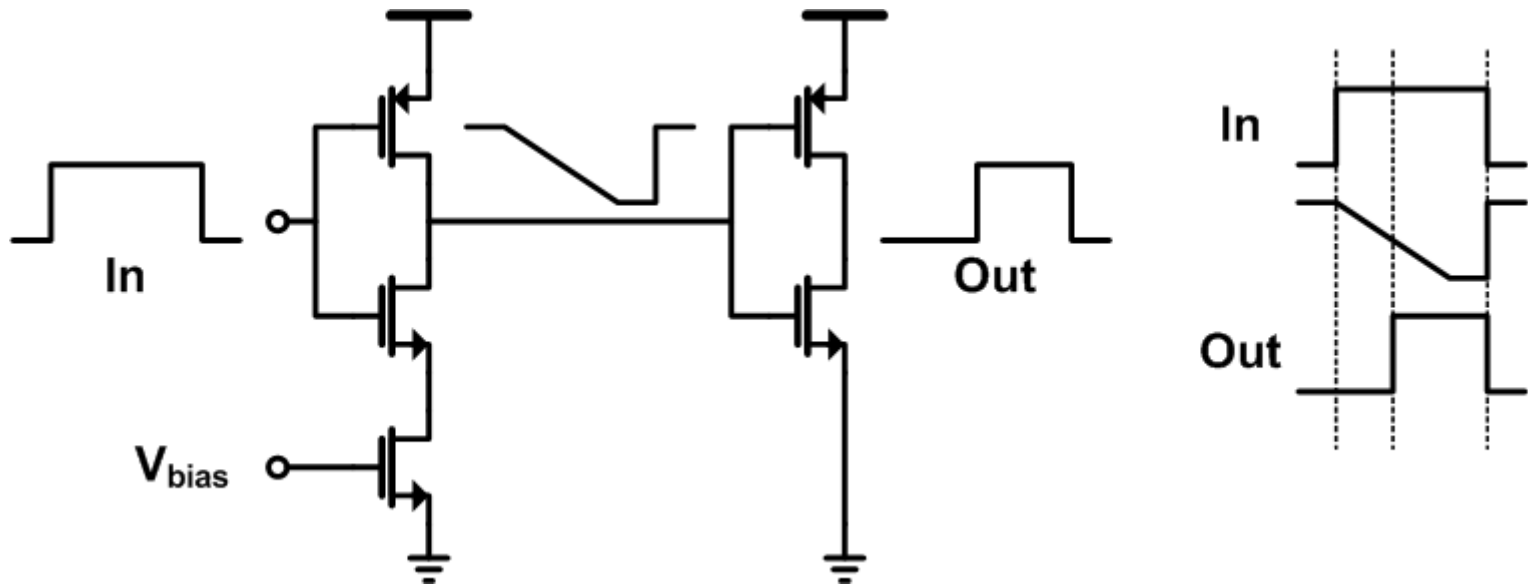
$$T_{err,stop}[k-1] = T_{err,start}[k]$$

$$T_{err} = T_{err,stop}[k] - T_{err,stop}[k-1]$$

First order noise shaping of the quantization error

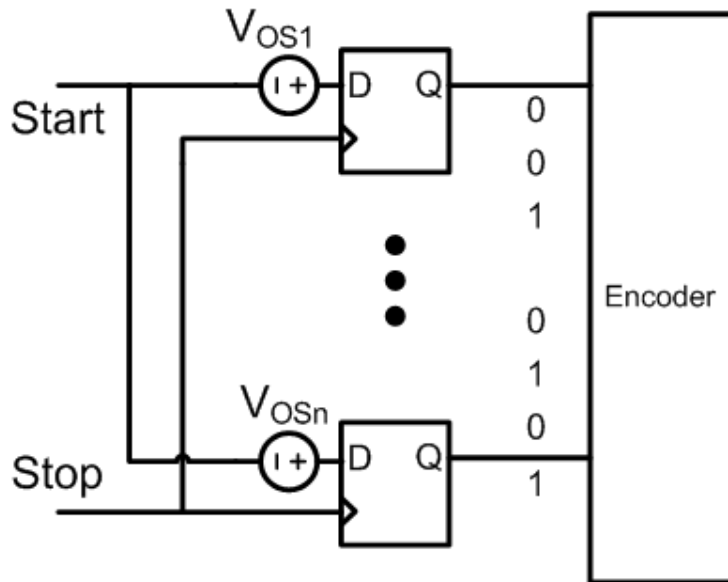
Pulse Shrinking TDC (2)

- The propagation of the rising edge of the input pulse is slowed down by the current starving transistor.

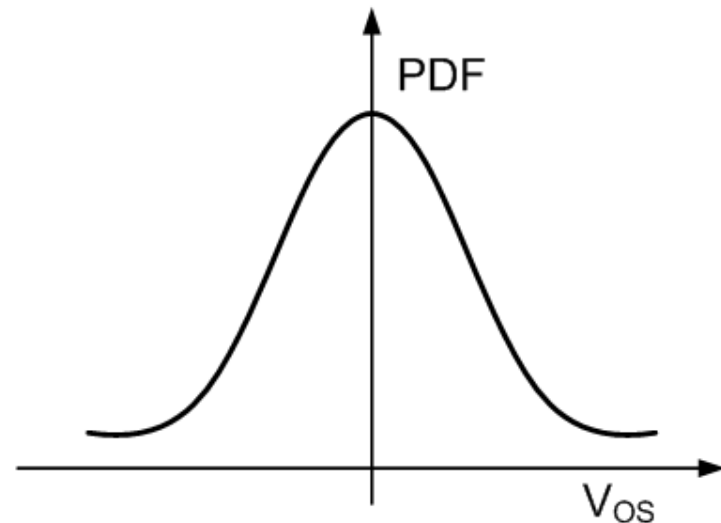


Stochastic TDC

- Using random sampling offset mismatch



(a) STDC architecture

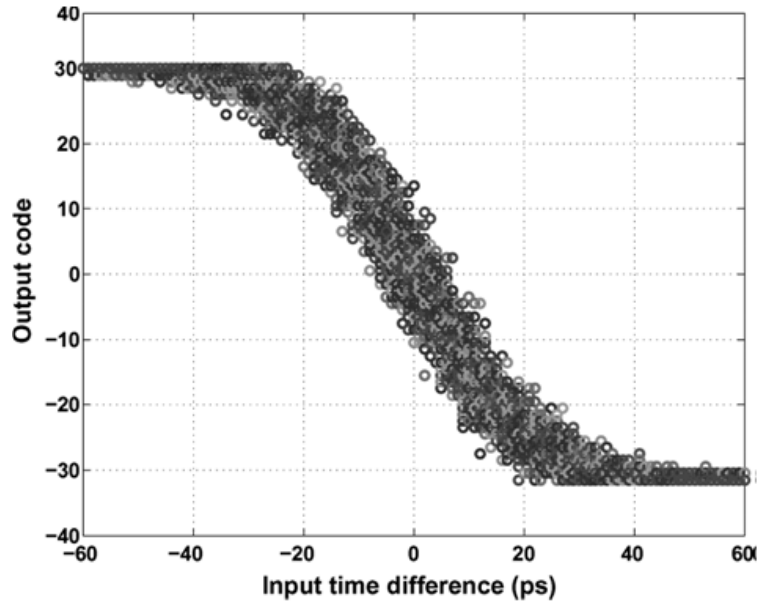


(b) PDF of V_{OS}

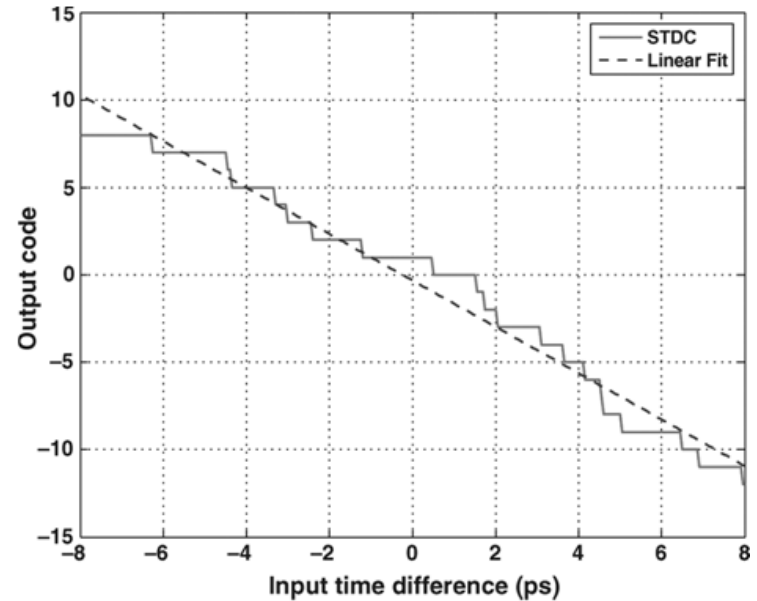
[18]Kratyuk,TCASI,2009

Stochastic TDC

- Behavioral simulations of 100 STDCs



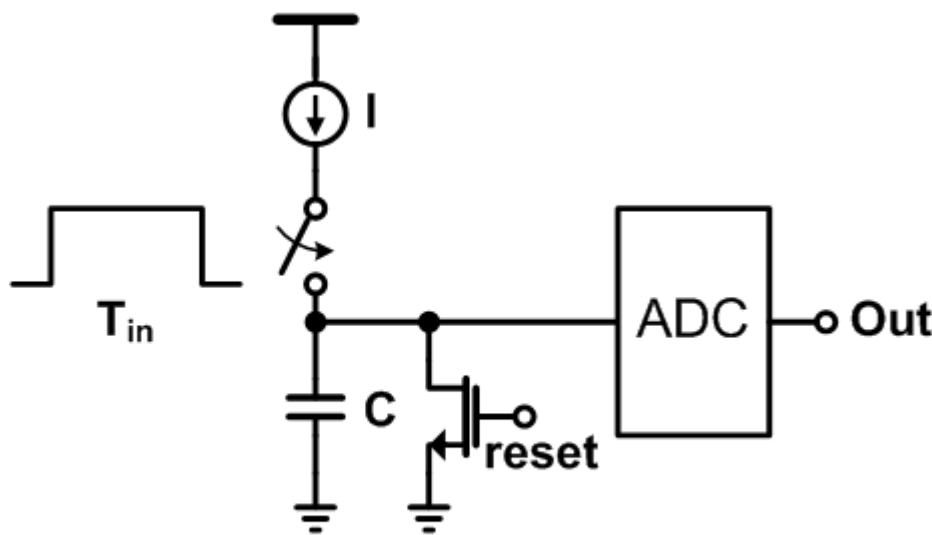
(a) STDC simulation result



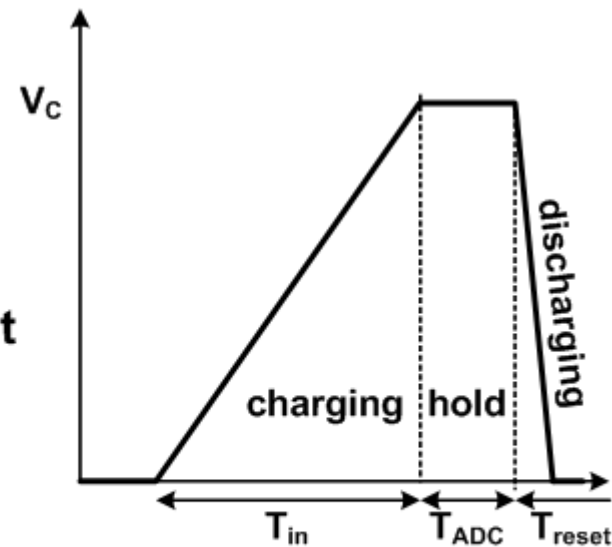
(b) STDC transfer curve

Time-to-Voltage followed by ADC

- The time interval is first converted into a voltage and then the voltage is converted into a digital value by ADC



(a) Simplified schematic



(b) V_C vs time

[19] Maatta, *Instrum.&Meas*,1998

Reference(1)

- [1] T. Rahkonen, et al., "Time interval measurements using integrated tapped CMOS delay lines," in *Circuits and Systems*, vol.1, pp. 201-205, Aug. 1989.
- [2] R. B. Staszewski, et al., "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90 nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 3, pp. 220–224, Mar. 2006.
- [3] B. N. Nikolic, *et al.*, "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 876–884, Jun. 2000.
- [4] P. Dudek, et al., "A high-resolution CMOS time-to-digital converter utilizing a vernier delay line," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 240-247, Feb. 2000.
- [5] S. Henzler, et al., "A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1666-1676, July 2008.
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- [7] T. Tokairin, et al., "A 2.1-to-2.8GHz all-digital frequency synthesizer with a time-windowed TDC," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 470-471.
- [8] J. Lin, B., et al., "A PVT tolerant 0.18MHz to 600MHz self-calibrated digital PLL in 90nm CMOS process," in *IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 488-541.
- [9] C. Hsiang-Hui, et al., "A fractional spur-free ADPLL with loop-gain calibration and phase-noise cancellation for GSM/GPRS/EDGE," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 200-201.
- [10] Jianjun Yu, et al., "A 12-Bit vernier ring time-to-digital converter in 0.13um CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 830-842, Apr. 2010.
- [11] H. Chorng-Sii, et al., "A high-precision time-to-digital converter using a two-level conversion scheme," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 4, pp. 1349-1352, Aug. 2004.

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- [12] C. Poki, et al., "A PVT insensitive vernier-based time-to-digital converter with extended input range and high accuracy," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 2, pp. 294-302, Apr. 2007.
- [13] L. Minjae and A. A. Abidi, "A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769-777, Apr. 2008.
- [14] L. Seon-Kyoo, et al., "A 1GHz ADPLL with a 1.25ps minimum-resolution sub-exponent TDC in 0.18um CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 482-483.
- [15] I. Nissinen, et al., "A CMOS time-to-digital converter based on a ring oscillator for a laser radar," in *Proc. IEEE ESSCIRC*, 2003, pp. 469-472.
- [16] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089-1098, Apr. 2009.

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3.4. All-Digital Frequency Synthesizer

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***Integrated Systems Design Laboratory
Seoul National University***

Outline

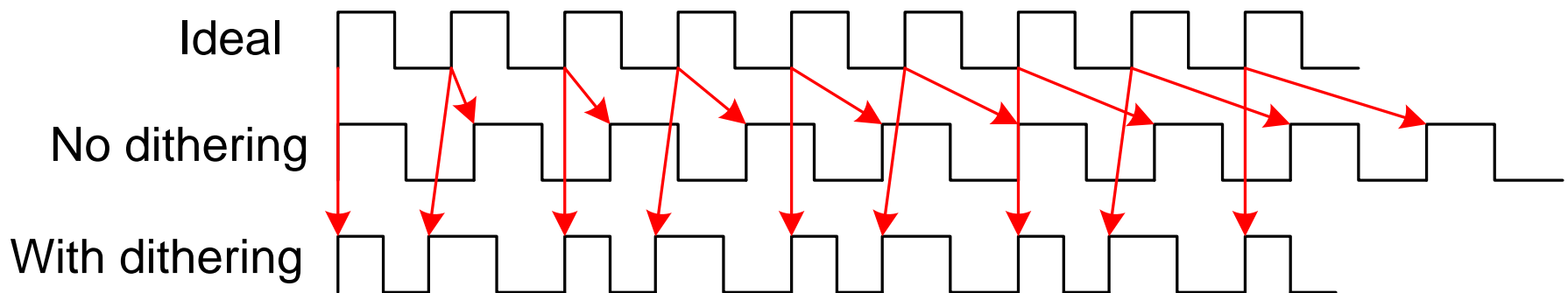
- **Introduction**
- **Recently Published Frequency Synthesizers**

PLL applications

- **Jitter reduction**
- **Skew suppression (zero delay buffer)**
- **Frequency synthesis**
 - **Clock multiplication and carrier generation in wireline and wireless communication systems**
 - **Multiple PLLs in a chip**
 - **Integer-N or fractional-N frequency synthesis**
- **Clock and data recovery**

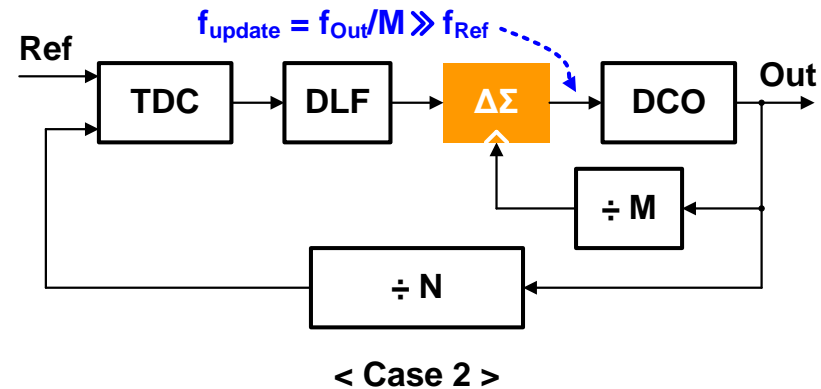
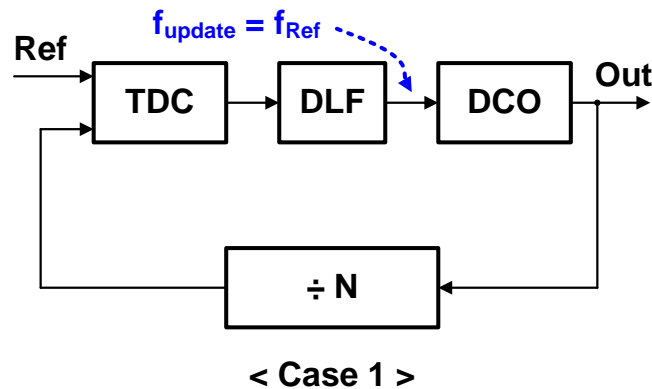
DCO Resolution Enhancement Using $\Delta\Sigma$ -Modulator

- We can't reduce DCO resolution which is determined by physical characteristics.
- However we can improve effective resolution of DCO by averaging a modulated signals.
- $\Delta\Sigma$ -dithering means to change frequency with high modulation frequency.
- Dithering prevents a jitter being accumulated. There only short-term jitter. (In other word, high frequency noise component)



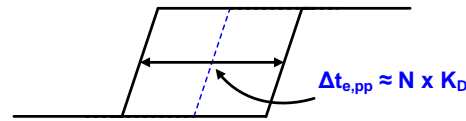
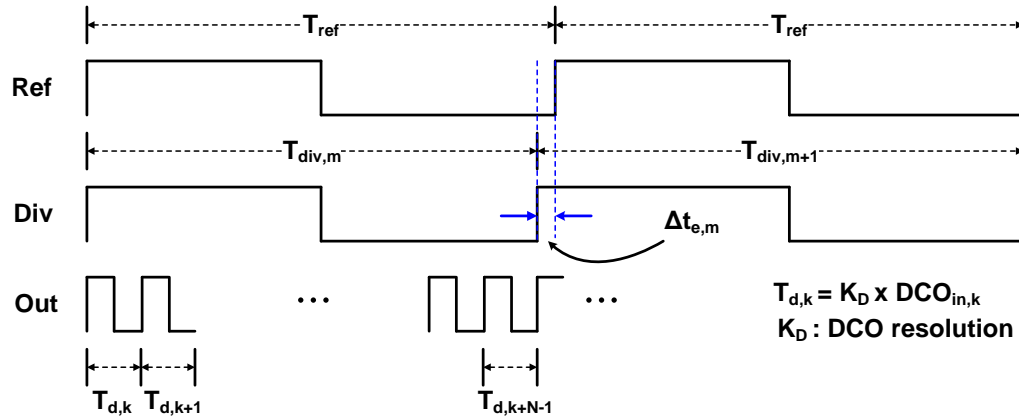
High Resolution DCO Using $\Delta\Sigma$ -Modulator

- Effective frequency resolution is improved by high-speed $\Delta\Sigma$ -dithering
- Higher update rate of DCO is important
 - Phase error accumulates for dithering cycles
 - Peak-to-peak jitter is inversely proportional to update frequency

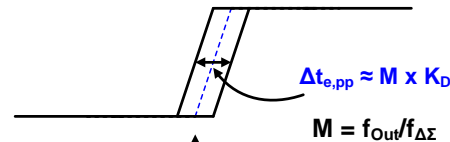


Low Jitter DCO Using $\Delta\Sigma$ -Modulator

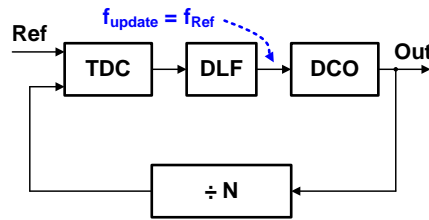
- Peak-to-peak jitter reduction



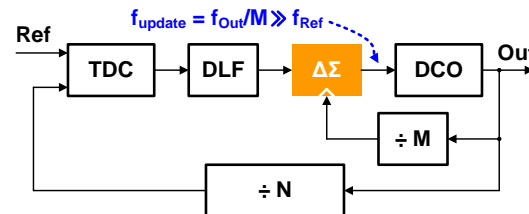
Lock point
< Case 1 >



Lock point
< Case 2 >



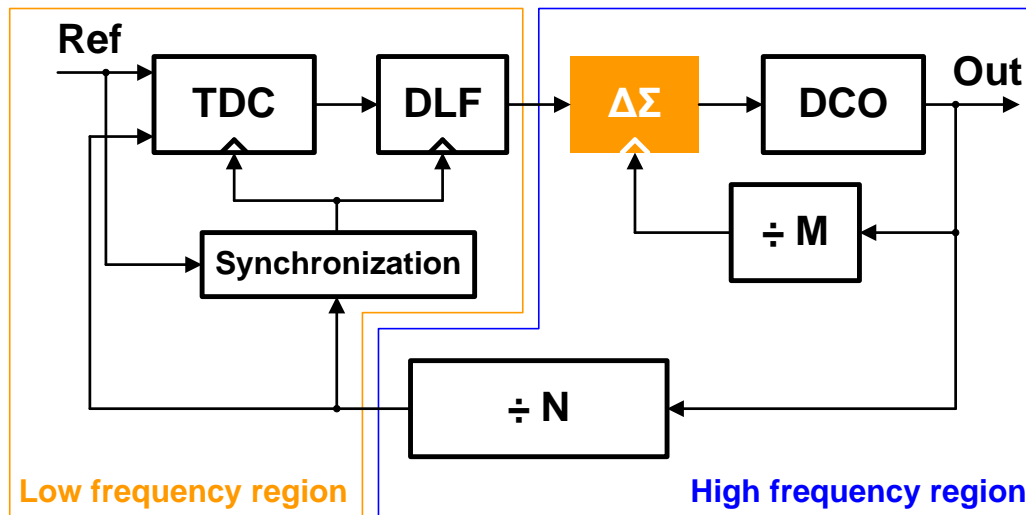
< Case 1 >



< Case 2 >

Low Jitter DCO Using $\Delta\Sigma$ -Modulator

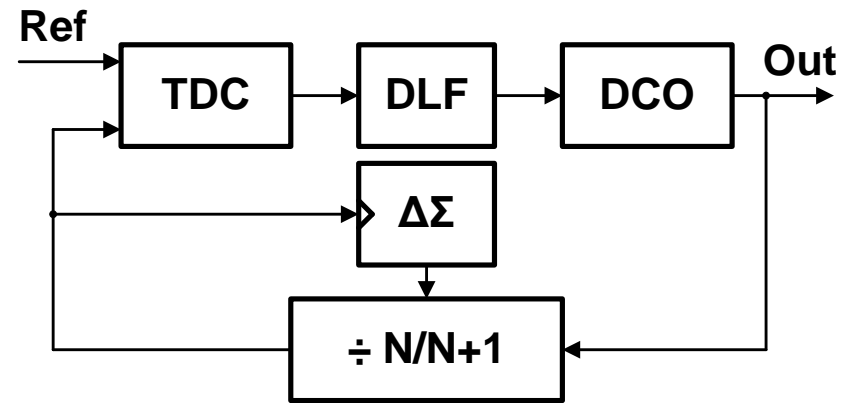
- Design issue
 - Synchronization between lower and higher frequency clock domain
 - Fast $\Delta\Sigma$ -dithering speed for low jitter generation
 - Noise shaping due to $\Delta\Sigma$
 - High frequency noise increases
 - Performance bottleneck in some RF applications



Frequency Multiplication

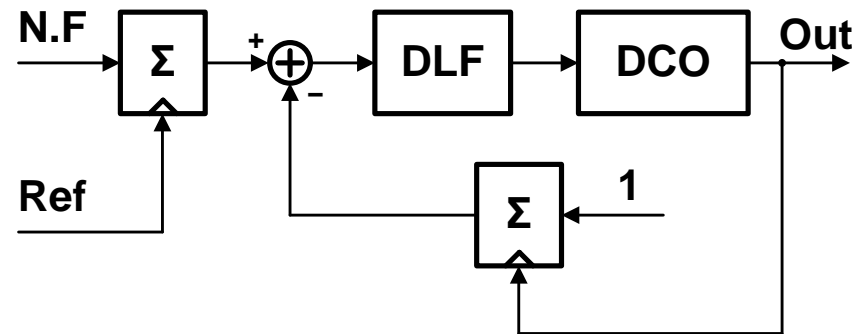
- **General fractional-N operation**

- Divider dithering using $\Delta\Sigma$



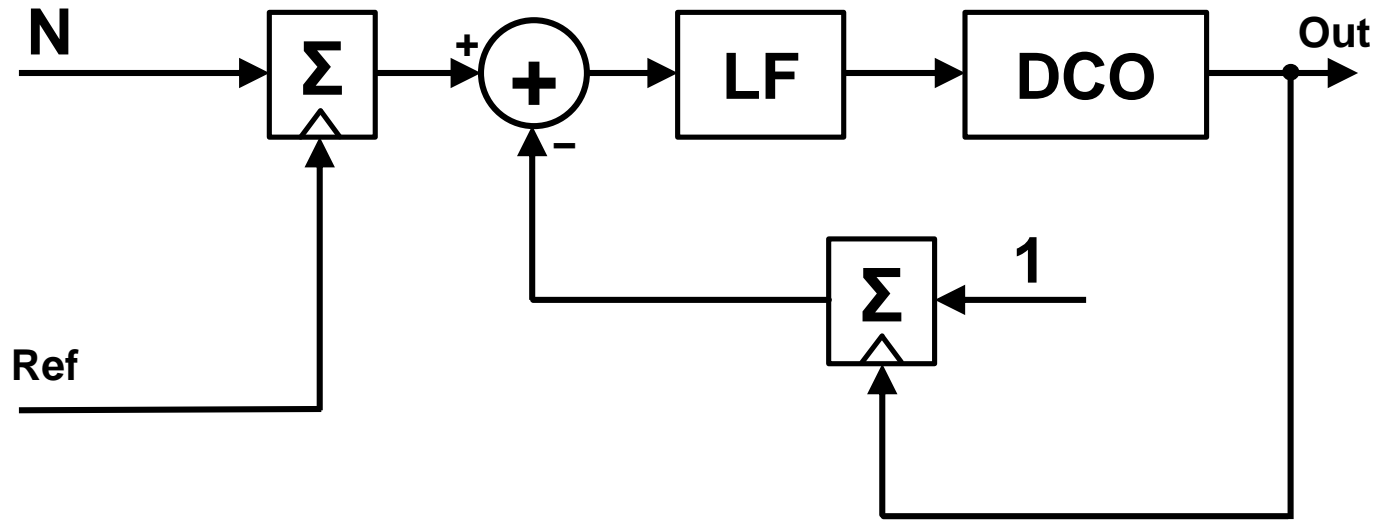
- **Phase-domain operation**

- Accumulate frequency control word (FCW)



Integer Frequency Multiplication

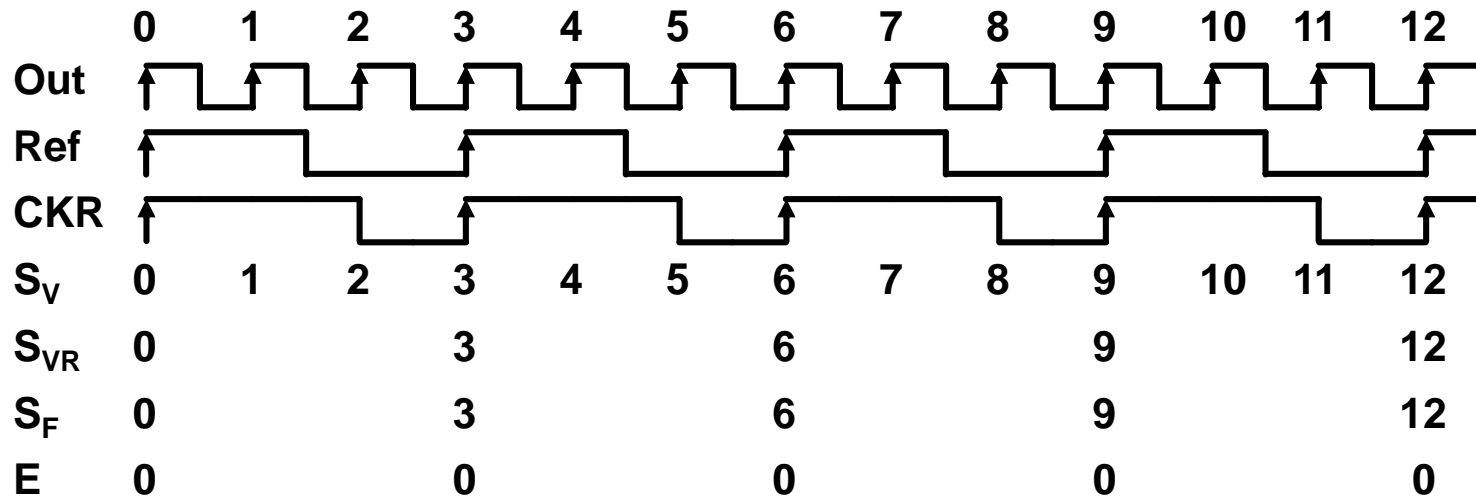
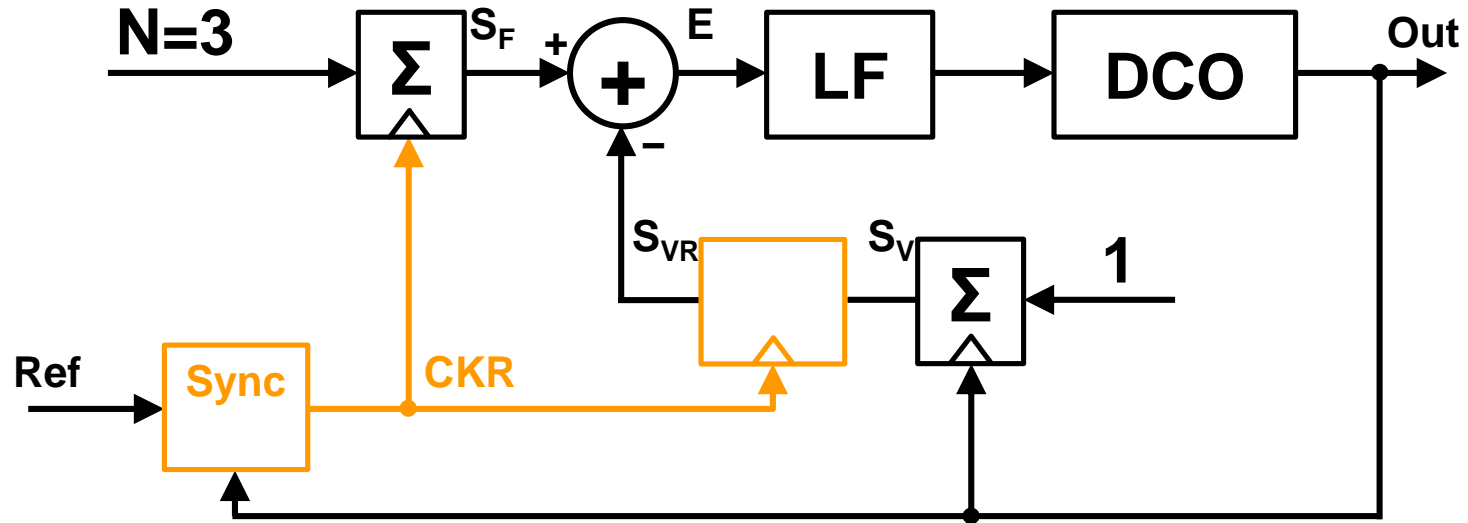
- **Phase-domain operation**



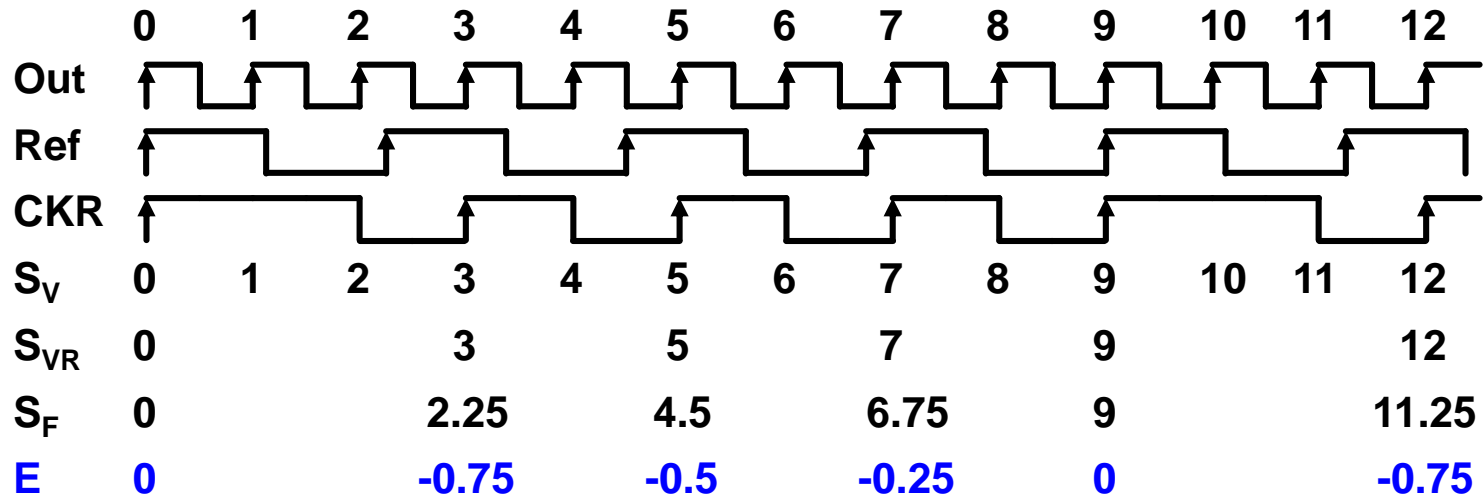
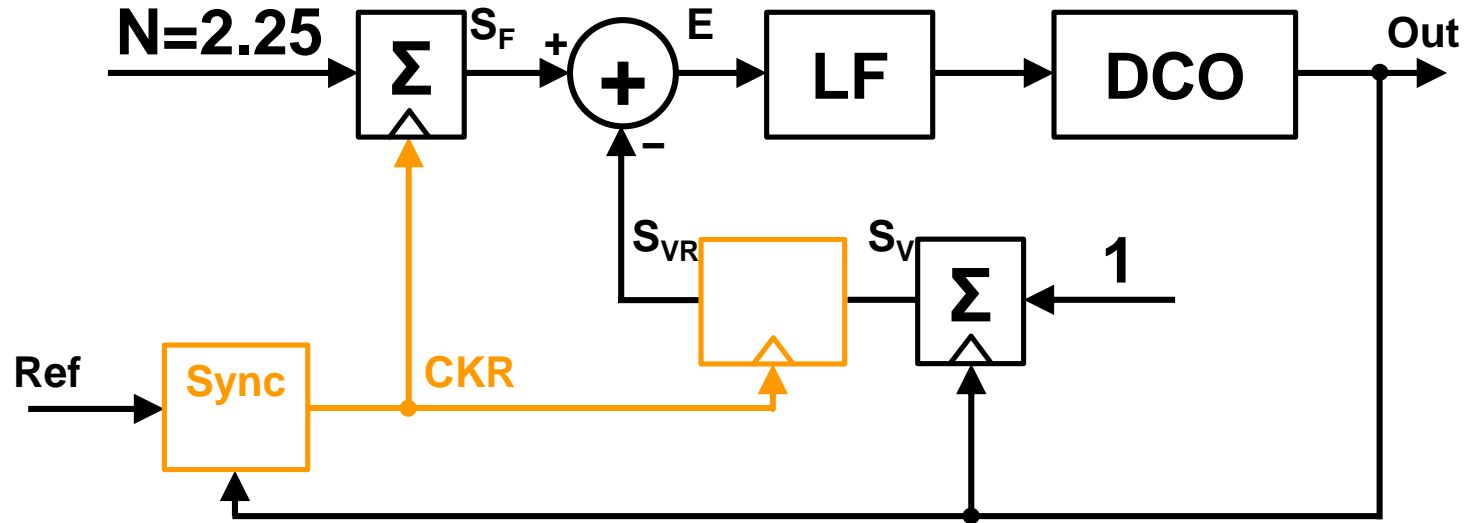
- Long term average: $f_{\text{Ref}} \times N = f_{\text{Out}} \times 1$
- Reference and output clock domains are not synchronous
- Spurious tones occur

[3] R. B. Staszewski TCASII 2005

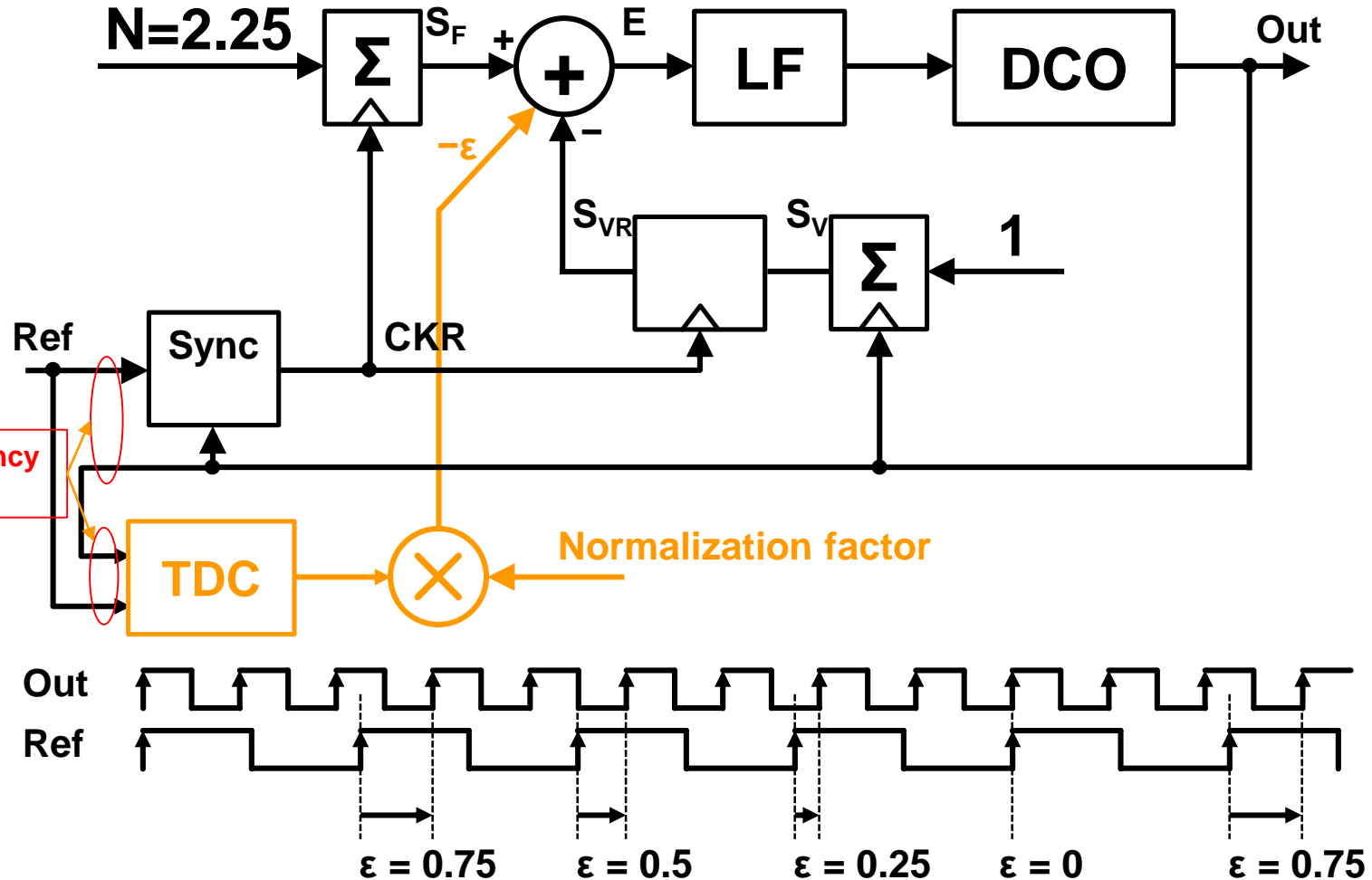
Integer Frequency Multiplication



Fractional Error



Fractional Error Correction



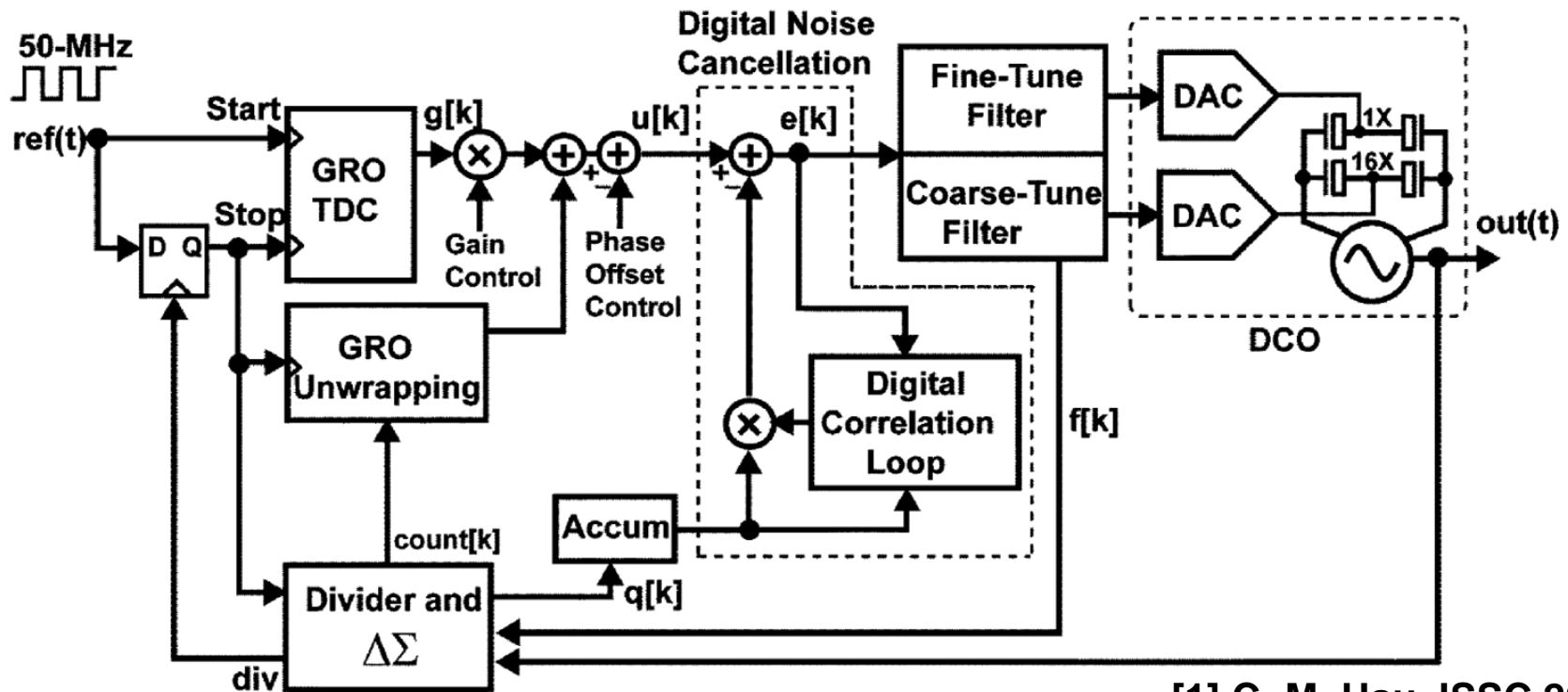
[3] R. B. Staszewski TCASII 2005

Outline

- Introduction
- **Recently Published ADPLLs**

ADPLL Example – 1 (1)

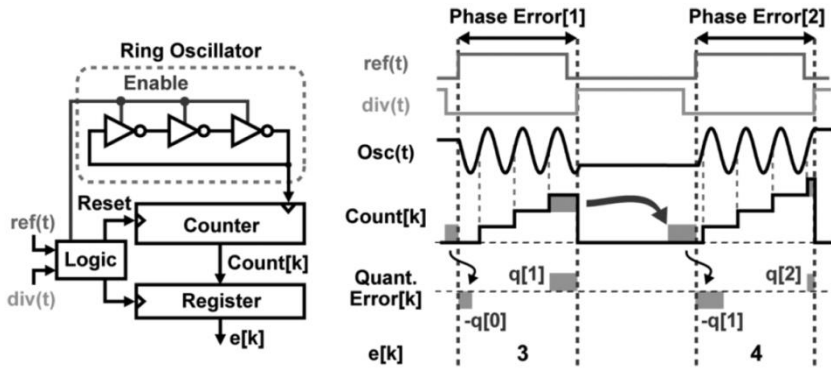
- Multipath gated ring oscillator TDC (GRO-TDC)
- Digital fractional noise cancellation
- Achieve low noise and wide bandwidth



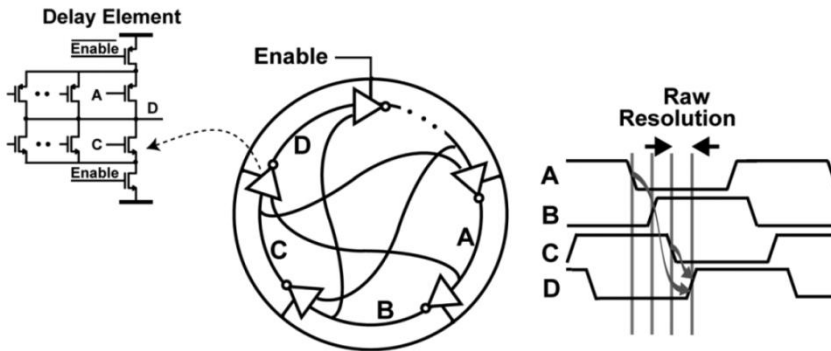
[1] C.-M. Hsu JSSC 2008

ADPLL Example – 1 (2)

Multipath GRO-TDC

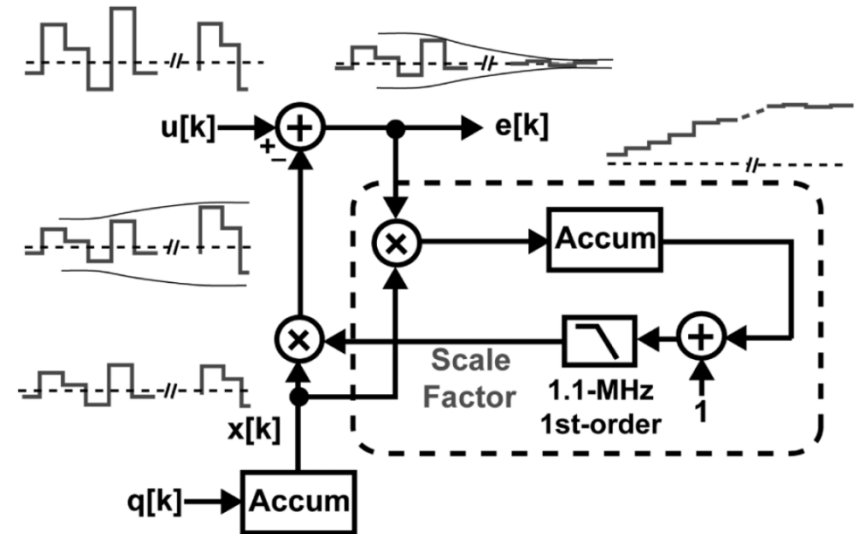


GRO-TDC



Multipath implementation

Digital noise cancellation

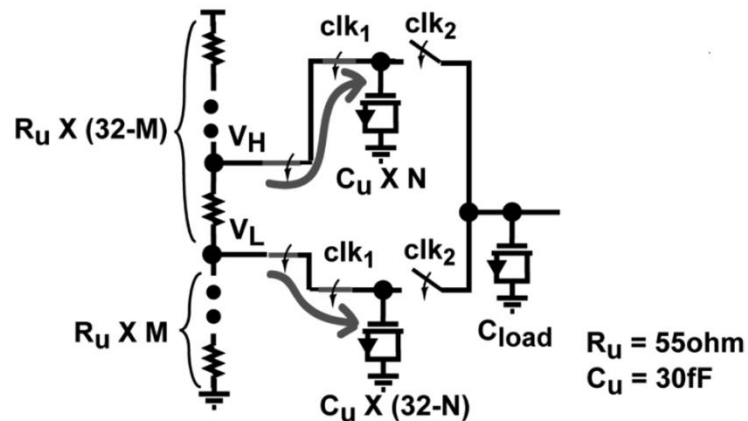


- Deal with the quantization noise directly in the digital domain
- Scale factor is easily computed

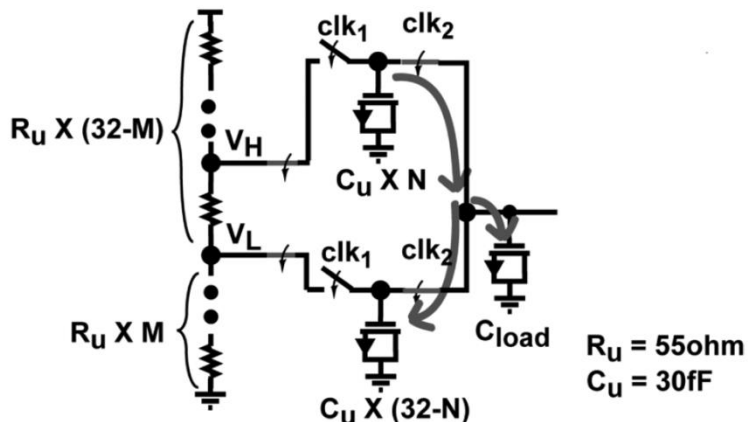
[1] C.-M. Hsu JSSC 2008

ADPLL Example – 1 (3)

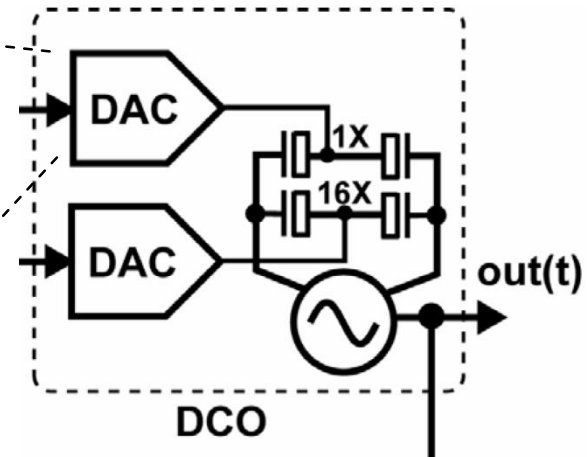
Passive DAC



Step 1: unit capacitor charged



Step 2: charge redistributed and filtered

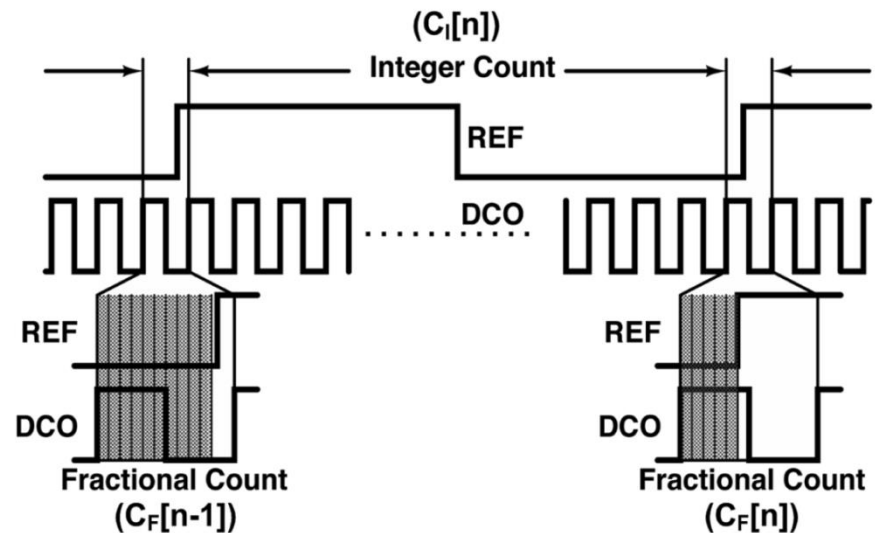
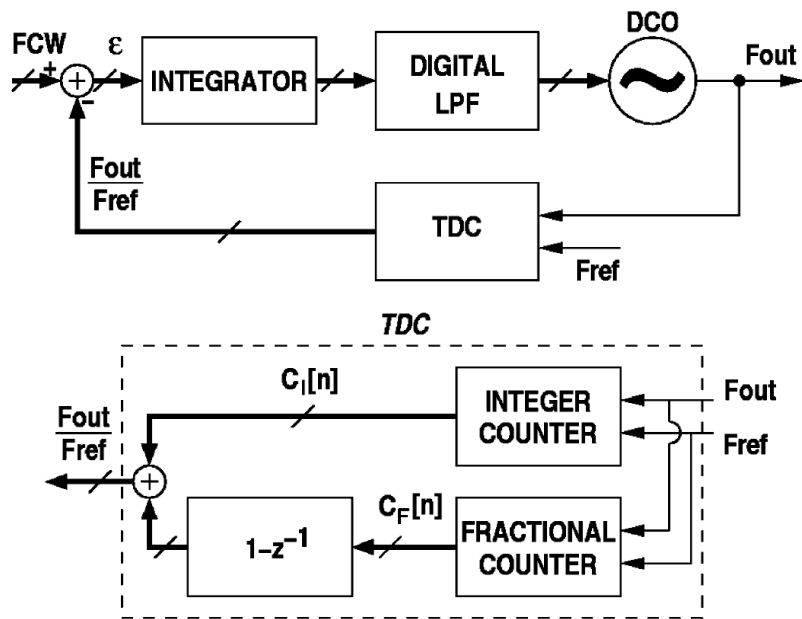


- 5-bit resistor ladder & 5-bit switch-capacitor array
- Minimize active circuitry and no transistor bias current
- Achieve monotonic DAC output with first-order filtering

[1] C.-M. Hsu JSSC 2008

ADPLL Example – 2 (1)

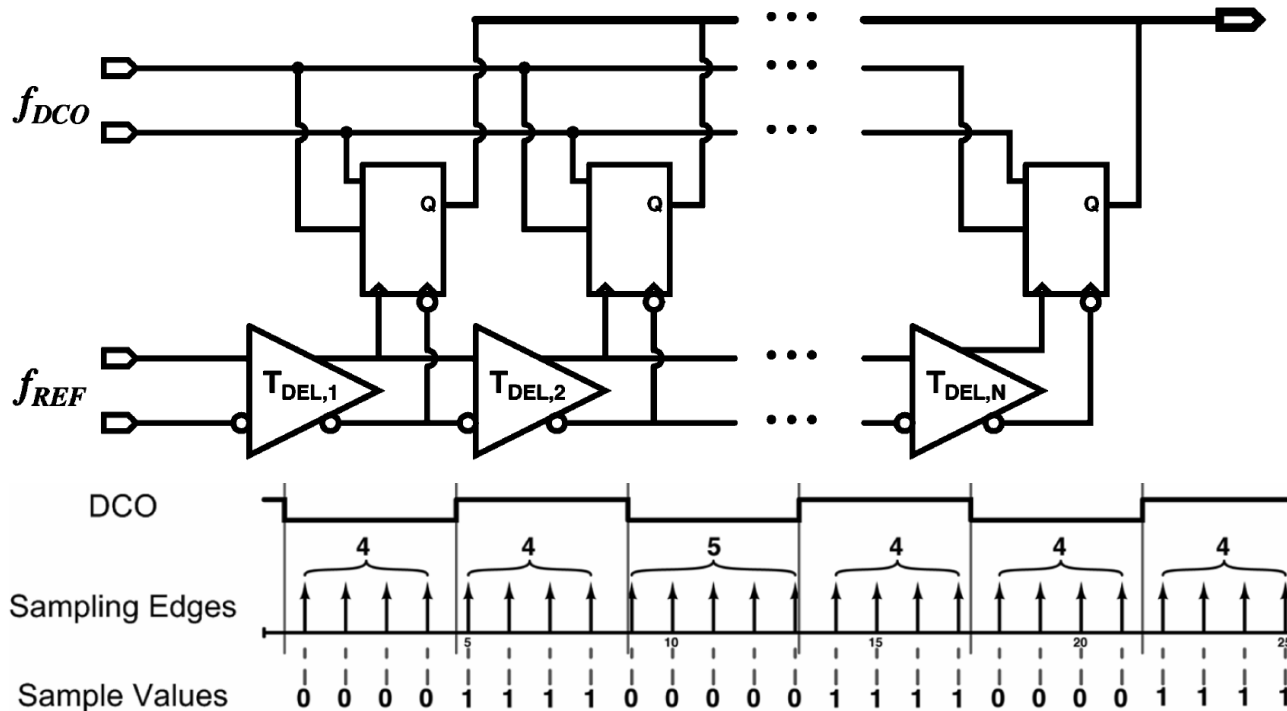
- Fractional ADPLL without feedback divider ([9] R. B. Staszewski TCASII 2005)
- Simplifies synthesizer core
- Requires more accurate TDC calibration to ensure the ratio between F_{out} and F_{ref}



[4] E. Temporiti JSSC 2009

ADPLL Example – 2 (2)

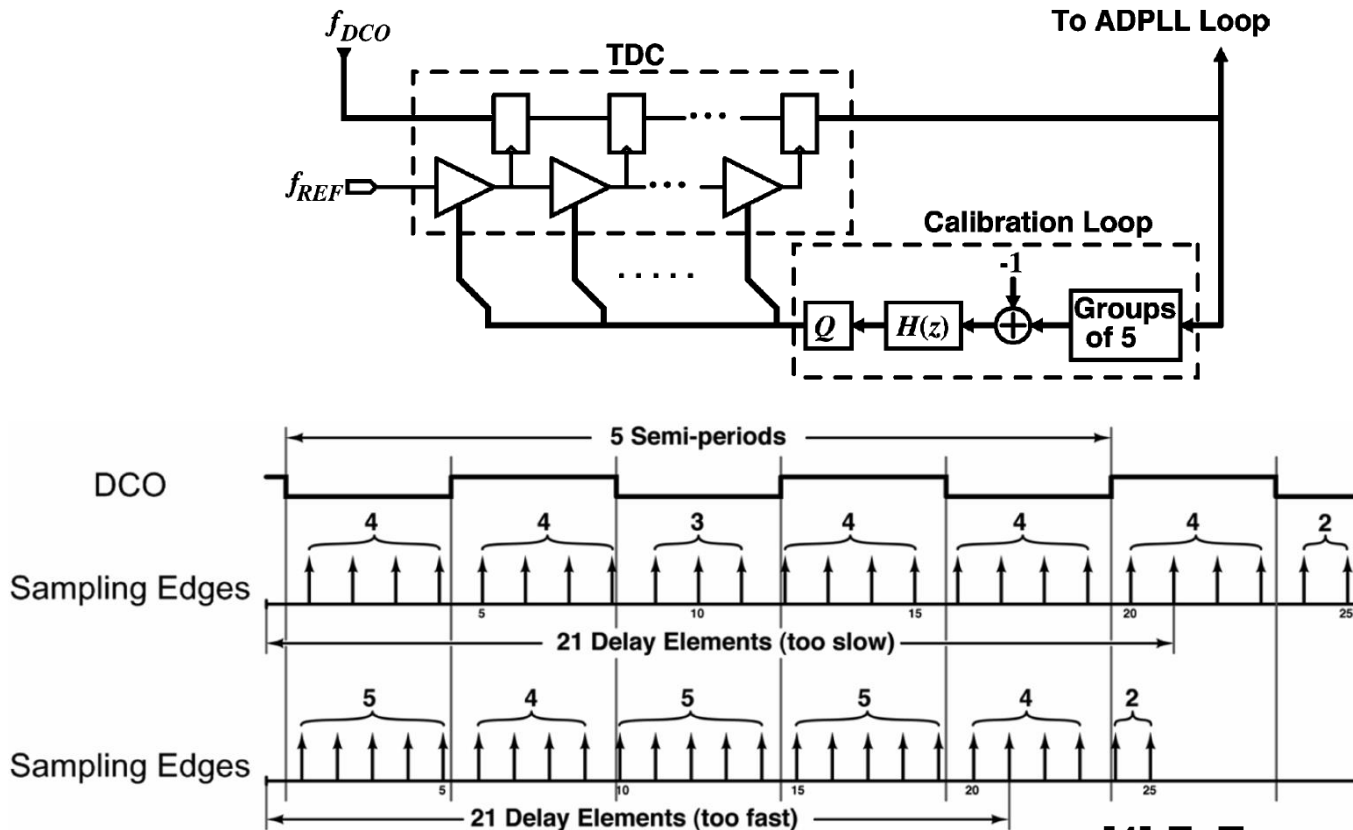
- Fractional counter should meet $N \cdot T_{del} = M \cdot T_{dco} / 2$
M and N are relatively prime
- In this implementation, $21 \cdot T_{del} = 5 \cdot T_{dco} / 2$



[4] E. Temporiti JSSC 2009

ADPLL Example – 2 (3)

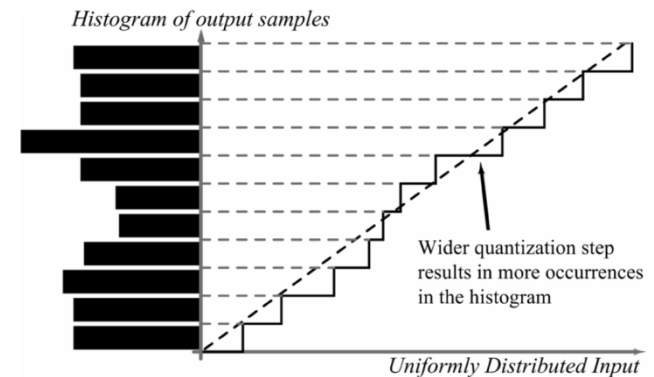
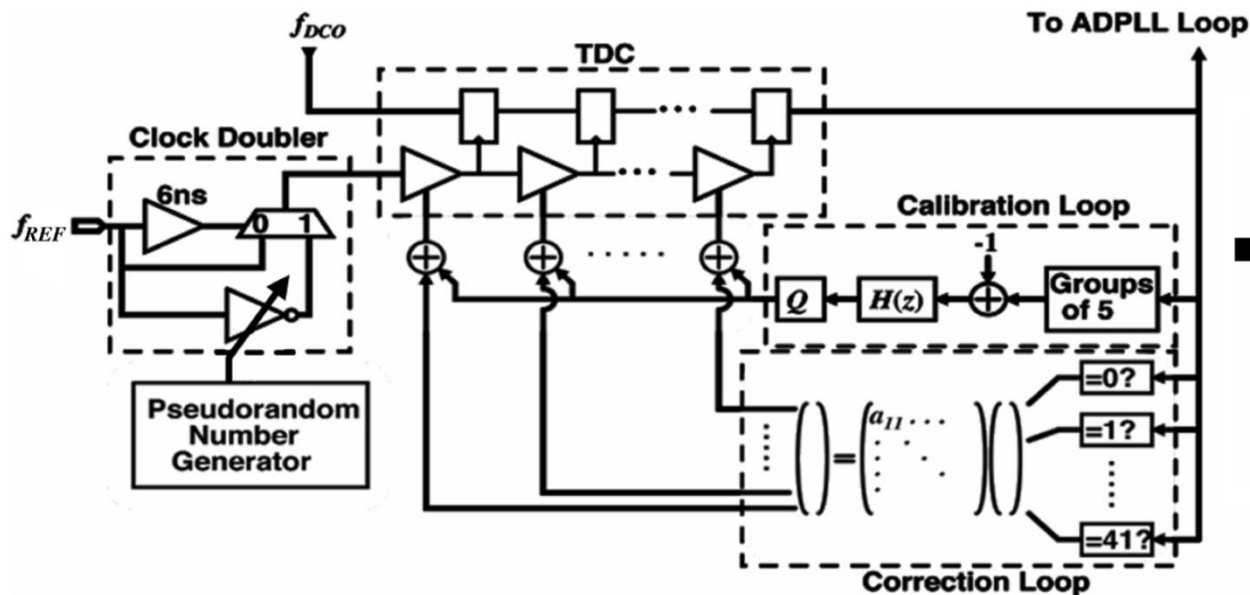
- Fractional counter calibration
 - Monitor the number of group of 5 identical bits



[4] E. Temporiti JSSC 2009

ADPLL Example – 2 (4)

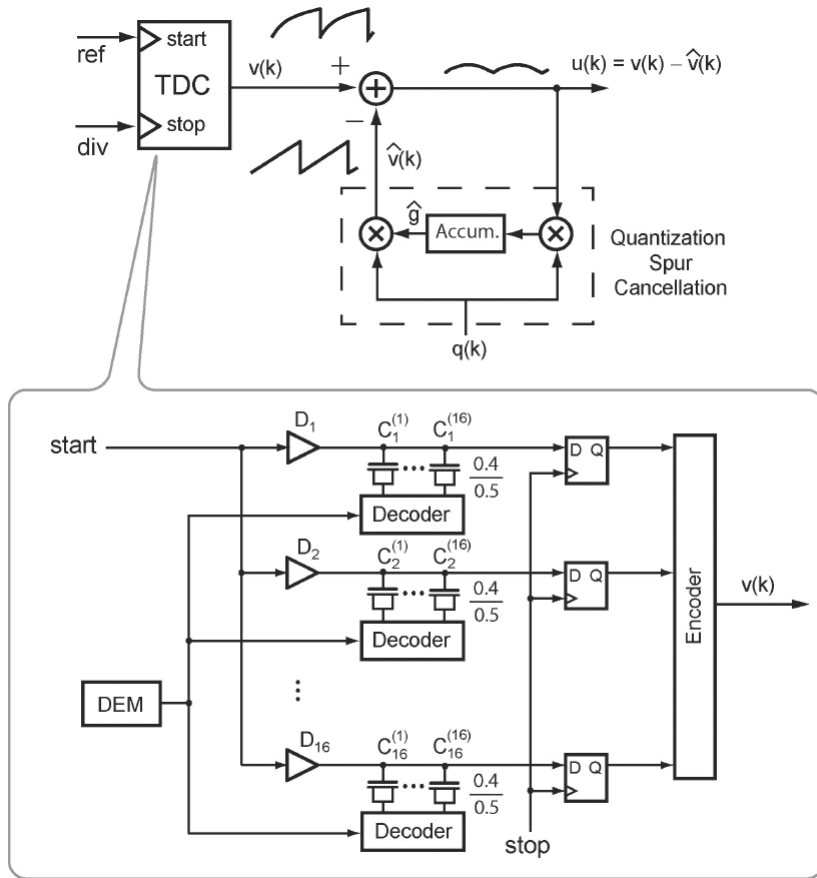
- Fractional counter mismatch correction
 - Reference clock rate is doubled
 - Generate pseudo random jitter injected ‘dirty edge’ only for calibration and correction (‘dirty edges’ are not used by the main loop)
 - Monitor the histogram of fractional counter



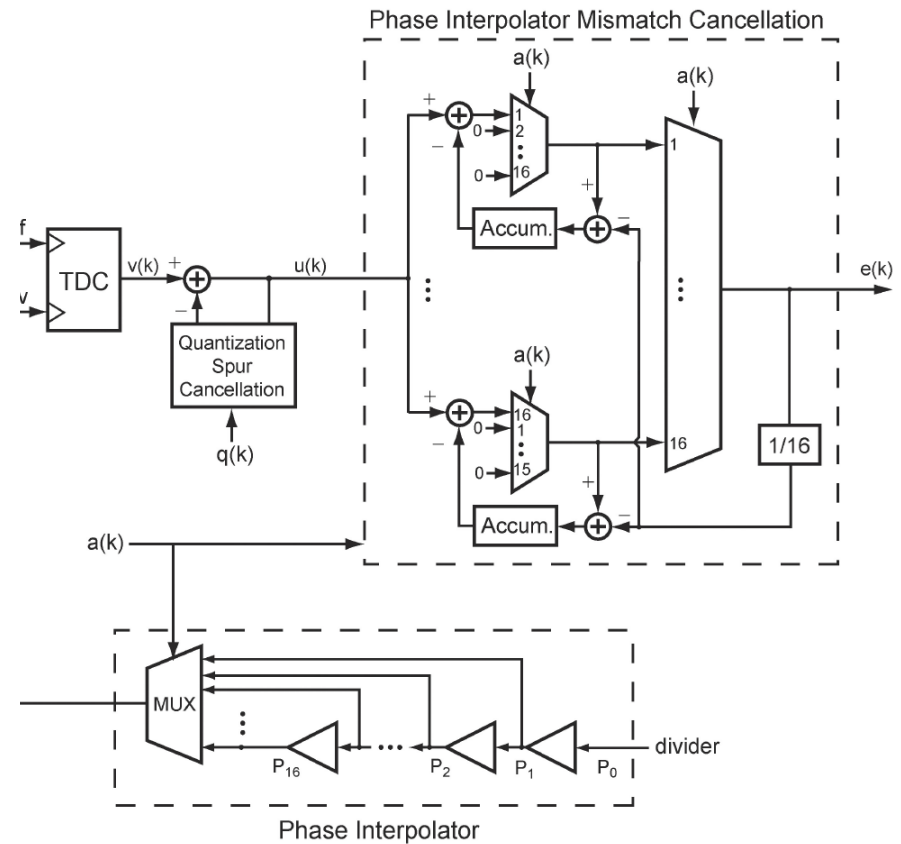
[4] E. Temporiti JSSC 2009

ADPLL Example – 3 (3)

TDC using DEM



Phase interpolator mismatch cancellation



[5] M. Zanuso ISSCC 2010

References (2)

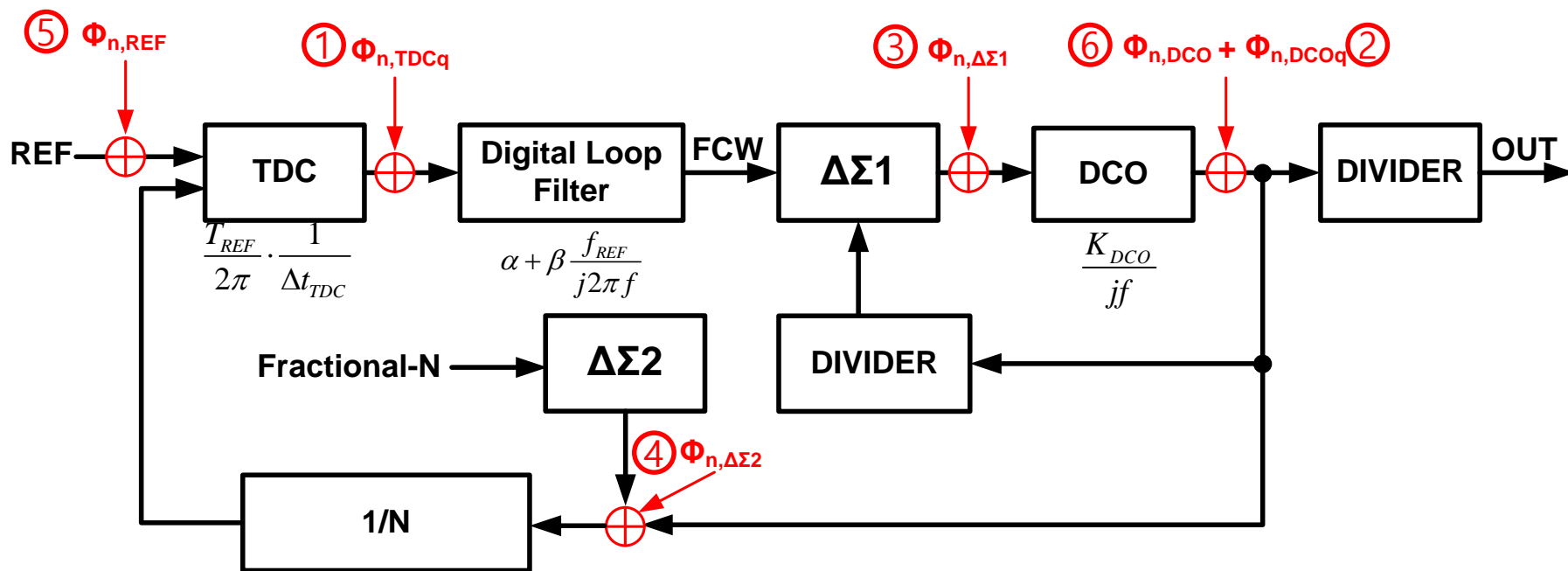
- [1] C.-M. Hsu, et al., “A low-noise wide-BW 3.6-GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776-2786, Dec. 2008.
- [2] R. B. Staszewski, et al., “A digitally controlled oscillator in a 90 nm digital CMOS process for mobile phones,” *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2203-2211, Nov. 2005.
- [3] R. B. Staszewski, et al., “Phase-domain all-digital phase-locked loop,” *IEEE Trans. Circuits and Syst. II: Express Briefs*, vol. 52, no. 3, pp. 159-163, Mar. 2005.
- [4] E. Temporiti, et al., “A 3 GHz fractional all-digital PLL with a 1.8 MHz bandwidth implementing spur reduction techniques,” *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 824-834, Mar. 2009.
- [5] M. Zanuso, et al., “A 3MHz-BW 3.6GHz digital fractional-N PLL with sub-gate-delay TDC, phase-interpolation divider, and digital mismatch cancellation,” in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 476-477

Noise Analysis of All-Digital Pixel Clock Generator

Outline

- ADPLL Block Diagram and Noise Sources
- Output Noise
 - Calculation of Power Spectral Density
 - Verilog Simulation
- Phase Noise and Jitter
 - RMS Jitter Calculation from Phase Noise
 - Verilog simulation
- Simulation Guide

ADPLL Block Diagram and Noise Sources



Open Loop Transfer function

$$A(f) = \frac{T_{REF}}{2\pi} \cdot \frac{1}{\Delta t_{TDC}} \cdot \left(\alpha + \beta \frac{f_{REF}}{j2\pi f} \right) \cdot \frac{K_{DCO}}{jf} \cdot \frac{1}{N}$$

Closed Loop Transfer function

$$G(f) = \frac{A(f)}{1 + A(f)}$$

Output Noise

● Power spectral density of output noise

$$S_{\Phi_{OUT}}(f) = S_{\Phi_{OUT}, TDCq}(f) + S_{\Phi_{OUT}, DCOq}(f) + S_{\Phi_{OUT}, \Delta\Sigma 1}(f) + S_{\Phi_{OUT}, \Delta\Sigma 2}(f) + S_{\Phi_{OUT}, REF}(f) + S_{\Phi_{OUT}, DCO}(f)$$

①
②
③
④
⑤
⑥

Q, TDC ① $S_{\Phi_{OUT}, TDCq}(f) = \frac{(2\pi)^2}{12} \cdot \left(\frac{\Delta t_{TDC}}{T_{REF}} \right)^2 \cdot \frac{1}{f_{REF}} \cdot |N \cdot G(f)|^2$

Q, DCO ② $S_{\Phi_{OUT}, DCOq}(f) = \frac{1}{12} \cdot \left(\frac{\Delta f_{DCO, eff}}{f} \right)^2 \cdot \frac{1}{f_{\Delta\Sigma}} \cdot \left(\text{sinc} \frac{f}{f_{\Delta\Sigma}} \right)^2 \cdot |1 - G(f)|^2$

DCO dither ③ $S_{\Phi_{OUT}, \Delta\Sigma 1}(f) = \frac{1}{12} \cdot \left(\frac{\Delta f_{DCO, eff}}{f} \right)^2 \cdot \frac{1}{f_{\Delta\Sigma}} \cdot \left(2 \sin \frac{\pi f}{f_{\Delta\Sigma}} \right)^{2n} \cdot |1 - G(f)|^2$

NTF1 is applied to ①, ④, ⑤

FDIVIDER ④ $S_{\Phi_{OUT}, \Delta\Sigma 2}(f) = \frac{(2\pi)^2}{12} \cdot \left(2 \sin \frac{\pi f}{f_{REF}} \right)^{2n-2} \cdot \frac{1}{f_{REF}} \cdot |G(f)|^2$

NTF2 is applied to ②, ③, ⑥

REF ⑤ $S_{\Phi_{OUT}, REF}(f) = \frac{2FkT}{P_{sig,1}} \cdot \left(1 + \left(\frac{f_{REF}}{2Q_{VCXO} \cdot f} \right)^2 \right) \cdot \left(1 + \frac{f_{1/f^3, REF}}{f} \right) \cdot |N \cdot G(f)|^2$

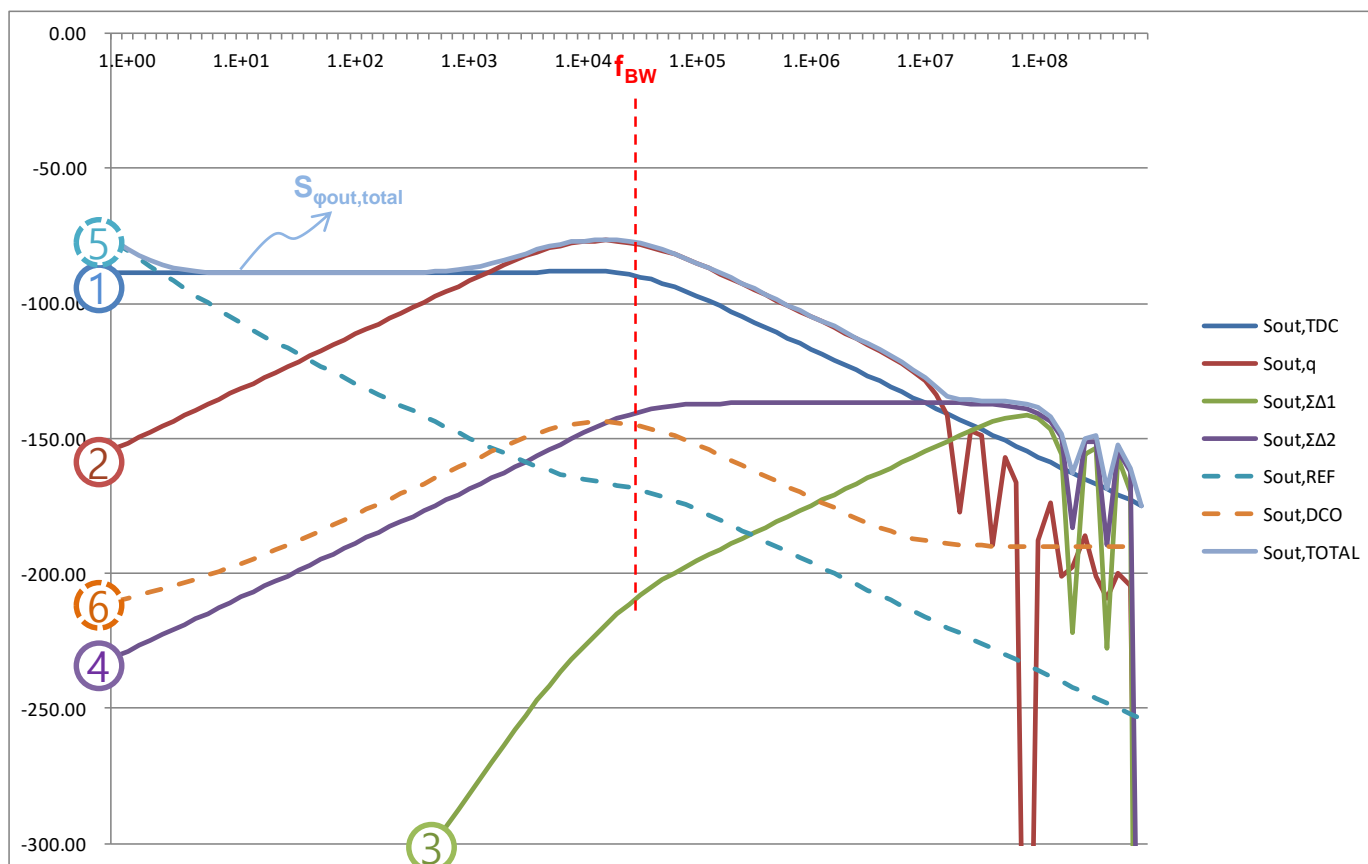
DCO ⑥ $S_{\Phi_{OUT}, DCO}(f) = \frac{2FkT}{P_{sig,2}} \cdot \left(1 + \left(\frac{f_{DCO}}{2Q_{DCO} \cdot f} \right)^2 \right) \cdot \left(1 + \frac{f_{1/f^3, DCO}}{f} \right) \cdot |1 - G(f)|^2$

Output Noise

- Plot of Power spectral density of output noise

$$S_{\Phi_{OUT}}(f) = S_{\Phi_{OUT},TDCq}(f) + S_{\Phi_{OUT},DCOq}(f) + S_{\Phi_{OUT},\Delta\Sigma1}(f) + S_{\Phi_{OUT},\Delta\Sigma2}(f) + S_{\Phi_{OUT},REF}(f) + S_{\Phi_{OUT},DCO}(f)$$

①
②
③
④
⑤
⑥



In this case, DCO quantization noise is dominant !!

Phase Noise and Jitter

- RMS Jitter calculation from phase noise

$$C(t) = A \sin(2\pi f_c t + \theta(t)) = A \sin\left(2\pi f_c \left(t + \frac{\theta(t)}{2\pi f_c}\right)\right) \rightarrow J_{PER} = \frac{\theta(t)}{2\pi f_c}$$

$$n(t) = \frac{A}{2} \theta(t) \quad S_n(f) = \int_{-\infty}^{\infty} n(t) e^{-2\pi f t} dt = \frac{A^2}{4} S_\theta(f)$$

$$S_\theta(f) = \frac{4}{A^2} \int_{-\infty}^{\infty} n(t) e^{-2\pi f t} dt = \frac{4}{A^2} S_n(f) = 10^{\frac{L(f)}{10}}$$

$$\langle \theta^2(t) \rangle = 2 \int_0^{\infty} S_\theta(f) df = 2 \int_0^{\infty} \frac{4}{A^2} S_n(f) df = 2 \int_0^{\infty} 10^{\frac{L(f)}{10}} df$$

$$J_{RMS} = \frac{1}{2\pi f_c} \sqrt{\langle \theta^2(t) \rangle} = \frac{1}{2\pi f_c} \sqrt{2 \int_0^{\infty} 10^{\frac{L(f)}{10}} df}$$

Phase Noise and Jitter

- Verilog simulation (calculation and simulation result comparison)

