Topics in IC Design

7.1 Modeling of Transmission Lines

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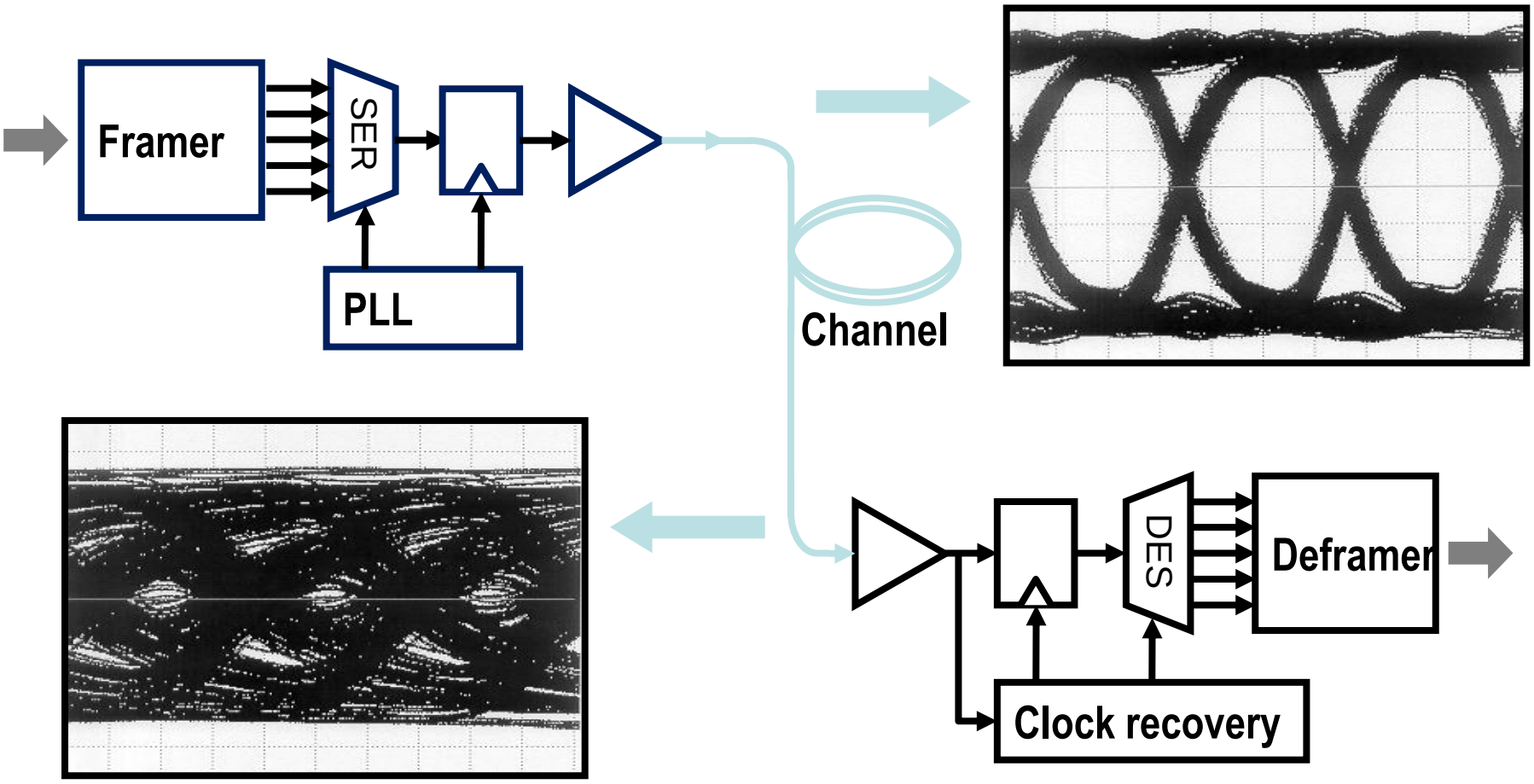
2020 Spring

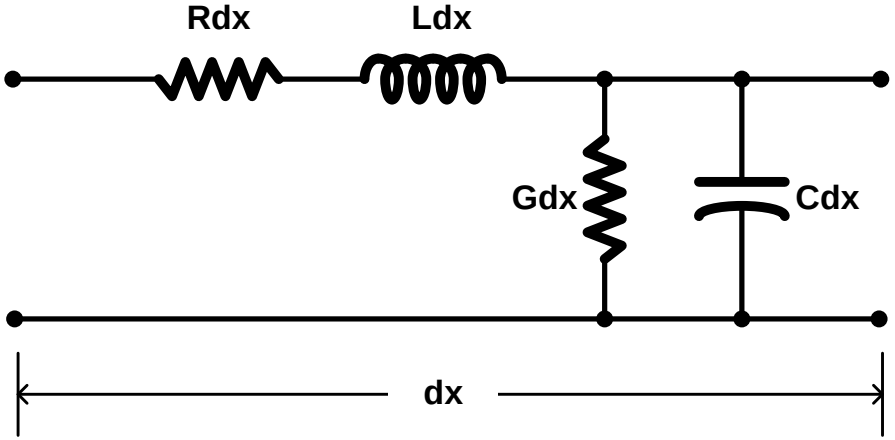
Serial-Link Architecture



Receiver should compensate channel loss to recover transmitted signal completely!!

Distributed Parameter Channel Model

Basic Transmission Line Model



$$V_+(t,x) = V_+(0,0)e^{j\omega t-\gamma x} \qquad V_-(t,x) = V_-(0,L)e^{j\omega t+\gamma x}$$

$$I_+(t,x) = I_+(0,0)e^{j\omega t-\gamma x} \qquad I_-(t,x) = I_-(0,L)e^{j\omega t+\gamma x}$$

$$V_+(t,x) = I_+(t,x)Z_0 \qquad V_-(t,x) = I_-(t,x)Z_0$$

$$V(t,x) = V_+(t,x) + V_-(t,x)$$

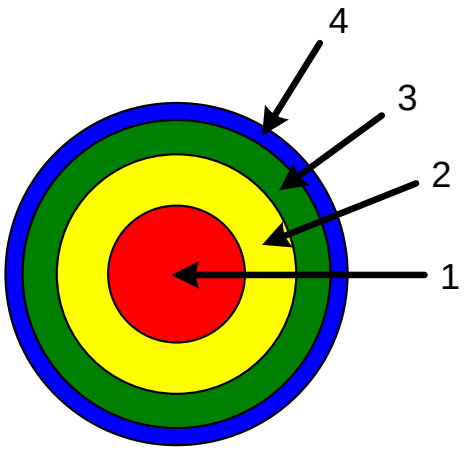
$$I(t,x) = I_+(t,x) - I_-(t,x)$$

$$\text{Complex propagation constant}: \gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

$$\text{Characteristic impedance}: Z_o = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Skin Effect

- **Skin effect is the tendency of an alternating electric current(AC) to distribute itself within a conductor so that the current density near the surface of the conductor is greater than at its core.**
- **The skin depth is the depth where the current has fallen off to e^{-1}(0.381) of its original value.**
- **The effective series resistance of the cable corresponding to this depth increases with square root of frequency**



Current Distribution Shell Model

Skin depth: $\delta_s = \sqrt{\frac{1}{\pi f \mu \sigma}}$

Surface resistance (Sheet resistance): $R_S = \frac{1}{\sigma \delta_s} = \sqrt{\frac{\pi f \mu}{\sigma}}$

Effective series resistance: $R_{skin} = \frac{1}{2\mathrm{r}} \sqrt{\frac{f \mu \rho}{\pi}}$

Skin effect frequency $f_{skin} = \frac{\rho}{\pi \cdot \mu \cdot r^2}$ (skin depth = radius)

Dielectric Loss

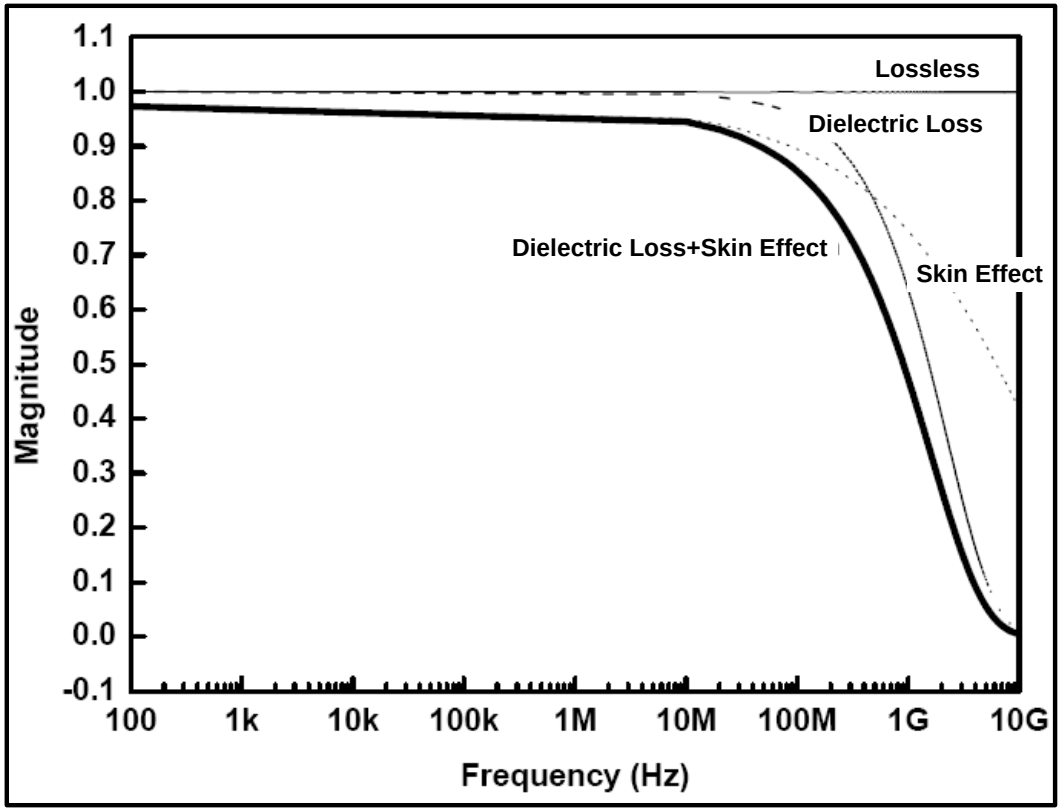
- **With some insulating materials, dielectric absorption causes frequency dependent attenuation**
  - This loss can be modeled as a conductance *G* between the signal wire and ground.

- **Dielectric loss for each material is usually expressed in terms of a parameter, called the loss tangent.**

$$\epsilon = \epsilon' - j\epsilon''$$

$$\tan \delta_D = \frac{\epsilon''}{\epsilon'} = \frac{G_{AC}}{\omega C}$$

Frequency Dependent Attenuation- Skin Effect + Dielectric Loss



$$R_{Skin} = \frac{1}{2r}\sqrt{\frac{f\mu\rho}{\pi}} \quad \Rightarrow \quad R_{skin} \propto \sqrt{f}$$

$$G_{AC} = \omega C \tan\delta_D \quad \Rightarrow \quad G_{AC} \propto f$$

$$\gamma = \alpha + j\beta = \sqrt{(R_{Skin} + j\omega L)(G_{AC} + j\omega C)}$$

$$\cong j\omega\sqrt{LC} + \frac{R_{Skin}}{2Z_0} + \frac{G_{AC}Z_0}{2}$$

Channel Transfer Function (1)

- **When properly terminated, the transfer-function of a cable is modeled by**

$$H(d,w) = e^{-d\gamma(\omega)} = e^{-d\alpha(\omega)}e^{-jd\beta(\omega)}$$

where propagation constant $\gamma(\omega) = \alpha(\omega) + j\beta(\omega)$

d : cable length

α, β : attenuation and phase constants

- **From lossy propagation constant where G=0**

$$\gamma(\omega) = \sqrt{(R + j\omega L)(j\omega C)}$$

$$= j\omega\sqrt{LC}\sqrt{1 + \frac{R}{j\omega L}}$$

Channel Transfer Function (2)

- **When you alter the path of current, you also alter the inductance.**

$$Z_{AC} = Z_{real} + Z_{image}$$

- Therefore, to fully characterize skin effect, you need to consider both the changes in resistance and inductance with frequency.
- Self-inductance per length = $\mu/8\pi$.
- By Wheeler's assumption about the equality of the real and imaginary parts of conductor internal impedance.

$$Z_{AC} = R_{AC}(1+\mathrm{j})\sqrt{\omega}\,[\,\Omega/\mathrm{m}]$$

[Wheeler H. A. "Formulas for the skin-effect", Proc. IRE, Vol. 30, 412-424, 1942

- The term (1+j) signifies the real(resistive) and imaginary(inductive) parts are equal

$$R = R_{DC} + R_{AC}(1+j)\sqrt{\omega}\ @\ R_{DC} = \frac{\rho}{A}$$

$$R_{Skin} = \frac{1}{2r}\sqrt{\frac{f\mu\rho}{\pi}} = R_{AC}\sqrt{\omega} \qquad \therefore\ R_{AC} = \frac{1}{2\pi r}\sqrt{\frac{\mu\rho}{2}}$$

Channel Transfer Function (3)

- **If frequency is very high**

$$R \approx R_{AC}(1+j)\sqrt{\omega}$$

$$\gamma(\omega) = j\omega\sqrt{LC}\sqrt{1+\frac{R}{j\omega L}}$$

$$= j\omega\sqrt{LC}\sqrt{1+\frac{R_{AC}(1-j)}{L\sqrt{\omega}}}$$

- **Using approximation $(1+x)^{1/2} \approx 1+x/2$ for $x \ll 1$**

$$\alpha(\omega) = \frac{R_{AC}}{2}\sqrt{\frac{\omega C}{L}}\ (\text{same}), \quad \beta(\omega) = \omega\sqrt{\text{LC}} + \frac{R_{AC}}{2}\sqrt{\frac{\omega C}{L}}\ (\text{second term added})$$

$$H_{dB}(d,f) = 20\log_{10}\left|H(d,f)\right| = -8.68d \times R_{AC}\sqrt{\frac{\pi f C}{2L}}$$

$$\therefore \textit{The gain in dB} \propto -\sqrt{f}$$

Coaxial Cable

- **Resistance at DC**

$$R = \frac{\sigma}{\pi d^2}$$

- **Series resistance**

$$R_{Skin} = \frac{R_s}{2\pi}\left(\frac{1}{D} + \frac{1}{d}\right)$$

- **External Series Inductance**

$$L = \frac{\mu}{2\pi}\ln(D/d) = \frac{\mu_0\mu_r}{2\pi}\ln(D/d)$$

- **Internal Self-Inductance at DC**

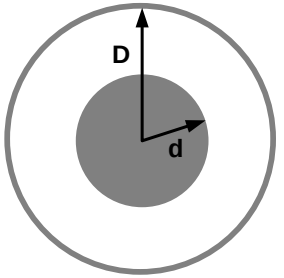
$$L_0 = \frac{\mu}{8\pi}$$

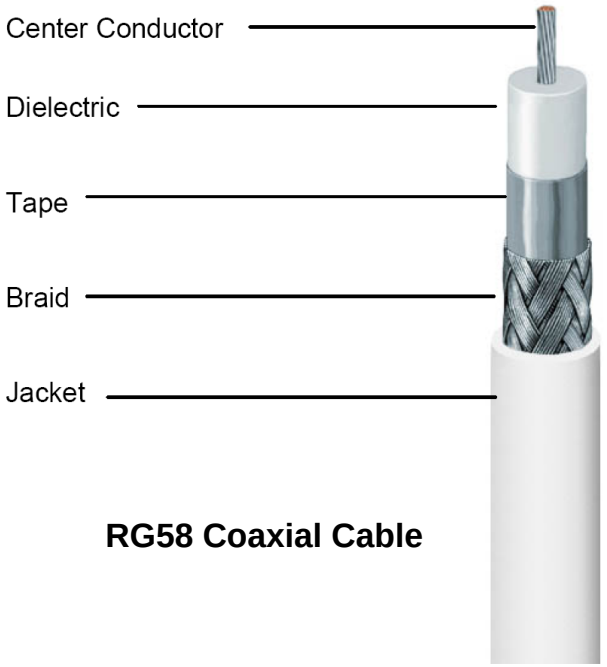
$$\text{permittivity}: \ \varepsilon = \varepsilon' - j\varepsilon''$$

$$\text{permeability}: \mu = \mu_0\mu_r$$

$$\text{Surface resistance}: R_s = 1/\sigma\delta_s$$

Coaxial Cable Cross Section





RG58 Coaxial Cable

Coaxial Cable

- **Shunt conductance per unit length**

$$G = \frac{2\pi\omega\varepsilon''}{\ln(D/d)}$$

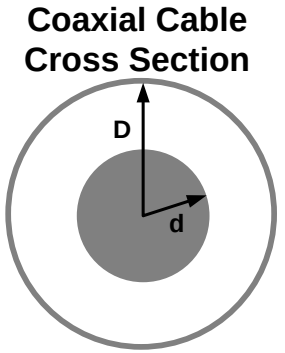
- **Shunt capacitance per unit length**

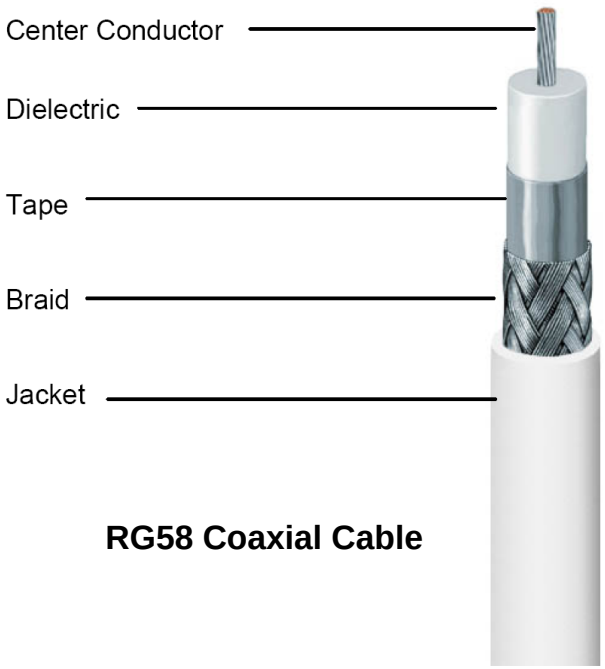
$$C = \frac{2\pi\varepsilon'}{\ln(D/d)} = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln(D/d)}$$

$$\text{permittivity}: \ \varepsilon = \varepsilon' - j\varepsilon''$$

$$\text{permeability}: \mu = \mu_0\mu_r$$

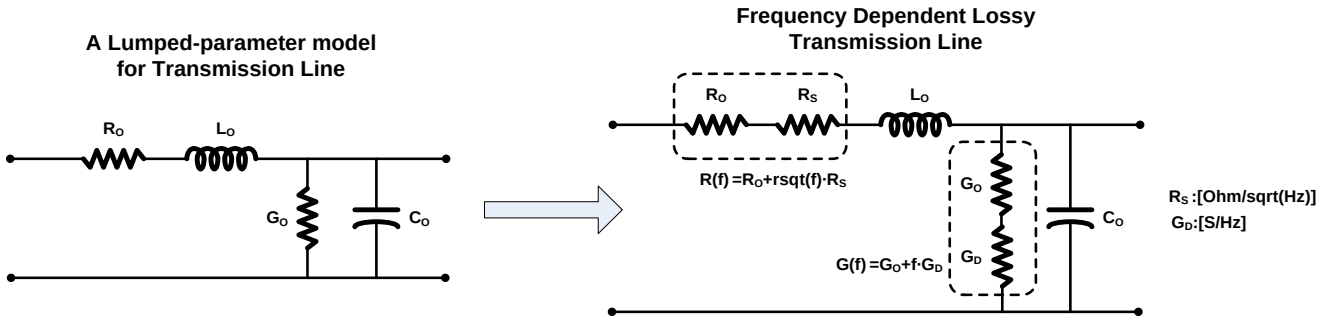
$$\text{Surface resistance}: R_s = 1/\sigma\delta_s$$



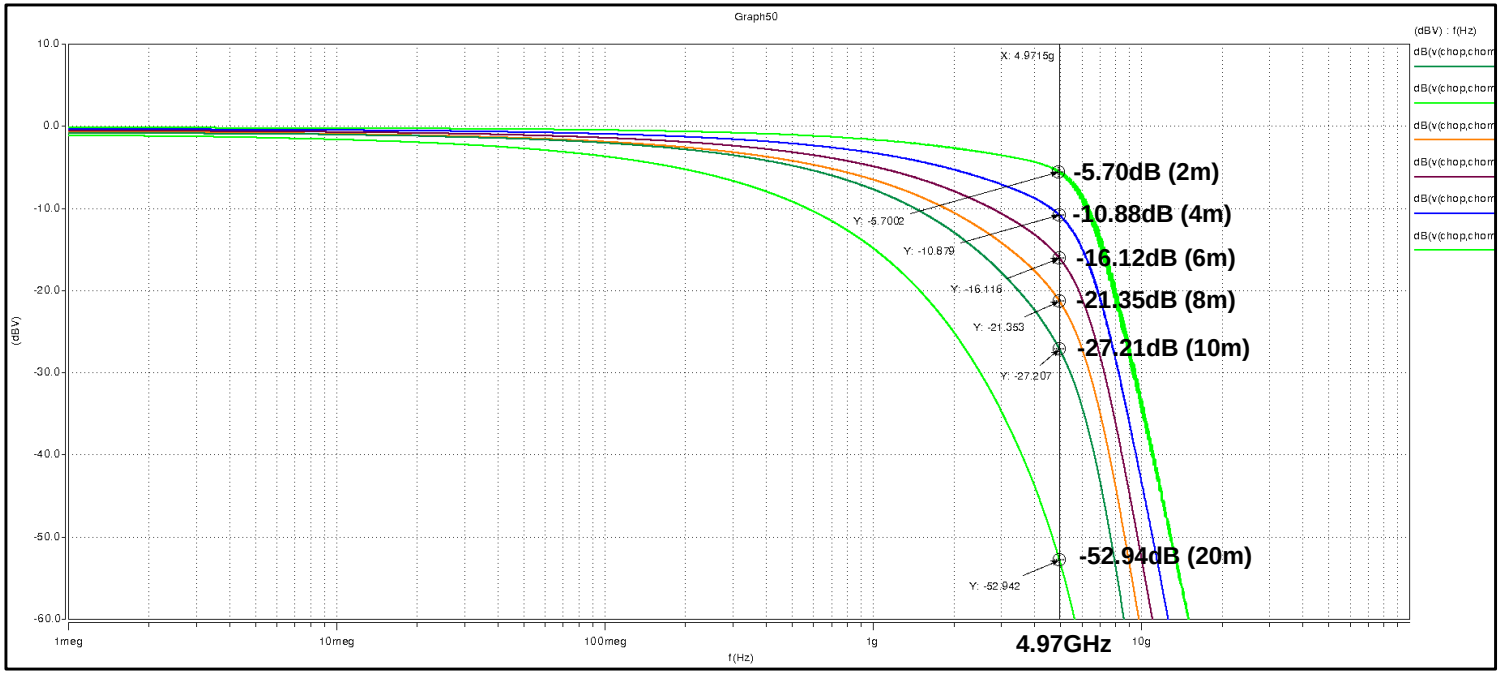


RG58 Coaxial Cable

Channel Loss



RG58 Coaxial Cable Frequency Response



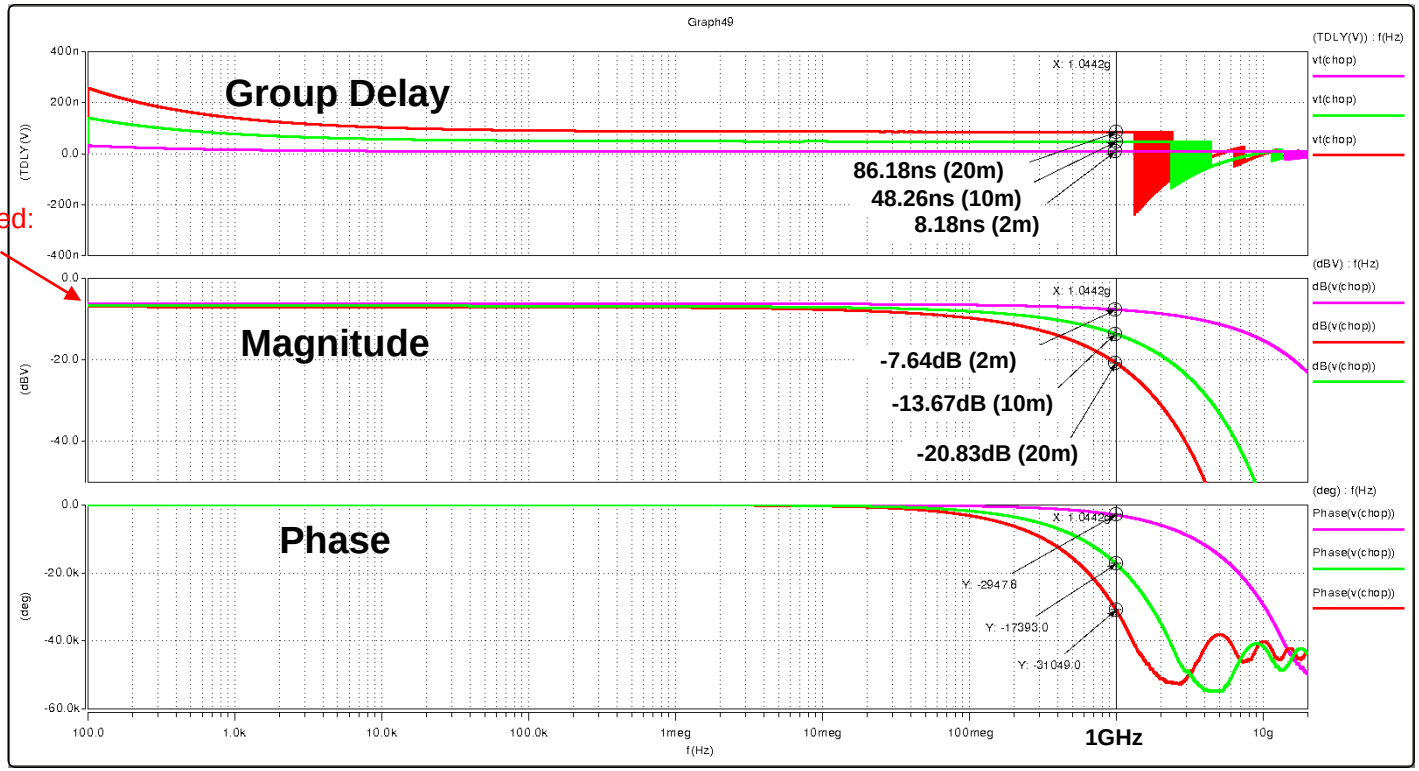
Channel Group Delay

- **Group Delay: A measure of the transit time of a signal through a device under test, versus frequency.**

$$\text{Group Delay } \tau_g(\omega) = -\frac{d\phi}{d\omega} = -\frac{1}{360} \cdot \frac{(phase_2 - phase_1)}{(f_1 - f_2)}$$

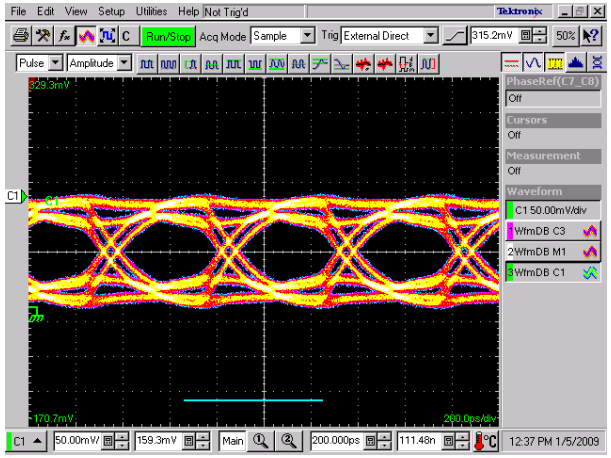
RG58 Coaxial Cable Frequency Response

Source Terminated:
-6dB loss at DC

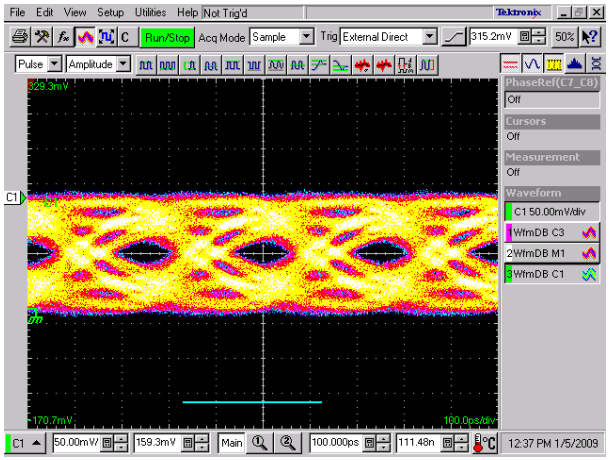


Channel Loss vs Frequency

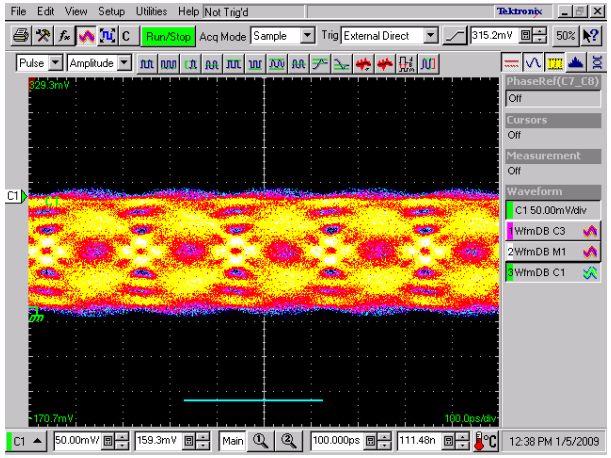
12 inch PCB trace @ 2Gbps



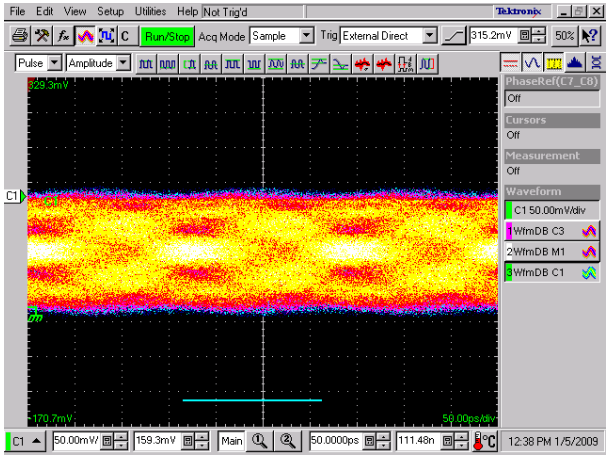
12 inch PCB trace @ 4Gbps



12 inch PCB trace @ 5Gbps

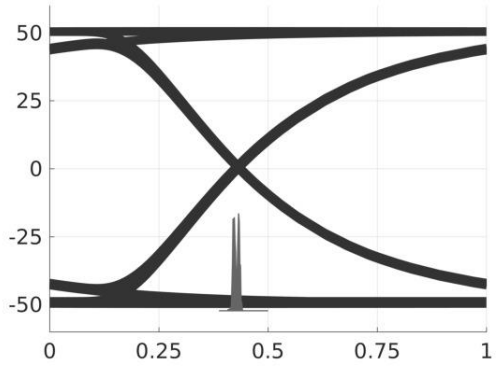


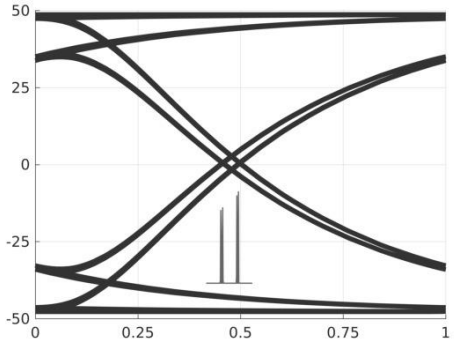
12 inch PCB trace @ 6Gbps

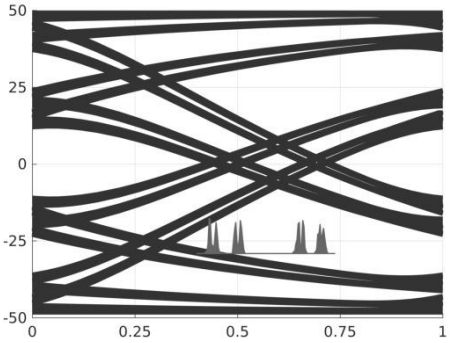


Data-Dependent Jitter: ISI

- **Previous symbol does not settle completely**



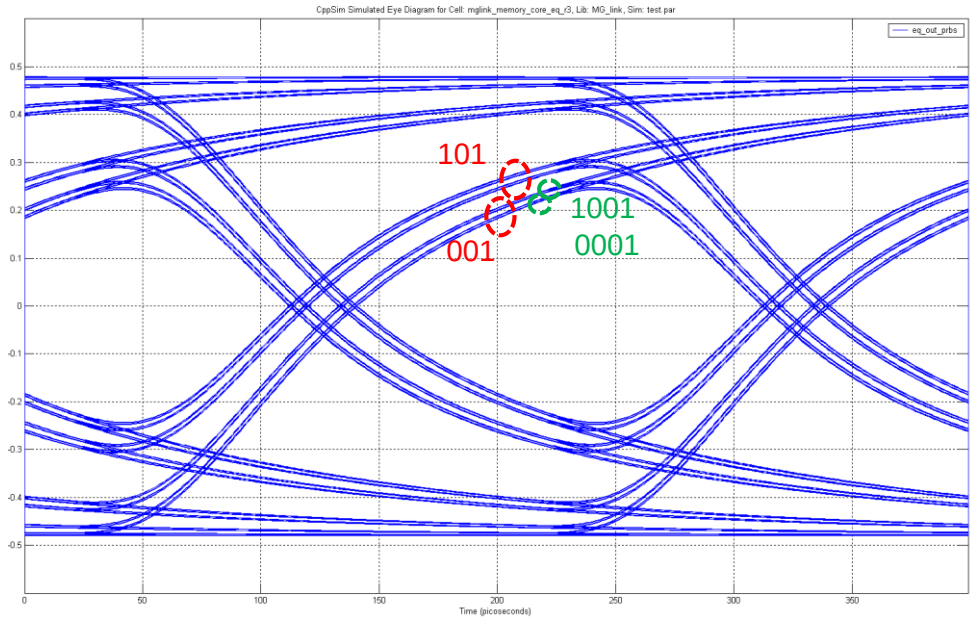


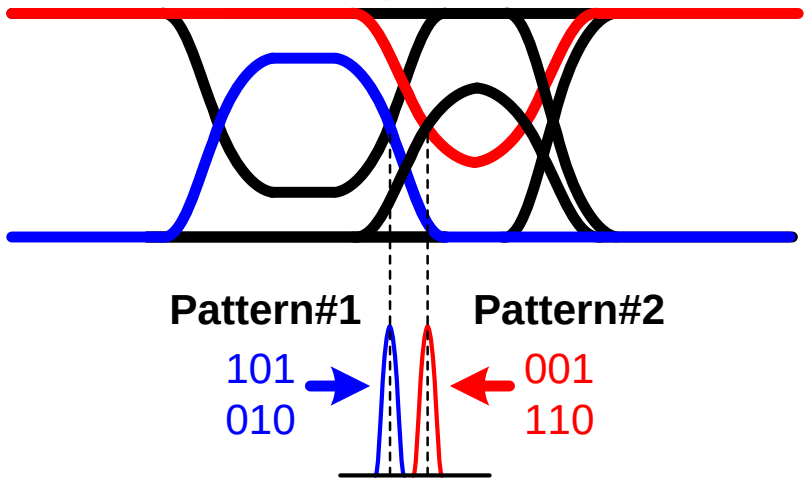


Almost no ISI, **ISI spanning over 1 bit,** **ISI spanning over 2 bits**

Pattern Dependent Histogram

- **Data dependent jitter**
  - **When a transition follows consecutive bits (e.g. 110)**
    → edge-shift backward
  - **When a transition follows alternating bits (e.g. 010)**
    → edge-shift forward
- **Random Jitter**
  - **Convolution with data dependent jitter**
- **As the channel loss increases, the eye histogram splits**





References

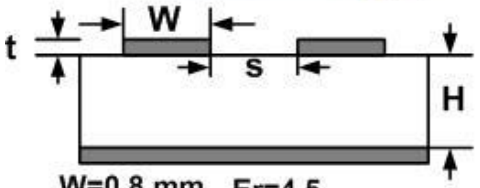
- Bidyut K. Sen and Richard L. Wheeler. “Skin Effects Models for Transmission Line Structures using Generic SPICE Circuit Simulators”, IEEE 7th Topical Meeting on Electrical Performance of Electronic Packaging, 1998

- S Kim and D.P. Neikirk, “Compact Equivalent Circuit Model for the Skin Effect”, IEEE MTT-S International Microwave Symposium Digest, 1996

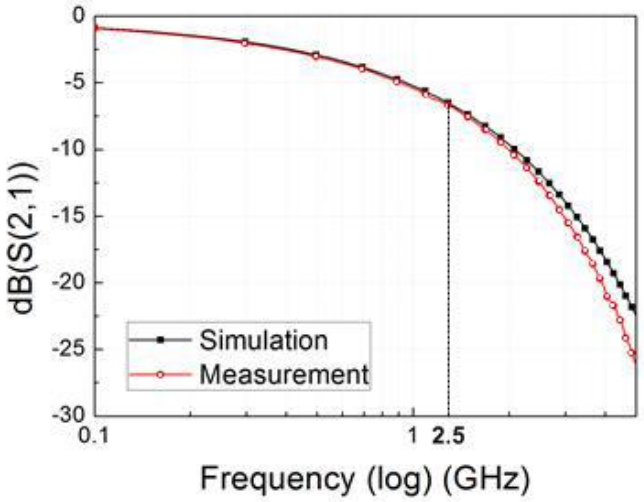
- M. Tsuk, “The Internal Impedance of Conductors with Arbitrary Cross Sections”, Progress in Electromagnetics Research Symposium, July 2000

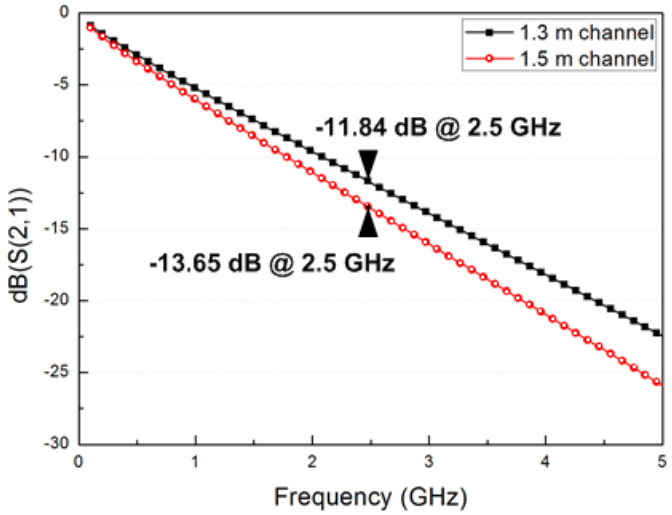
- David M. Pozar, “Microwave Engineering” John Wiley & Sons, Inc. 2005

Backplane Example



W=0.8 mm Er=4.5
H=0.4 mm Con. Of Cu=5.8e+07
T=35 um Loss Tangent=0.02
S=2.4 mm





Topics in IC Design

7.2 Equalizers

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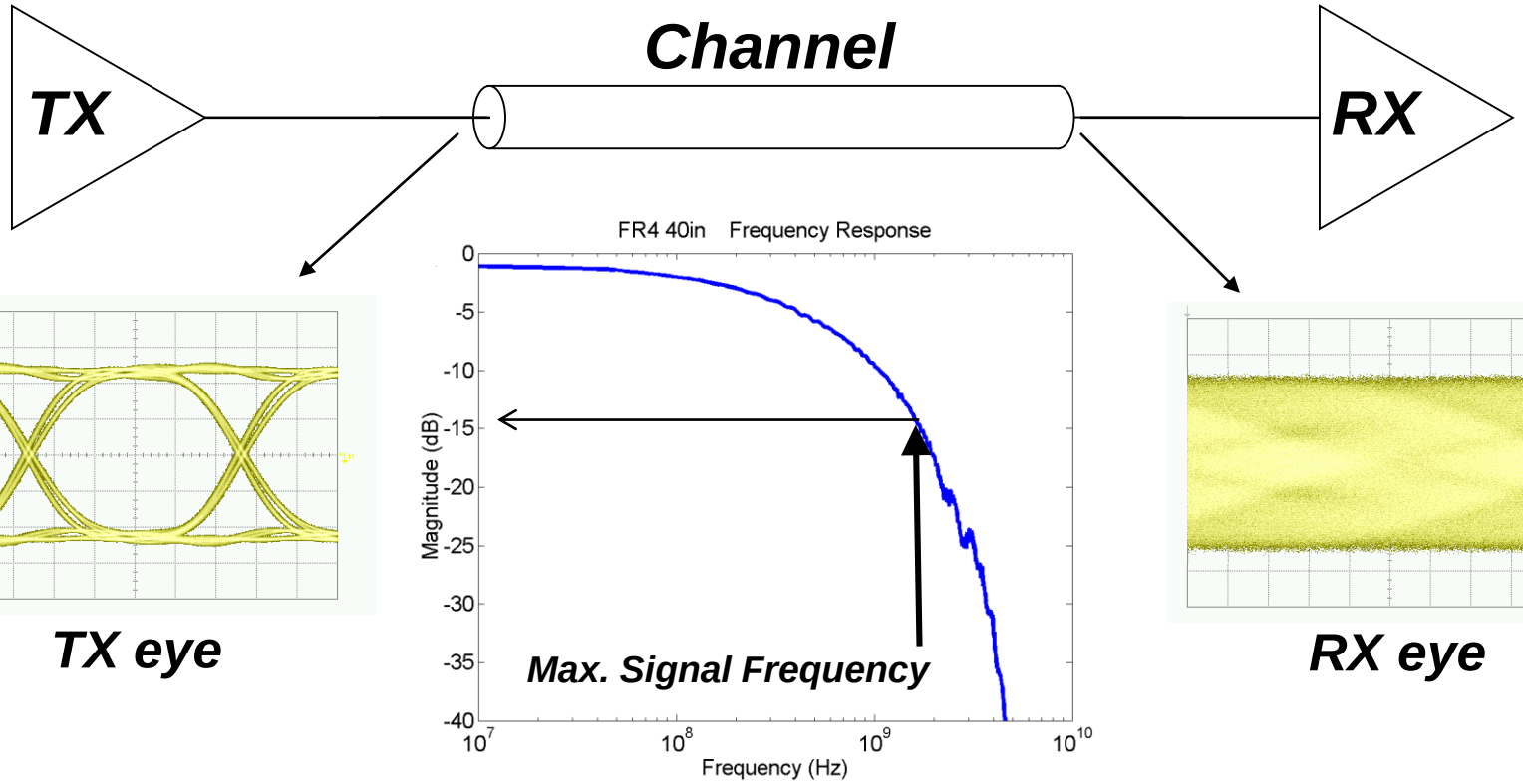
Outline

- **Equalizer Overview**
- **TX Equalizer**
  - **FIR (Finite Impulse Response) Filter**
  - **Pre-de-emphasis**
- **Continuous-Time RX Equalizer**
  - **CT Linear Equalizer (CTLE)**
  - **Bandwidth extension techniques**
- **Discrete-Time Equalizer**
  - **Feed-Forward Equalizer (FFE)**
  - **Decision Feedback Equalizer (DFE)**
- **Equalizer Adaptation**

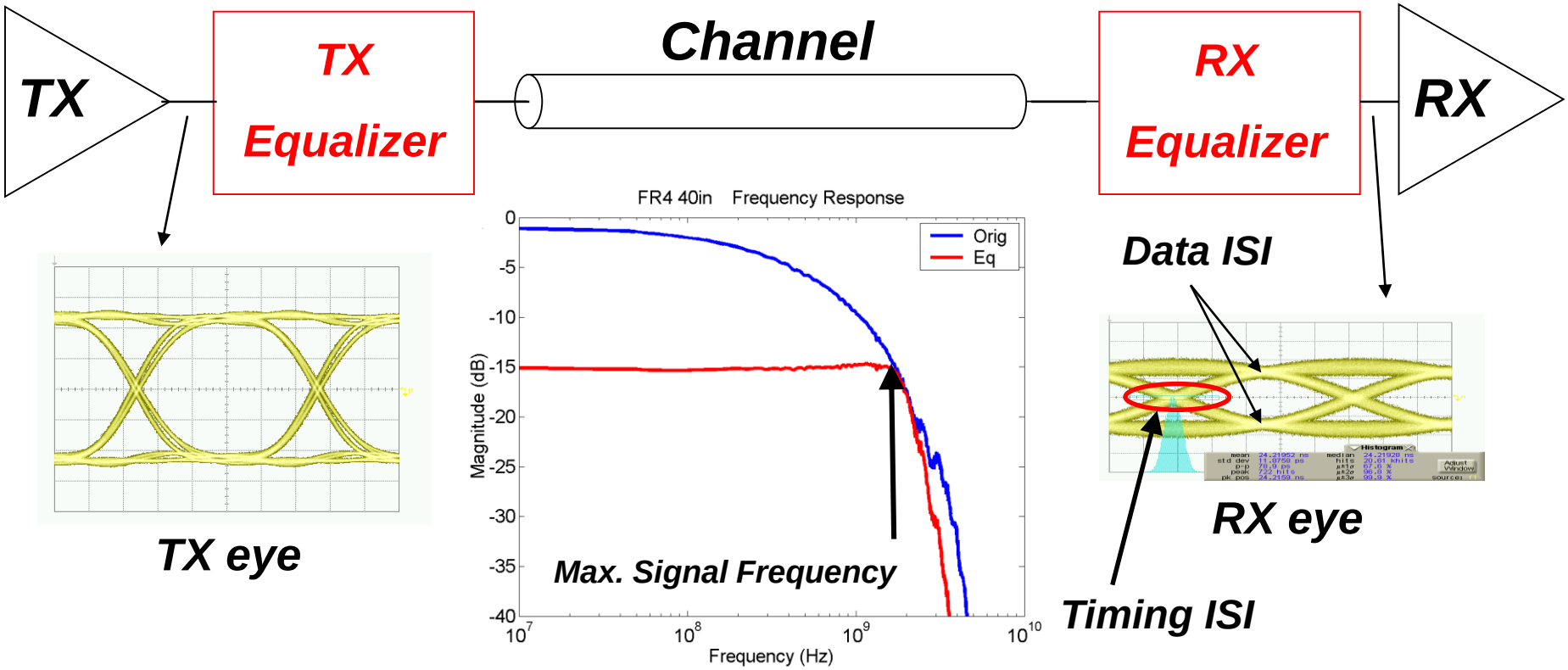
Channel Bandwidth and ISI



- An I/O link = transmitter (TX) + channel + receiver (RX)
- TX,RX contributes voltage noise and timing jitter
- Limited channel bandwidth introduces inter-symbol interference (ISI)
- Bit error rate (BER) depends on voltage noise, timing jitter and ISI

[Broadcom Corp., Wong]

Channel Equalization



- **ITRS roadmap predicts that I/O clock rate increases 20% per year**
- **Channel bandwidth is not scaling at the same rate**
- **One of the bottlenecks of increasing I/O speed is limited channel band width.**
- **Channel equalization compensates ISI**

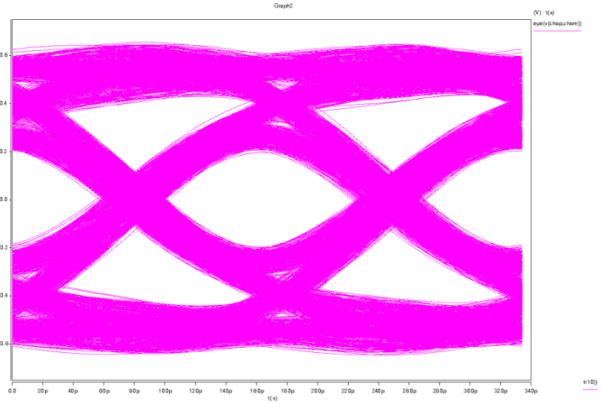
[Broadcom Corp., Wong]

Definitions of Equalization

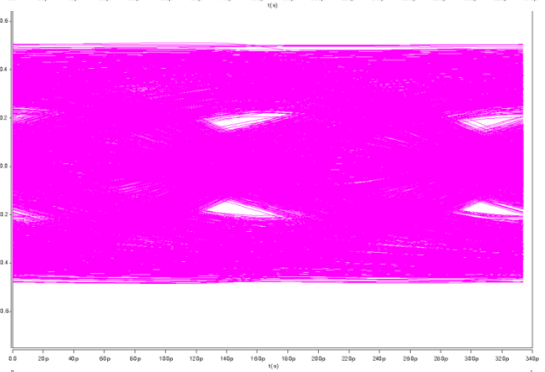
- Equalization is the process of using passive or active electronic elements or digital algorithms for the purpose of **flattening the frequency response** characteristics of a system.

Channel Loss and Equalization

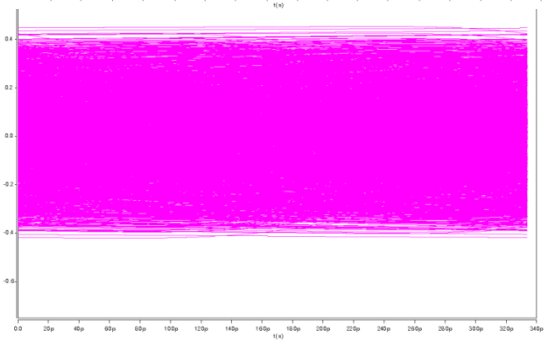
6Gbps@ RG58 - 2m

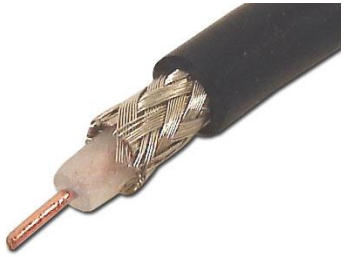


6Gbps@ RG58 - 10m

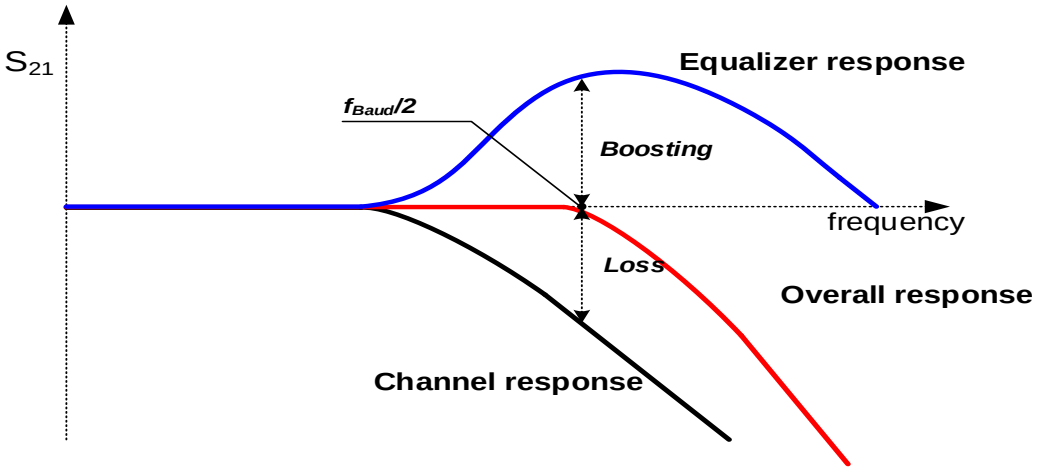


6Gbps@ RG58 - 20m



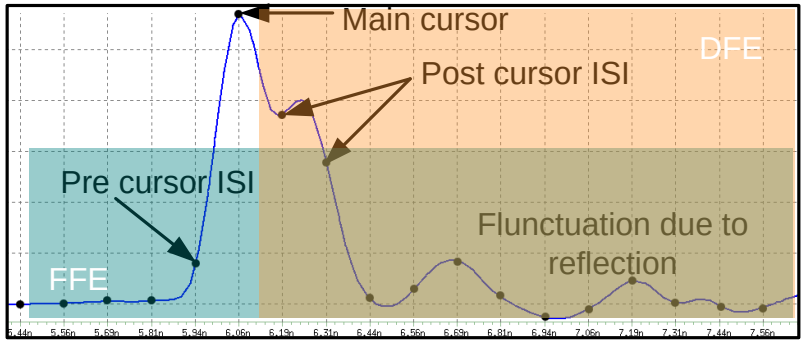


Equalization in frequency domain



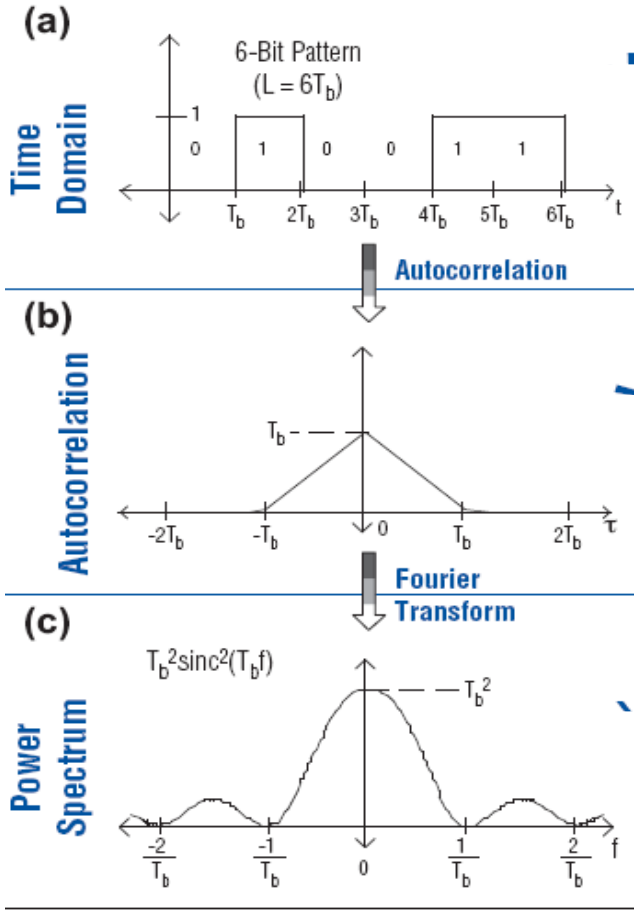
Equalizer Classification

- **On-chip vs Off-chip**
  - **On-chip: Pre-emphasis, CT-Linear, FFE, DFE**
  - **Off-chip: Cable equalization**
- **TX vs RX**
  - **TX: Pre-de-emphasis**
  - **Rx: CT-Linear equalizer, DFE, FIR filter**
- **Continuous Time vs Digitally Sampled**
  - **Analog: Linear equalizer, Continuous-time equalizer**
  - **Digital: DFE, FIR filter**
- **Decision Feedback vs Feed-forward**

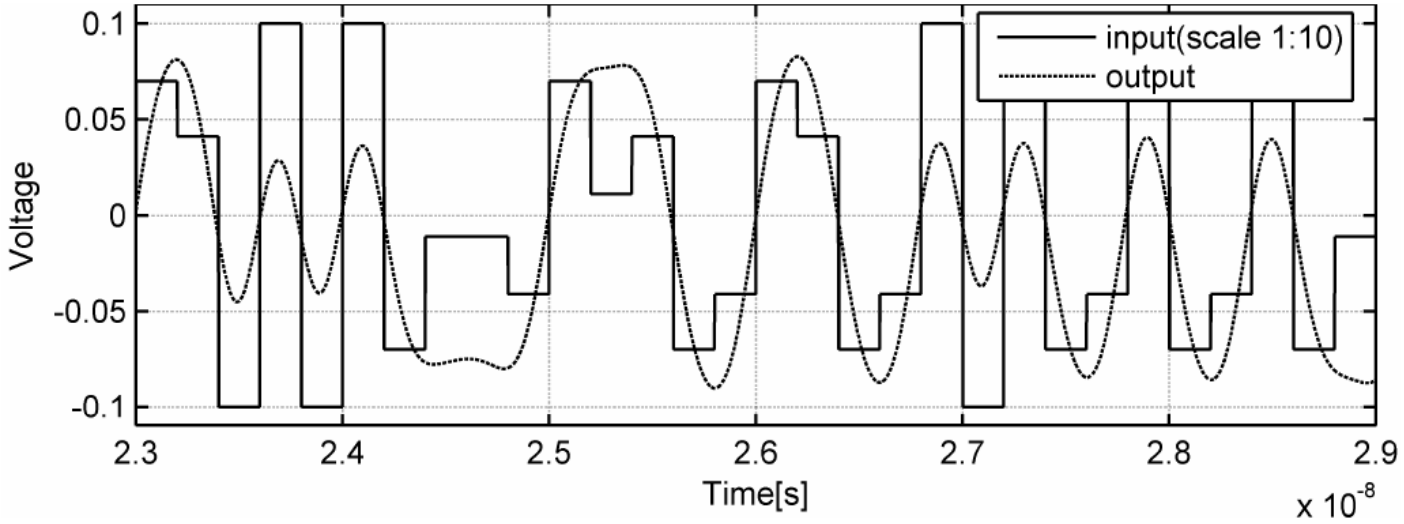


Power Spectral Density of NRZ

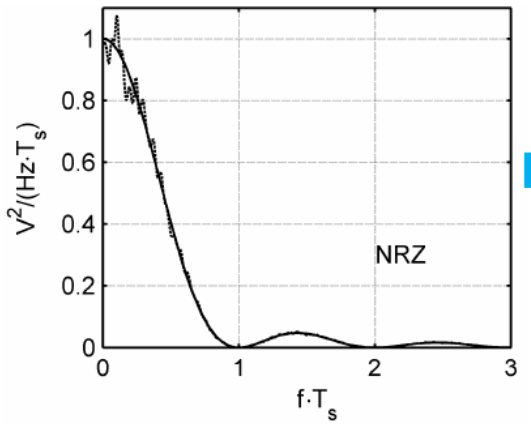
- $\text{sinc}^2(f)$



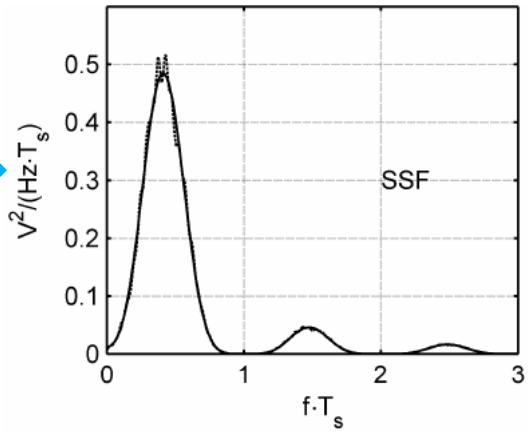
PSD after FIR filter



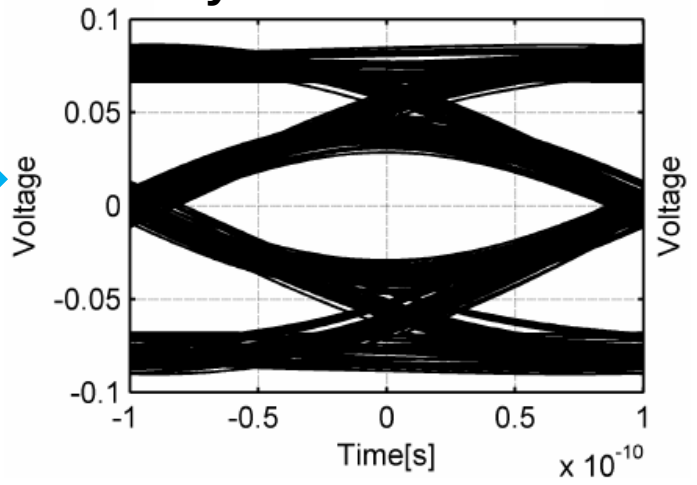
PSD of NRZ



PSD of FIR filter

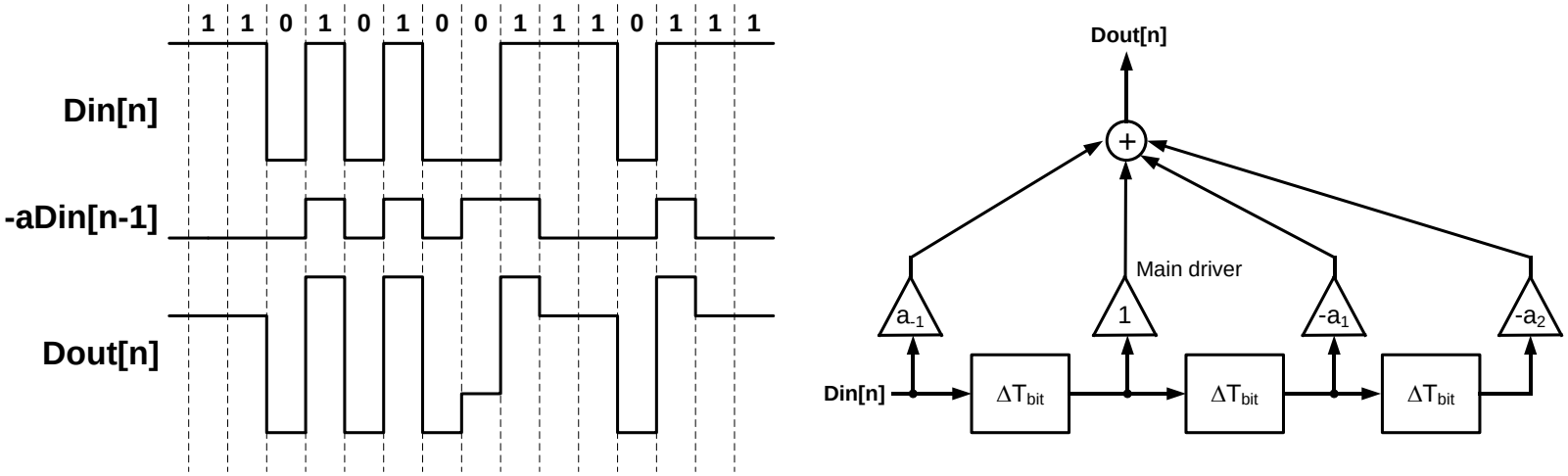


Eye after FIR filter



Pre-emphasis

- **Attenuates the low-frequency contents.**
- **The output swing of the Tx driver is limited.**
  - **Be careful about the amplitude of output signal.**
  - **Sum of all abs values of coeffs must be smaller than the allowed peak.**

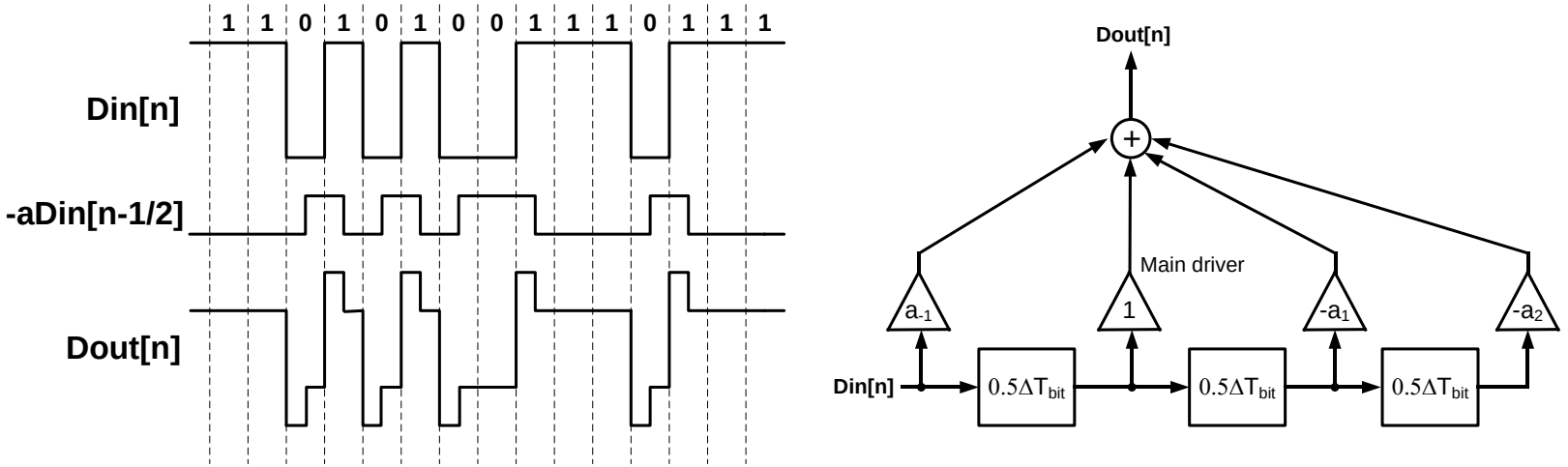


Symbol Rate pre-emphasis

$$Dout[n] = a_{-1}Din[n+1]+Din[n]-a_1Din[n-1] -a_2Din[n-2]$$

Pre-emphasis

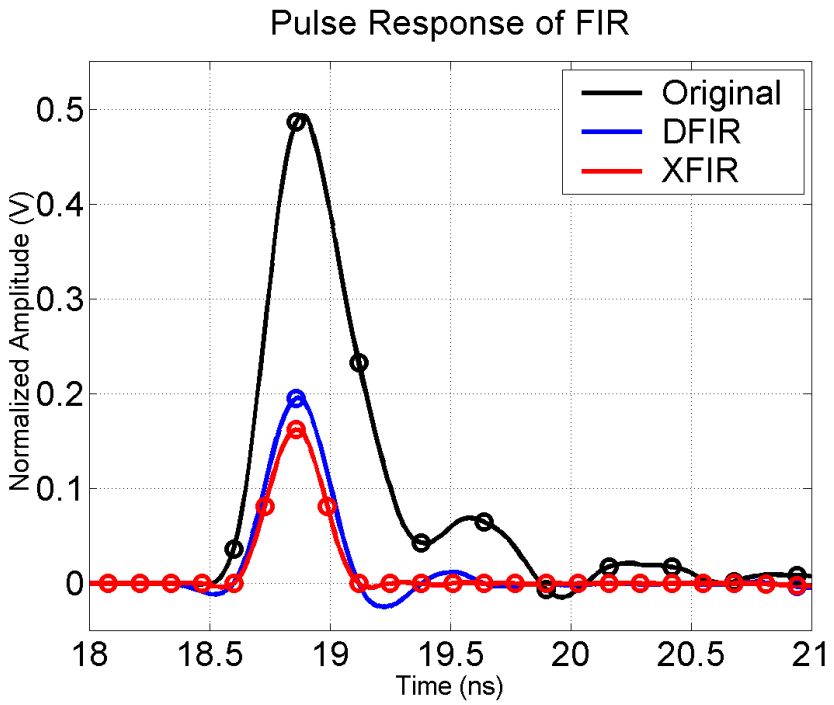
- **Half-symbol rate by using latch with a half-cycle delay**



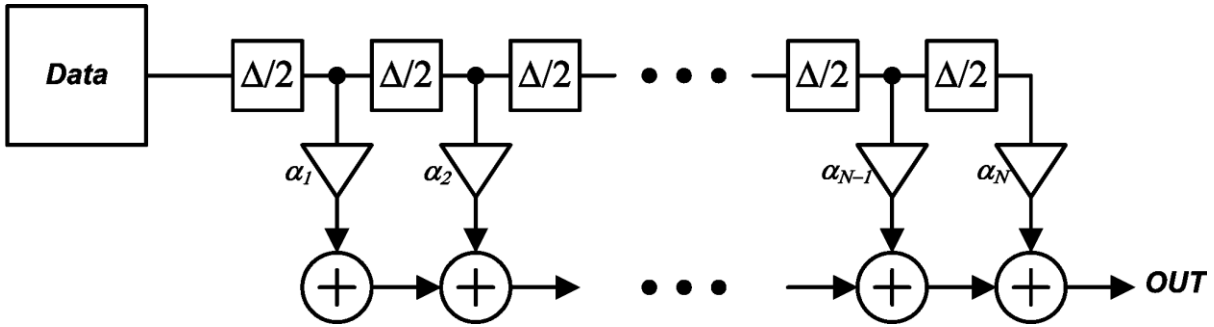
Half-symbol Rate pre-emphasis

$$Dout[n] = a_{-1}Din[n+1/2]+Din[n]-a_1Din[n-1/2] -a_2Din[n-1]$$

TX Equalization Example(1)

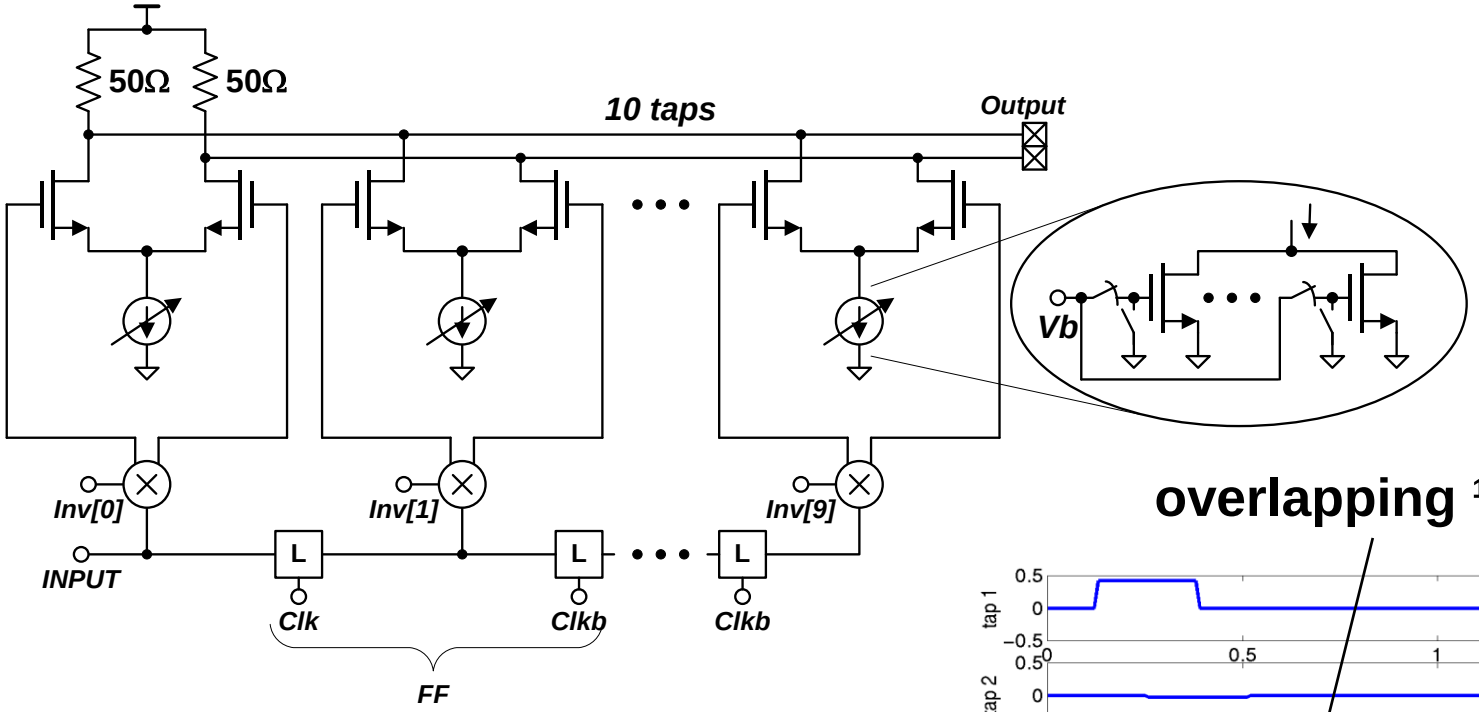


- Delay signal by multiple of ½ cycle time
- FIR with edge equalization (XFIR)
- Trade-off between voltage and timing margin

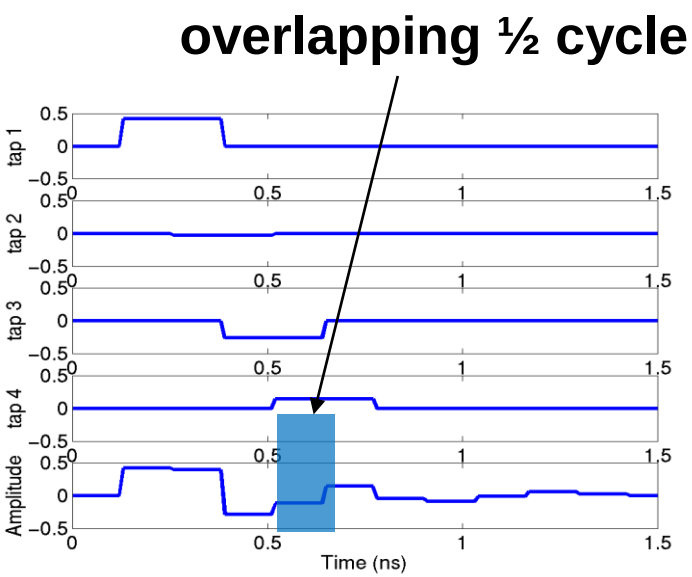


[JSSC'08, Wong]

Tx Equalization Example(1)

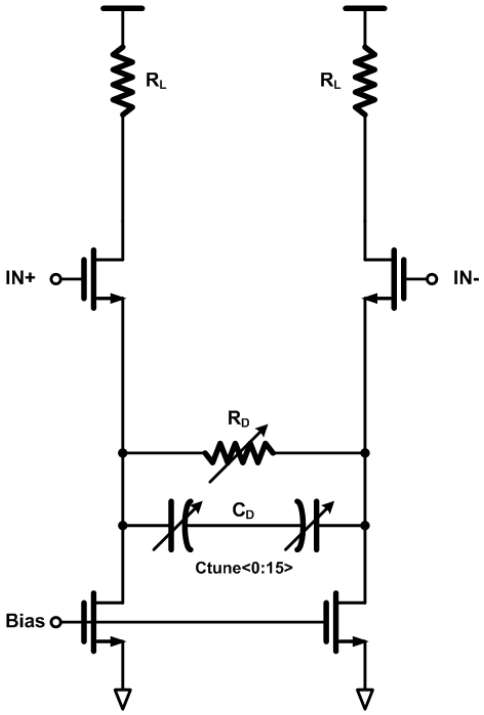


- **Use latch as ½ cycle delay elements**



[JSSC'08, Wong]

Linear Equalizer



$$A_v = \frac{-g_m R_L}{1+g_m Z_S}$$

$$A_v = \frac{-\frac{g_m R_L}{1+0.5 R_D g_m}(1+sR_D C_D)}{1+\frac{sR_D C_D}{1+0.5 g_m R_D}}$$

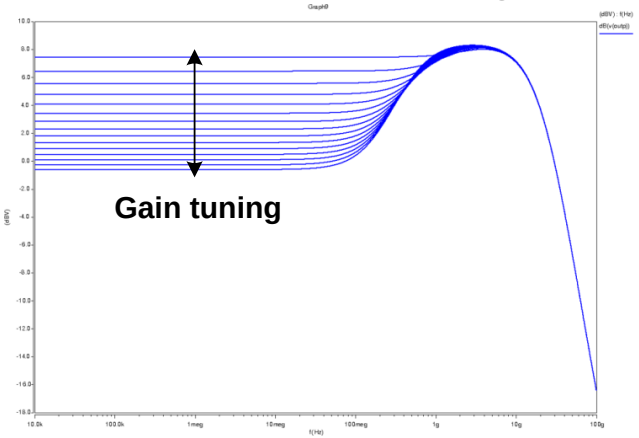
$$\omega_Z \approx \frac{1}{R_D C_D}$$

$$\omega_P \approx \frac{1+0.5 g_m R_D}{R_D C_D}$$

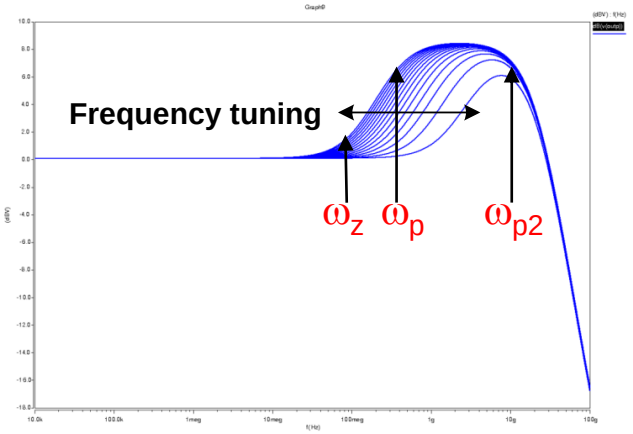
$$A_{V,Low} \approx \frac{g_m R_L}{1+0.5 R_D g_m}$$

- **Addition of zero to boost high frequency**
- **Capacitive and resistive degeneration**

Resistance Tuning

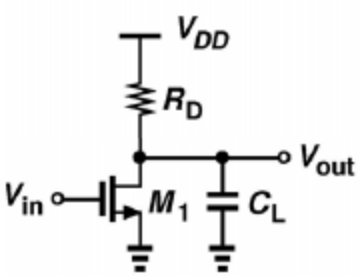


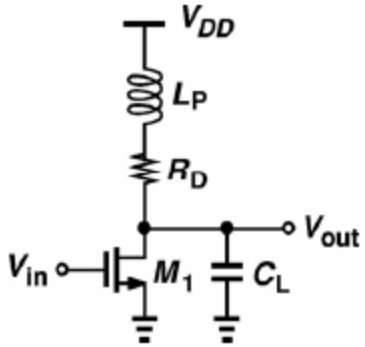
Capacitance Tuning

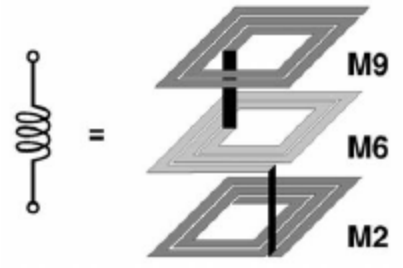


High Performance Techniques

- **Inductive Peaking**







$$f_{-3dB} = \frac{1}{2\pi R_D C_L}$$

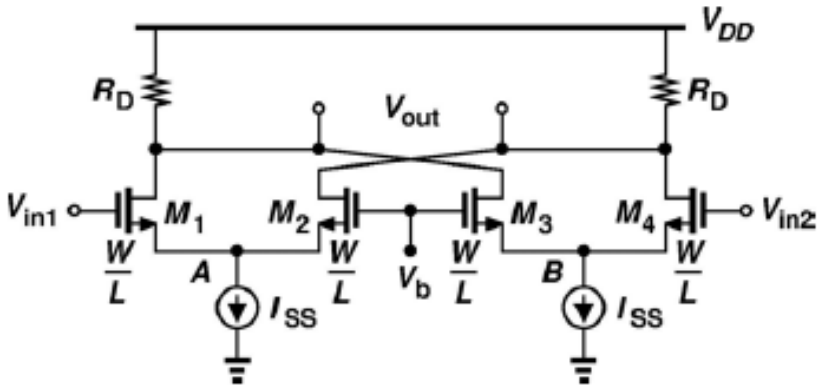
$$\frac{V_{out}}{V_{in}} = -g_m R_D \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} \frac{\omega_n}{2\zeta}$$

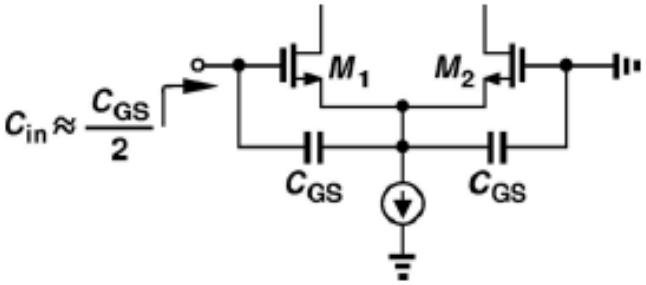
$$f_{-3dB} = \frac{1.79}{2\pi R_D C_L} \quad \text{for} \quad \zeta = 1/\sqrt{2}$$

- **Bandwidth extension by 79%**
- **No extra power consumption**
- **Area penalty**

High Performance Techniques

- f_T **Doubler**



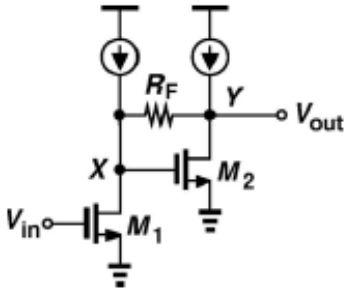


$$V_{out} = g_m(V_{in1} - V_{in2})R_D$$

- **Bandwidth Extension**
  - **Decrease the effective input capacitance**
  - **Parasitics on tail current sources degrade the performance**

High Performance Techniques

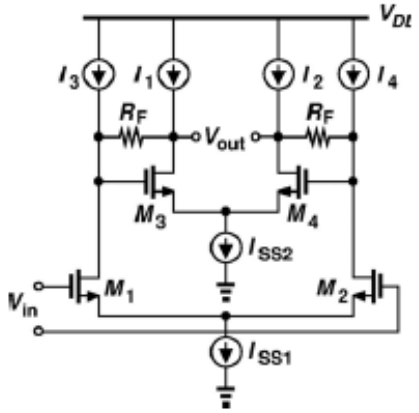
- **Cherry Hooper Amplifier**

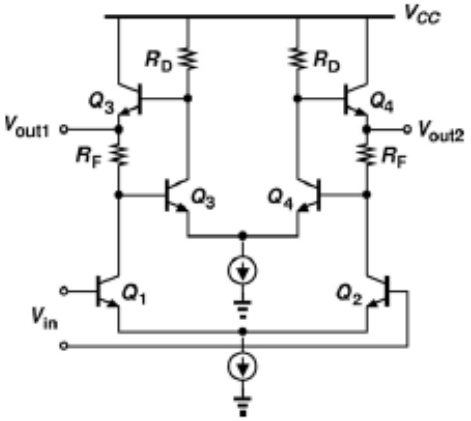


$$\frac{V_{out}}{V_{in}} = g_{m1}R_F - \frac{g_{m1}}{g_{m2}}$$

$$\omega_{p,X} \approx \frac{g_{m2}}{C_X}$$

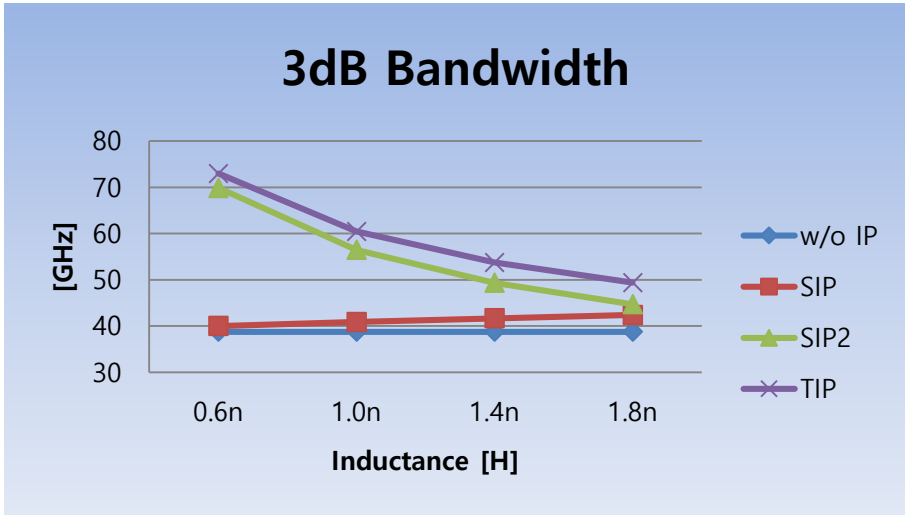
$$\omega_{p,Y} \approx \frac{g_{m2}}{C_Y}$$

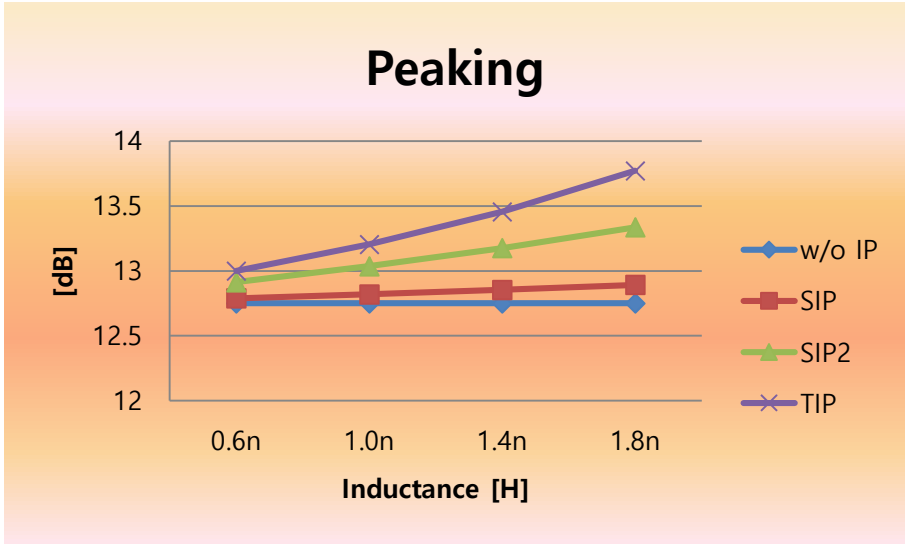


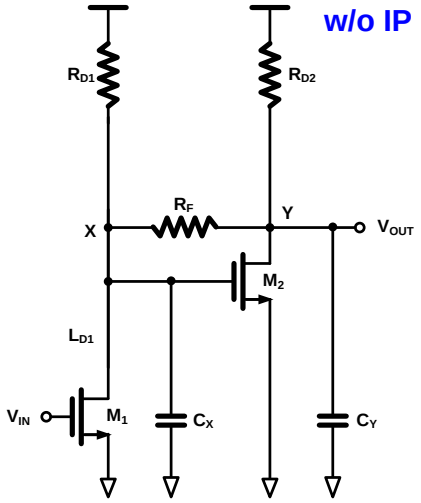


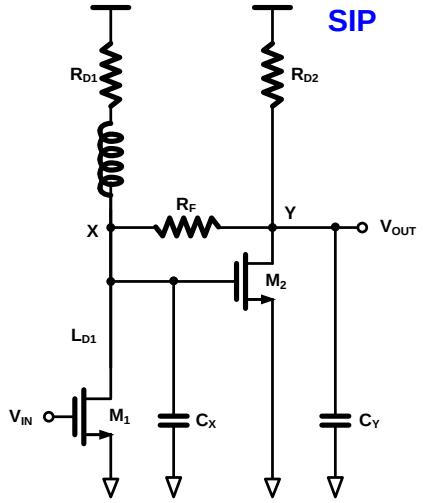
- **Bandwidth Extended**
- **Reduced voltage headroom**

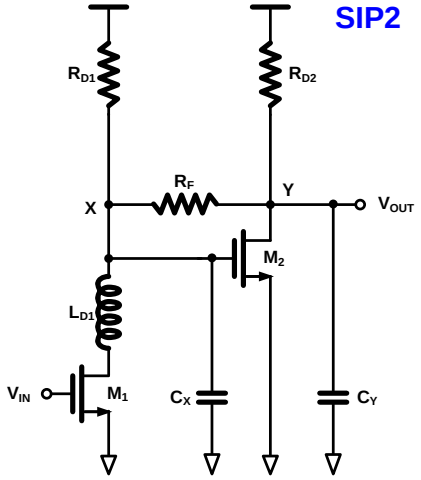
High Performance Techniques

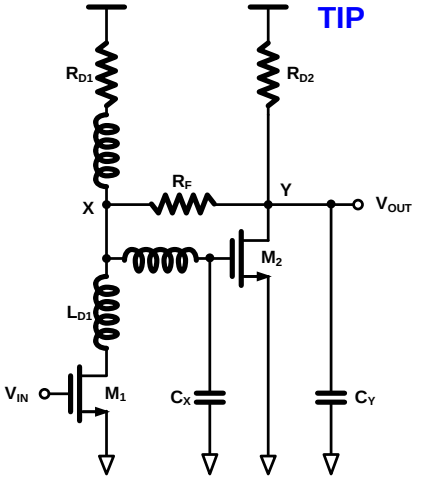




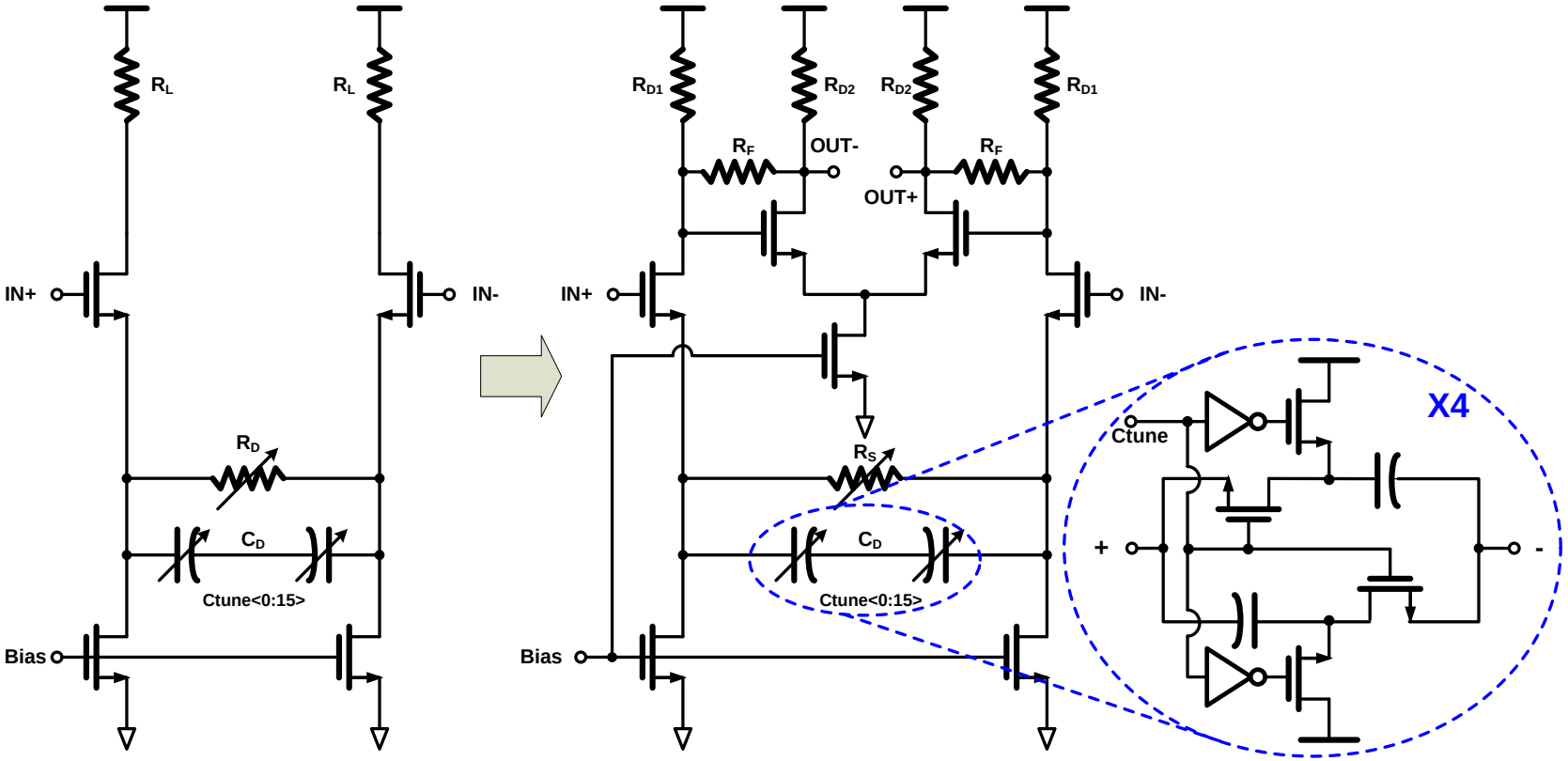






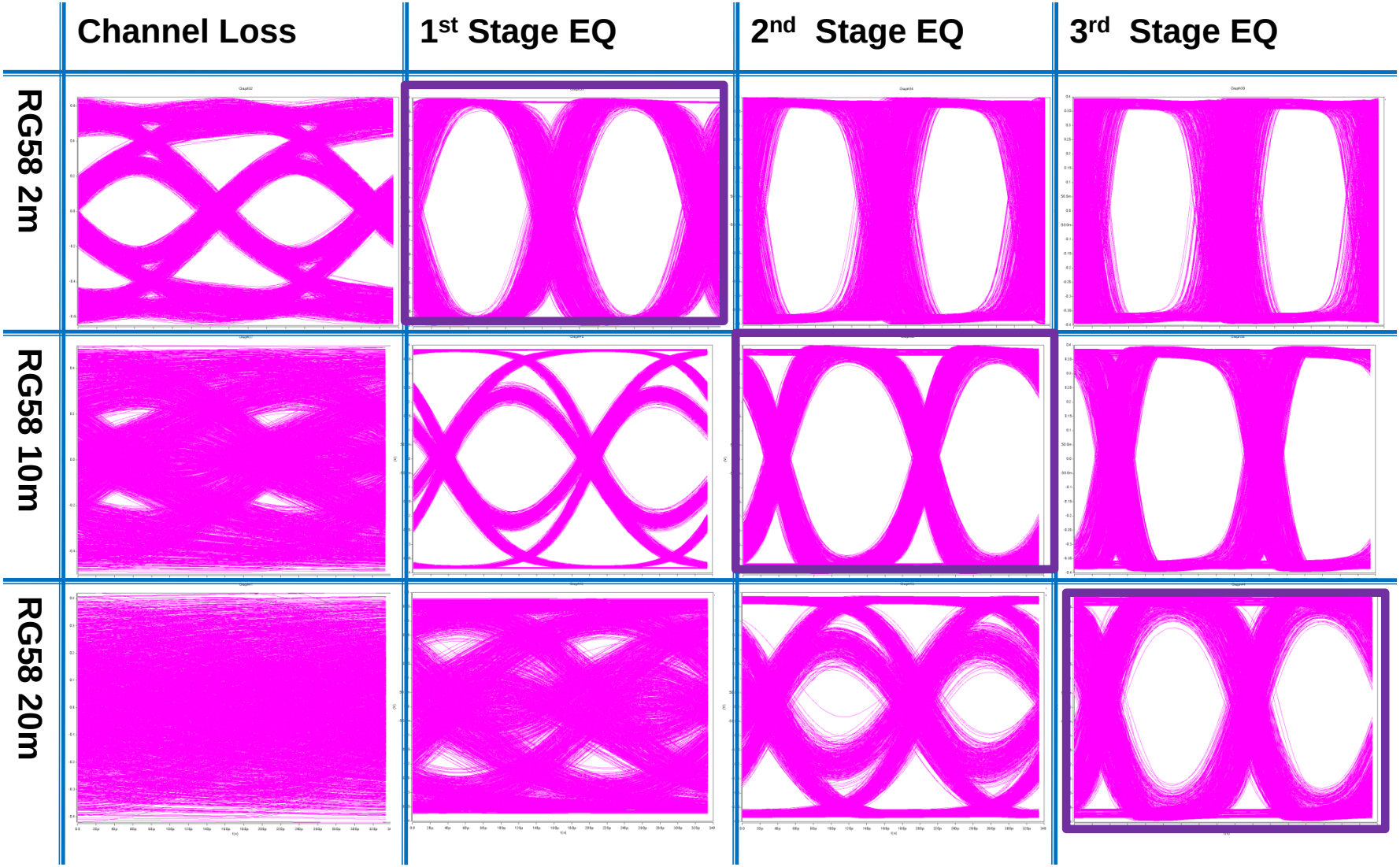


Linear Equalizer Examples(1)

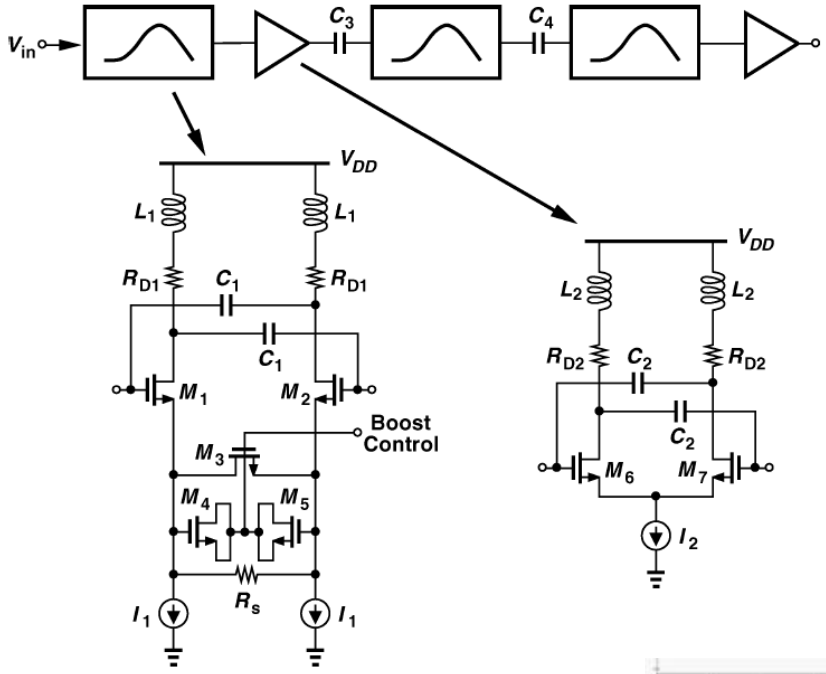


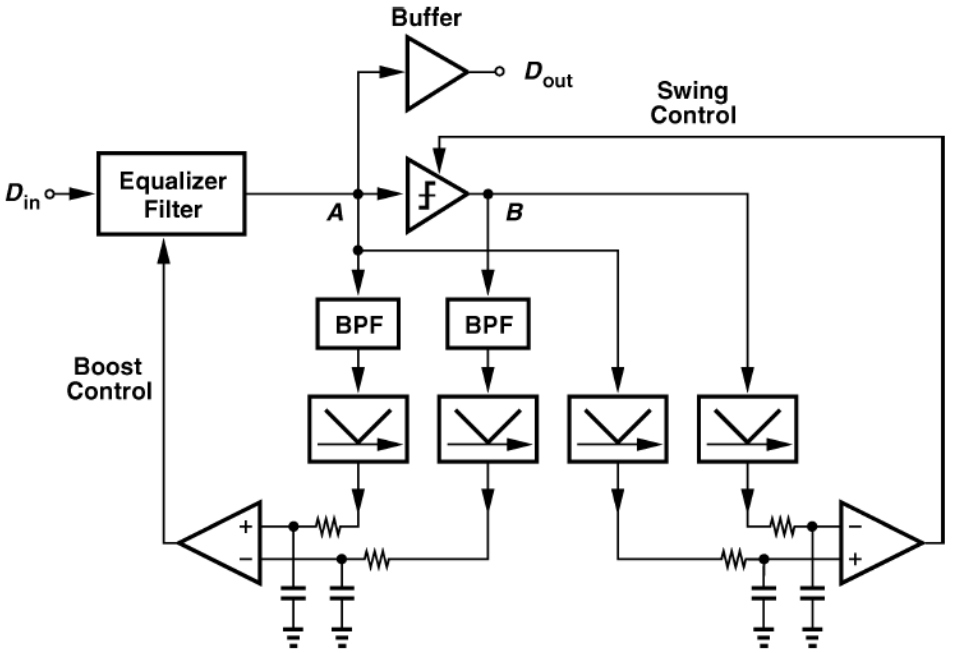
- **30% Bandwidth increase**

Linear Equalizer Examples(1)

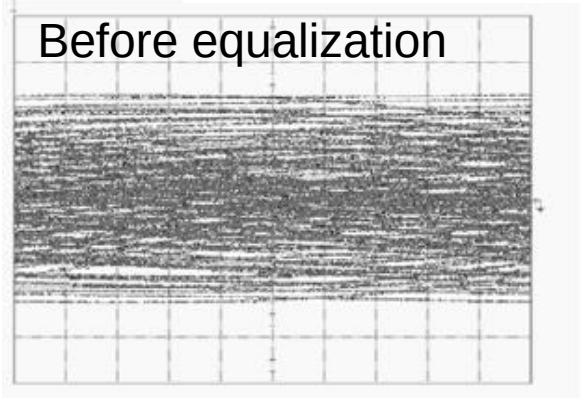


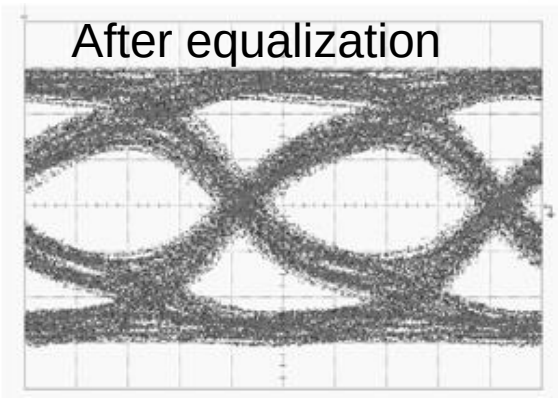
Linear Equalizer Examples(2)





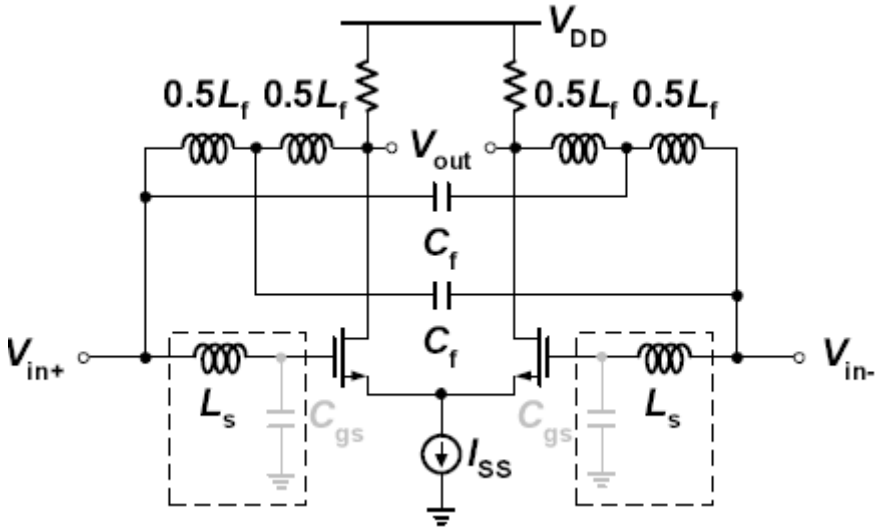
10Gbps Eye diagram

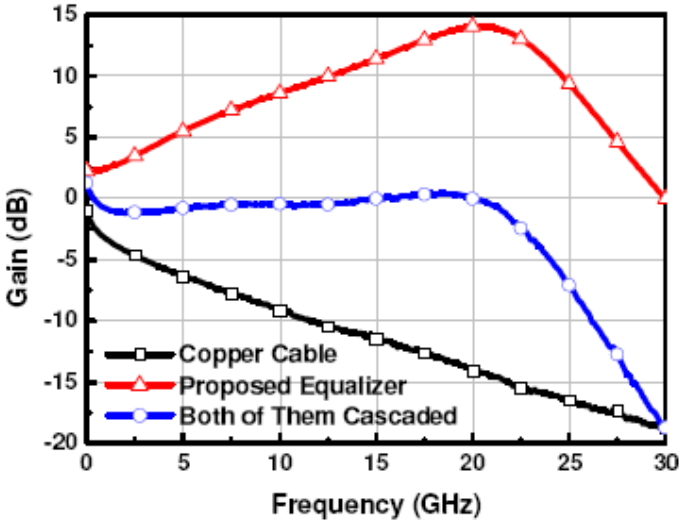


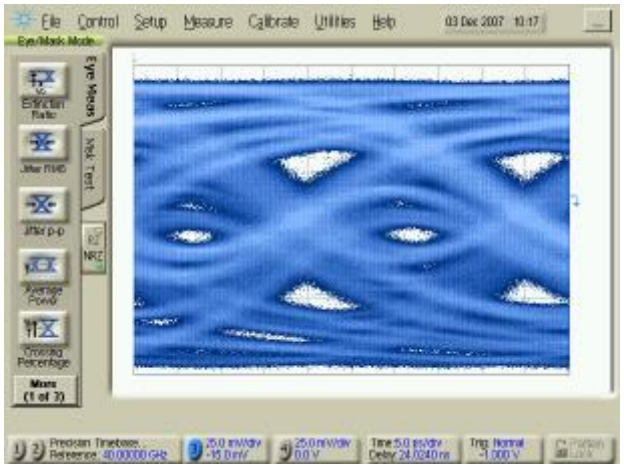


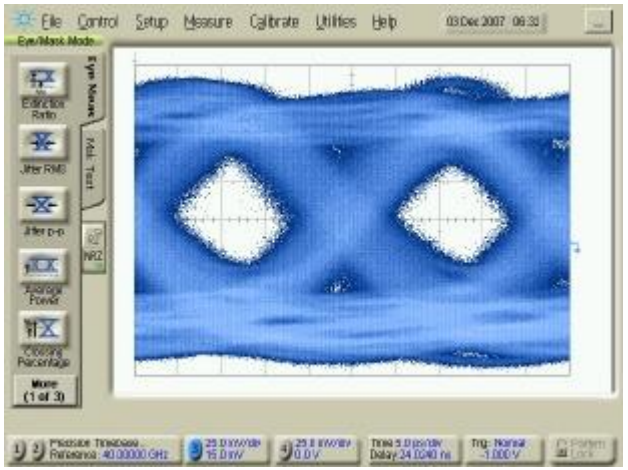
[JSSC'07, Razavi]

Linear Equalizer Examples(3)







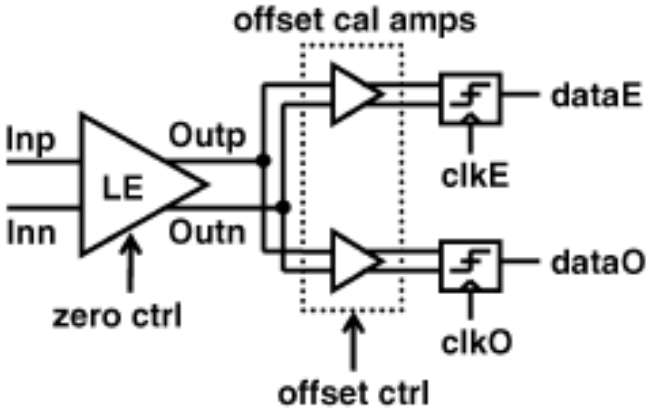


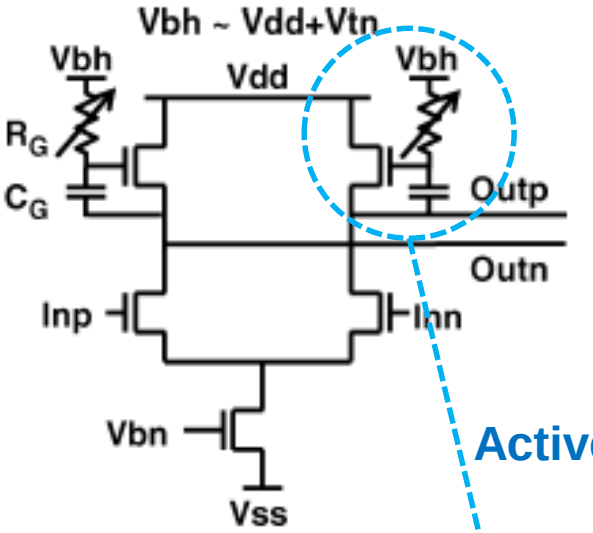
40Gbps Eye(before LE)

40Gbps Eye(after LE)

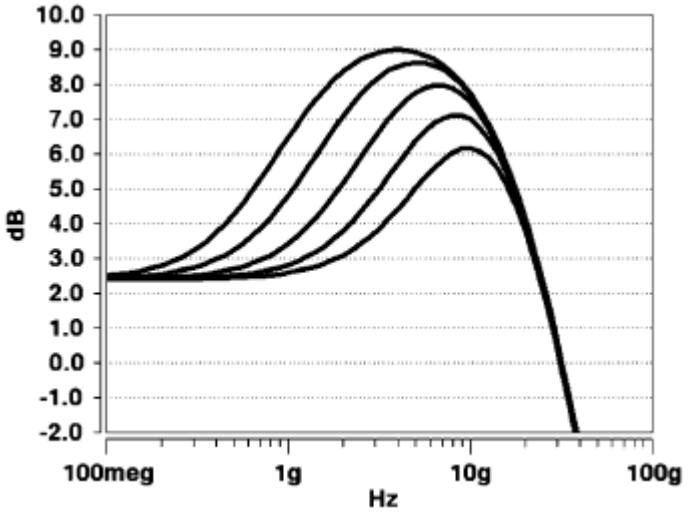
[SOVC'08, Jian-Hao Lu]

Linear Equalizer Examples(4)





Active Inductor

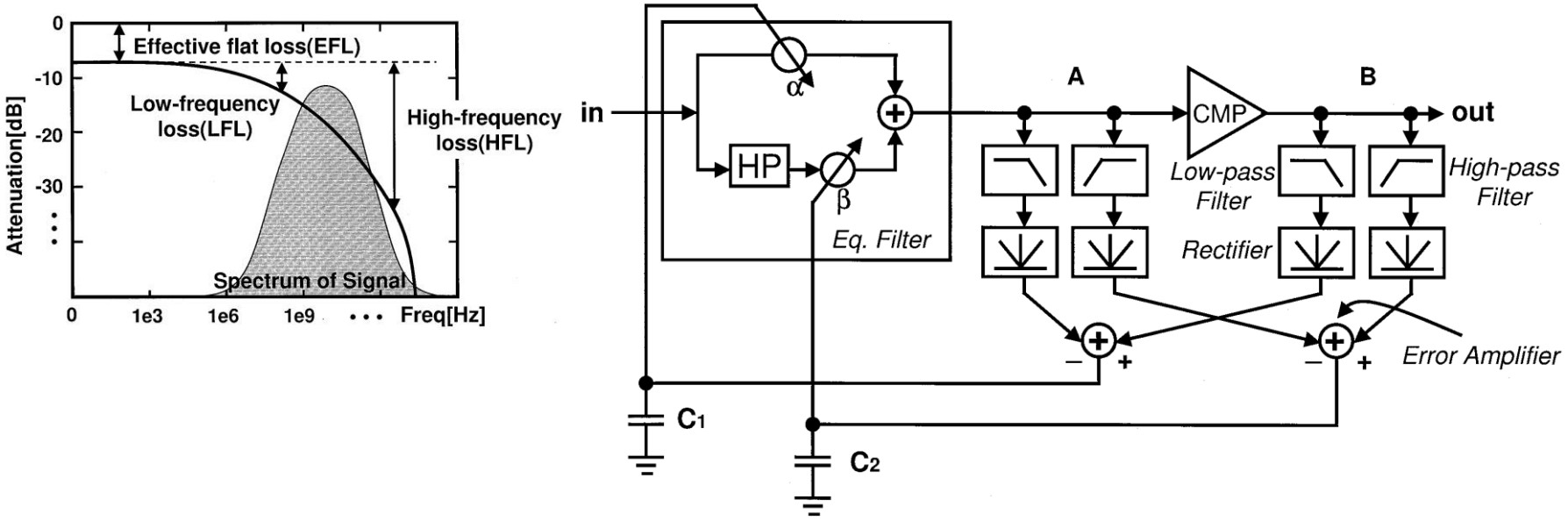


AC response in nominal corner

$$A_V(s) = \frac{g_m}{g_{m,L}} \cdot \frac{sR_GC_G + 1}{s^2 \frac{R_GC_GC_L}{g_{m,L}} + s\frac{(C_L + C_G)}{g_{m,L}} + 1}$$

[JSSC'09, Haechang Lee]

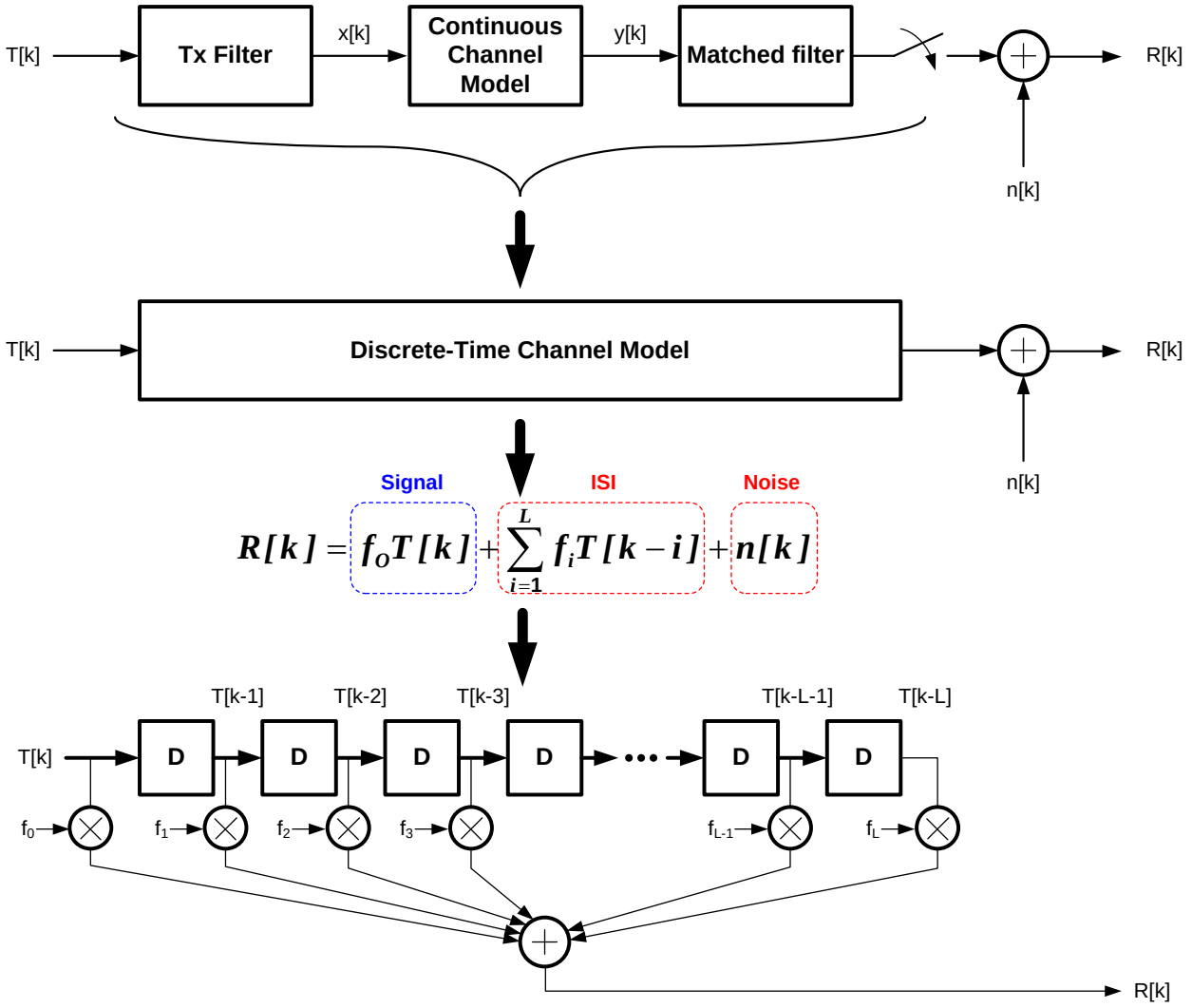
Continuous-Time Equalizer



- **Advantages and Disadvantages**
  - **No dependency with the timing recovery**
  - **Speed is limited by the equalizing filter**
  - **Tradeoff between adaptation accuracy and operating frequency**

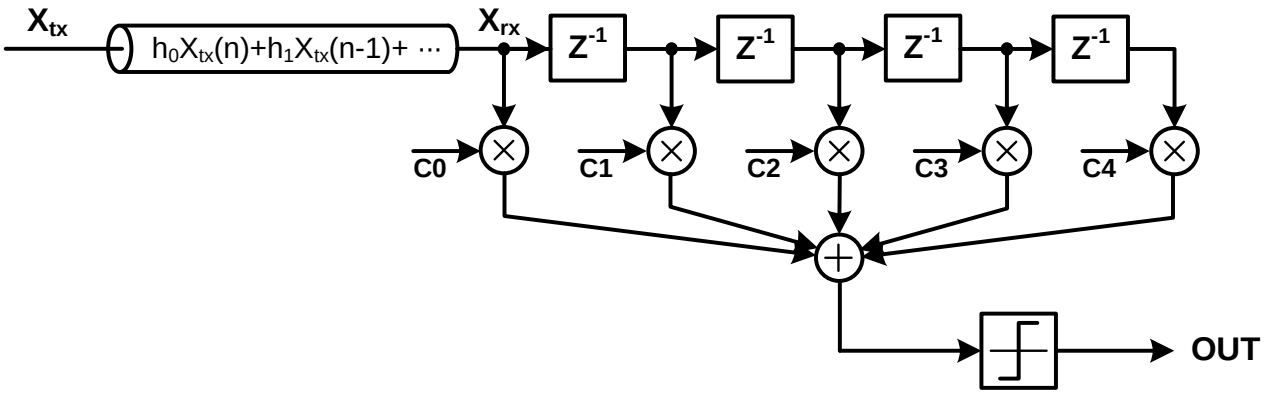
[JSSC'04, Choi]

Discrete-time Channel Modeling

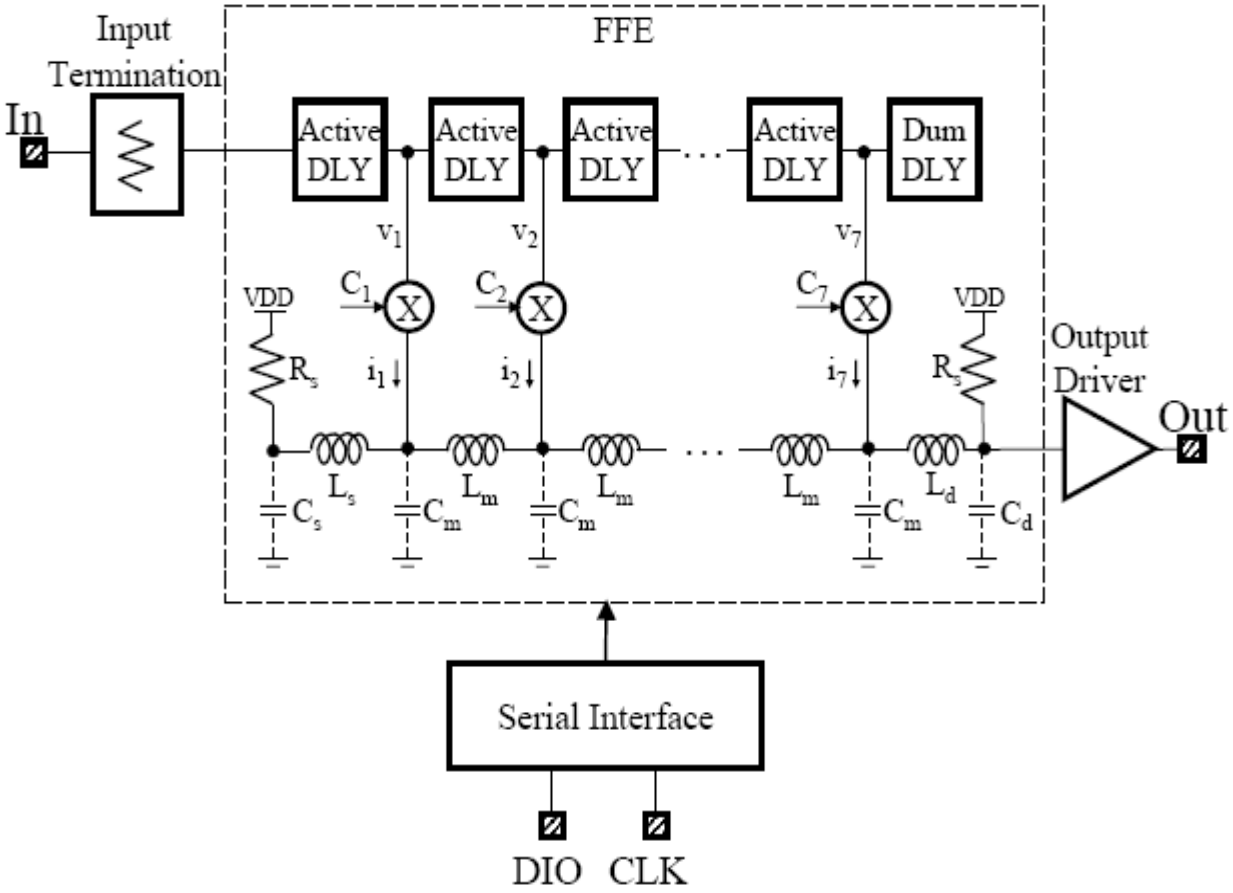


Feed-Forward Equalizer

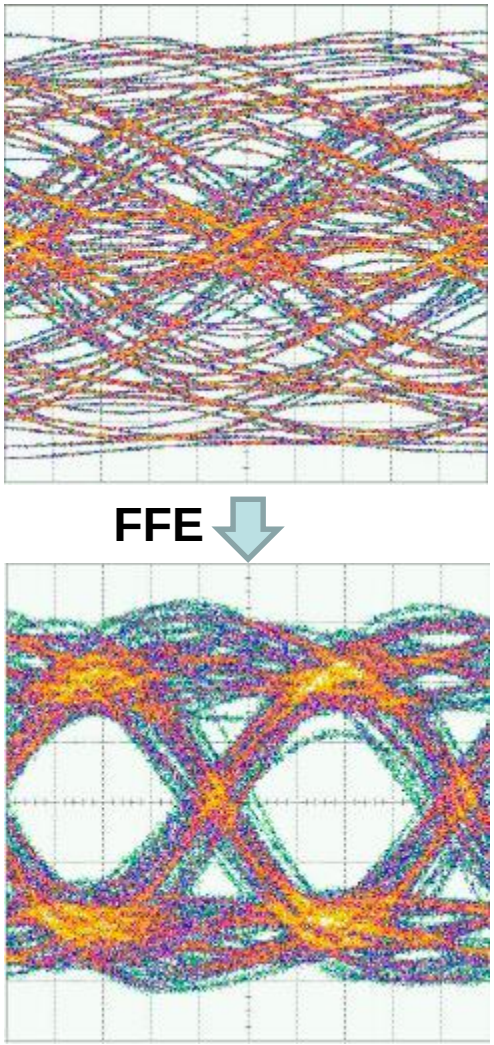
- **AD conversion required**
- **Relaxed timing constraints**
  - **Timing constraint easy to meet**
  - **No time-critical feedback path**
- **Boosts high-freq. noise as well**
- **High power consumption**
  - **ADC and digital blocks**



FFE Examples(1)



40Gb/s 7-Tap FFE



[ISSCC'09, A. Momtaz]

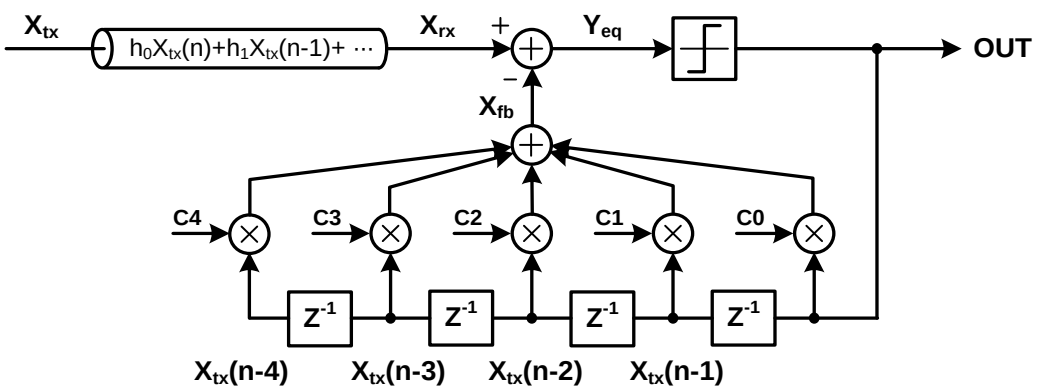
Decision Feedback Equalizer

- **Superior performance but timing constraints**
  - **Hard to design DFE**
- **Only post-cursor cancelled**
  - **Linear equalizer can equalize both pre- and post-cursors**

$$X_{rx}(n)=h_oX_{tx}(n)+h_1X_{tx}(n-1)+\ldots$$

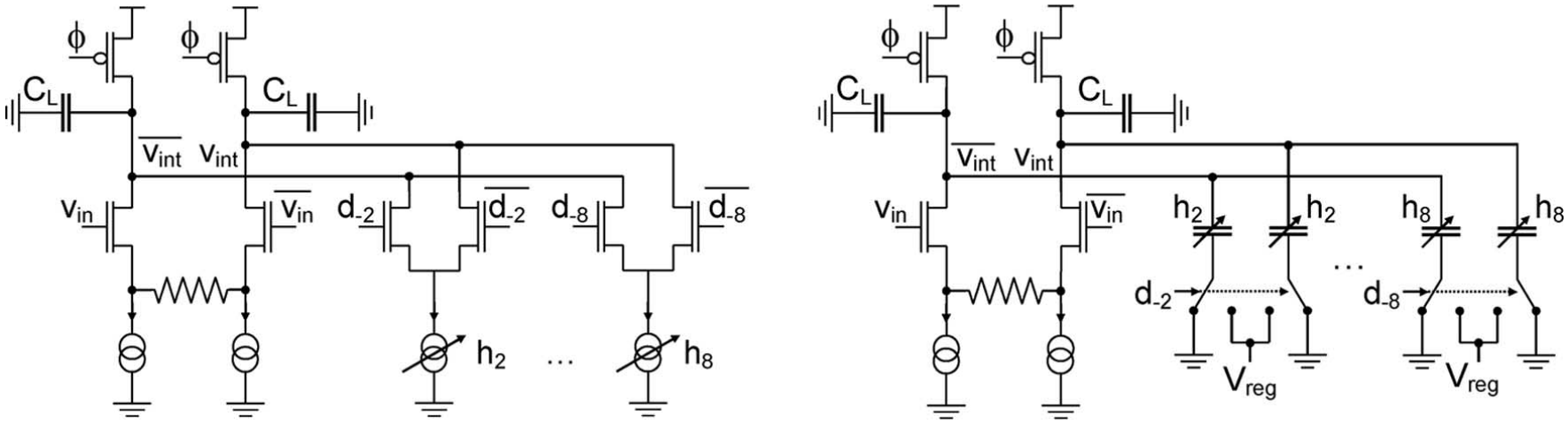
$$X_{fb}(n)=C_0X_{tx}(n)+C_1X_{tx}(n-2)+\ldots$$

$$Y_{eq}(n)=h_oX_{tx}(n)+h_1X_{tx}(n-1)+\ldots$$
$$-C_0X_{tx}(n)-C_1X_{tx}(n-2)-\ldots$$



If $C_0=0$ & $C_1=h_1$ & $C_2=h_2$ & ..., then $Y_{eq}(n)=h_oX_{tx}(n)$
- All ISI due to post-cursors cancelled.

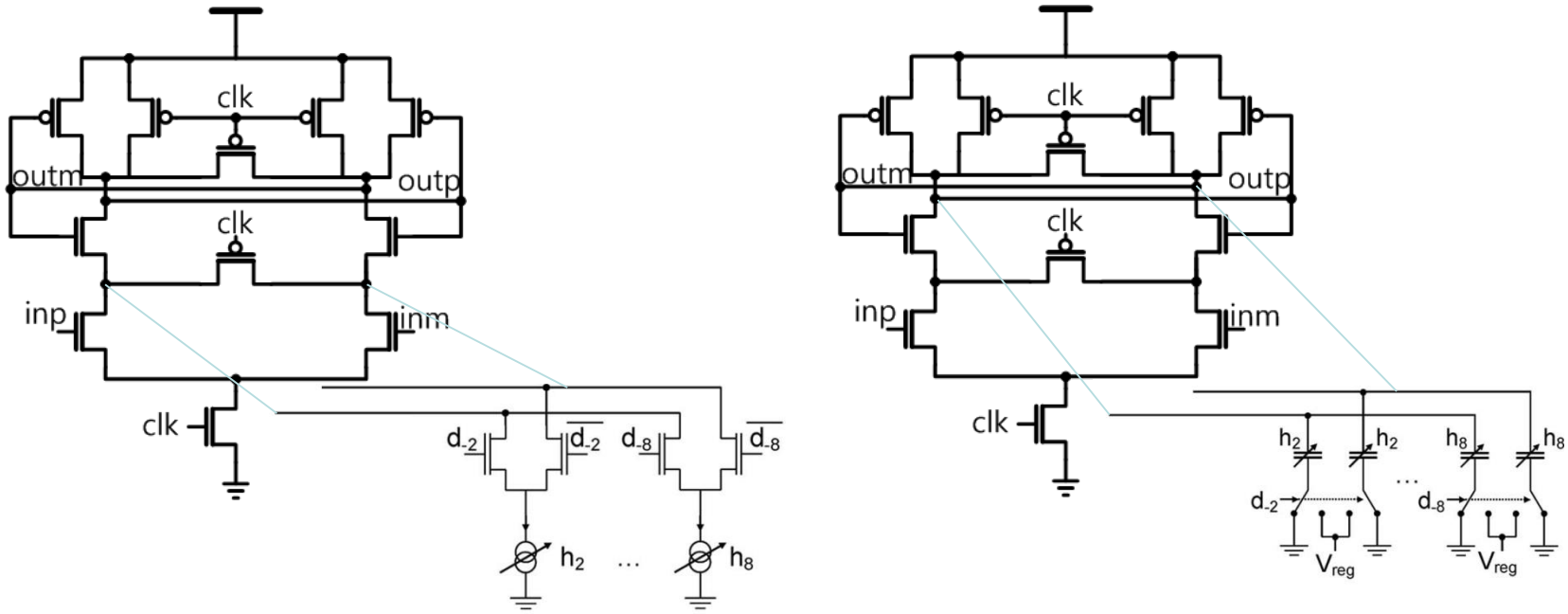
Summer Implementation



- **Current summer or Capacitor switching**
  - **In front of a sampler**
  - **Resettable PMOS load can replace load resistor**
  - **Summer must settle within a certain level of accuracy for ISI cancellation**
  - **Trade-off between summer output swing and settling time**
  - **Can result in large bias current for input and taps**

[JSSC'12, Thomas Toifl]

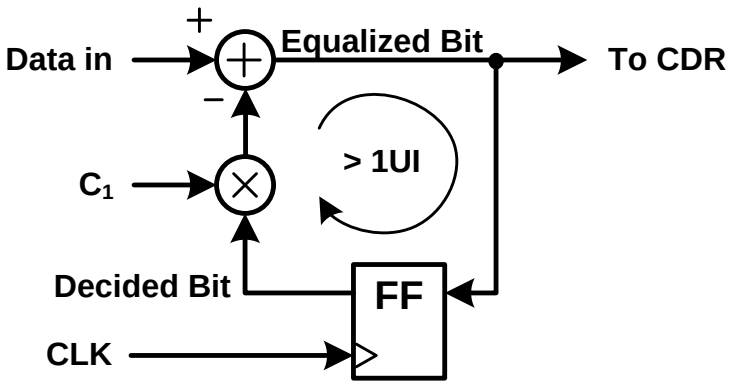
Summing Sampler Implementation



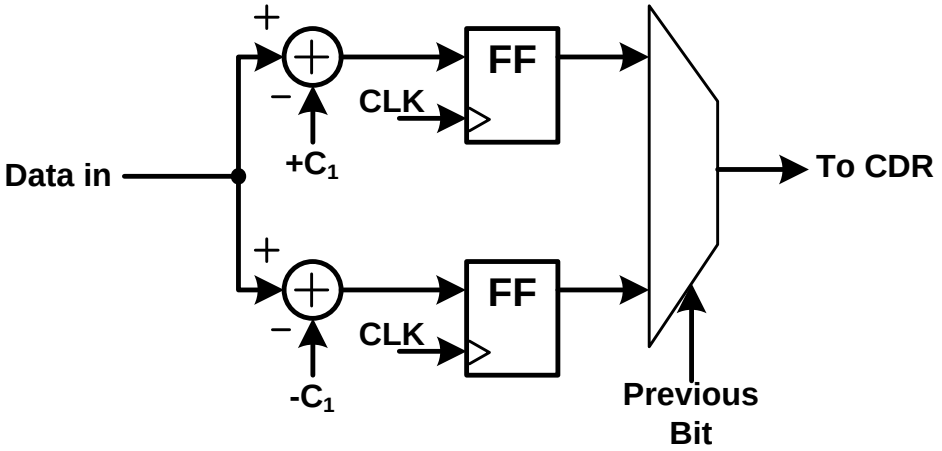
- **Summer merged at sampler**
  - **Both current and capacitance switching can be used**
  - **Latency reduced**
  - **Speed limited by increased summation node capacitance**

DFE Implementation

Direct Feedback



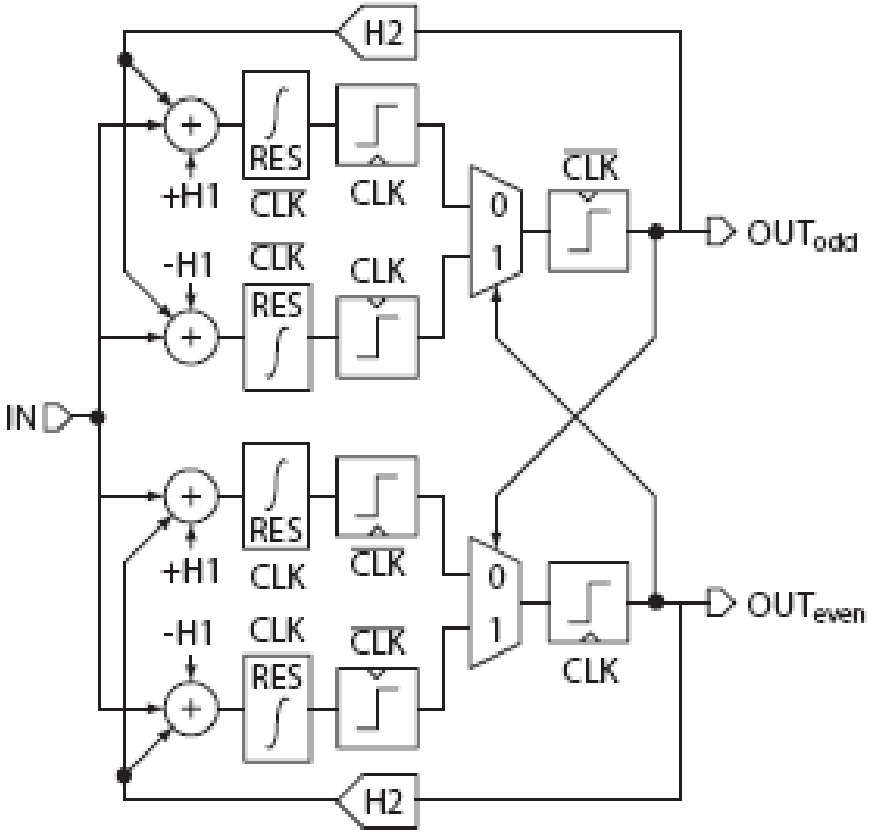
Loop Unrolling



- **Direct feedback**
  - **Simple architecture**
  - **Critical path delay should be less than 1UI**
- **Loop unrolling**
  - **Relaxes time constraints**
  - **Reduces the loading at the summing node**
  - **Increase complexity**

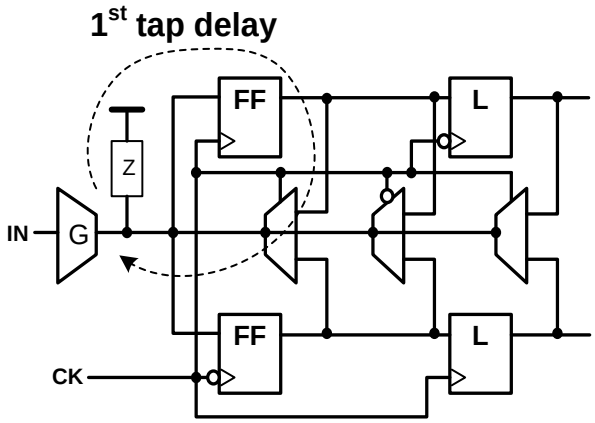
Loop Unrolling (Speculation)

- **Half-rate 2-tap DFE Architecture**

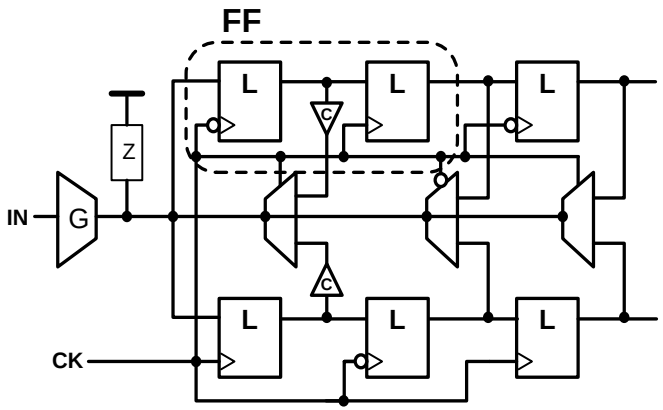


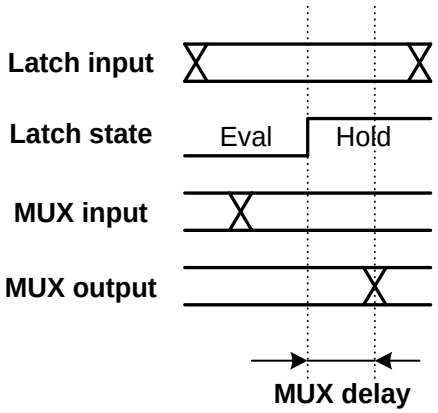
Reduction of Critical Path Delay

Flip-Flop Topology



Latch Topology(’09 JSSC Pozzoni)





- **Flip-Flop Topology**
  - **The 1st tap feedback delay consists of FF and MUX delay.**
- **Latch-Based Topology**
  - **MUX incorporates the function of the 2nd latch in a FF.**
  - **The propagation delay to be limited to the MUX delay.**

[JSSC’09, Pozzoni]

References

- Sameh Abrahim and Behzad Razavi, “A 20-Gbps Serial Link for High-Loss Channels” UCLA
- MAXIM, “Spectral Content of NRZ Test Patterns”
- Koon-Lun Jackie Wong, E-Hung Chen, and Chih-Kong Ken Yang, “Edge and Data Adapti ve Equalization of Serial-Link Transceivers” IEEE, JSSC Sep. 2008
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- Massimo Pozzoni, “A Multi-Standard 1.5 to 10 Gb/s Latch-Based 3-Tap DFE Receiver With a SSC Tolerant CDR for Serial Backplane Communication” IEEE, JSSC Apr. 2009
- Srikanth Gondi and Behzad Razavi, “Equalization and Clock and Data Recovery Techniques for 10-Gb/s CMOS Serial-Link Receivers”, IEEE JSSC Sept. 2007
- Jian-Hao Lu “A 40Gb/s Low-Power Analog Equalizer in 0.13um CMOS Technology”, IEEE SOVC 2008
- A. Momtaz “An 80mW 40Gb/s 7-Tap T/2-Spaced FFE in 65nm CMOS”, IEEE ISSCC 2009

Topics in IC Design

7.3 DFE (by example)

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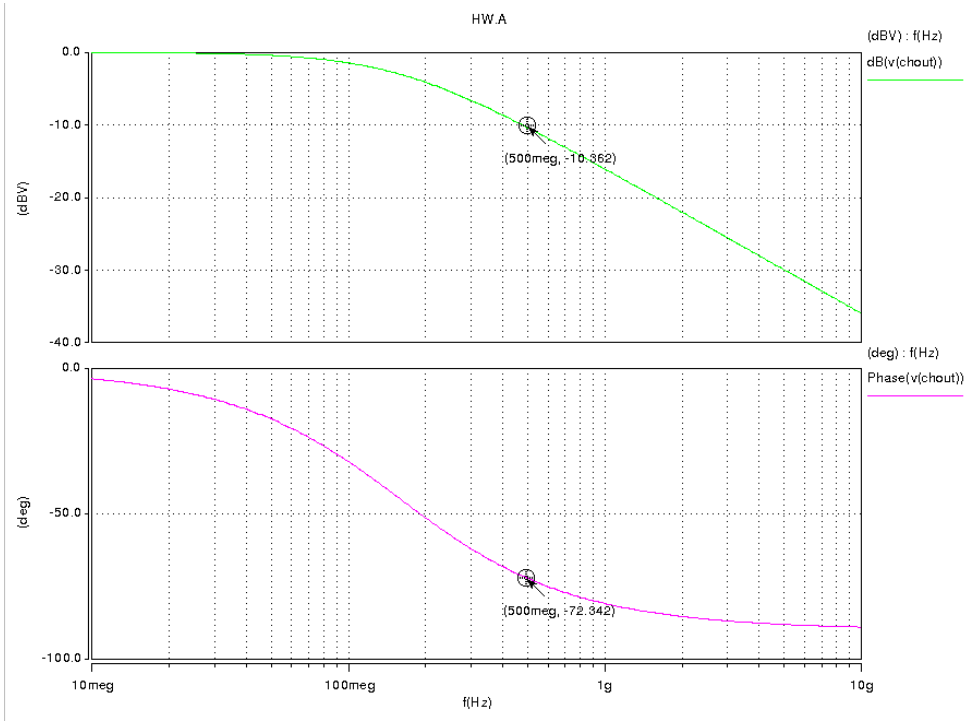
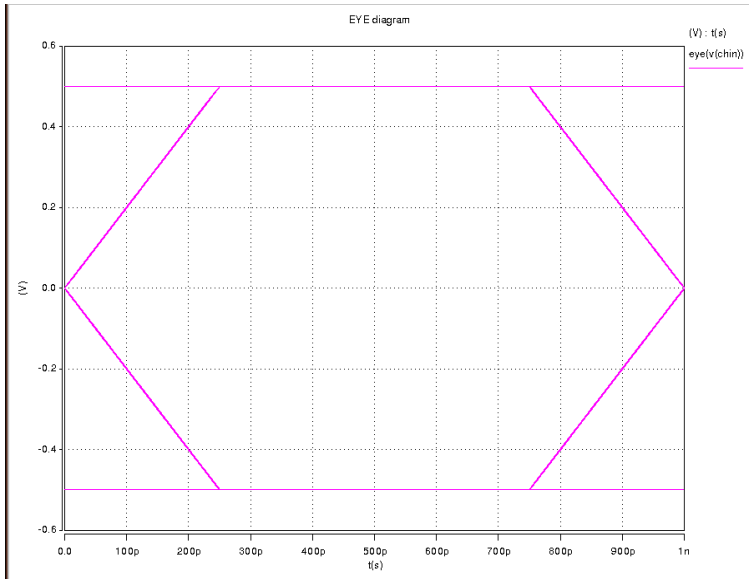
Example Channel

- **Channel characteristics**
  - **1st-order RC channel (R=50 Ω, C = 20pF)**
  - **At the transmission rate of 1 Gbps**
  - **Attenuation at Nyquist Frequency = $1/\sqrt{(1+\pi^2)}$ = -10.352 dB**
  - **Phase delay at Nyquist Frequency = -72.3°**

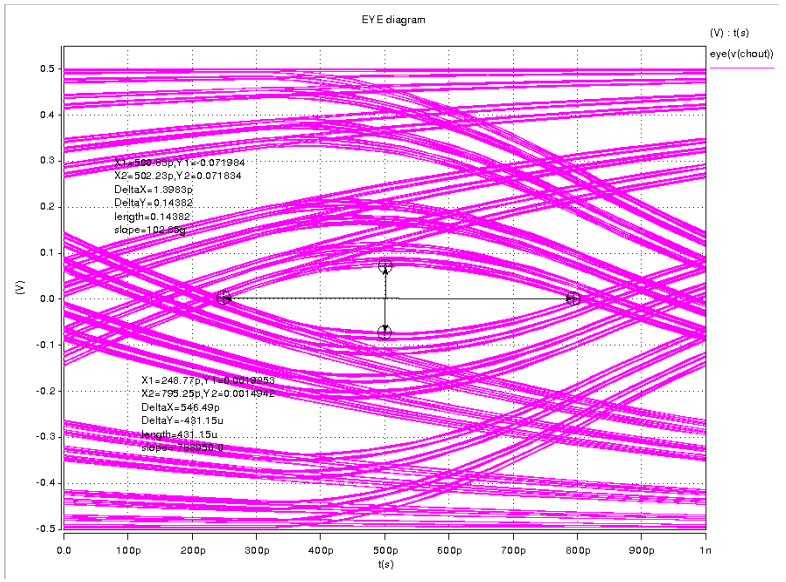


TX and RX Eye Diagrams

- **PRBS-7 NRZ**



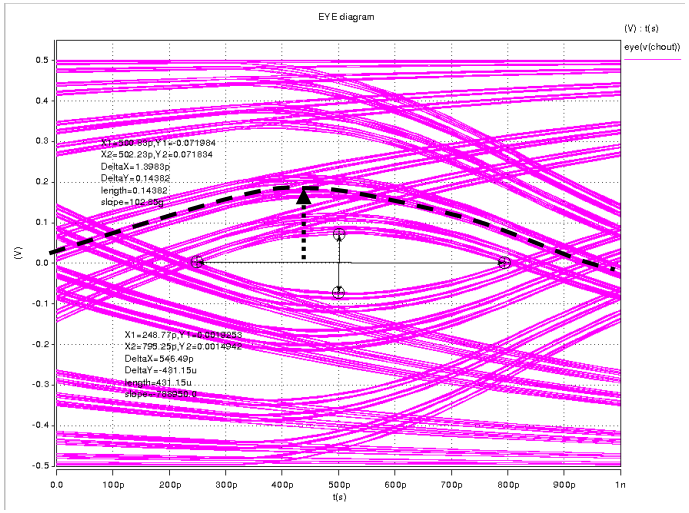
Height: 1 V
Time width: 1 ns



Height: 0.143 V
Time width: 546 ps

Eye Diagram and Channel Loss

- **Loss at the Nyquist frequency.**
  - **The 1010 pattern contains the Nyquist frequency**
  - **Swing of this pattern indicates the attenuation**
  - **See the dotted line and arrow in the picture above. 20log(0.17/0.5)= -9.4dB (-10.35dB)**

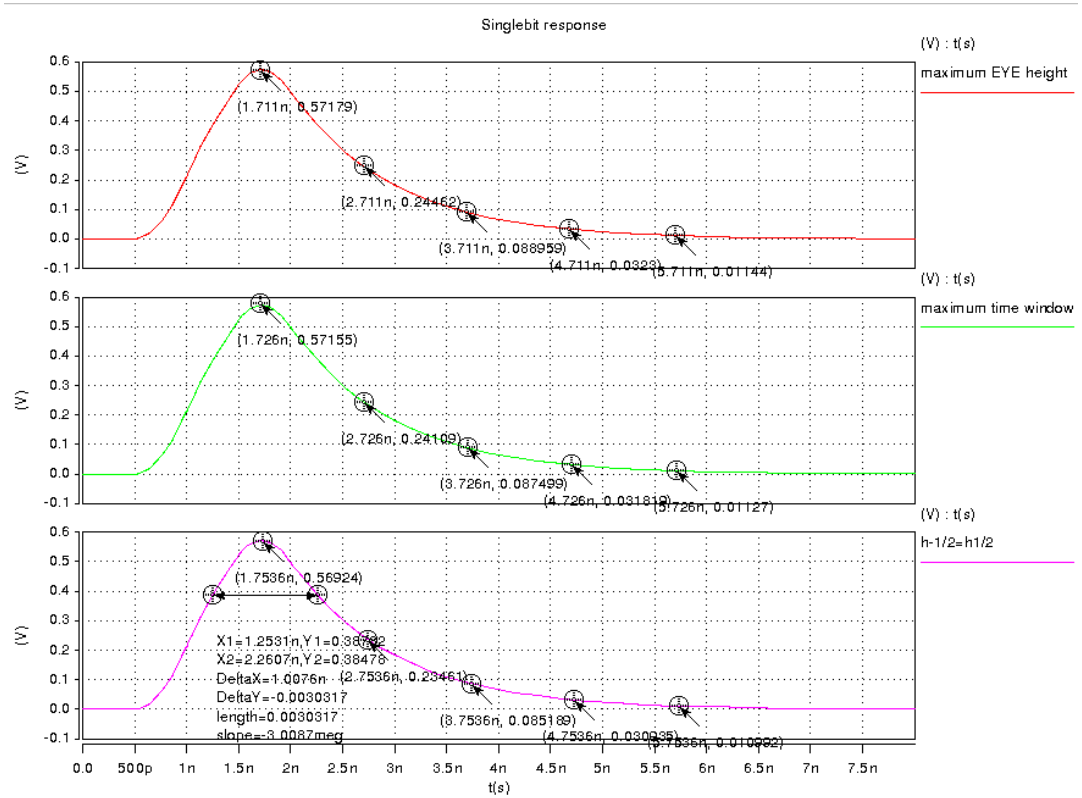


Single Bit Response

A. h_0 at maximum height

B. h_0 at maximum width

C. h_0 at mid-point between two points of $h_{1/2} = h_{-1/2}$



Single Bit Response

A. h_0 at maximum height

B. h_0 at maximum width

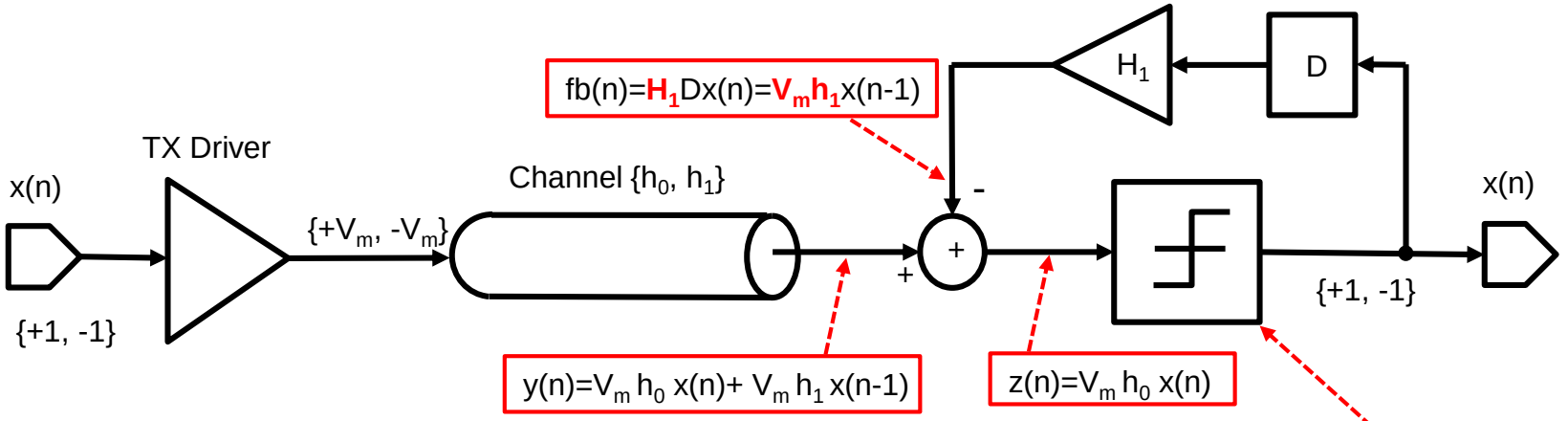
C. h_0 at mid-point between two points of $h_{1/2} = h_{-1/2}$

CASE	h_0	h_1	h_2	h_3	h_4
A. Maximum height	0.5718	0.2446	0.0889	0.0323	0.0114
B. Maximum time width	0.5716	0.2411	0.0875	0.0318	0.0113
C. $h_{1/2}=h_{-1/2}$	0.5692	0.2346	0.0852	0.0309	0.0110

- **Precursor $h_{-1} \approx 0.05$**
- **Sum of all coefficients = 0.949, 0.9433, 0.9309 + precursor ≈ 1**

DFE Architecture

- **1-tap DFE**
  - **$H_1 = V_m$* (h_1 of SBR) = V_m*0.2446 (= 0.1223 if V_m =0.5V)**
  - **Other post-cursors not cancelled**



- **DFE transfer function**

$$DFE\ Gain(z) = \frac{\frac{1}{V_m h_0}}{1 + H_1 \frac{1}{V_m h_0} z^{-1}} = \frac{1}{V_m} \frac{1}{h_0 + h_1 z^{-1}}$$

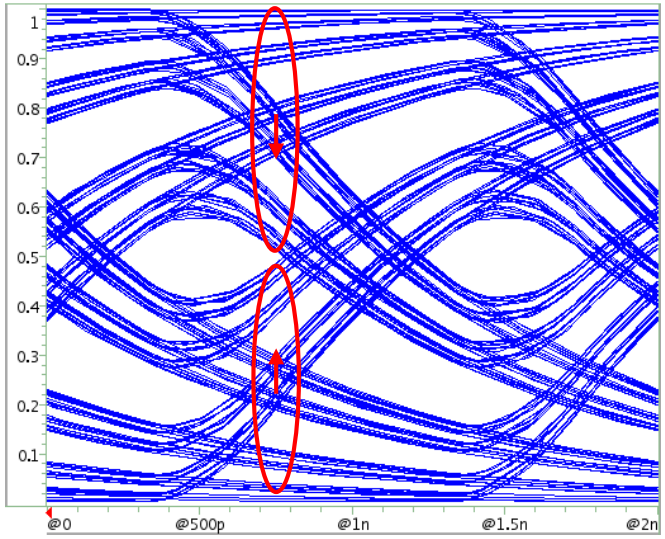
Maximum Boost of 1-tap DFE

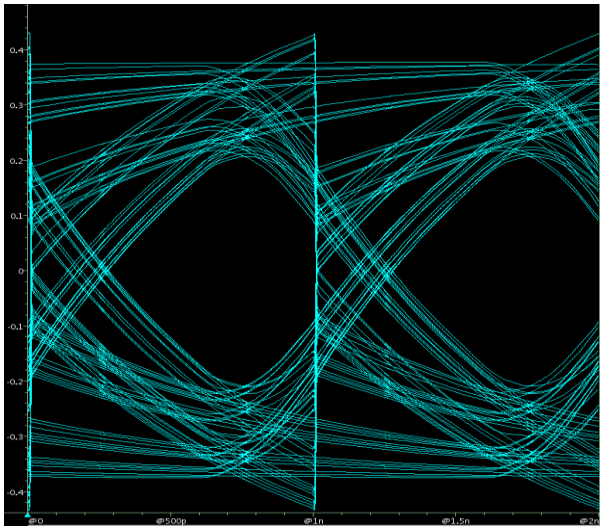
$$\text{DFE Gain}(\omega) = \frac{1}{V_m}\frac{1}{|h_0 + h_1 e^{-j\omega T}|} = \frac{1}{V_m}\frac{1}{\sqrt{h_0^2+2h_0h_1\cos(\omega T)+h_1^2}}$$

- **DFE Gain at DC = $1/(h_0+h_1)/V_m$= 2.450 = 7.78dB (with V_m=0.5V)**
- **DFE Gain at Nyquist = $1/(h_0-h_1)/V_m$ = 6.112 = 15.72dB(with V_m=0.5V)**
- **DFE Max Boost**
  - **= $(h_0+h_1)/(h_0-h_1)$ = (0.5718+0.2446)/(0.5718-0.2446)**
  - **= 2.496 = 7.94dB**
- **Channel DC Gain with all postcursors = V_m= 0.5V**
- **Overall DC gain = 0.5*2.450=1.225=1.76dB (≠ 1, due to no 2nd or higher-order postcursor cancellation)**
- **Overall gain at Nyquist = -10.53dB+7.94dB =-2.59dB**

Eye Diagram with 1-tap DFE

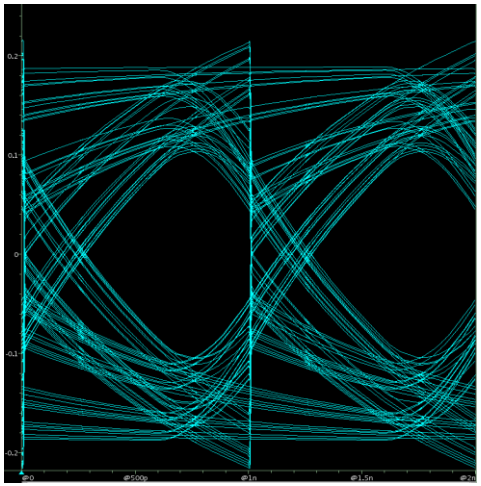
- **With feedback delay of 0.25ns**

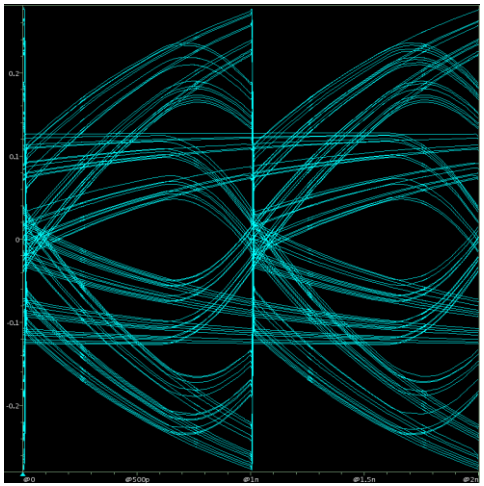




What if input amplitude changed?

- **Input amplitude (V_m) is increased from 1.0V to 0.5V, while DFE tap coefficient (V_m*h_1) is fixed.**
- **Tap coeff is reduced by half in effect.**
- **Need to change tap coeffs depending on the input amplitude!**





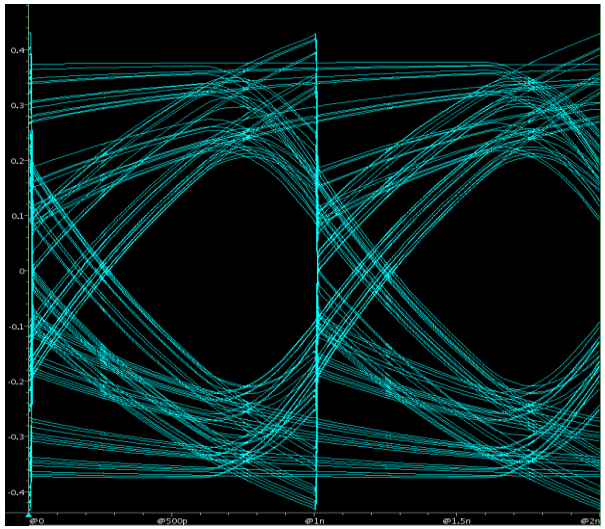
4-Tap DFE

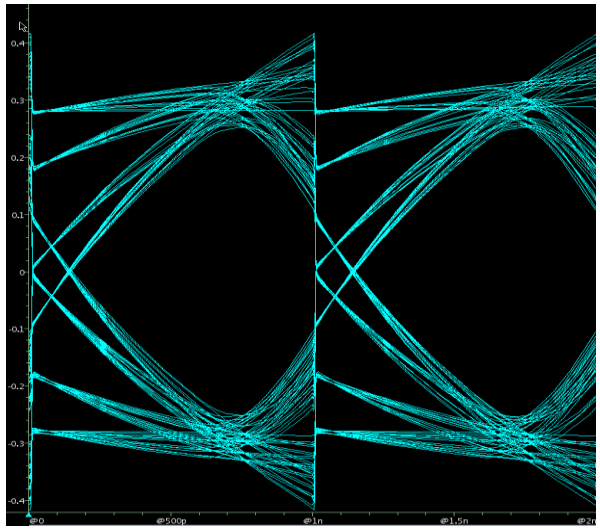
$$\text{DFE Gain}(\omega) = \frac{1}{V_m} \frac{1}{|h_0 + h_1 e^{-j\omega T} + h_2 e^{-j2\omega T} + h_3 e^{-j3\omega T} + h_4 e^{-j4\omega T}|}$$

- DFE Gain at DC = $1/(h_0+h_1+h_2+h_3+h_4)/V_m$= 2.107=6.47dB (with V_m=0.5V)
- DFE Gain at Nyquist = 5.061 = 14.08dB (with V_m=0.5V)
- DFE Max Boost
  = 14.08dB - 6.47dB = 7.61dB
- Channel DC Gain with all postcursors = V_m= 0.5V
- Overall DC gain = 0.5*2.107=1.054=0.45dB (≠ 1, due to no 2nd or higher-order postcursor cancellation)
- Overall gain at Nyquist = -10.53dB+7.61dB =-2.92dB

Eye Diagram with 4-tap DFE

- **With feedback delay of 0.25ns**
- **Almost all the post-cursors removed**
- **Remaining ISI due to precursors**





References

- Sameh Abrahim and Behzad Razavi, “A 20-Gbps Serial Link for High-Loss Channels” UCLA
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- Srikanth Gondi and Behzad Razavi, “Equalization and Clock and Data Recovery Techniques for 10-Gb/s CMOS Serial-Link Receivers”, IEEE JSSC Sept. 2007
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- A. Momtaz “An 80mW 40Gb/s 7-Tap T/2-Spaced FFE in 65nm CMOS”, IEEE ISSCC 2009

Topics in IC Design

7.4 Adaptive DFE and Timing Recovery

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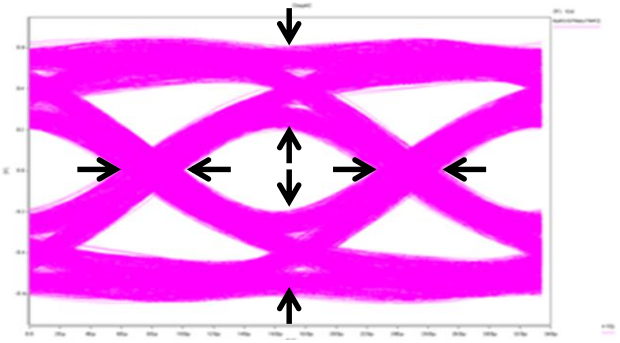
Equalizer Adaptation

- **Adaptive Equalization**
  - **Compensate changes in the transmission channel characteristics**
  - **Compensate manufacturing variation**
  - **Suitable for multi-standard**
- **Can be applied to any equalizers; FFE, CTLE, and DFE**



DFE Adaptation

- **LMS algorithm**

$$fb = \sum_{k=1}^{2} C_k y(n-k)$$

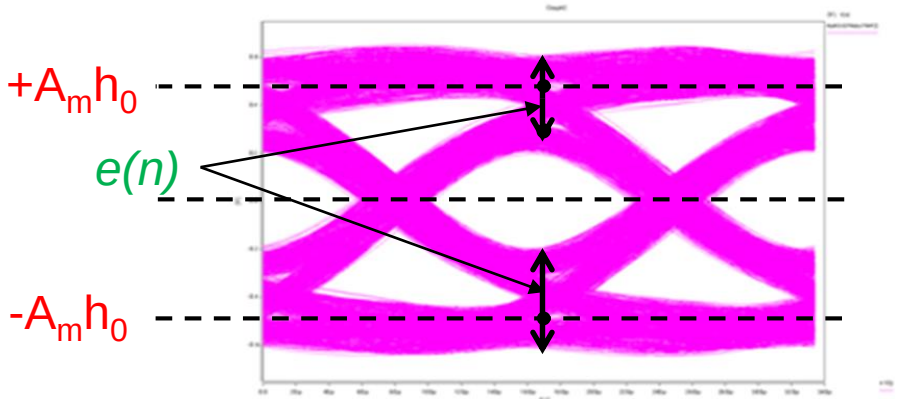
$$e(n) = y(n) - a(n)$$

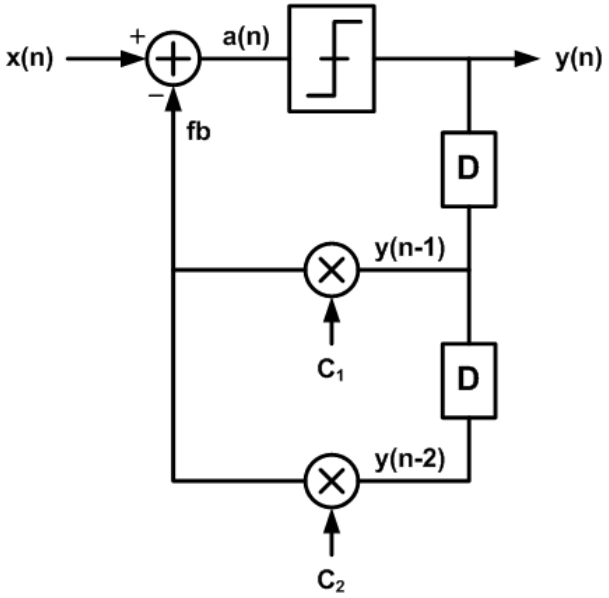
$$a(n) = x(n) - \sum_{k=1}^{2} C_K y(n-k)$$

With LMS updating equation

$$C_k(n+1) = C_k(n) + \mu e(n) y(n-k)$$

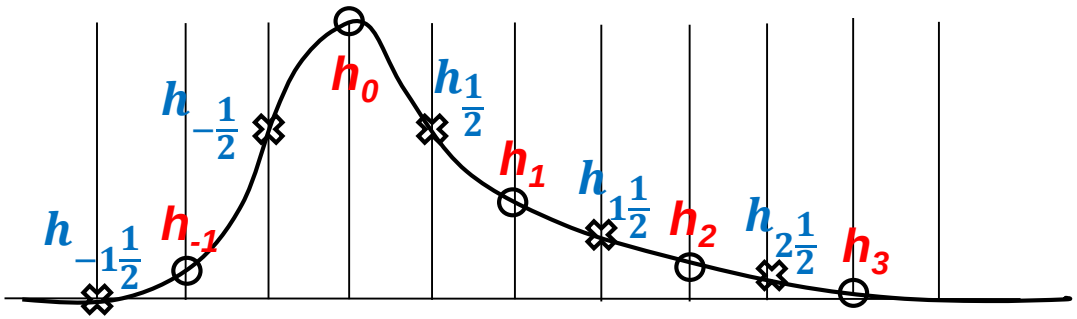
Or use sign-sign adaptation

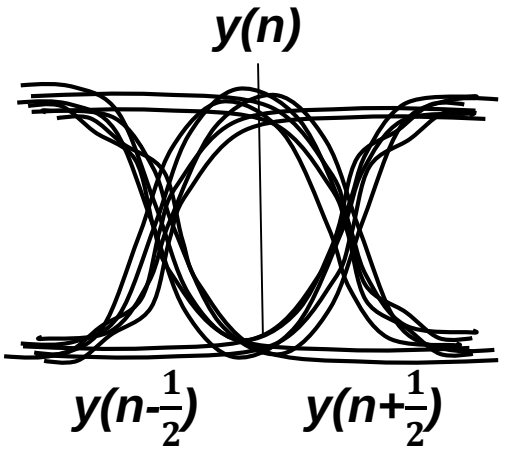




- **How to set $A_m h_0$?**
  - Must know a priori or
  - Adapt so that E[e(n)] = 0.

Single Bit Response & Eye Diagram





- **Data Samples:**

$$y(n) = h_3x(n-3) + h_2x(n-2) + h_1x(n-1) + h_0x(n) + h_{-1}x(n+1)$$

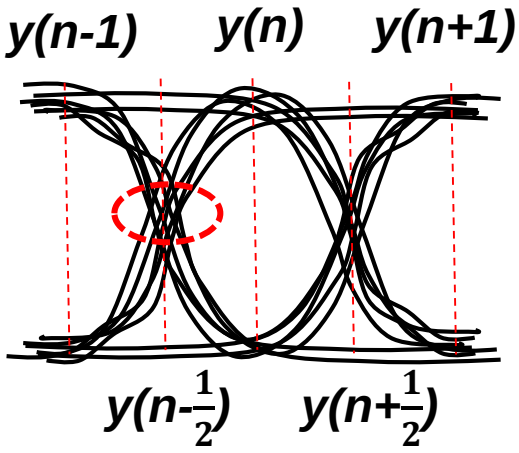
ISI due to Post-Cursor Main Cursor ISI due to Pre-Cursor

- **Edge Samples:**

$$y\left(n-\frac{1}{2}\right) = h_{2\frac{1}{2}}x(n-3) + h_{1\frac{1}{2}}x(n-2) + h_{\frac{1}{2}}x(n-1) + h_{-\frac{1}{2}}x(n) + h_{-1\frac{1}{2}}x(n+1)$$

$$y\left(n+\frac{1}{2}\right) = h_{2\frac{1}{2}}x(n-2) + h_{1\frac{1}{2}}x(n-1) + h_{\frac{1}{2}}x(n) + h_{-\frac{1}{2}}x(n+1) + h_{-1\frac{1}{2}}x(n+2)$$

Eye Diagram and Timing Recovery



For the -1 -> +1 transition at (n-1/2) (A),
if $h_{\frac{1}{2}} > h_{-\frac{1}{2}}$, then y(n-1/2) > 0.
Alexander PD asserts DOWN (VCO too fast), and the next sampling time pushed down, then $h_{-\frac{1}{2}}$ goes down and $h_{\frac{1}{2}}$ goes up, eventually making $h_{\frac{1}{2}} = h_{-\frac{1}{2}}$.

Same result for +1->-1 transition (B)

- **Zero Crossing levels at y(n-1/2)**

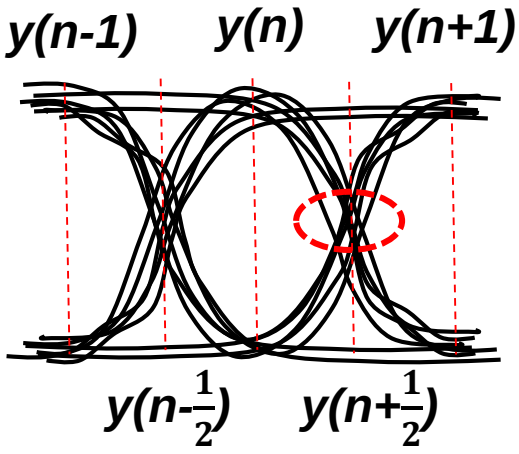
A. -1->+1 transition at y(n-1) = -1, y(n) = +1

$$y\left(n-\frac{1}{2}\right) = h_{2\frac{1}{2}}x(n-3) + h_{1\frac{1}{2}}x(n-2) - h_{\frac{1}{2}} + h_{-\frac{1}{2}} + h_{-1\frac{1}{2}}x(n+1)$$

B. +1->-1 transition at y(n-1) = +1, y(n) = -1

$$y\left(n-\frac{1}{2}\right) = h_{2\frac{1}{2}}x(n-3) + h_{1\frac{1}{2}}x(n-2) + h_{\frac{1}{2}} - h_{-\frac{1}{2}} + h_{-1\frac{1}{2}}x(n+1)$$

Eye Diagram and Timing Recovery



For the -1 -> +1 transition at (n+1/2) (B), if $h_{\frac{1}{2}} < h_{-\frac{1}{2}}$, then y(n+1/2) > 0.

Alexander PD asserts UP (VCO too slow), and the next sampling time pulled up, then $h_{-\frac{1}{2}}$ goes up and $h_{\frac{1}{2}}$ goes down, eventually making $h_{\frac{1}{2}} = h_{-\frac{1}{2}}$.

Same result for +1->-1 transition (B)

- **Zero Crossing levels at y(n+1/2)**

A. -1->+1 transition at y(n) = -1, y(n+1) = +1

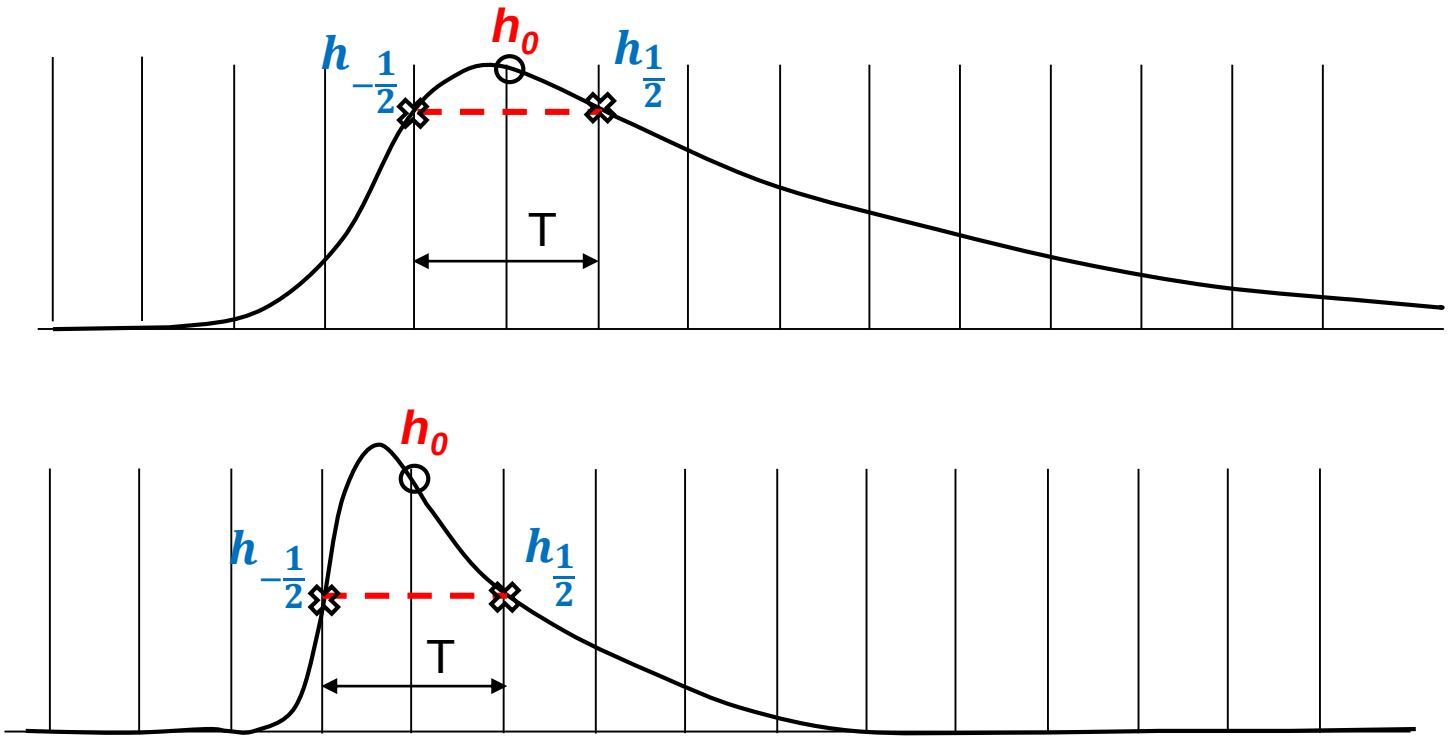
$$y\left(n+\frac{1}{2}\right) = h_{2\frac{1}{2}}x(n-2) + h_{1\frac{1}{2}}x(n-1) - h_{\frac{1}{2}} + h_{-\frac{1}{2}} + h_{-1\frac{1}{2}}x(n+2)$$

B. +1->-1 transition at y(n) = +1, y(n+1) = -1

$$y\left(n+\frac{1}{2}\right) = h_{2\frac{1}{2}}x(n-2) + h_{1\frac{1}{2}}x(n-1) + h_{\frac{1}{2}} - h_{-\frac{1}{2}} + h_{-1\frac{1}{2}}x(n+2)$$

Eye Diagram and Timing Recovery

- **2x oversampling with Alexander PD,**
  - $h_{\frac{1}{2}} = h_{-\frac{1}{2}}$ **holds.**
  - **may not offer max SNR when SBR is not symmetric.**



Edge Equalization

- **Reduce DDJ at edge for low-jitter clock recovery**
- **Edge DFE**
  - **Reduce the ISI due to edge post-cursors $h_{1\frac{1}{2}}$, $h_{2\frac{1}{2}}$, etc.**
  - **Not possible to cancel ISI due to edge pre-cursors $h_{-1\frac{1}{2}}$, etc.**

- **Edge Samples:**

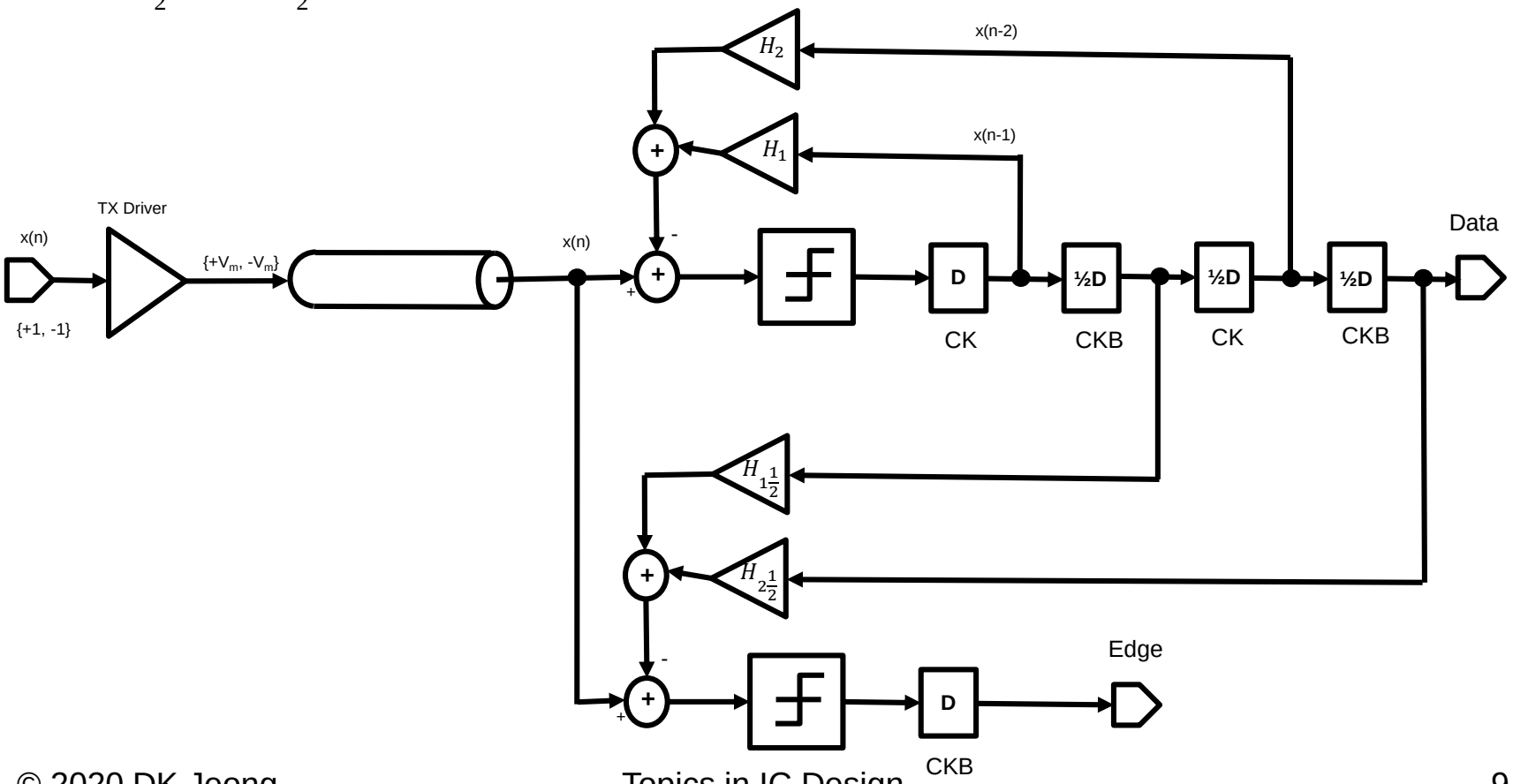
$$y\left(n-\frac{1}{2}\right) = h_{2\frac{1}{2}}x(n-3) + h_{1\frac{1}{2}}x(n-2) + h_{\frac{1}{2}}x(n-1) + h_{-\frac{1}{2}}x(n) + h_{-1\frac{1}{2}}x(n+1)$$

$$y\left(n+\frac{1}{2}\right) = h_{2\frac{1}{2}}x(n-2) + h_{1\frac{1}{2}}x(n-1) + h_{\frac{1}{2}}x(n) + h_{-\frac{1}{2}}x(n+1) + h_{-1\frac{1}{2}}x(n+2)$$

Edge DFE Architecture

- **Edge Adaptation**

$$H_{k+\frac{1}{2}}' = H_{k+\frac{1}{2}} - \mu \cdot x(n-k) \cdot [x(n) - x(n-1)] \cdot \mathrm{sign}[x(n+\frac{1}{2})]$$



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