Topics in IC Design

8.1 Introduction to Optical Interfaces

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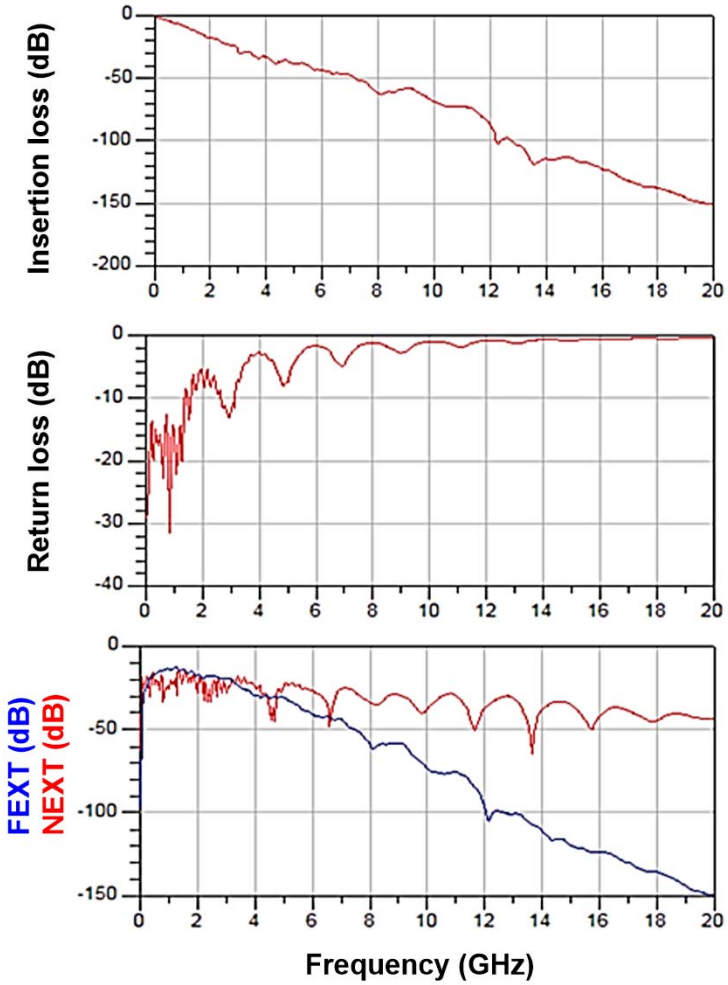
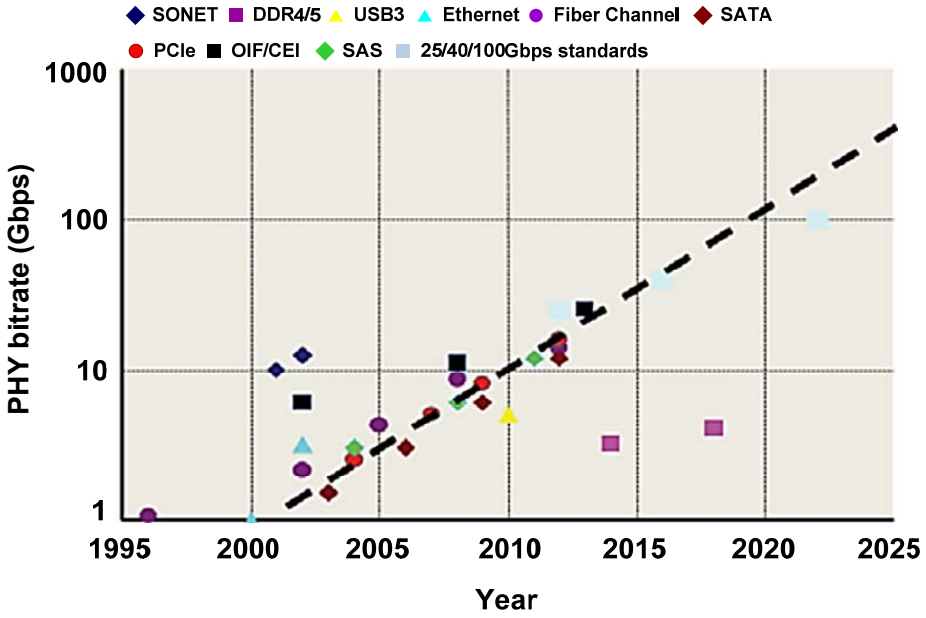
(Compliments to 배우람, 정규섭, 김윤수, 주하람, 황정호**)**

Limits of Cu Interconnect

PCIE Channel Characteristics



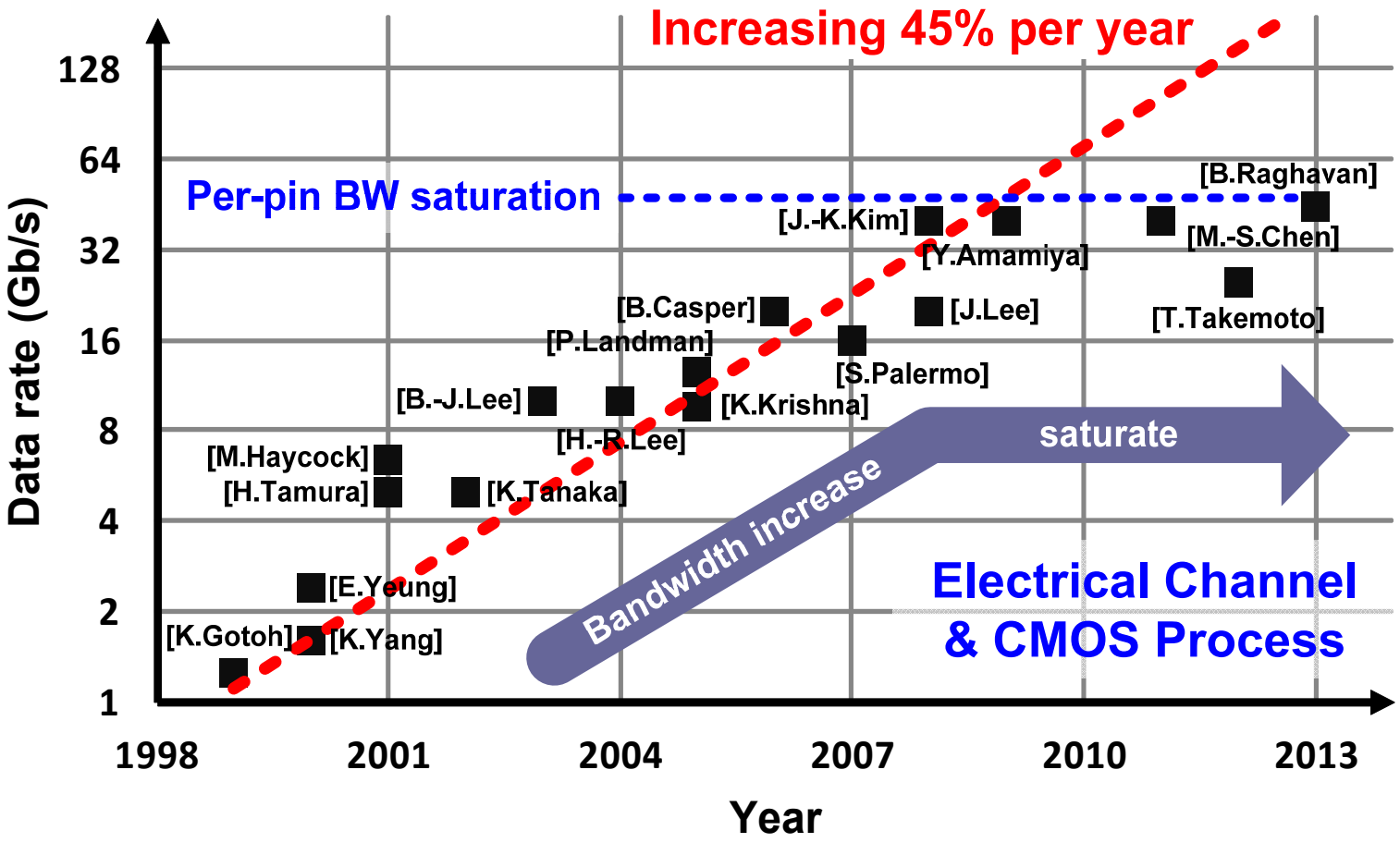
[ITRS, 2009 revision]



[Source: Altera Corp., Overcome Copper Limits with Optical Interfaces, 2011]

I/O Data Rate in the Last 15 Years

- **Fastest electrical transceivers reported in ISSCC/VLSIC**



Electrical vs. Optical (1)

< Electrical link model >

- Simultaneous bidirectional
- Low swing current mode, bipolar, differential signaling
- High performance GETEK board
- Flip-chip package
- Circuits for clock recovery and equalization are not considered
- Noise: Proportional, X-talk, Imp. Mismatch, Package…

< Optical link model >

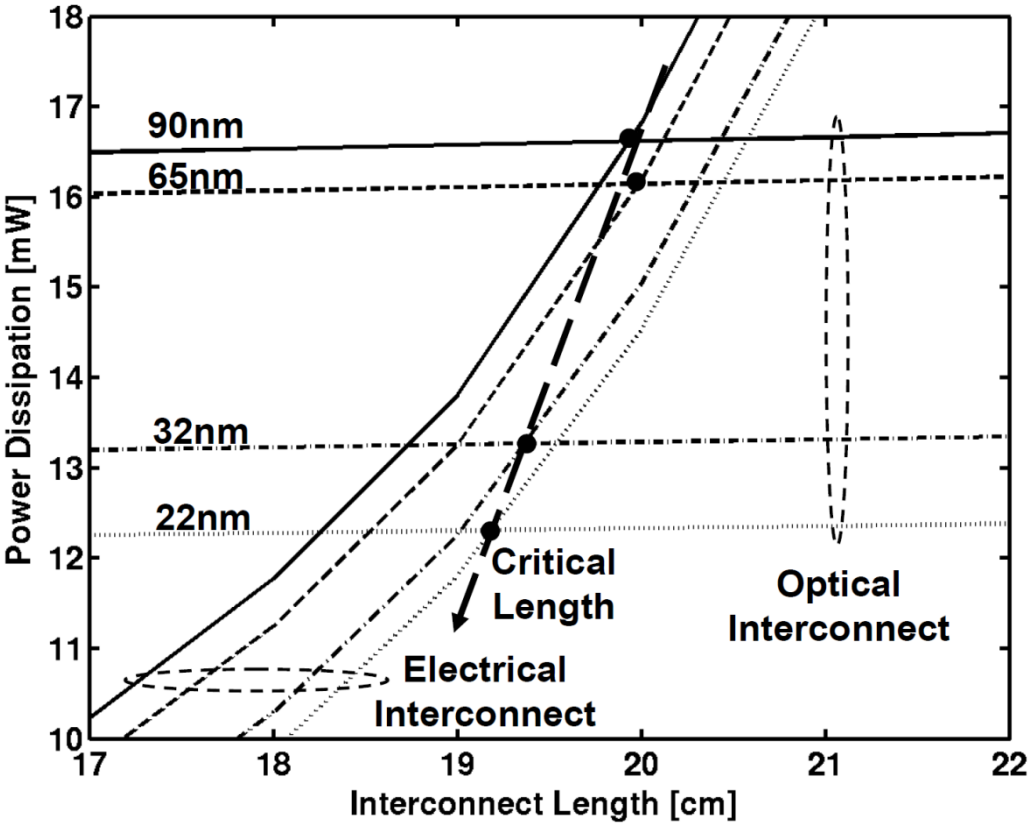
- Modulator (driven by an exponentially sized buffers)
- 50fF detector capacitance
- 0.5A/W PD responsivity
- TIA and gain stages

❖ Based on 180nm technology using BSIM3v3 technology SPICE simulations

[H. Cho, Ph.D. Thesis, Stanford University][4]

Electrical vs. Optical (1)

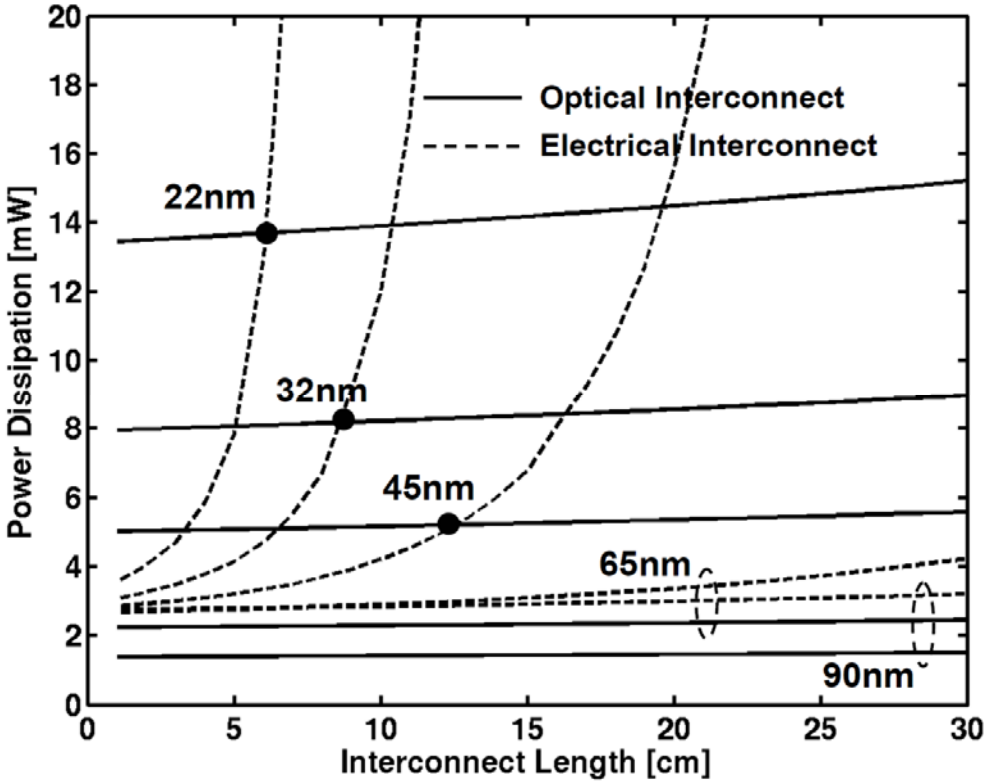
- Comparison between electrical and optical power dissipation for a scaled technology at a fixed bit rate



[H. Cho, Ph.D. Thesis, Stanford University][4]

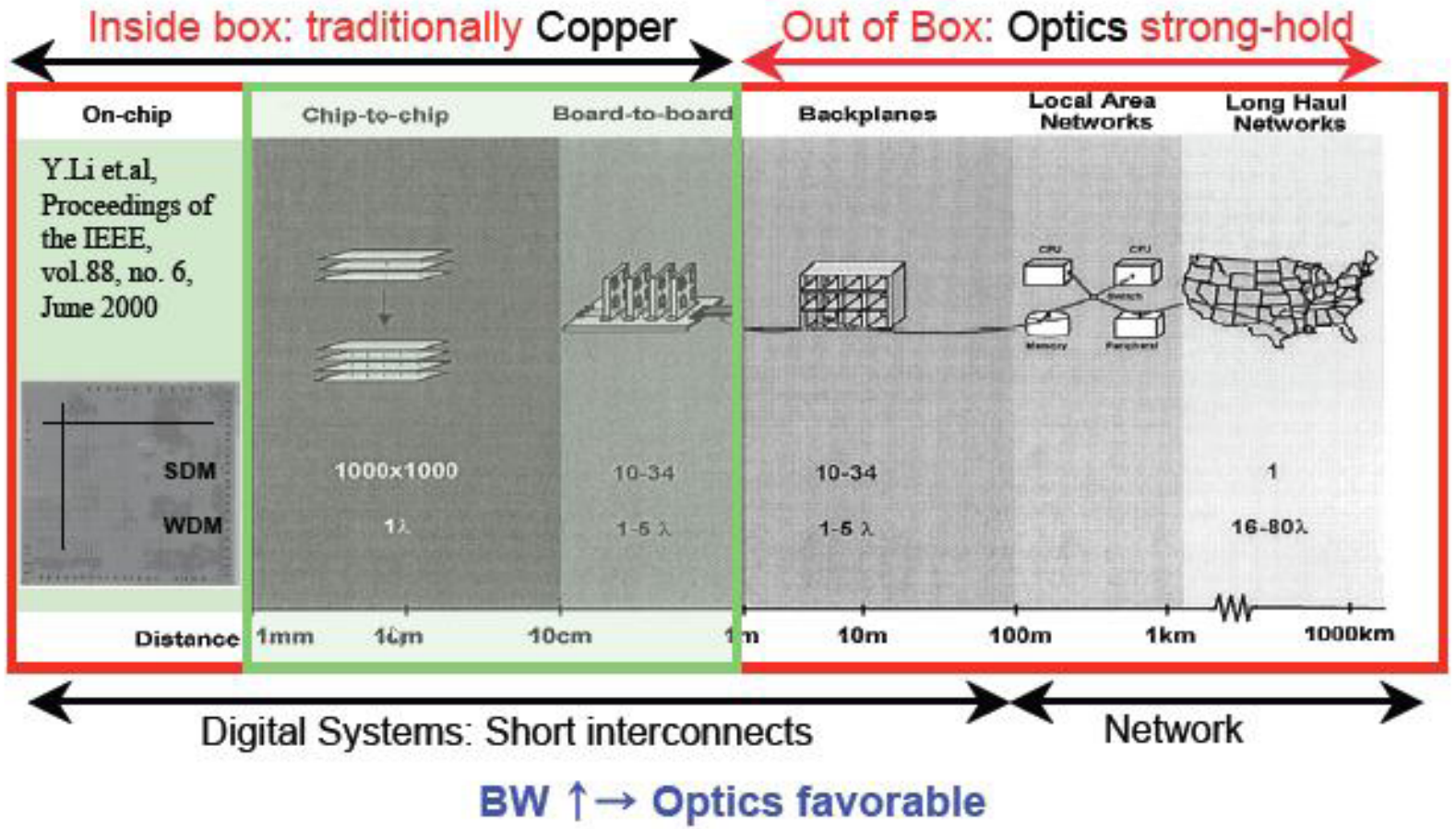
Electrical vs. Optical (2)

- Comparison incorporating both transistor performance improvement and higher bit rate with technology scaling



[H. Cho, Ph.D. Thesis, Stanford University][4]

Optics is Creeping Closer to the Chip



[ITRS 2011, Assembly and Packaging][2]

Optical Standards

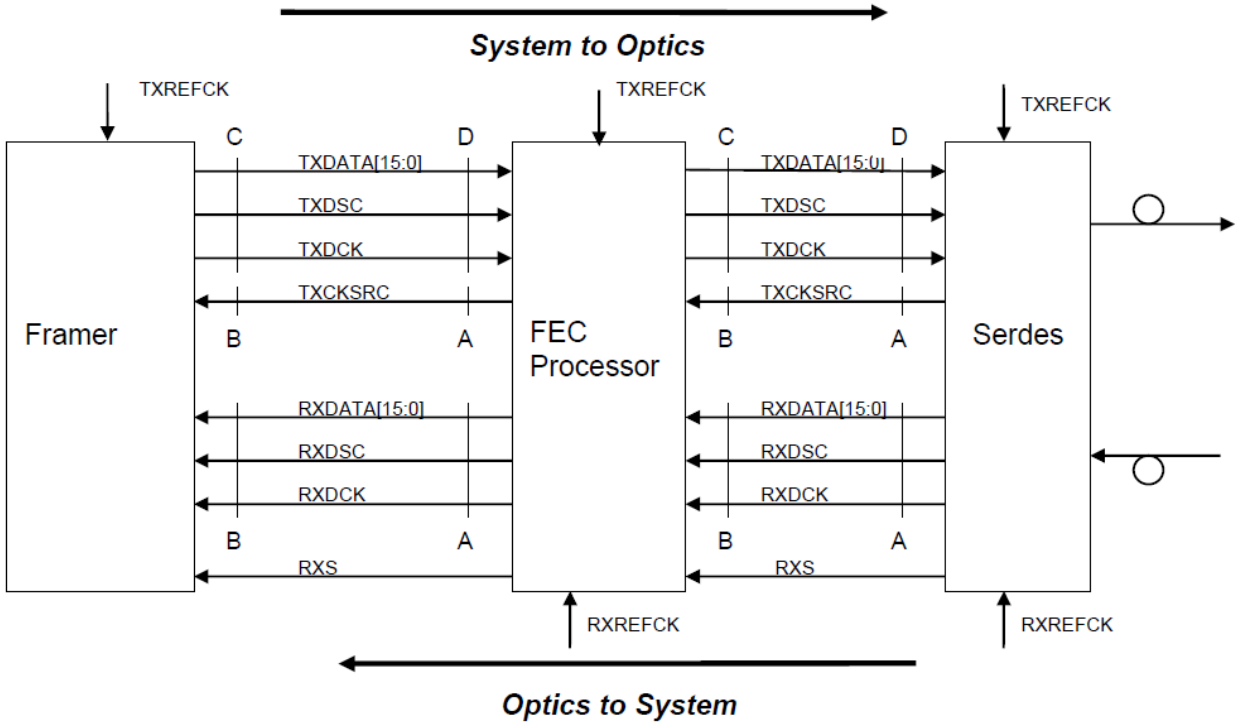
- **SONET OC-768 / SDH STM-256 / OTN OTU-3** — Data-rate specification
  - ✓ OC-XXXs specify transmission bandwidth for fiber optic networks
  - ✓ OC-768 : data-rate of up to 39,813.12 Mbit/s (768 x 51.84 Mbit/s)
  - ✓ STM-256 : same as OC-768 (256 x 155.52 Mbit/s)
  - ✓ OTU-3 : 43.01 Gbit/s, OTN designed to provide support for WDM

- **Serdes Framer Interface level 5 (SFI-5)** — PHY interface specification
  - ✓ Supports up to 50 Gb/s bi-directional aggregate data throughput such as SONET OC-768, SDH STM-256 and OTN OTU-3
  - ✓ Support Forward Error Correction (FEC)

- **Quad Small Form-factor Pluggable (QSFP)** — Connector specification
  - ✓ Hot-pluggable transceiver
  - ✓ Interfaces a network device motherboard to a fiber optic cable
  - ✓ 4 x 10 Gbit/s ~ 4 x 28 Gbit/s

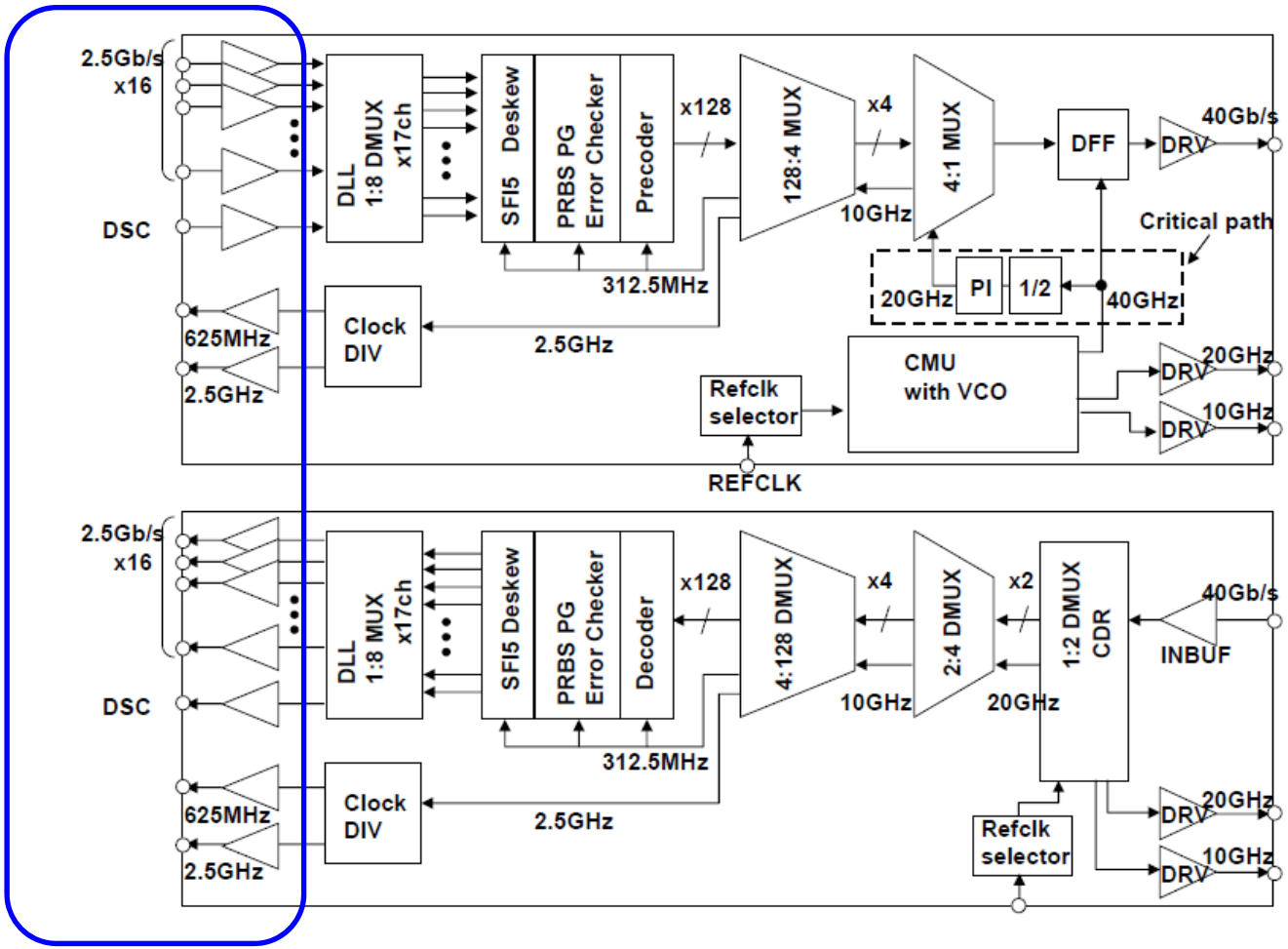
Optical Standards (cont'd)

- **OIF SFI-5**
  - ✓ SONET/SDH framer ↔ FEC processor ↔ serdes
  - ✓ 16-bit wide data bus with each channel operating at up to 3.125 Gb/s
  - ✓ Supports OC-768, STM-256, and OTU-3 with up to 25% FEC overhead



Optical Standards (cont'd)

❖ **SFI-5 interface implementation (ISSCC 2009)**



References

1. Altera Corporation, “Overcome Copper Limits with Optical Interfaces,” 2011
2. International Technology Roadmap for Semiconductors, http://www.itrs.net.
3. W. Bae et al., “A 0.36 pJ/bit, 12.5 Gb/s Forwarded-Clock Receiver with a Sample Swapping Scheme and a Half-Bit Delay Line,” Proceedings of the ESSCIRC, pp. 447-450, 2014
4. H. Cho, “Performance Comparison Between Copper, Carbon Nanotube, and Optics for Off-chip and On-Chip Interconnects,” Thesis of Stanford University, 2007
5. Y. Li et al., “Special Issue on Optical Interconnections for Digital Systems,” Proceedings of the IEEE, pp. 794-805, 2000
6. Proceedings of the IEEE, July 2009

Topics in IC Design

8.2 Optical Devices - TX

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Laser Diode

- Types of Laser Diode
  - Distributed Bragg reflector (DBR)
  - Distributed feedback laser (DFB)
  - Vertical-cavity surface-emitting laser (VCSEL)
- Direct Drive of VCSEL
- Mach-Zehnder Modulator
- MicroRing Modulator

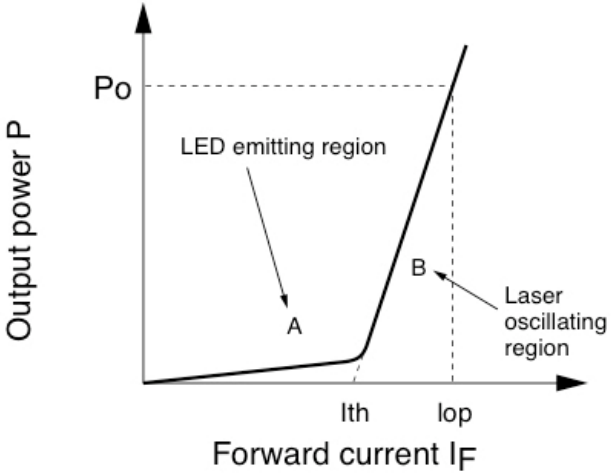
Key Parameters of Laser Diode

1) Slope efficiency

$$\eta_{slope} = \left(\frac{\Delta P_o}{\Delta I} \right)_{\text{above threshold}} \approx \frac{P_o}{I - I_{th}}$$

2) External quantum efficiency

$$\eta_{\text{EQE}} = \frac{\#\text{ of photons per sec}}{\#\text{ of electrons per sec}} = \frac{P_o / h\nu}{I / e} \approx \frac{eP_o}{E_g I}$$



Output power vs. Forward current (P-I$_F$)

3) Differential external quantum efficiency

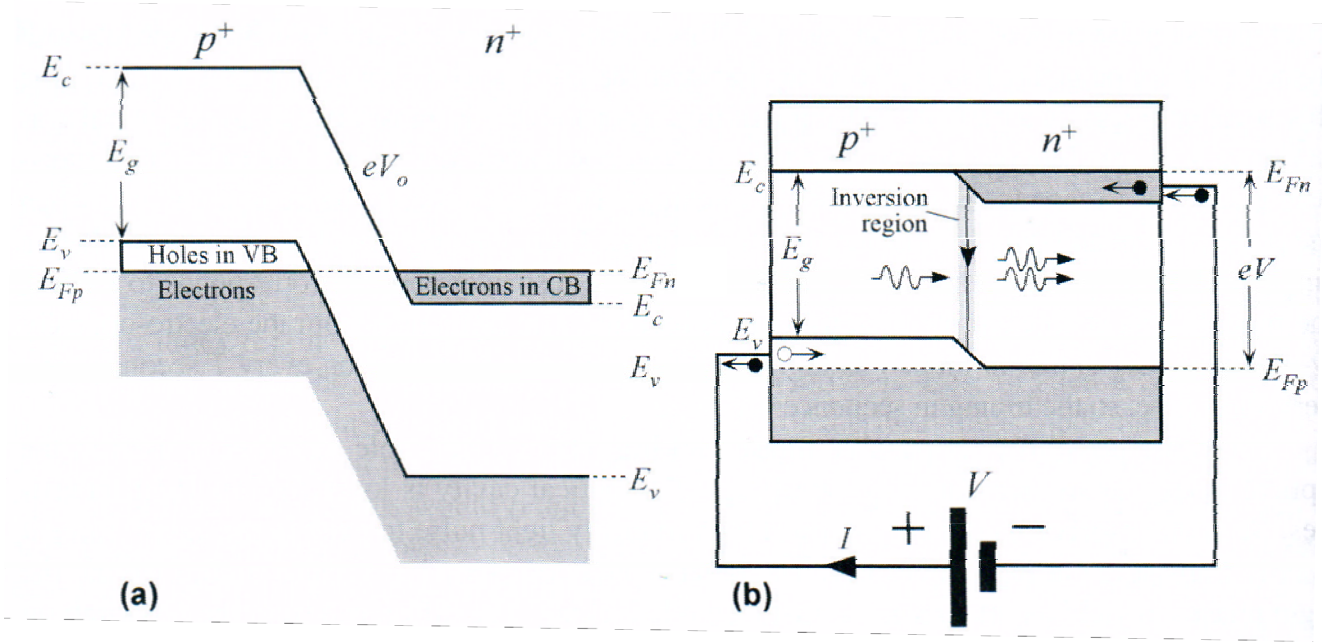
$$\eta_{\text{EDQE}} = \frac{\Delta P_o / h\nu}{\Delta I / e} = \eta_{slope} \frac{e}{h\nu} \approx \left(\frac{e_o}{E_g} \right) \frac{P_o}{I - I_{th}}$$

4) Power conversion efficiency

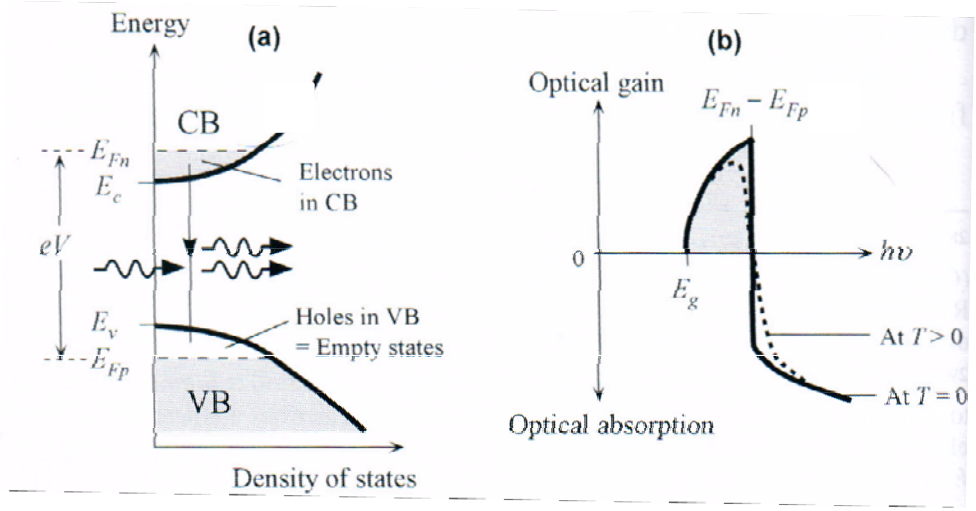
$$\eta_{\text{PCE}} = \frac{\text{Optical output power}}{\text{Electrical input power}} = \frac{P_o}{IV} \approx \eta_{\text{EQE}} \left(\frac{\text{E}_\text{g}}{eV} \right)$$

Laser Diode Principle – (1)

- **Forward bias in PN junction ($eV > E_g$)**
  - **Population inversion**
  - **# of electrons near E_c > # of electrons near E_v**

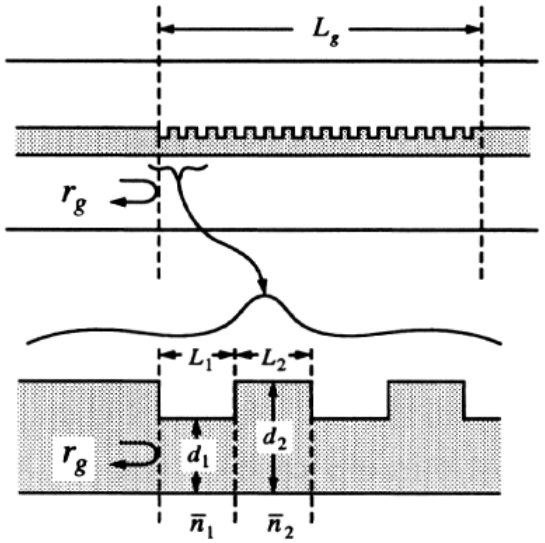


Laser Diode Principle – (2)



- **Dependency on photon energy**
  - $E_g < h\nu < E_{Fn} - E_{Fp}$ **: photon emission**
  - $h\nu > E_{Fn} - E_{Fp}$ **: photon absorption**

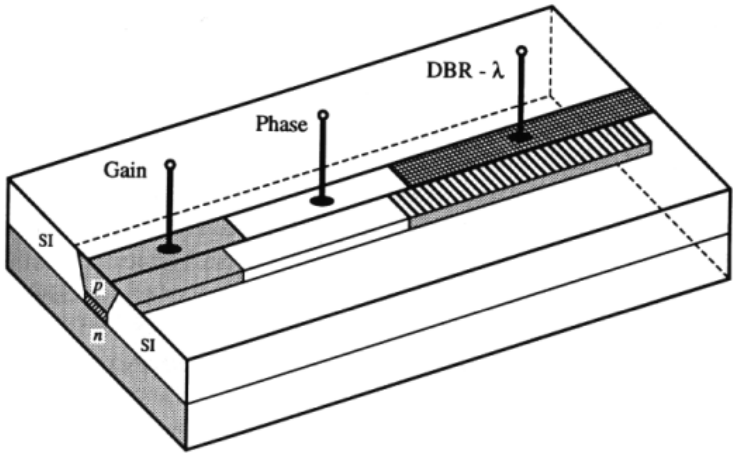
Distributed Bragg Reflector Mirror



DBR mirror structure

- **Frequency selection**
  - **$L_1 + L_2 = \lambda / 2$: Constructive interference**

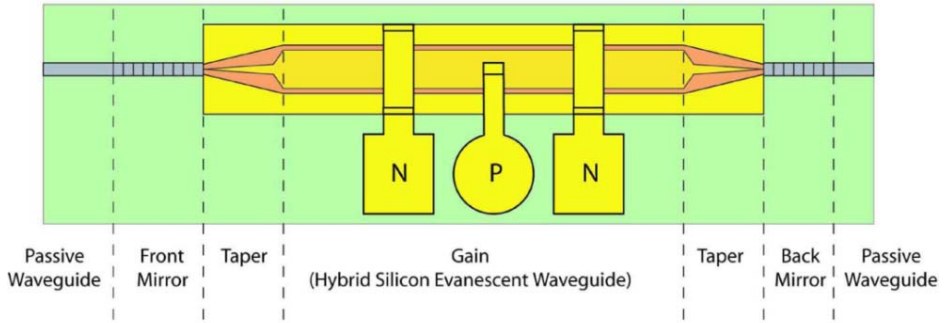
DBR Laser – (1)

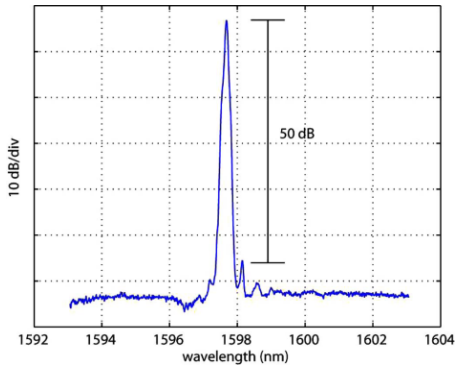


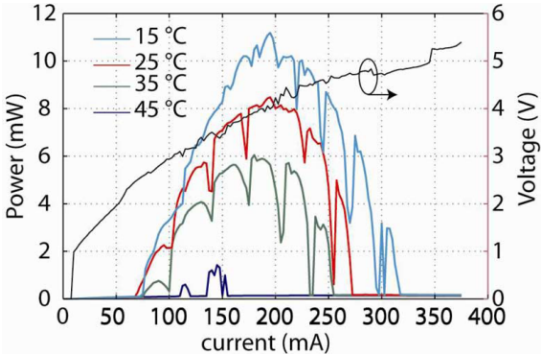
DBR laser structure

- **Three sections**
  - **Gain (active) : light generation**
  - **Phase : independent mode phase control**
  - **DBR – λ : mode selective filter**

DBR Laser – (2)



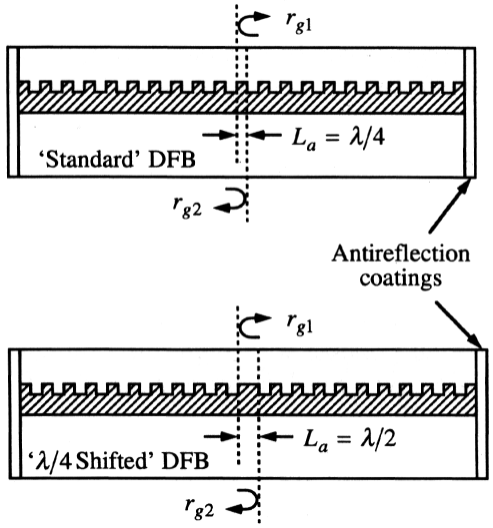




- **Two passive DBR mirrors**
  - **Back mirror : 97 %**
  - **Front mirror : 44%**

[Intel Fang 2009]

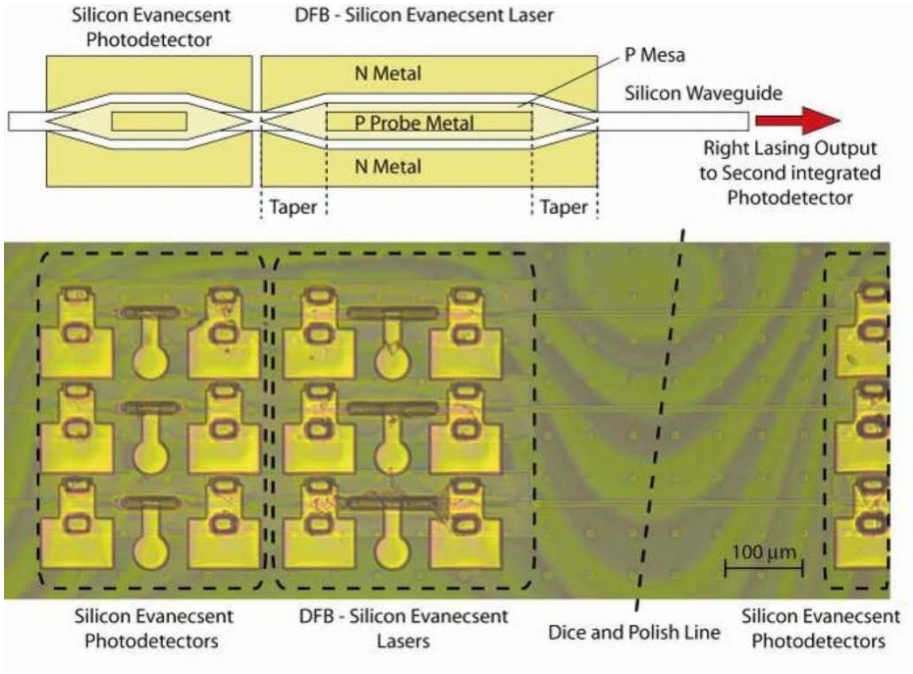
DFB Laser – (1)

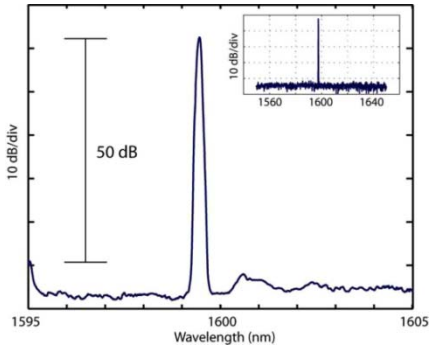


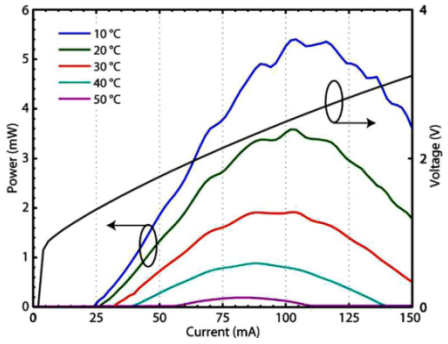
DFB laser structure

- Grating is included in the gain region
- Two types
  - Standard DFB: symmetric two modes around Bragg frequency
  - 'λ/4 Shifted' DFB: suppress one mode

DFB Laser – (2)



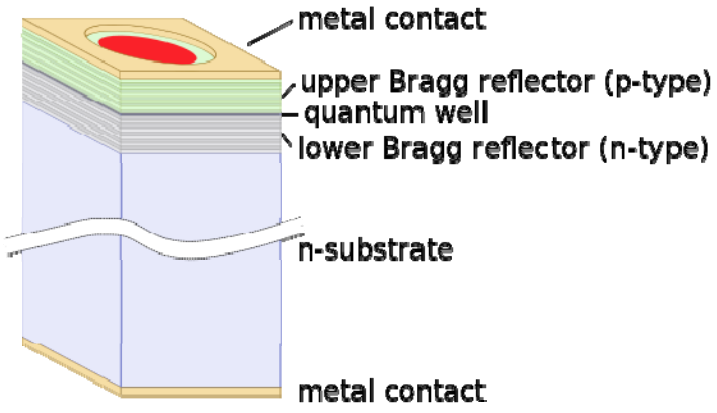




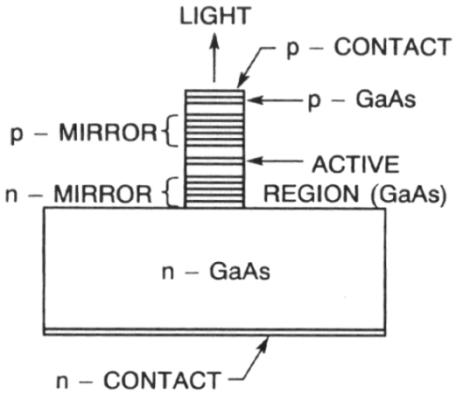
[Intel Fang 2009]

- **λ/4 Shifted**
- **Integrated PD for on-chip test**

VCSEL



VCSEL structure

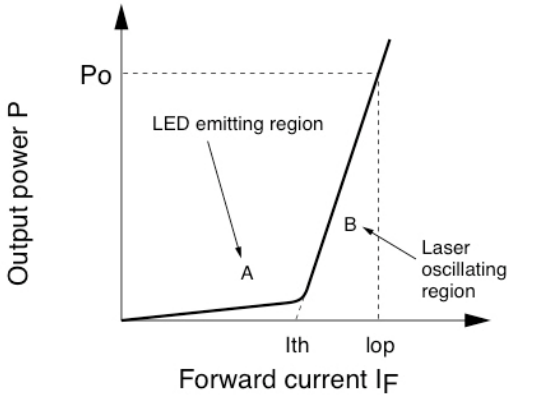


Mesa etched VCSEL

- **Pros**
  - **Small footprint**
  - **Easy to test**
  - **Narrow and circular beam output**

Commercial VCSEL

- **Oclaro**
  - **20Gbps**
  - **λ= 850nm**
  - **R_{diff} = 70 Ω**
  - **C = 200 fF**



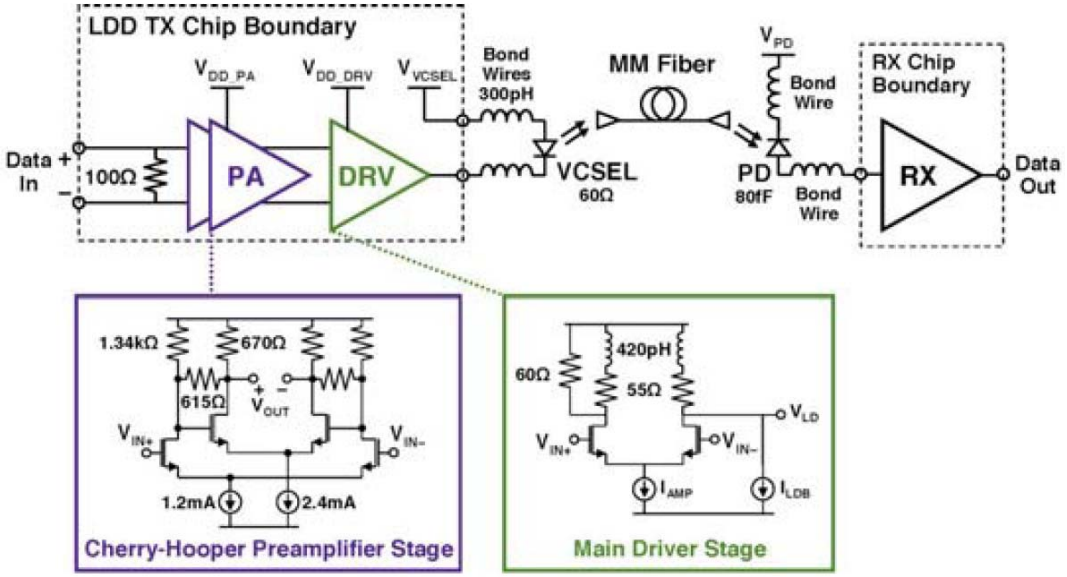
Output power vs. Forward current (P-IF)

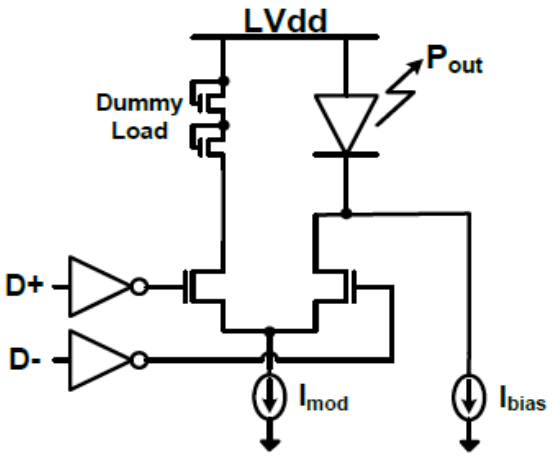
Electro – Optical Characteristics*

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Threshold current	I_{th}				1.0	mA
Operating current	I_{op}			6.0		mA
Slope efficiency	η	$I=I_{th}+1mA$	0.3	0.5	0.8	mW/mA
Optical output power	P_{out}	$I=I_{op}$		2.5		mW
Operating voltage	U_{op}	$I=I_{op}$		2.0		V
Differential resistance	R_d	$I=I_{op}$		70		Ω
Emission wavelength	λ	$I=I_{op}$, T=0°C - 85°C	830	850	860	nm
Capacitance	C			0.2		pF
Modulation bandwidth	f_{3dB}	$I=I_{op}$	14	16		GHz

VCSEL Driver

- **25Gb/s in 90nm CMOS**





ISSCC 2012, IBM

Silicon Optical Modulator

- **Light intensity modulator**
  - Electro-optic effect (EO)
  - Acousto-optic effect (AO)
  - Thermo-optic effect (TO)
  - Opto-optic effect (OO)

- **When an electrical signal changes…**
  - Real part of RI : Electrorefraction (Δn)
  - Imaginary part of RI : Electroabsortion ($\Delta \alpha$)

- **Electro-optic effect**
  - $\Delta n = a_1 F$: Pockels effect (linear EO effect)
  - $\Delta n = a_2 F^2$: Kerr effect (2nd-order EO effect)
  - Franz-Keldysh effect : strong E-field

[Source : Intel 40Gbps Silicon Modulator]

Key Parameters of Si Modulator

1) Modulation Depth (MD)

$$\eta_m = \frac{I_{0,max} - I_{0,min}}{I_{0,max}}$$

→ Digital modulation (Switch) : $\eta_m = 1$

→ Analog modulation : $\eta_m < 1$

2) Modulation Bandwidth (MB)

highest frequency at which the MD falls to 50%

3) Insertion Loss

$$L_i = 10\ log\ (\frac{I_t}{I_0})$$

(I_t : no modulator, I_0 : no signal)

4) Power Consumption

Driver power per unit bandwidth (mW/MHz)

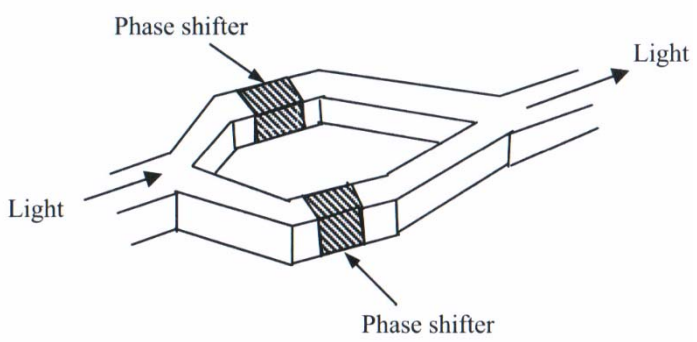
5) Isolation

$$Isolation\ (dB) = 10\ log(\frac{I_2}{I_1})$$

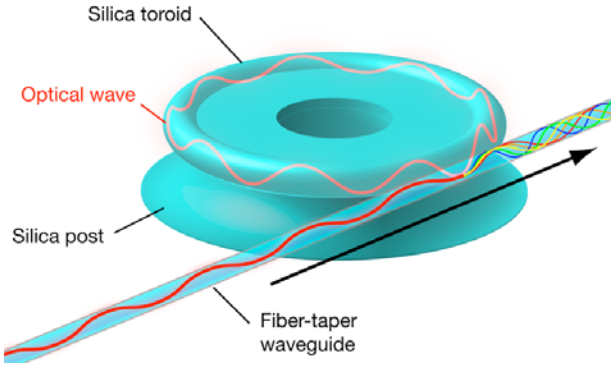
(I_1 : driving point, I_2 : driven point)

Types of Optical Structures

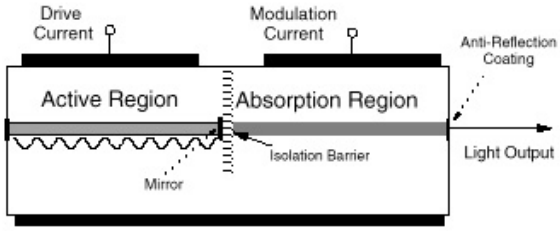
- **Interferometer-based modulator**
  - **Mach-Zehnder interferometer (MZI)**
    : Simple, but large area & lower BW comparing w/ ring-type



- **Resonator-based modulator**
  - **Fabry-Perot resonators : plane parallel mirrors**
  - **Ring resonators**
  - **Bragg gratings**
  - **Photonic band gap mirrors**



- **Electro-absortion modulator (EAM)**
  - **Integrated on Distributed Feedback Lasers (DFL)**



The Characteristics of Modulators

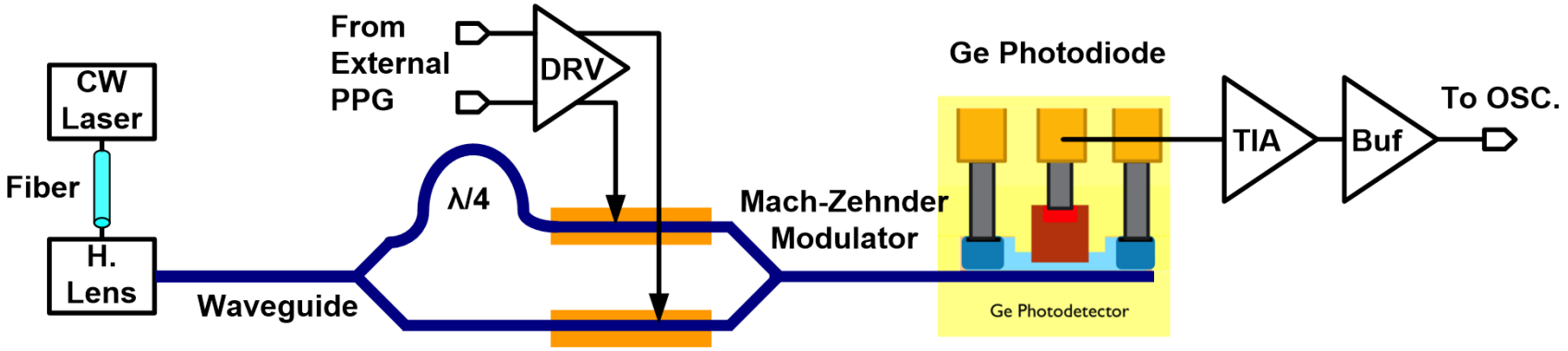
- **[Table] All silicon electro-optic modulators reported until 2007**

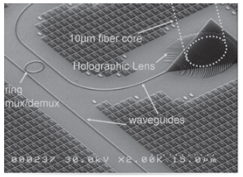
Year	Author	Electrical	Optical	M (%)	J (kA/cm^2)	Power (mW)	t_s (ns)	Length (μm)	D/P
1991	Treyz *et al.*	p^+–p(i)–n	FCAM	75	3.0	—	50	500	D
1991	Treyz *et al.*	p–i–n	MZ	65	1.6	—	<50	500	D
1991	Xiao *et al.*	p–i–n	FP	10	6.0	—	25	v.d.	D
1994	Liu *et al.*	p–i–n	*y*-switch	>90	9.0	—	200	800	D
1994	Liu *et al.*	p–i–n	TIR switch	>90	12.5	—	100	200	D
1995	Tang *et al.*	p–i–n	FCAM		0.175		20 MHz		D
1995	Zhao *et al.*	p–i–n	MZ	98	—	—	200	816	D
1995	Liu *et al.*	p–i–n	FP	80	—	—	—	20.9	P
1996	Zhao *et al.*	p–i–n	ZGDC	97.2	1.027	123.7	210	1103	D
1997	Cutolo *et al.*	p–i–n	Bragg reflector	50	—	4	24.7	3200	P
1997	Cutolo	BMFET	FCAM	20	2.3	126	6	1000	P
2000	Irace *et al.*	BMFET	*y*-junction	92	—	~350	16	5000	D
2003	Sciuto *et al.*	BMFET	FCAM	75	—	160	—	400	D
2003	Barrios *et al.*	p–i–n	FP	80	0.116	0.025	21	20	P
2003	Barrios *et al.*	p–i–n	FP	80	0.61	0.014	1.3	10	P
2003	Irace *et al.*	p–i–n	BG				1.4 GHz	3000	D
2004	Barrios *et al.*	p–i–n	FP/BR	53		20 mW	—	20	D
2004	Liu *et al., Nature* 427,615,04	MOS	MZ				1.4 GHz	2.500	D
2005	Liao *et al., Opt Exp.* 13,3129 2005	MOS	MZ				10 GHz	3450	D
	Liao *et al.*	MOS	MZ				40		D
2006	Xu *et al. Opt Exp.* 2007	Pin	Ring	100%			12.5 gGb/s	~ few μm ϕ	D
2007	Liu	MOS	MZ			613			D
2007	Green *et al.*	p–i–n	MZ			287 μW	10 Gb/s	200 μm	D
2007	Green *et al.*		Ring						D
2008	Liu *et al.*	p–n	MZ	15 dB			30 Gb/s	1 mm	D

BMFET: bipolar mode field-effect transistor; FCAM: free carrier absorption modulator; FP: Fabry–Perot; MOS: Metal Oxide Semiconductor; MZ: Mach Zehnder; TIR: total internal reflection; ZGDC: zero gap directional coupler; M: amplitude modulation depth; J: current density; t_s: switching time; v.d.: vertical device; D: demonstrated; and P: proposed.

Optical Modulators

- **Mach-Zehnder modulator & micro-ring modulator**

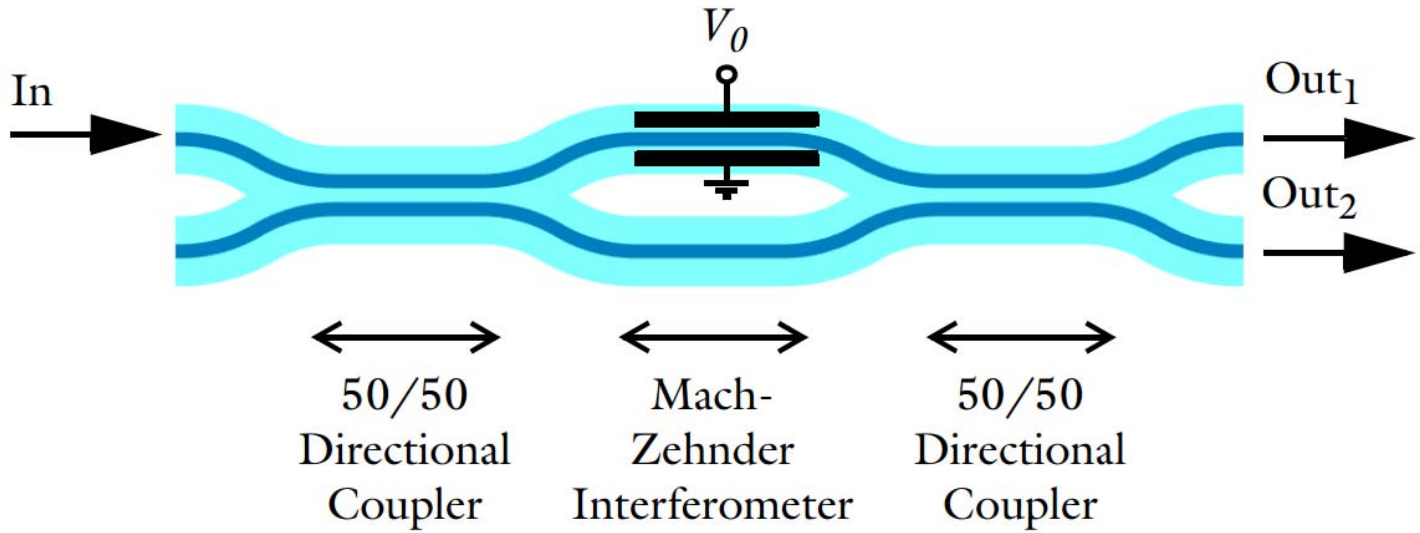




"Low-noise and high-speed TIA"

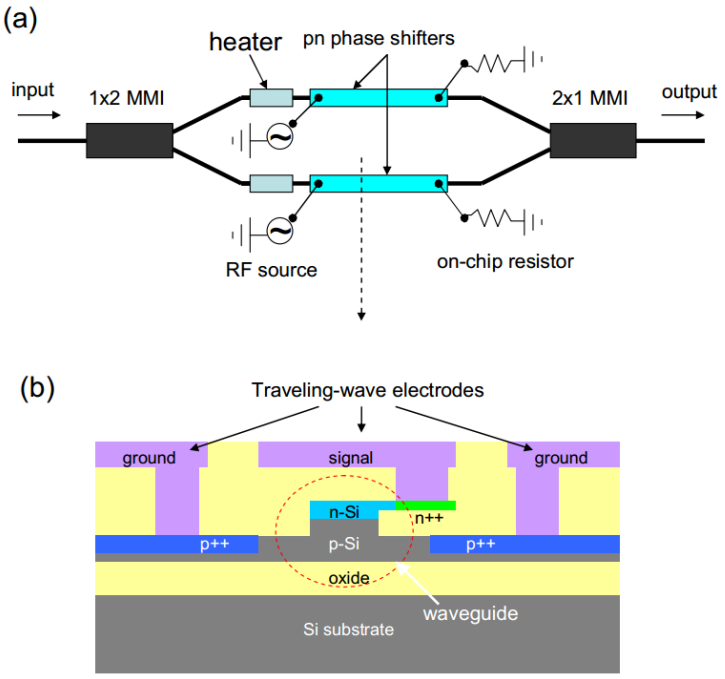
Mach-Zehnder Modulator

- V_0 generates electric field to modify the refractive index in the material
- By changing the applied voltage, the amount of light exiting from the two output waveguides can be continuously controlled

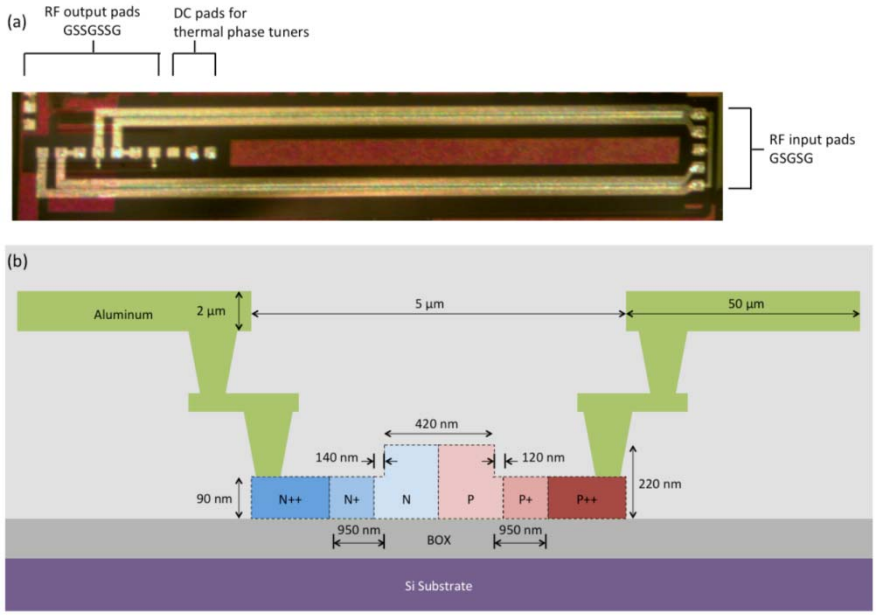


Structures of MZM

- **Vertical and lateral structure**



[Ansheng Liu et al., "Optical silicon modulator and photonic integration", Microwave photonics, pp. 295-297, 2008]



[Matthew Streshinsky et al., "Low power 50 Gb/s silicon traveling wave Mach-Zehnder modulator near 1300 nm", Optics express, pp. 30350-30357, 2013]

Commercial MZM

- **Gigoptix**
  - 40Gbps
  - λ= 1550nm
  - $V_\pi = 2\ V_{pp\text{-}single}$
  - 50Ω terminated
  - Ac-coupled input

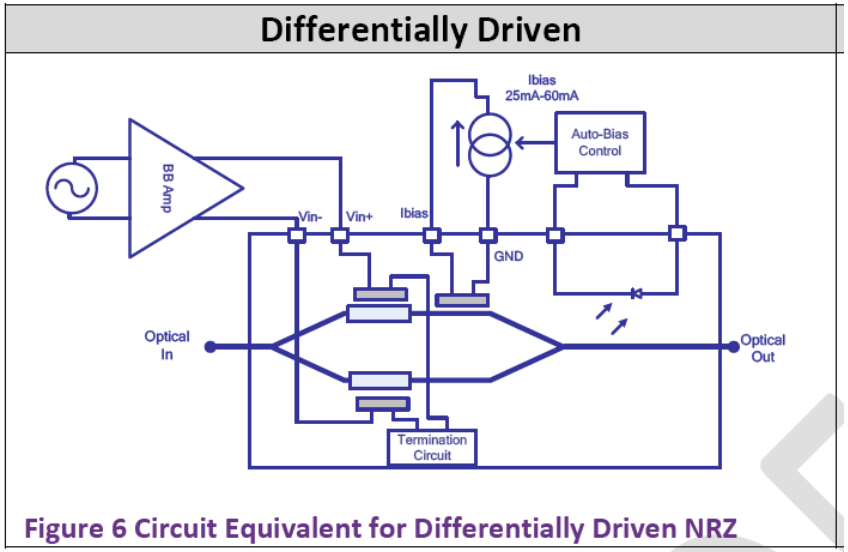
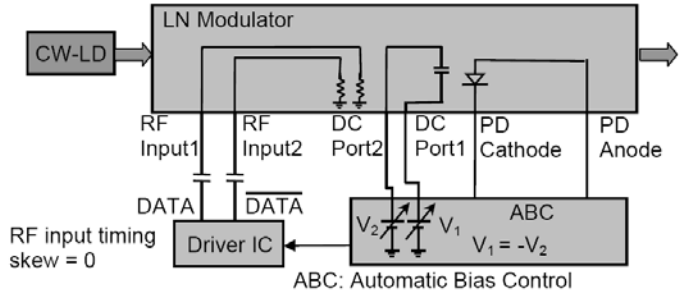
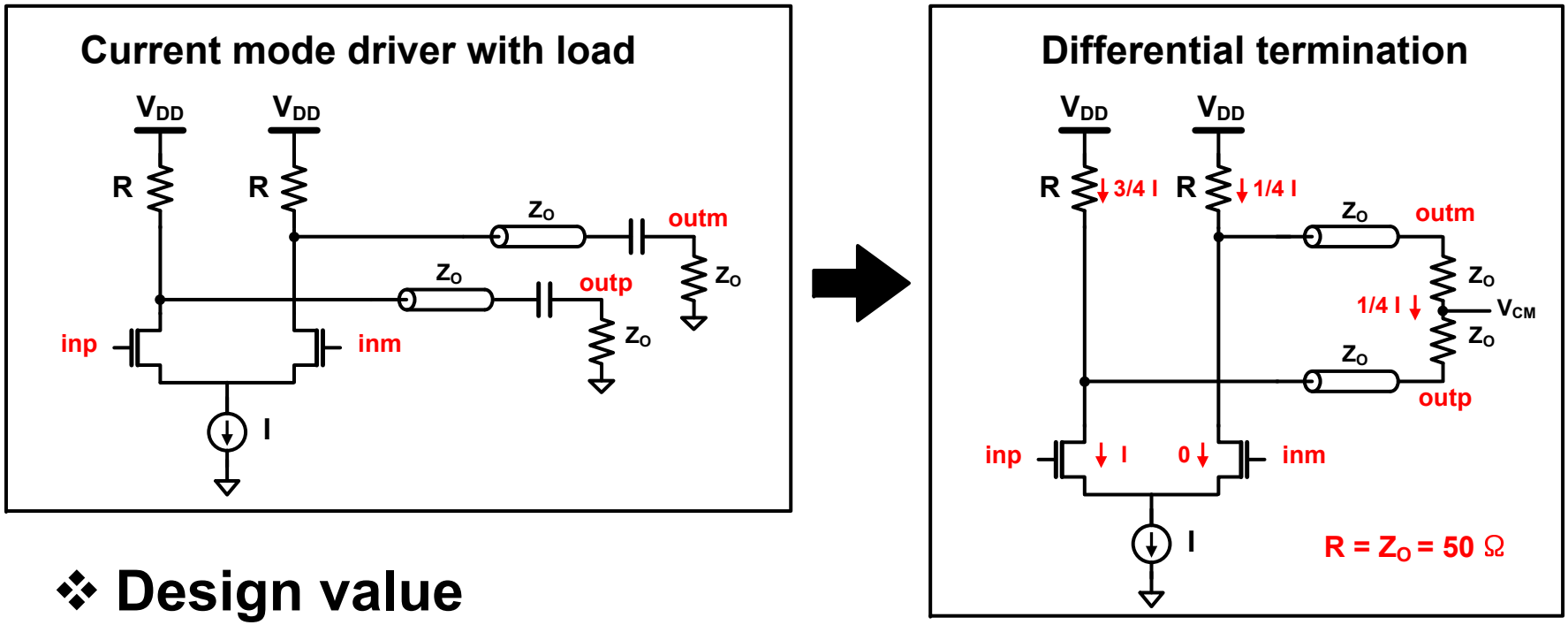


Figure 6 Circuit Equivalent for Differentially Driven NRZ

Typical Circuit for Dual-drive



MZM Driver

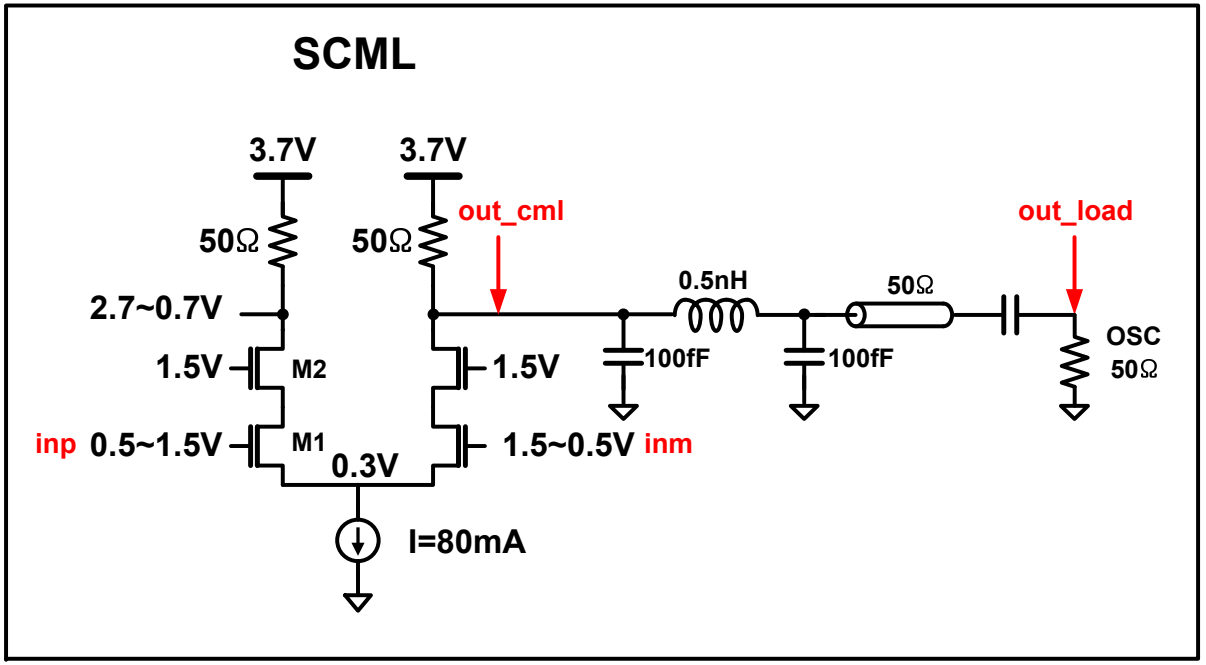


❖ Design value

- $V_{SW} = 2 \cdot 1/4\ I \cdot Z_O = 2\ V$
- $R = Z_O = 50\ \Omega \rightarrow I = 80\ mA$

MZM Driver

❖ Target
- 40Gbps
- Ac-50 Ω load
- V_{SW} = 2 V

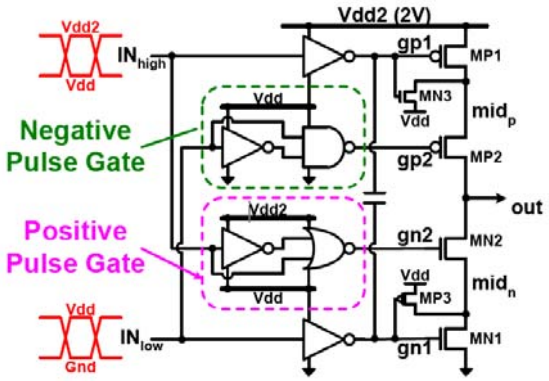
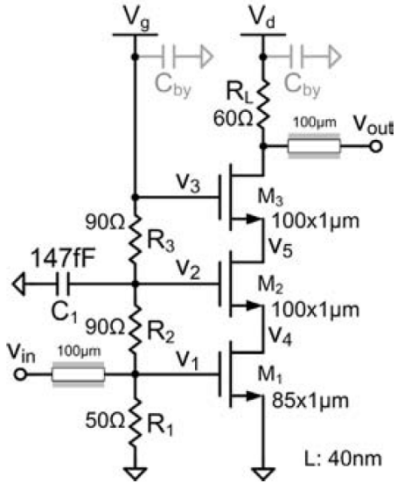
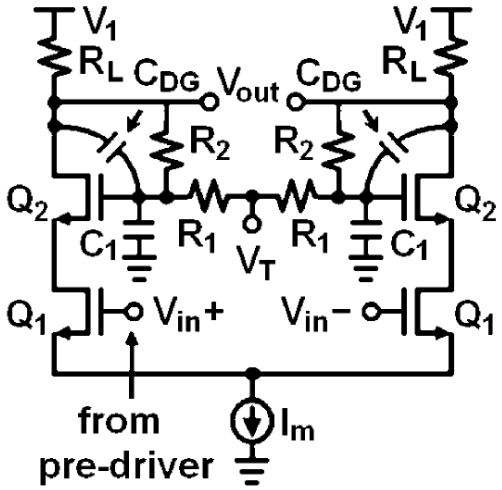


❖ Topology
- Stacked CML

• Issue
- Bonding wire as a series peaking inductor

MZM Driver Topologies

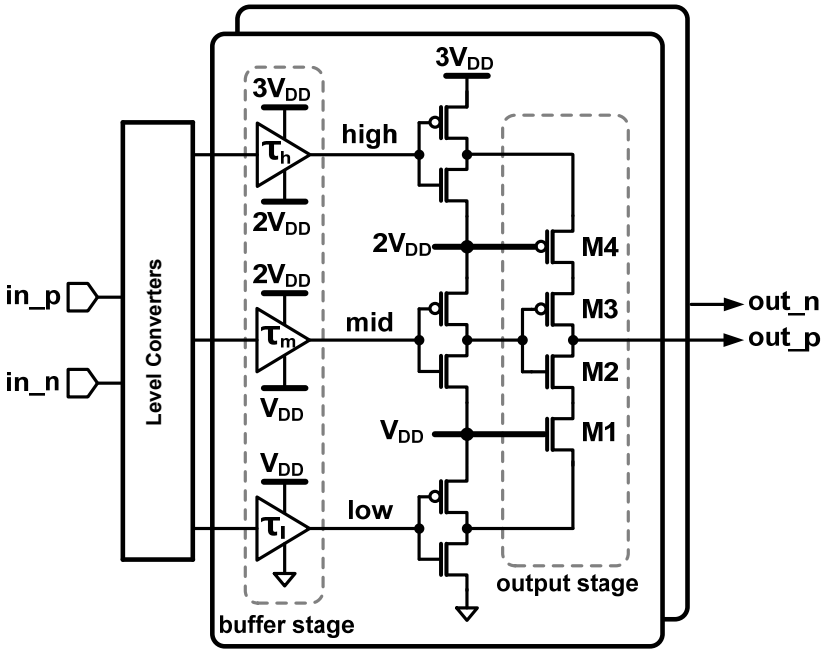
- **High output voltage swing**

Pulsed-cascode	Stacked-FET	Local FB networks
		
ESSCIRC 2006 (CMOS)	CICC 2010 (SOI-CMOS)	JSSC 2006 (CMOS)

About 2X V_{DD} swing

Stacked Drivers (1)

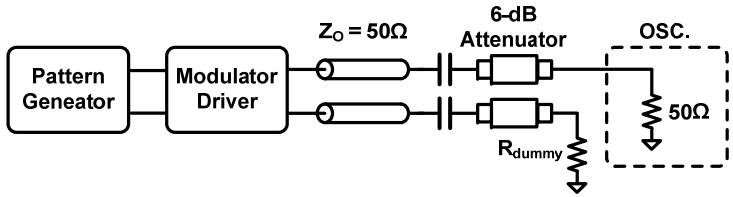
<Triple stacked-FET>



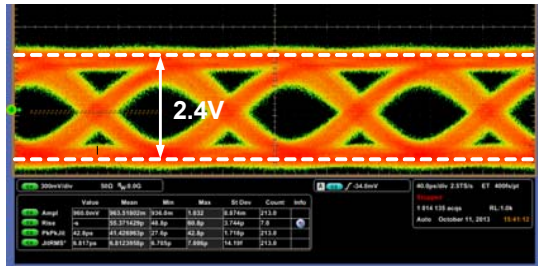
3X V_{DD} swing

[Y. Kim, ISCAS, 2014]

<Measurement setup>



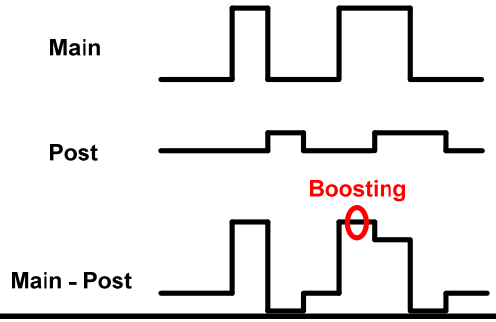
<Measurement result>



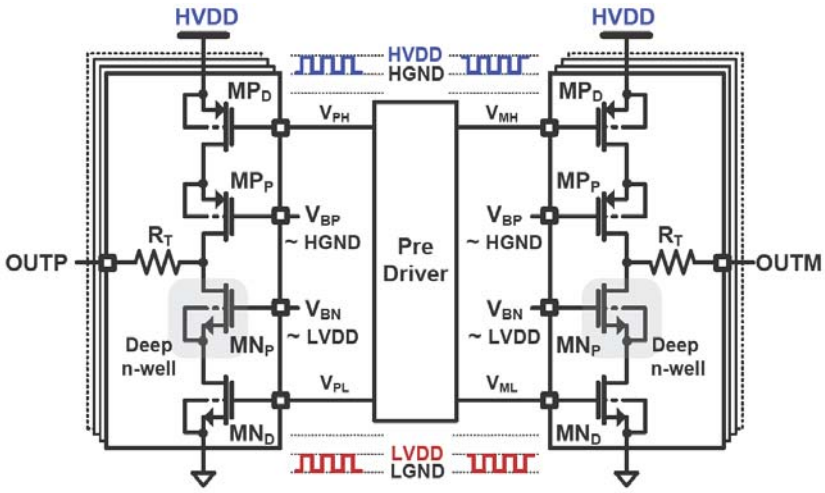
Performance summary	
Process	65-nm CMOS
Output swing	$6V_{PP\text{-}Diff}$
Speed	10 Gb/s
Power	98 mW
Area	0.04 mm^2

Stacked Drivers (2)

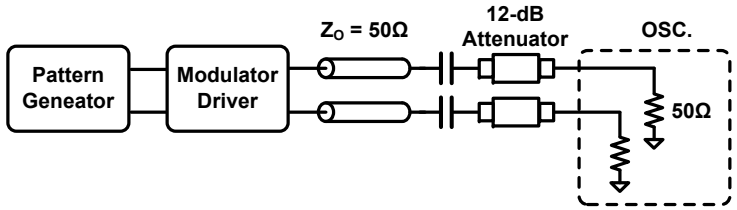
<Pre-emphasis>



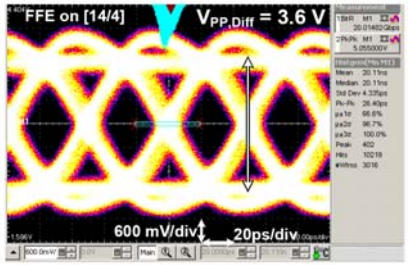
<SST driver with 2-tap FFE>



<Measurement setup>



<Measurement result>



Performance summary	
Process	65-nm CMOS
Output swing	$3.6V_{PP\text{-}Diff}$
Speed	20 Gb/s
Power	477 mW
Area	0.24 mm^2

Ring Resonator

- [Nature] Micrometre-scale silicon electro-optic modulator
- p-i-n type: high modulation depth, relatively slower than MOS
- Carrier-injection type / Carrier-depletion type

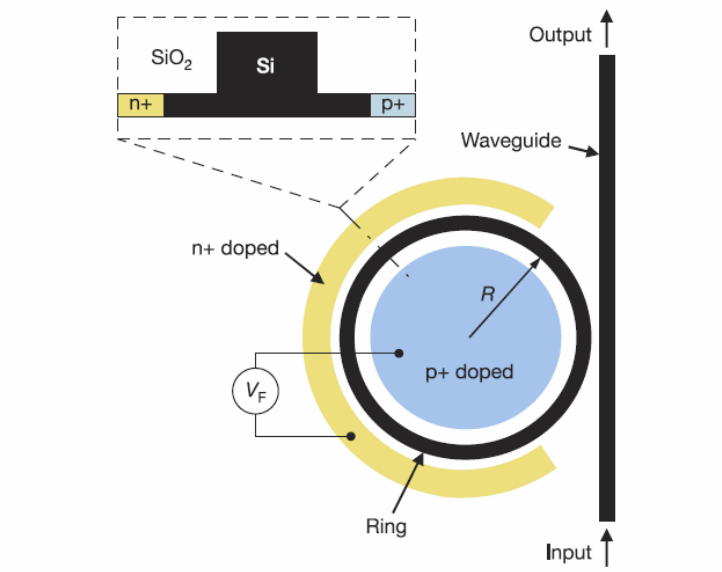


Figure 1 | Schematic layout of the ring resonator-based modulator. The inset shows the cross-section of the ring. R, radius of ring. V_F, voltage applied on the modulator.

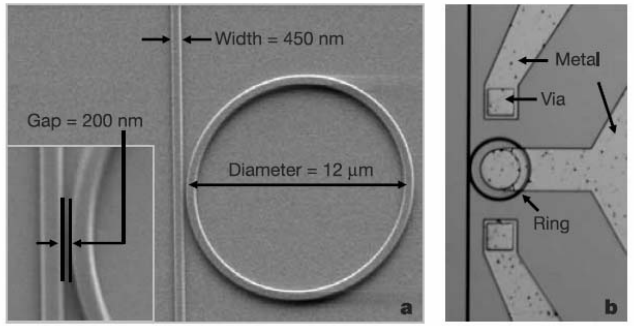


Figure 2 | SEM and microscope images of the fabricated device. a, Top-view SEM image of the ring coupled to the waveguide with a close-up view of the coupling region. **b**, Top-view microscope image of the ring resonator after the metal contacts are formed. The metal contact on the central p-doped region of the ring goes over the ring with a 1-μm-thick silicon dioxide layer between the metal and the ring.

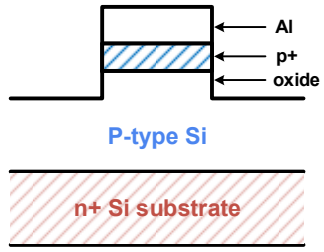
[Nature, 2005]

Characteristics of Ring Resonator

- Extremely small footprint
- Can achieve high extinction ratio (above 10 dB)
- Low modulation speed (injection type): can be enhanced by employing pre-emphasis
- Performance susceptible to fabrication tolerance and temperature
- Tuning scheme is essential for reliable operation. (especially when utilized for WDM)

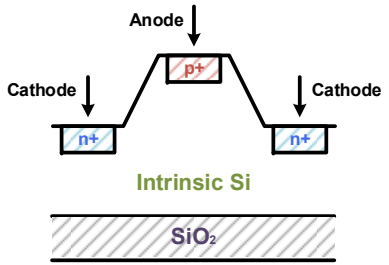
Types of Electrical Structures

- **p-i-n structures**
  - Using free-carrier absortion (forward bias)
  - High loss due to weak vertical confinement
  - Silicon-on-insulator (SOI) structures



[IEEE E.D. letter, Treyz et al., 1991]

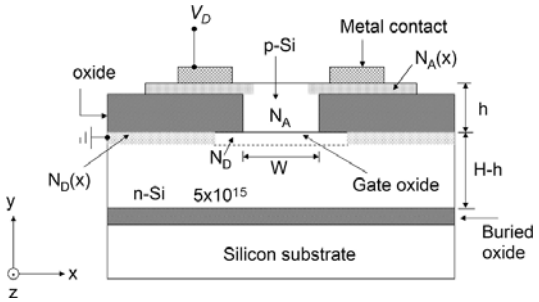
- **Three-terminal structures**
  - Substrate acted as the drain
  - Free-carrier drift is faster → shorter switching time



[IEEE E. letter, Tang et al., 1995]

- **Smaller structures**
  - High sensitivity to small changes in RI
  - Lower power consumption

- **MOS Capacitors**
  - Faster than conventional PIN modulator
  - Further improvements



[Nature, Liu et al., 2004]

Examples of Si Ring Resonator

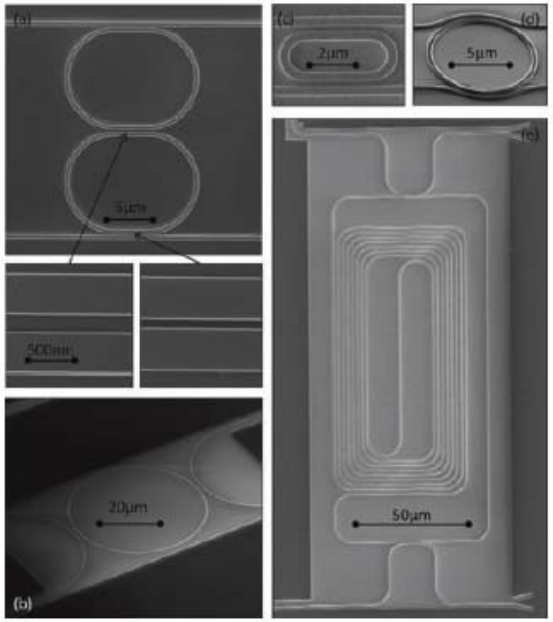


Figure 1 Examples of silicon ring resonators. (a) Double ring resonator with tuned directional coupling sections, (b) Circular ring with large coupler gaps, (c) Ultra-small racetrack ring with 1 μm bend radius, (d) ring with conformal coupling sections, (e) Large folded-spiral ring.

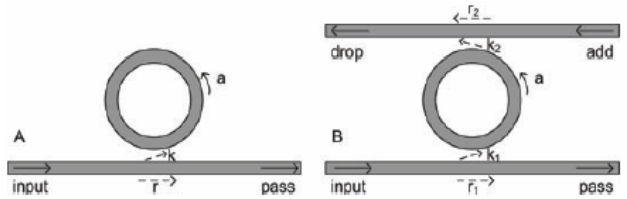
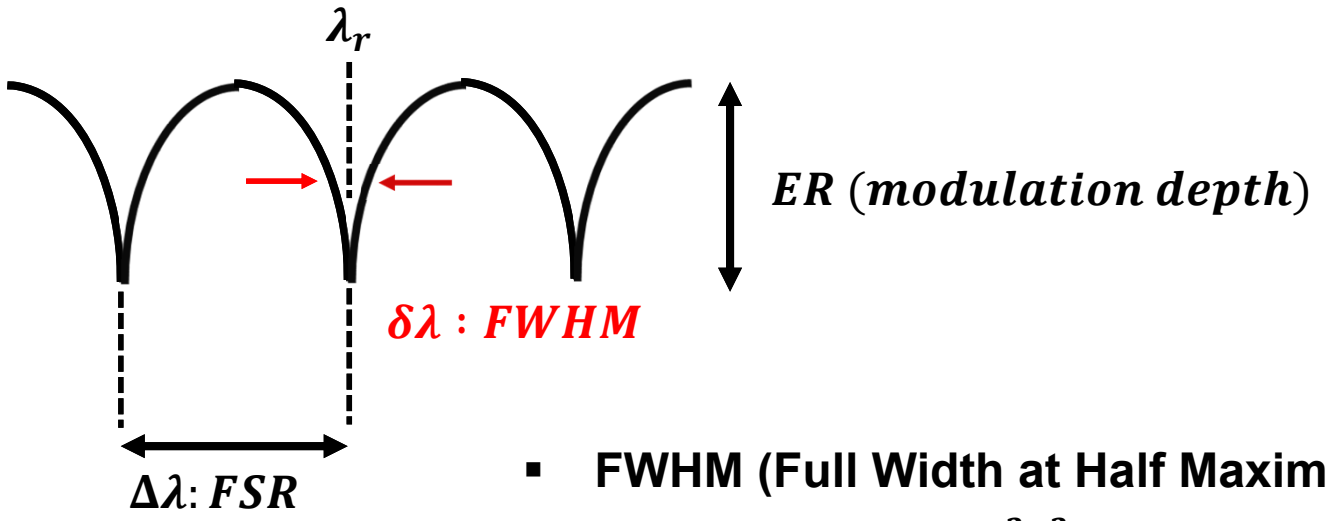


Figure 2 (A) All-pass and (B) add-drop ring resonator.

[W. Bogaerts, 2012]

Key Factors of Ring Resonator



- **Resonance wavelength**

$$\lambda_r = \frac{n_{eff}L}{m} = \frac{2\pi R n_{eff}}{m}, m = 1, 2, 3, \ldots$$

- **FSR (Free Spectral Range)**

$$\Delta\lambda = \frac{\lambda^2}{n_g L}, \qquad n_g = n_{eff} - \lambda\frac{\delta n_{eff}}{\delta\lambda}\ (Group\ Index)$$

- **FWHM (Full Width at Half Maximum)**

$$\delta\lambda = \frac{\kappa^2\lambda^2}{\pi L n_g}$$

- **Finesse (Spectral sensitivity 1)**

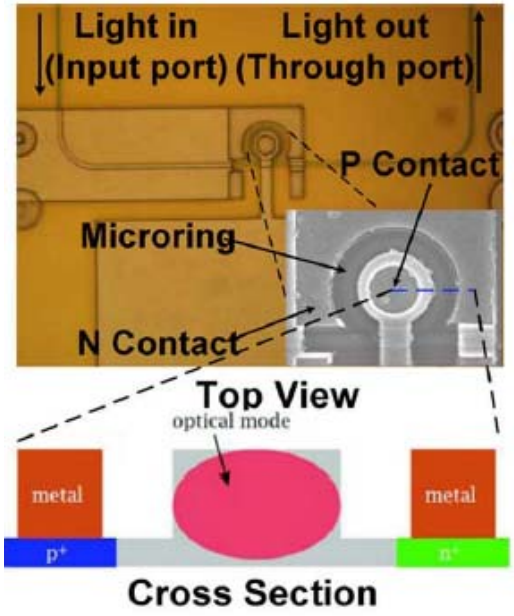
$$F = \frac{FSR}{FWHM} = \frac{\Delta\lambda}{\delta\lambda}$$

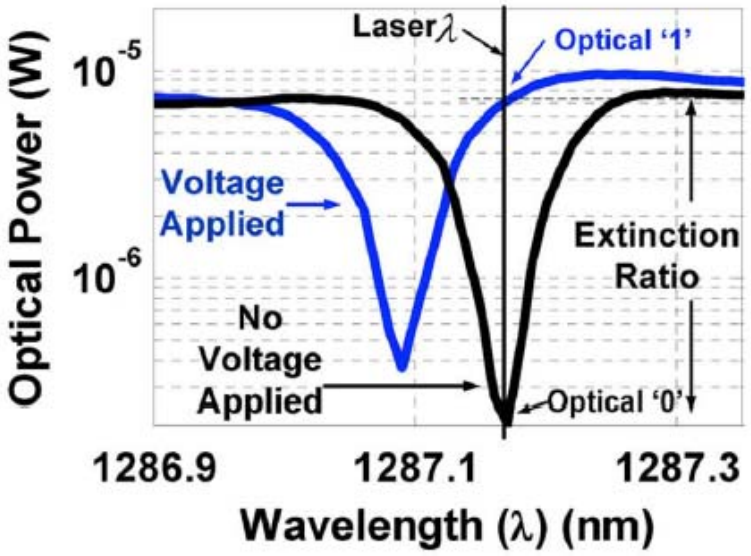
- **Q–factor (Spectral sensitivity 2)**

$$Q = \frac{\lambda}{\delta\lambda}$$

Ring Resonator: An Example

- **Condition for resonance : $2\pi r n_{eff} = m\lambda_m$**
- **At resonance wavelength, input light mostly circulates in the circular waveguide. (notch)**

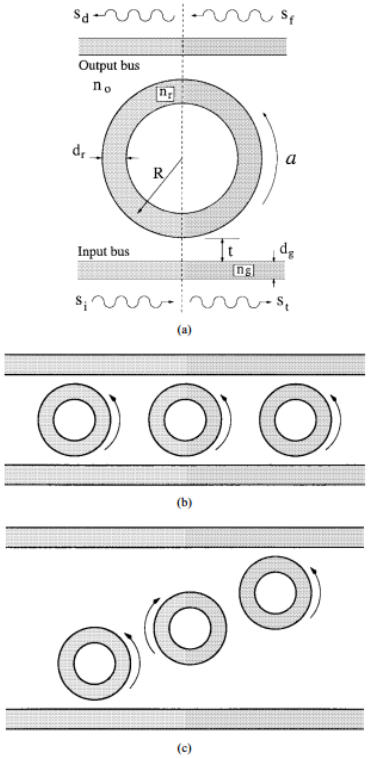


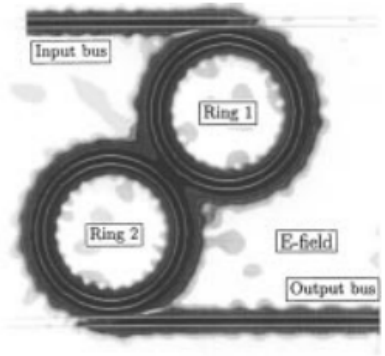


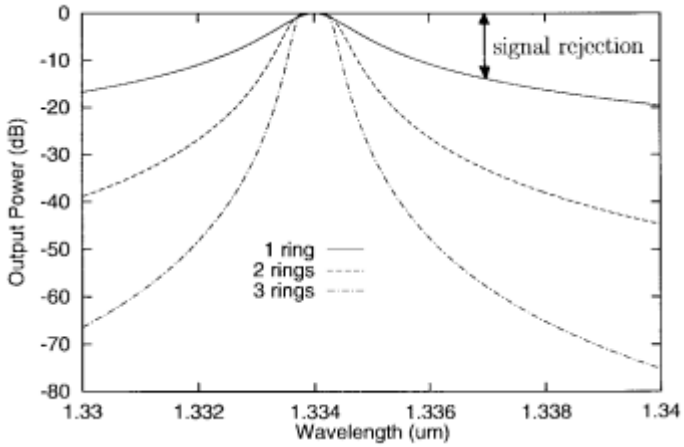
[Cheng Li, 2014]

Ring Resonator: RX WDM Drop Filter

- **Implementation of band-pass filter , MUX / DeMUX**
- **Single, cascade, or coupled rings can be utilized**



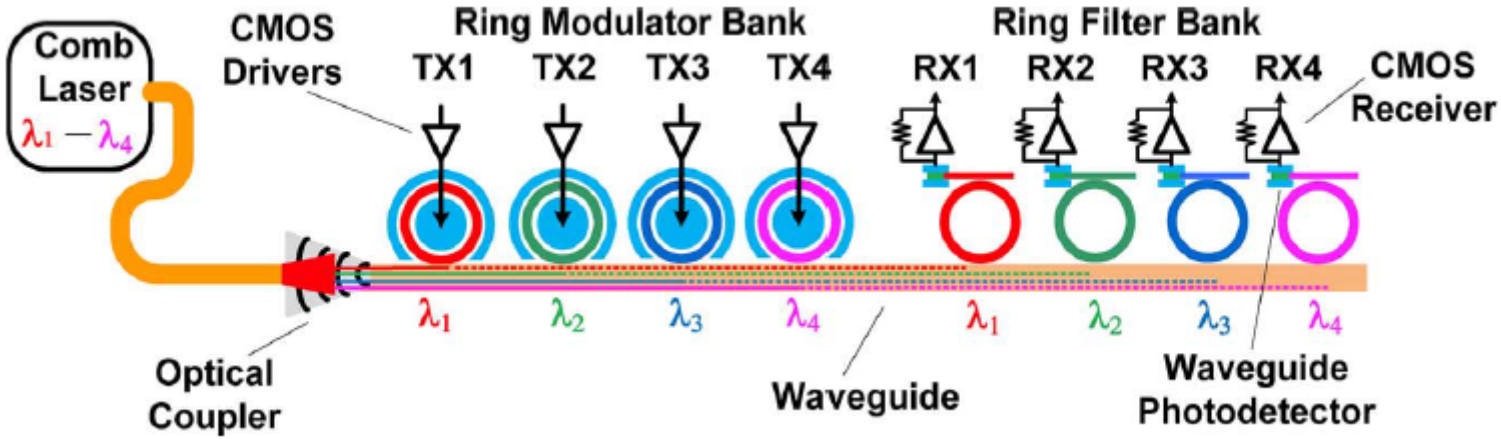




[Journal of Lightwave Technology, 1997]

Complete WDM System

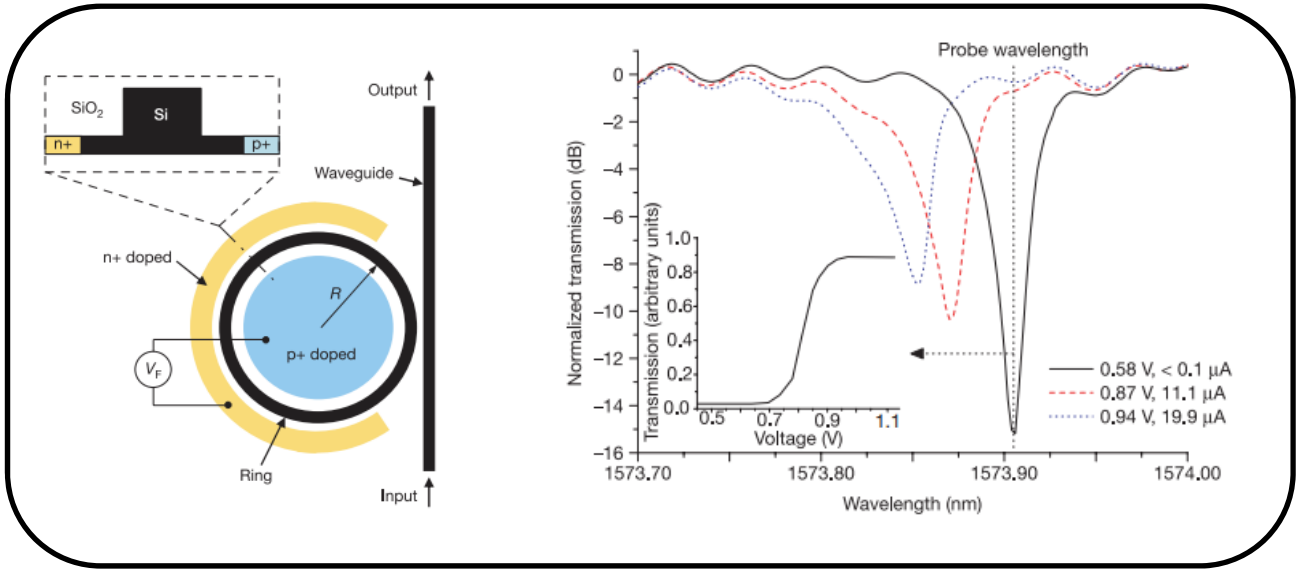
- Ring resonator as modulator at transmitter side
- Ring resonator as drop filter at receiver side
- Comb laser, more effective than DFB laser for DWDM



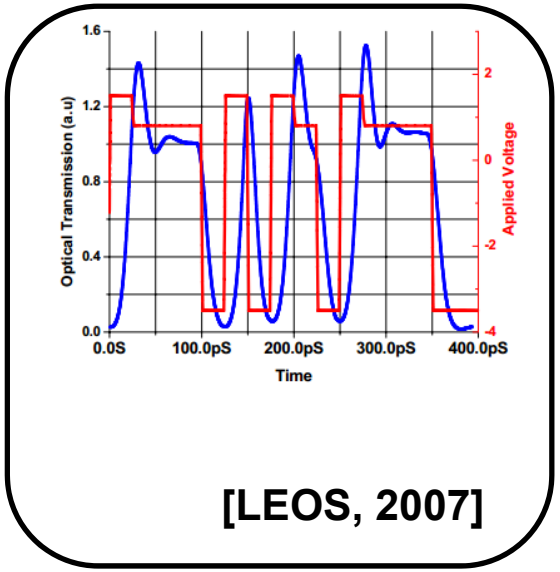
Types of p-i-n Ring Resonator

- **Carrier-injection type**
  - **High modulation depths (high ER)**
  - **Low modulation speed (long rise time)**

Modulation data rate of 18 Gb/s
Using pre-emphasis



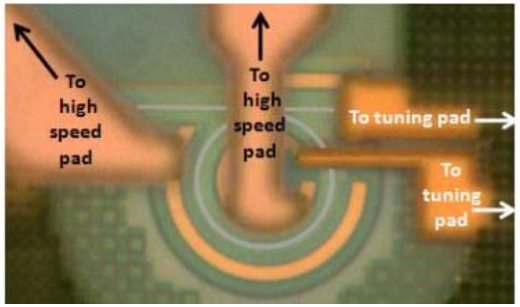
[Nature, 2005]



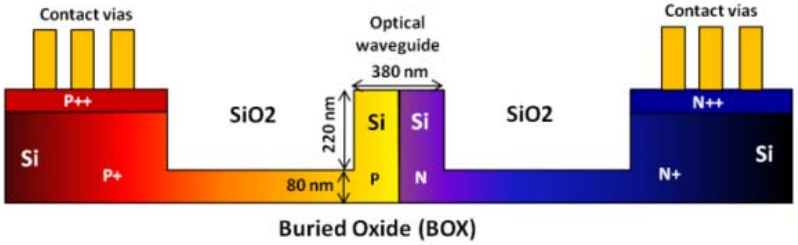
[LEOS, 2007]

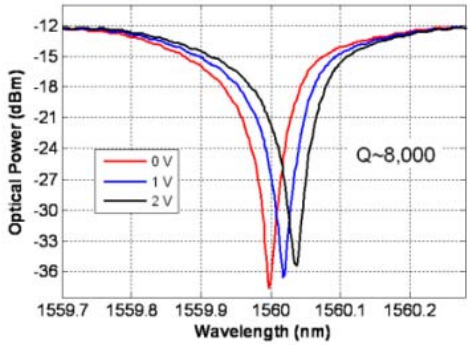
Types of p-i-n Ring Resonator

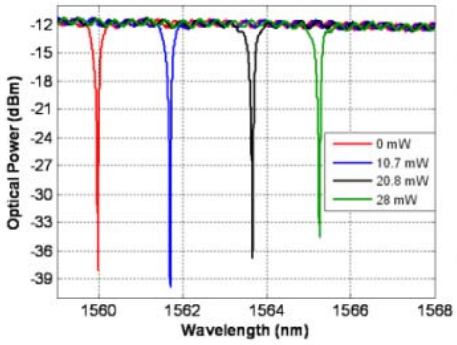
- **Carrier-depletion type**
  - **Low modulation depths**
  - **High modulation speed**

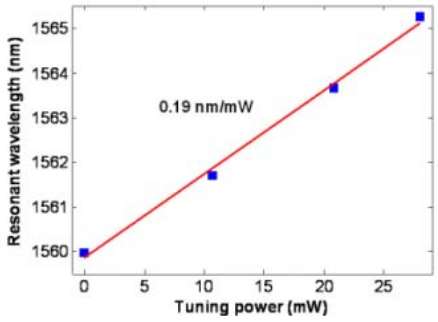


Modulation data rate of 25 Gb/s





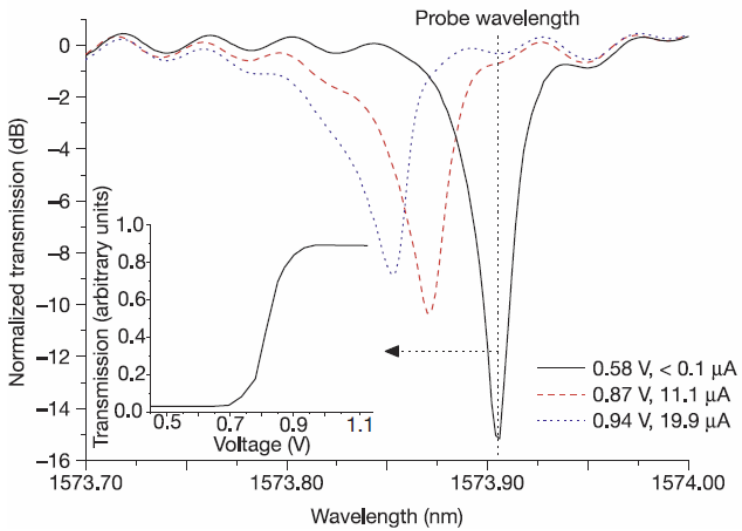




[GFP, 2011]

Design Issues (1)

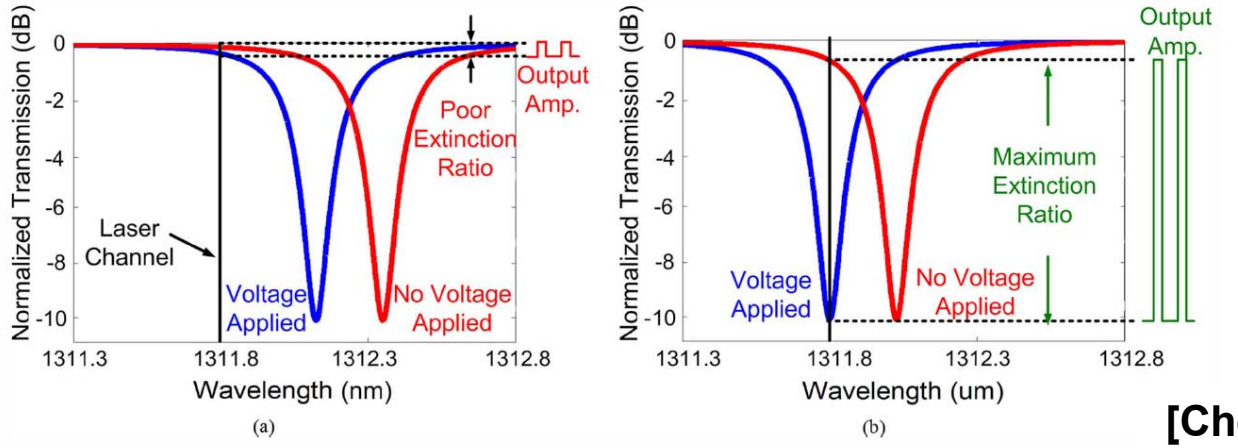
- **Reduce total optical losses**
  - **Coupling loss: between Fibre & waveguide**
  - **Propagation loss: essential to cascading (e.g. 9dB / 7.5mm)**
- **Input common-mode voltage range**
  - **Forward bias about the built-in potential of the junction**
  - **Blue shift**



[Nature, 2005]

Design Issues (2)

- **Adaptive modulation depth stabilization loop**
  - **Using bias-tuning feedback loop**
  - **Blue shift due to lowering the effective index (carrier injection)**

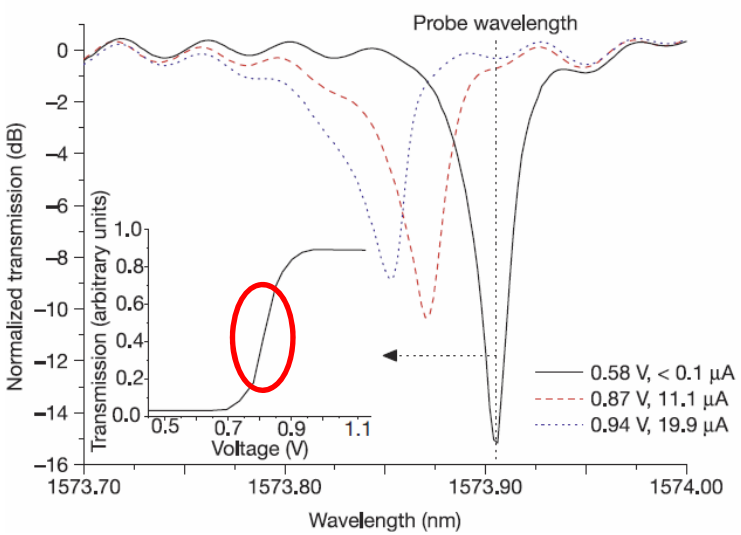


[Cheng Li, 2014]

- **Spectral sensitivity compensation (high Q-factor)**
  - **Corresponds to a cavity photon lifetime, resonant nature of the device structure (Q ~ 39350)**

Design Issues (3)

- **High-speed operation (above ~10Gb/s)**
  - **Optical rise time far less than the electrical rise time of ~10ns with high forward bias (peak-to-peak ~3.3V)**

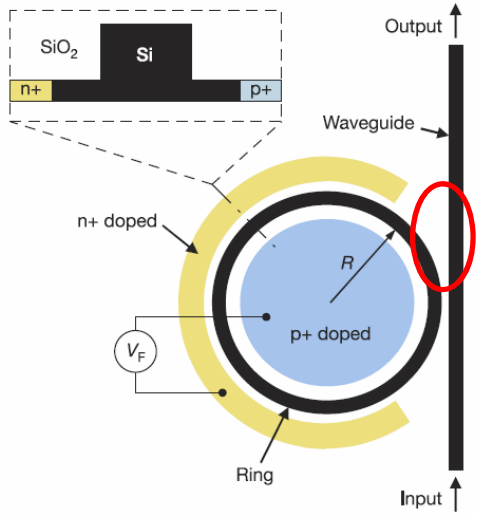


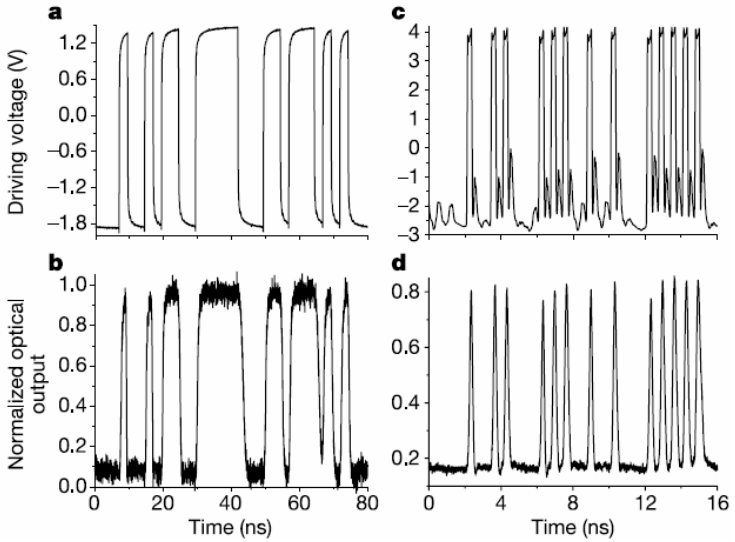
[Nature, 2005]

- **Noise consideration**
  - **Noise tolerant nature of ring resonator compared with MZI**

Design Issues (4)

- **Other high-speed modulation considerations**
  - **RZ operation : not p-i-n junction region → long fall time(~1.5ns) after long forward-biasing periods**
  - **Higher voltage swing (~6.9V) → reducing the contact resistance**
  - **Reduce the portion of non p-i-n region surface**



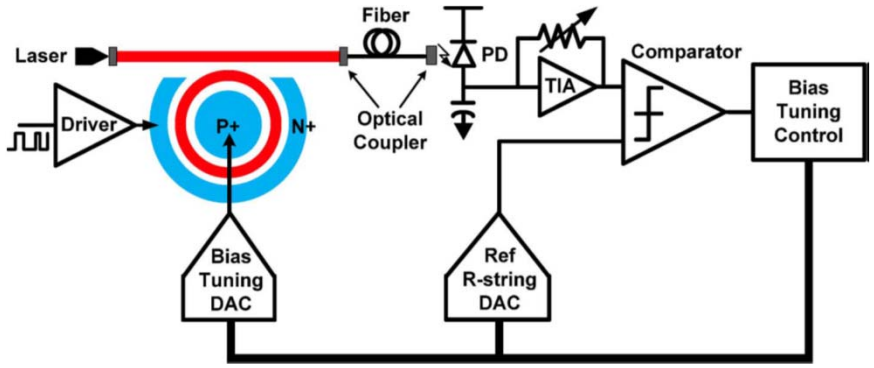


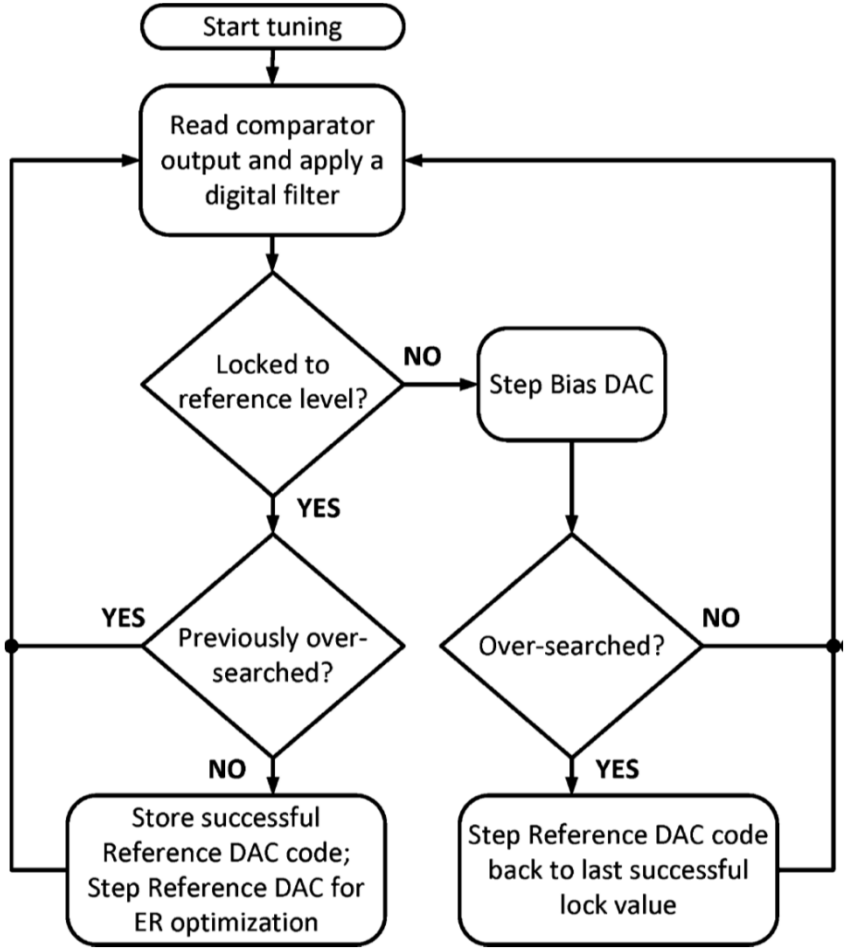
[Nature, 2005]

- **Random variation of the ring dimension**
- **Thermal tuning**

Bias Tuning Scheme

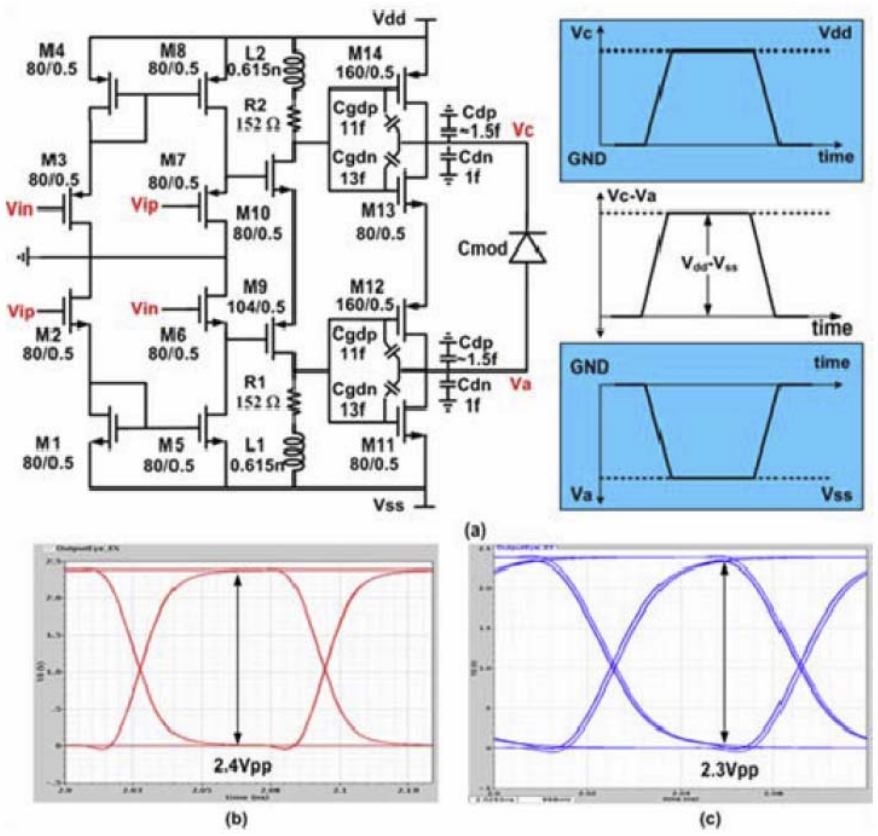
- **Semi-digital wavelength stabilization loop**





  - **Optical power measured using a monitor PD**
  - **Optimum point fined with the aid of a tuning algorithm**

25Gb/s Transmitter in 130nm SOI



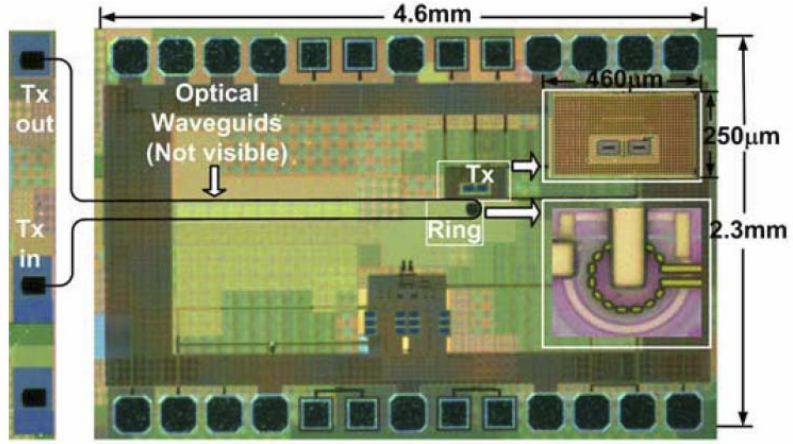


Fig. 3. A micro-photograph of the fabricated transmitter with the ring modulator and the driver circuit showing in the inset pictures.

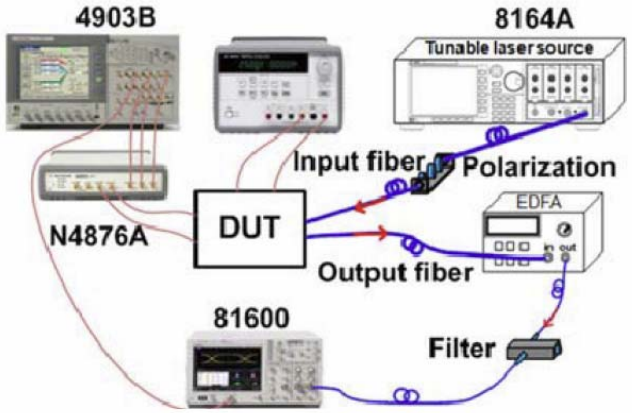


Fig. 4. Test set up for integrated 25 Gb/s transmitter.

10Gb/s Ring Modulator

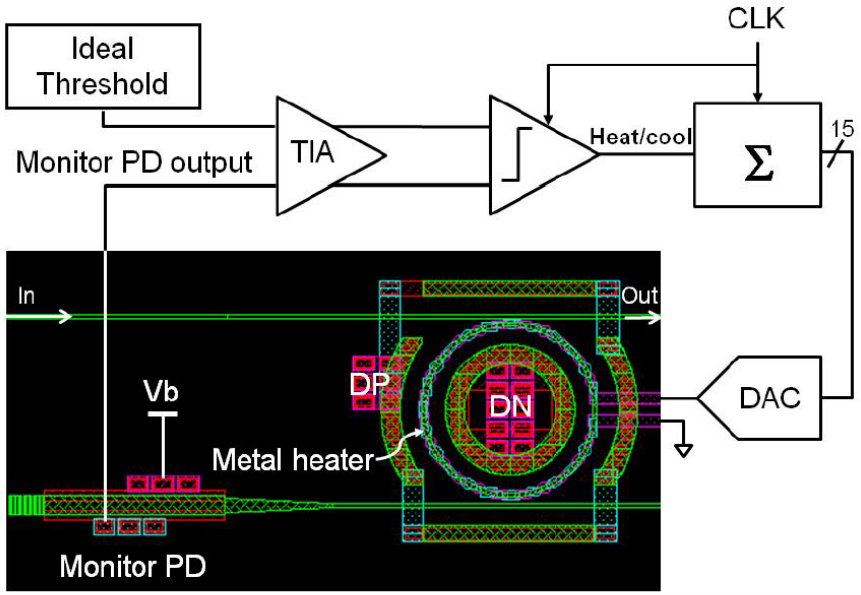
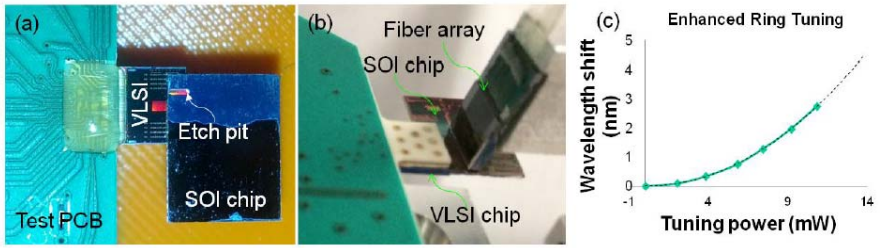
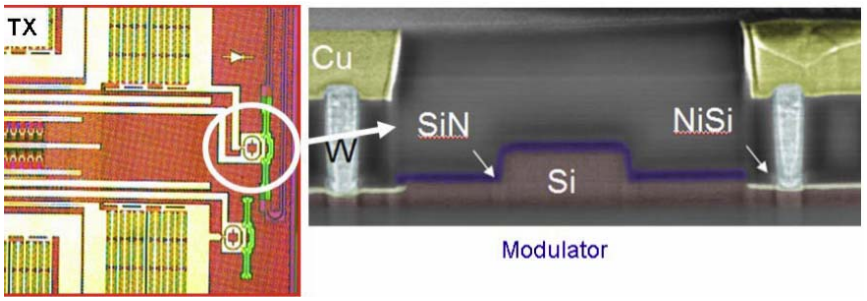


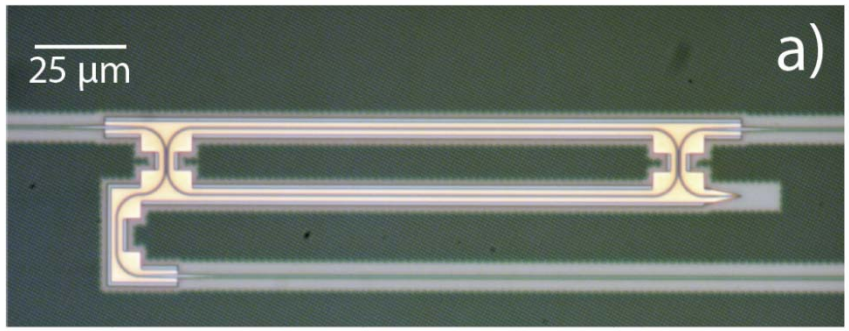
Fig. 1. A complete Si ring modulator with closed-loop wavelength control.



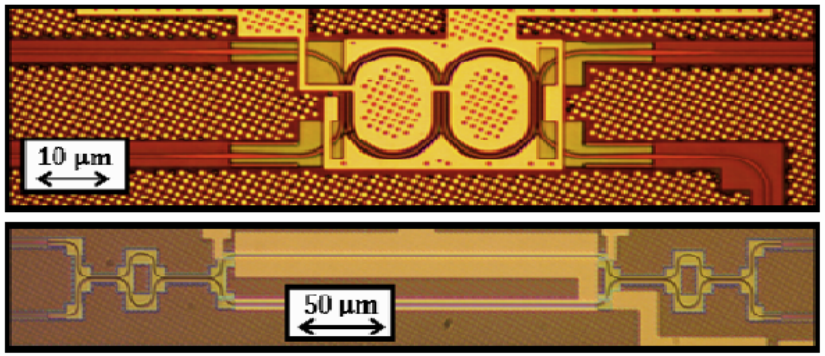
The State of the Art: IBM



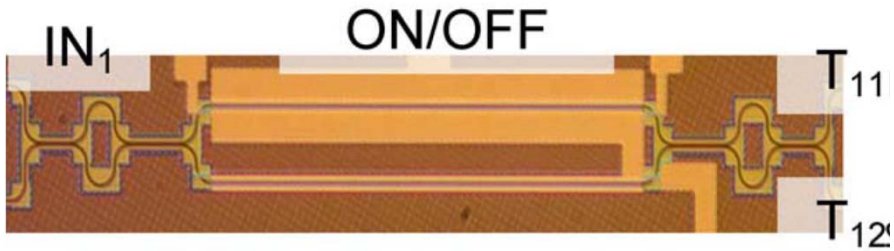
[IPC, Assefa et al., 2012]
Monolithic Integration – MZI modulator



[IPC, Rosenberg et al., 2011]
High-speed & low-power microring modulators

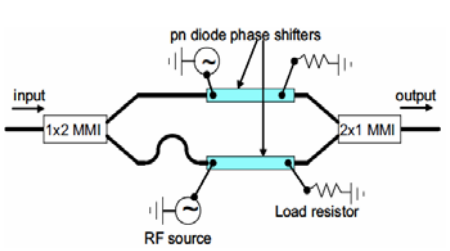


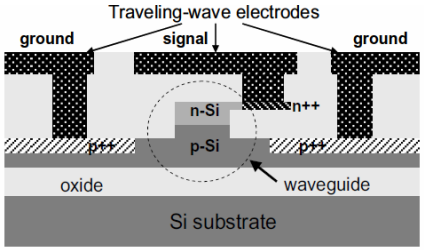
[IEEE Photonics Society, Lee et al., 2010]
Comparison ring resonator & MZI modulator

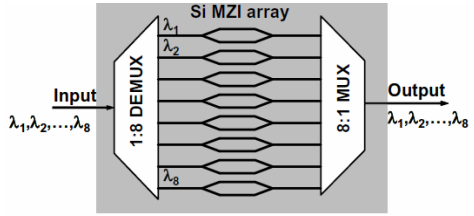


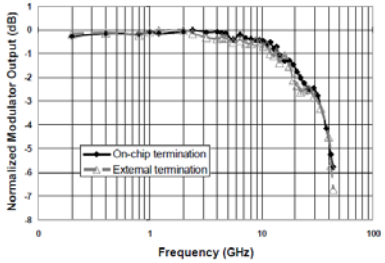
[JSSC, Rylyakov et al., 2011]
Wavelength-intensitive MZI (WIMZ) molulator

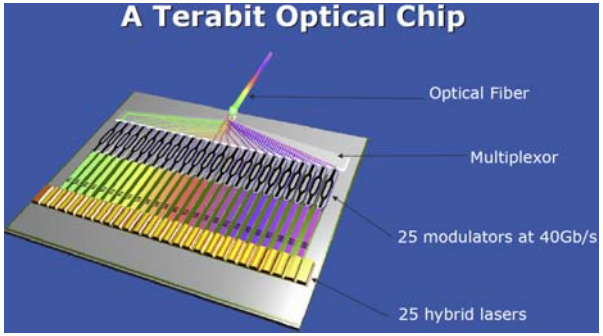
The State of the Art: Intel

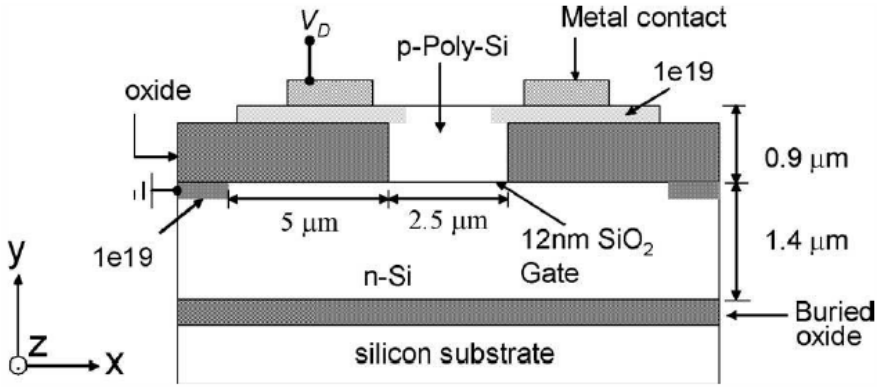


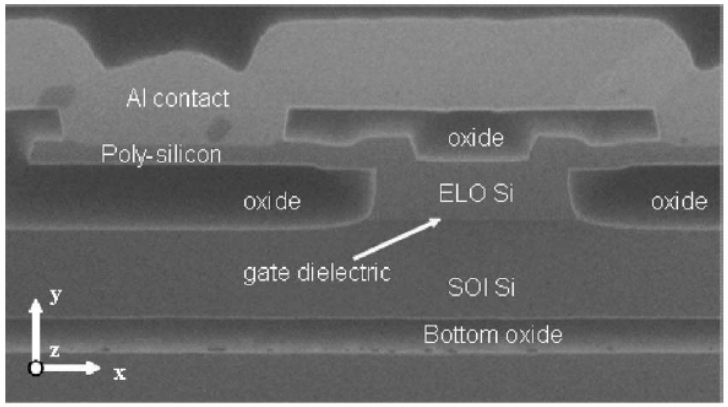












[Microwave photonics, Liu et al., 2008]
40Gbps optical silicon modulator

[IEEE JSTQE, Izhaky et al., 2006]
New type of phase shifter

References

1. Palermo, S., Horowitz, M., “High-Speed Transmitters in 90nm CMOS for High-Density Optical Interconnects,” Proceedings of the ESSCIRC, pp .508-511, 2006
2. J. Kim, et al. “A 40-Gb/s optical transceiver front-end in 45nm SOI CMOS technology,” Custom Integrated Circuits Conference (CICC), 2010 IEEE, pp.1-4, 19-22, 2010
3. D. Li, et al. “10-Gb/s modulator drivers with local feedback networks,” IEEE Journal of Solid-State Circuits, vol.41, no.5, pp.1025-1030, May. 2006
4. Zhao, Y. et al., “A 10 Gb/s, 6 V p-p , Digitally Controlled, Differential Distributed Amplifier MZM Driver,” IEEE Journal of Solid-State Circuits, vol.49, no.9, pp.2030-2043, Sep. 2014
5. Y. Kim et al., “A 10-Gb/s 6-Vpp differential modulator driver in 65-nm CMOS,” Circuits and Systems (ISCAS), 2014 IEEE International Symposium on, pp.1869-1872, 2014

Topics in IC Design

8.3 Optical Devices - RX

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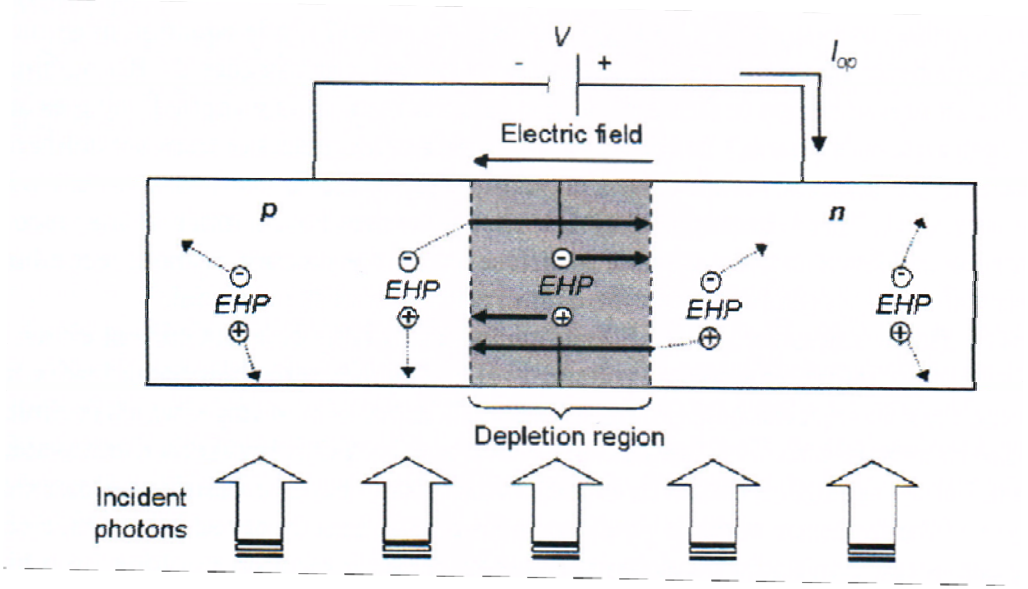
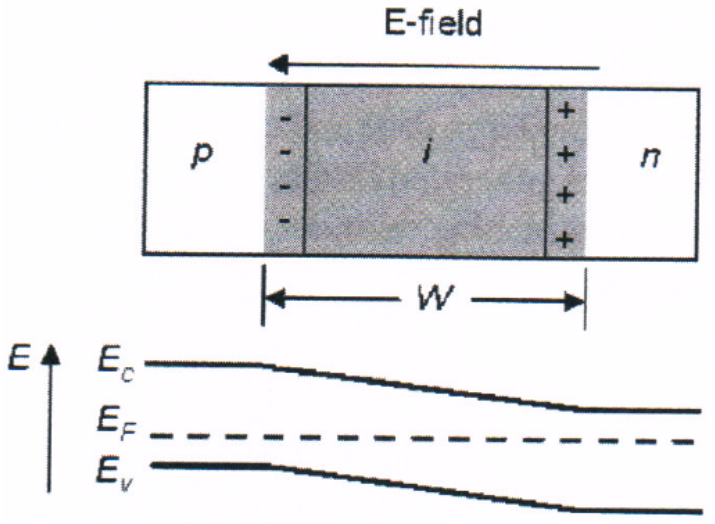
2017 Spring

P-N Junction for EHP Generation

- **An illuminated reverse-biased p-n junction**



Typical p-n structure



p-i-n structure

$$I = I_0(e^{\frac{qV}{kT}} - 1) - Iop$$

$$I_{op} = qAG_{op}(Lp + Ln + W)$$

Photodiode Performance Parameters

- **Quantum efficiency**
  - **Probability that a single photon will generate an EHP that contributes to the detector current**

    (= the number of EHPs generated per incident photon)

  - **External efficiency**

    $$\eta_{ext} = \frac{I_{op}/q}{P/h\nu} = TopFEHP(1 - e^{-\alpha L}),\ 0 < \eta < 1$$

  - **Internal efficiency**

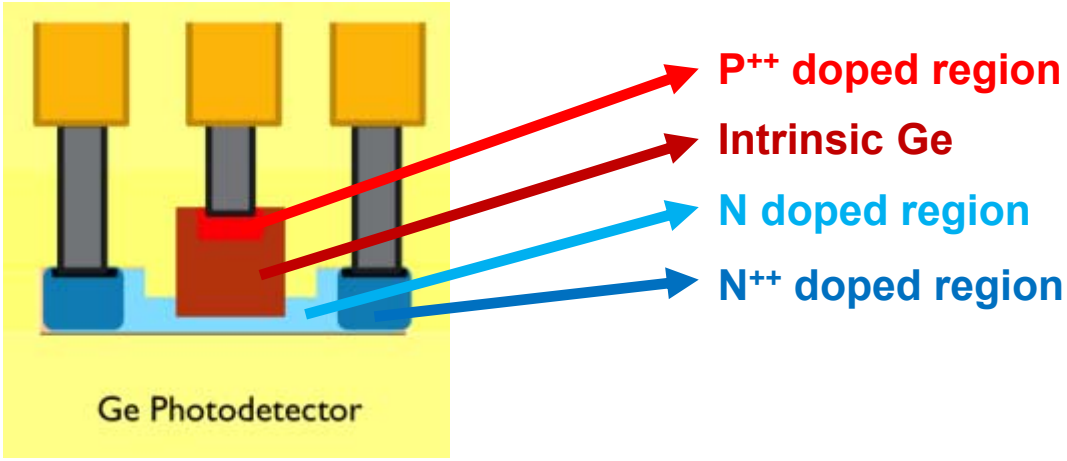
    $$\eta_{int} = \eta_{ext}/Top$$

Photodiode Performance Parameters

- **Responsivity**
  - Photo Current per Optical Power in [A/W]
- **Response time**
  - Transit time of carriers & RC time constant
  - Three governing factors
    : diffusion time, drift time, junction capacitance
  - R almost neglected
- **Noise**
  - Shot noise (dark current)
  - Thermal noise

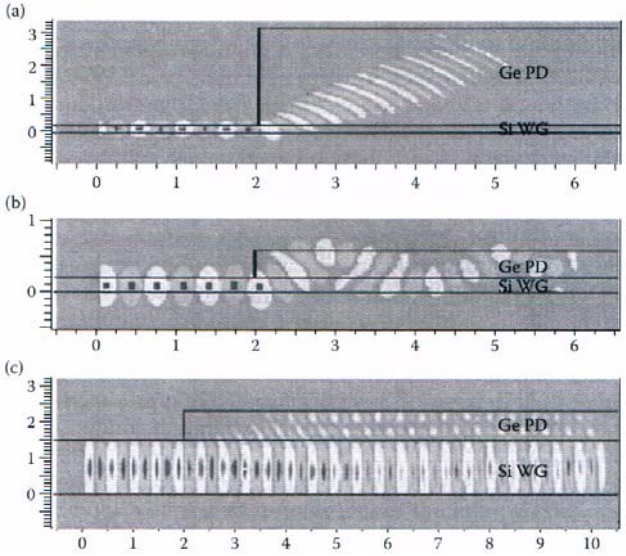
Types of Photo Diodes

- Ge PD
- P-I-N structure
- Bandwidth of 20 GHz
- Responsivity of 0.6 A/W
- Dark current < 50 nA
- Evanescent coupled to Si waveguide

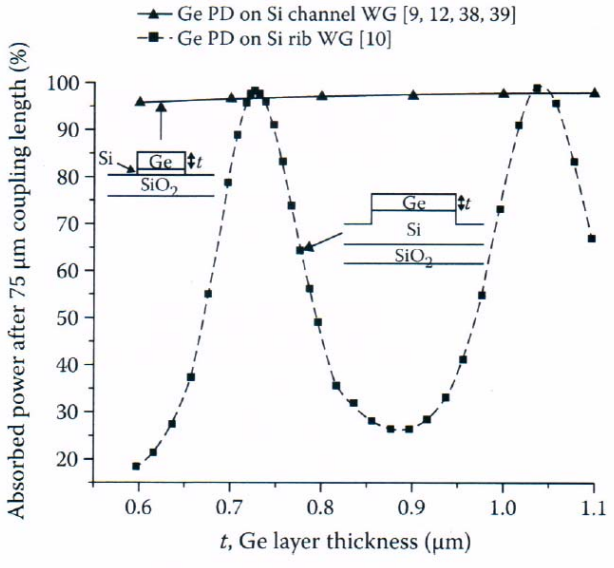


Evanescent Coupling

- Bottom waveguide: Ge growth on c-Si waveguide
- Top waveguide: no epitaxy requirement → flexibility
- The smaller refractive index difference, the better
- The smaller cross-sectional dimension and lower aspect ratio is desirable



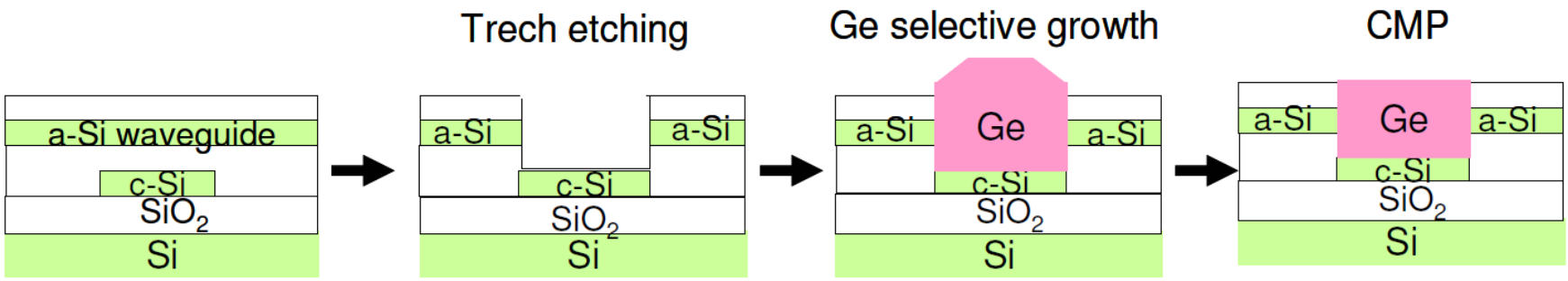
[D. Ahn, JLT, 2010]



[D. Ahn, JAP, 2011]

Butt Coupling

- Direct coupling → higher optical absorption
- Requires a stringent design for mode matching condition → less tolerant to fabrication errors



[J. F. Liu, Proceedings of IEEE Group IV Photonics Conference, 2006]

Key Parameters of Photodiode

1) External quantum efficiency

$$\eta_e = \frac{\#\text{ of electrons per sec}}{\#\text{ of photons per sec}} = \frac{I_{ph}/e}{P_o/h\nu}$$

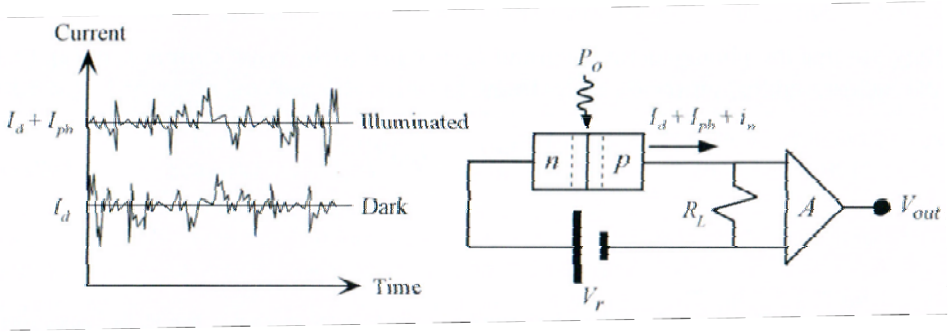
2) Responsivity

$$R = \frac{\text{Photo current (A)}}{\text{Incident optical power (W)}} = \frac{I_{ph}}{P_o} = \eta_e \frac{e}{h\nu}$$

3) Bandwidth

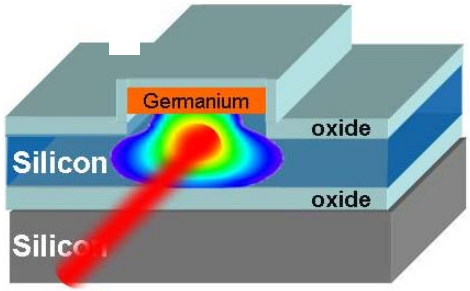
4) Dark current

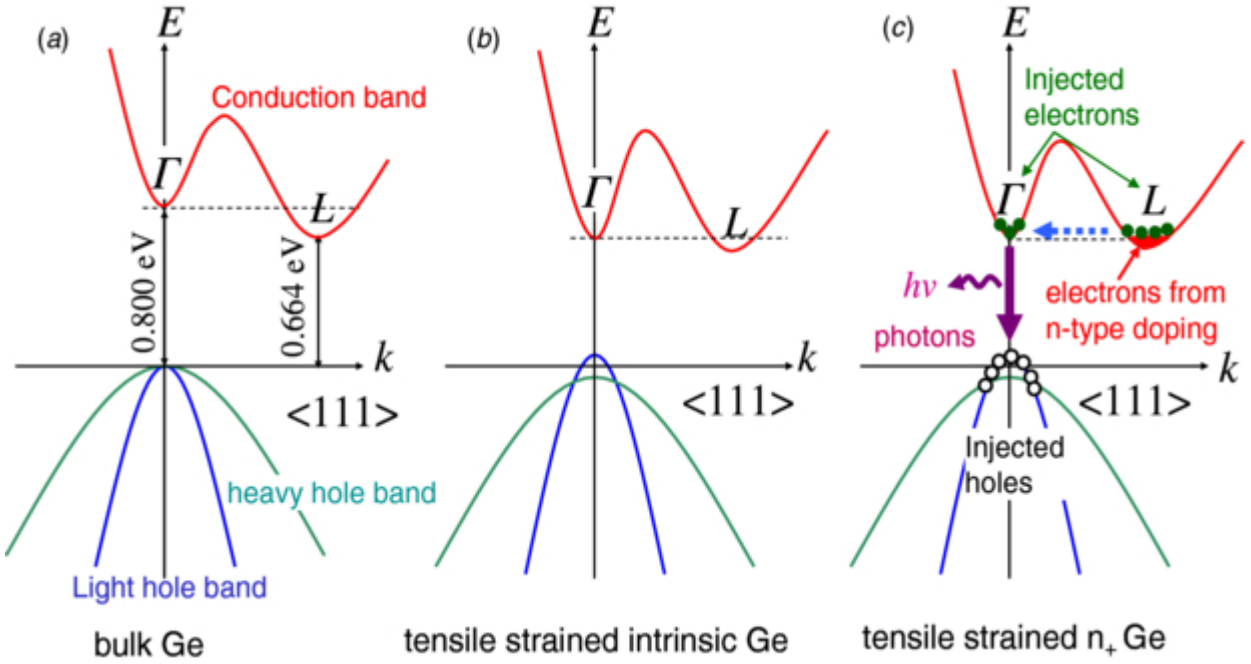
5) Shot noise



How to absorb light: Germanium

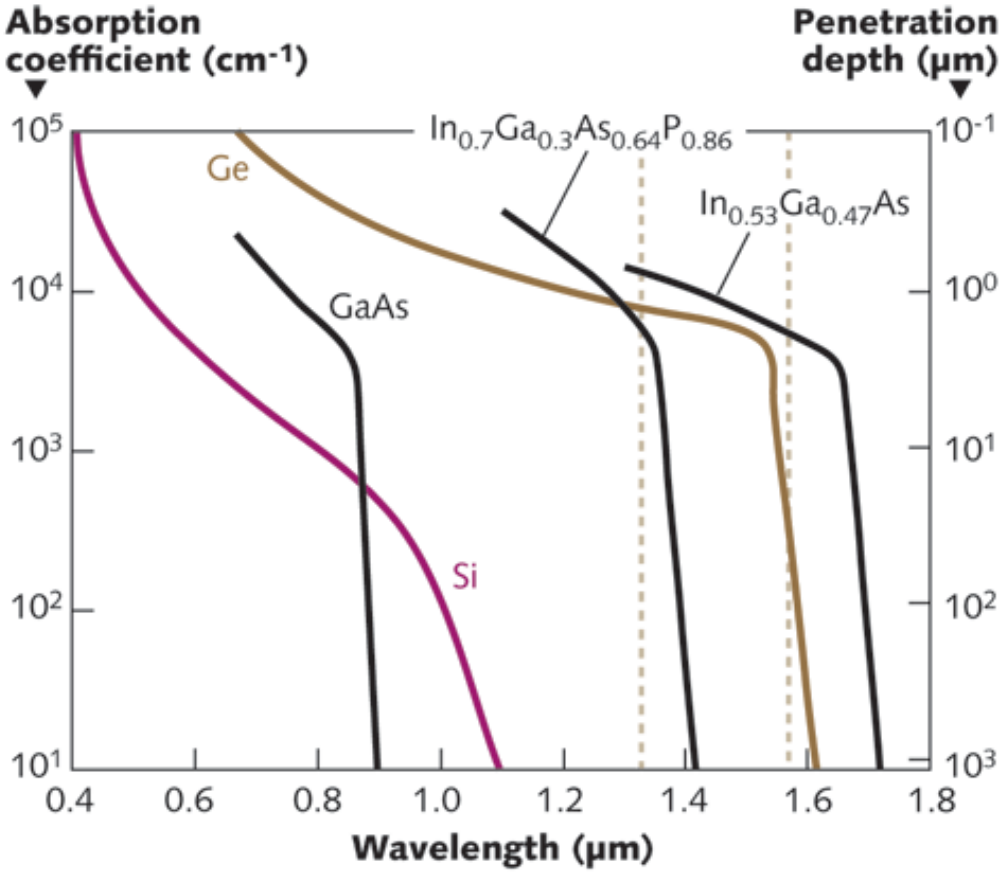
- Si, Ge: indirect bandgap
- III-V: direct bandgap
- Ge: epitaxial growth on Si





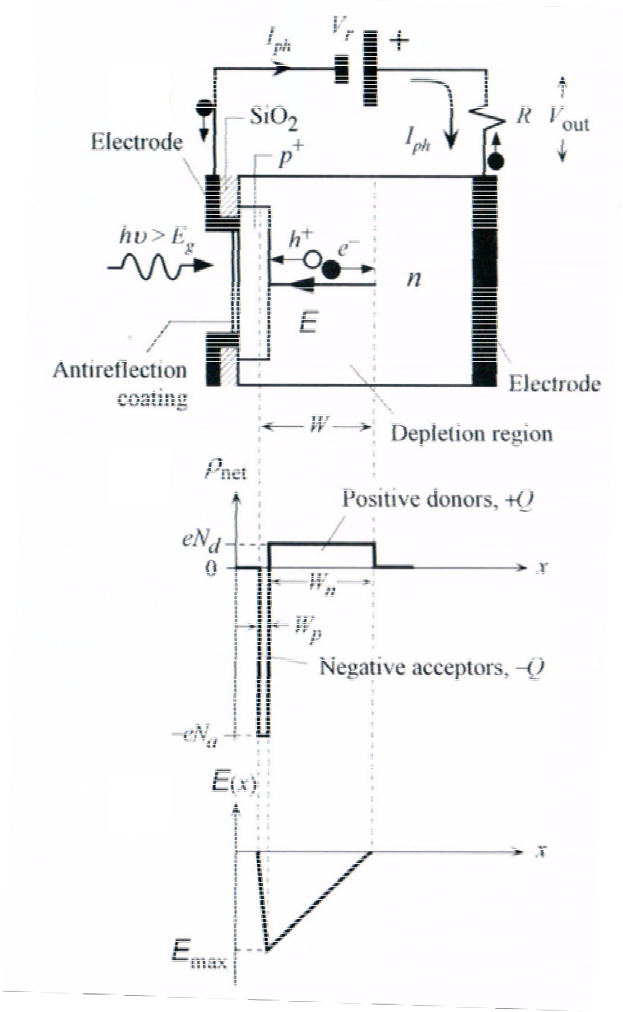
How to absorb light: Germanium

- **Bandgap and absorption coefficient**

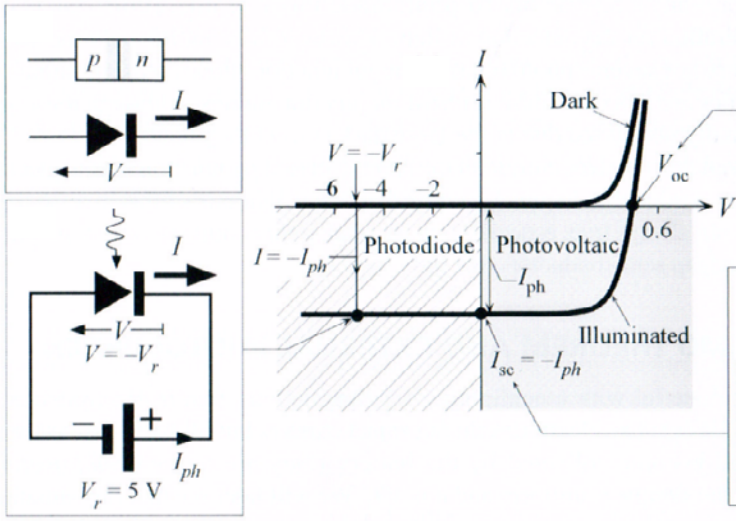


PN Junction Photodiode

PN photodiode principle



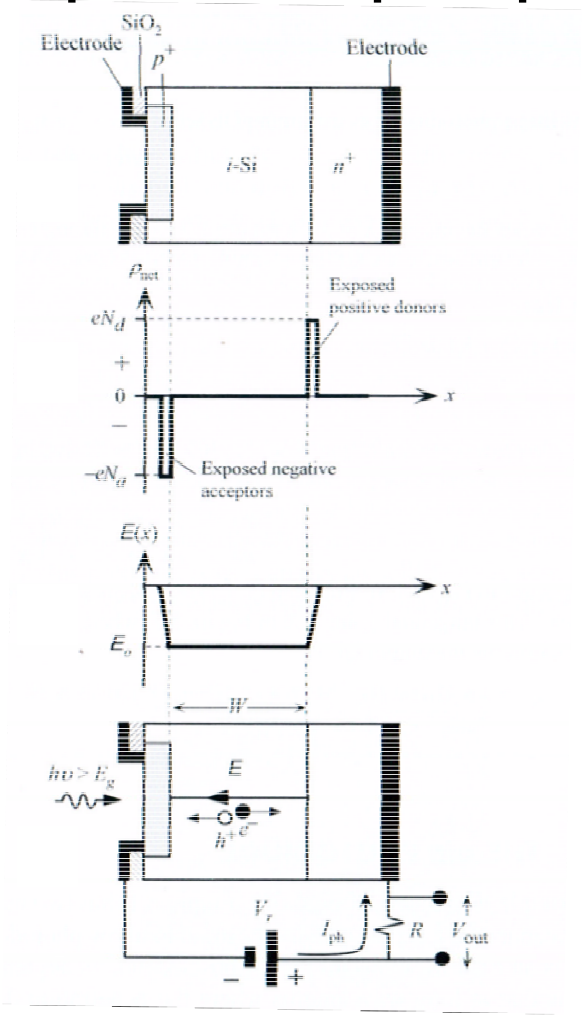
I-V curve

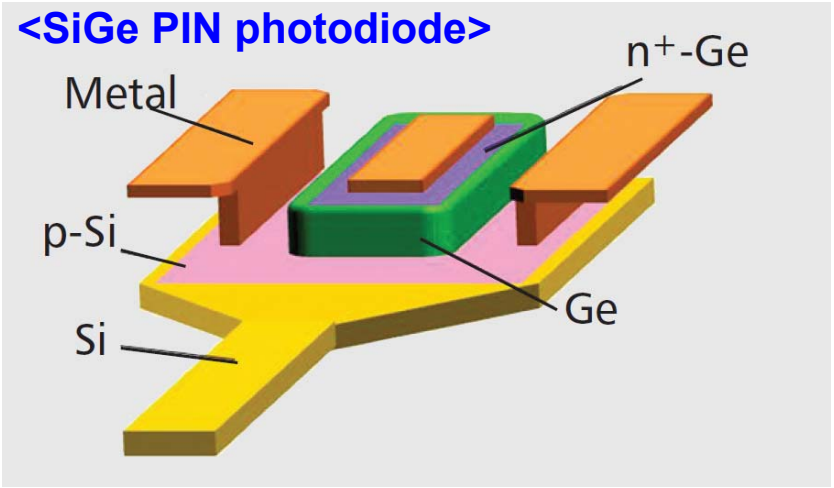


- ✓ **Reverse biased PN junction**
- ✓ **Photon → electron / hole pairs**
- ✓ **Electron moves in E-field → photo current**

P-Intrinsic-N Photodiode

PIN photodiode principle



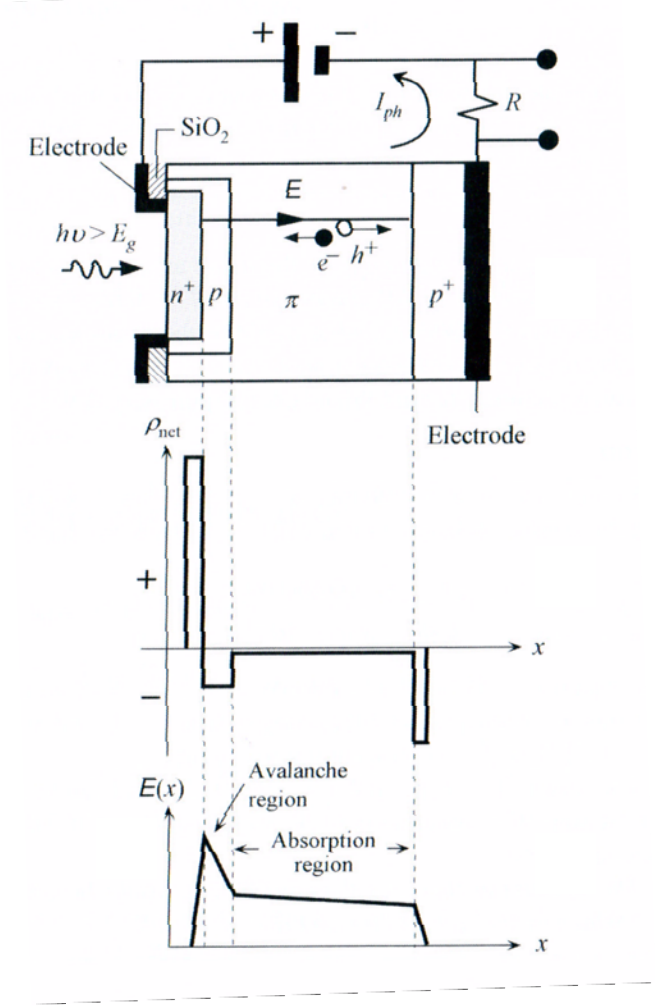


[Tokyo Univ. Yasuhiko 2013]

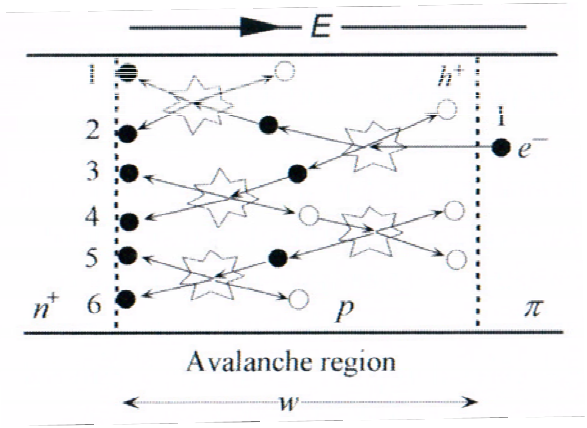
- ✓ Larger depletion region → reduced $C_{junction}$
- ✓ High speed

Avalanche Photodiode

Avalanche photodiode principle



Impact ionization



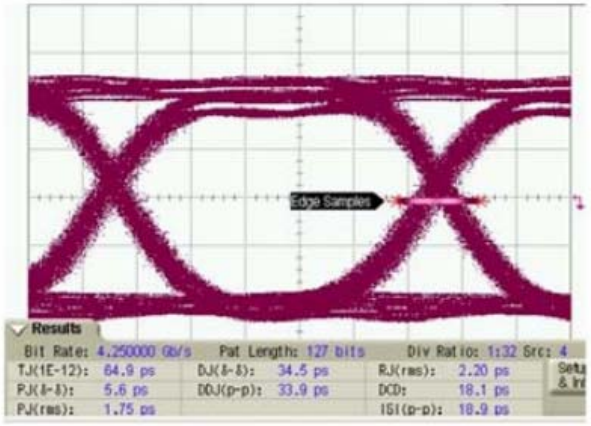
- ✓ **Avalanche → high responsivity (A/W)**
- ✓ **Avalanche → excess noise**
- ✓ **High speed**

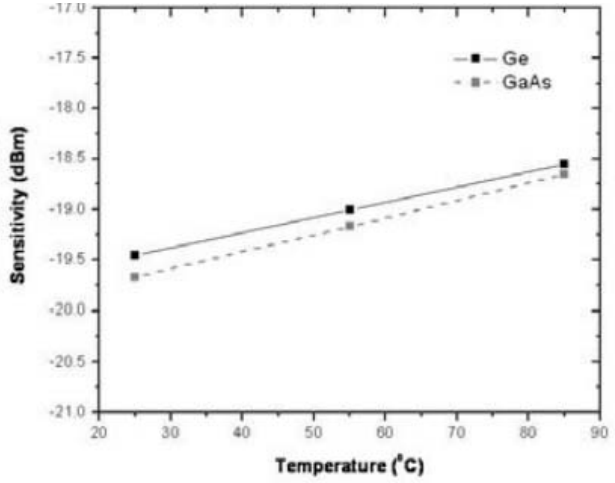
Ge on Si Photodiode

- Strong absorber at the infrared and
- Higher mobilities of electrons and holes,
- Ge, ideal candidate to replace III-V detectors
- Large lattice mismatch (4.2 %)
  - → critical thickness exists (due to strain)
  - → dislocations → dark current ↑, mobility ↓
- Photodiode on relaxed $Si_{1-x}Ge_x$ buffer layer
- Ge grown directly on Si
- Ge-on-insulator & Ge-on-silicon-on-insulator (SOI)
- Resonant cavity enhanced (RCE) and avalanche PD

850-nm Ge PD (Intel)

- Thin initial seed layer → Thick Ge film growth
- Hot annealing process for low dislocation density
- Responsivity of 0.6 A/W @ 850 nm
- Bandwidth of ~9 GHz
- Performance comparable to commercial GaAs

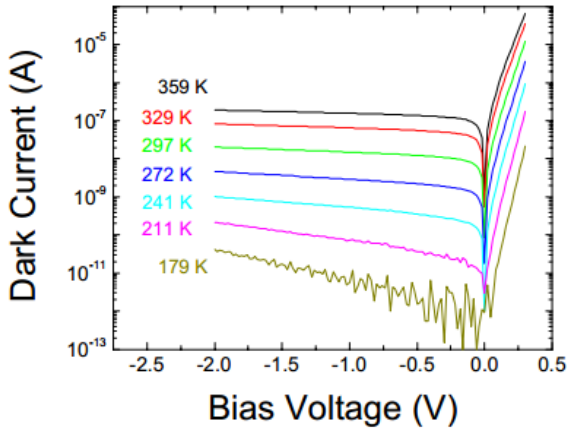




[M. Morse, Proceedings of IEEE Group IV Photonics Conference, 2006]

High Speed P-I-N Ge PD (IBM)

- Bandwidth maximized employing p-i-n structure
- Small bandgap & defects → dark current (temperature-sensitive)
- Proved that trap-assisted generation is dominant
- Bandwidth of 29 GHz, demonstration of 19 Gb/s operation



[S. J. Koester, Proceedings of IEEE Group IV Photonics Conference, 2006]

Waveguide-Coupled Photodiodes

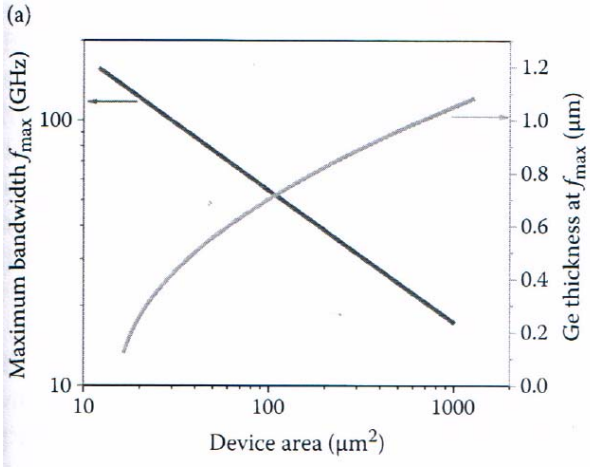
- **Bandwidth and quantum efficiency trade-off relieved**
- **Active device area reduced → lower dark current**

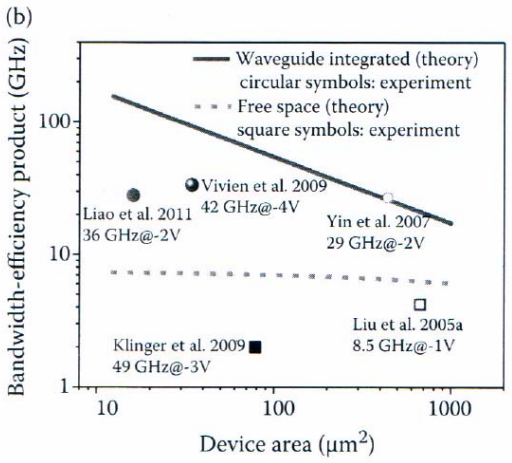
$$f_{RC} = \frac{1}{2\pi RC} = \frac{d}{2\pi R_L \varepsilon_{Ge} \varepsilon_0 A}$$

$$f_{transit} = \frac{0.44 vsat}{d}$$

$$f_{3dB} = \sqrt{\frac{1}{1/f^2_{transit} + 1/f^2_{RC}}}$$

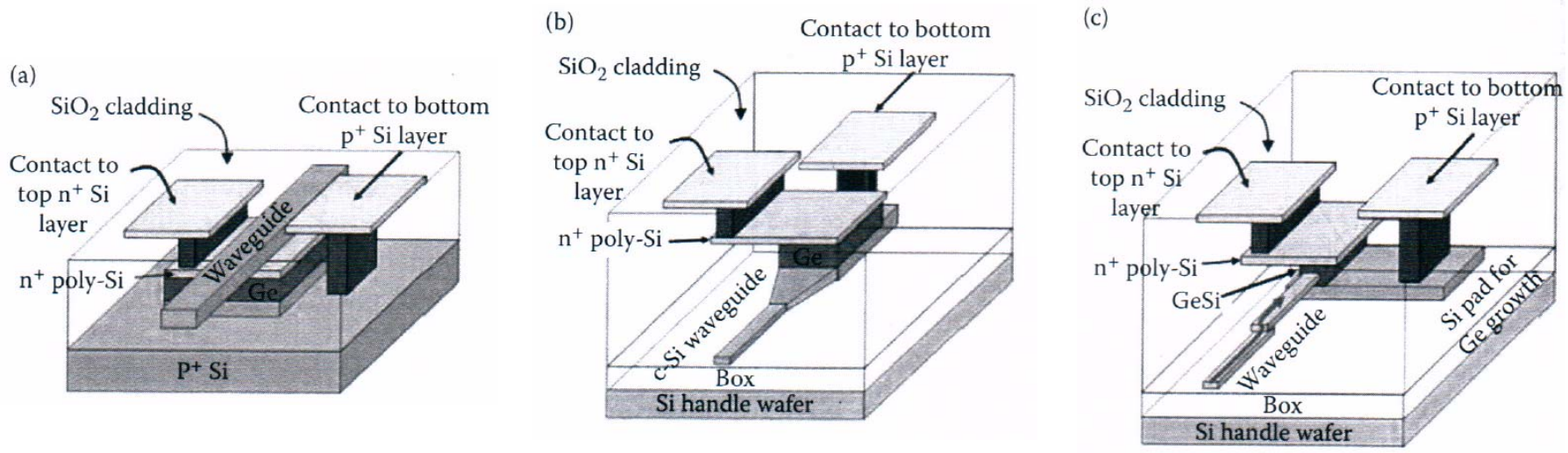
$$f_{max} = \sqrt{\frac{0.11 vsat}{\pi R \varepsilon_{Ge} \varepsilon_0 A}}, \qquad dopt = \sqrt{0.88 \pi R \varepsilon_{Ge} \varepsilon_0 A v_{sat}}$$





Waveguide Coupling Scheme

- **Evanescent coupling configured as either top- (a) or bottom- (b) coupled waveguides**
- **Butt coupling (c)**



Topics in IC Design

8.4 Transimpedance Amplifier

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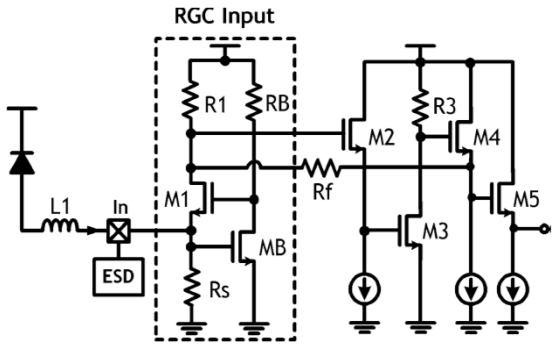
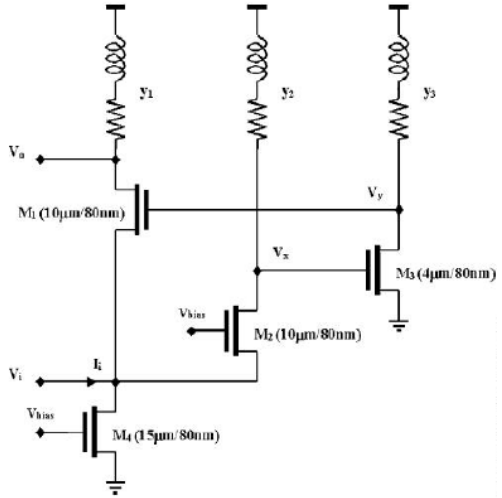
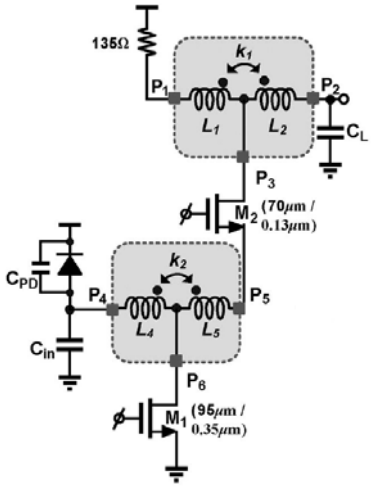
TIA Circuit Topologies

- TIA had to accommodate very large PD capacitance !!!

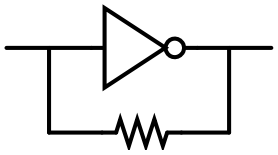
1.25-Gb/s RGC TIA	20-Gb/s RGC TIA	20-Gb/s CG TIA
		
JSSC 2004	JSSC 2004	TCAS II 2010

- RGC: ReGulated Cascode
- Not adequate for continuously "scaling-down" technology
- PD capacitance keeps shrinking – not a major issue any more

TIA Circuit Topologies

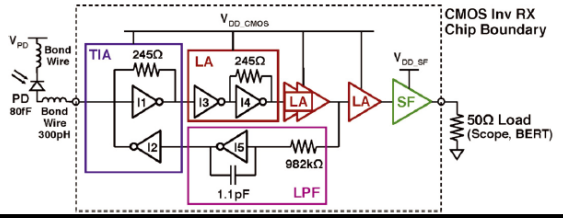
❖ **Various TIA topologies are being tried.**

Inverter-based TIA

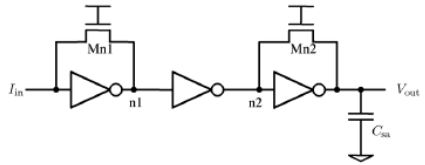


- ✓ Adequate for low V_{DD}
- ✓ No bias circuits
- ✓ High-gain
- ✓ Easy design
- ✓ Simple analysis

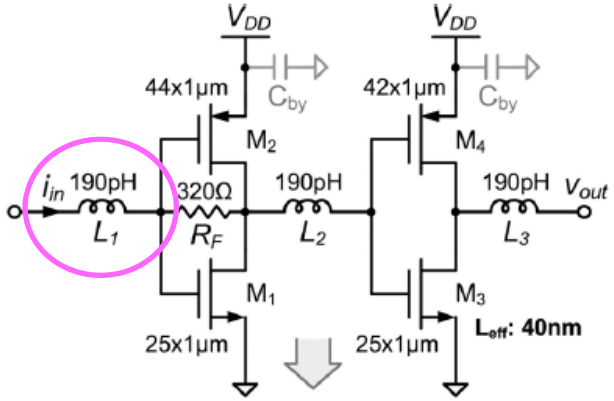
15-Gbps, ISSCC 2012



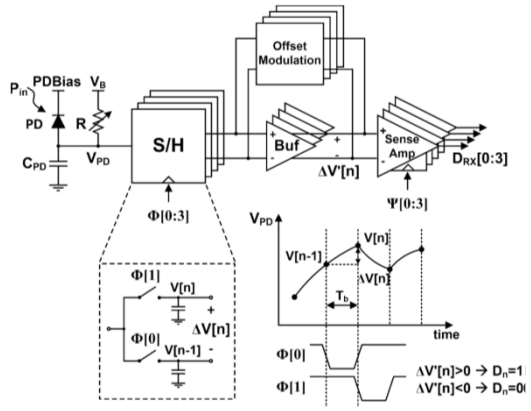
10-Gbps, JSSC 2012



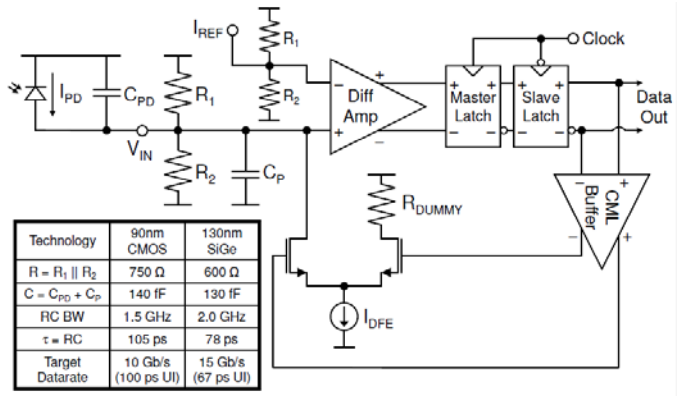
40-Gbps, JSSC 2012



Double-sampling receiver (24-Gbps, JSSC 2013)



DFE-IIR equalization (15-Gbps, ISSCC 2013)

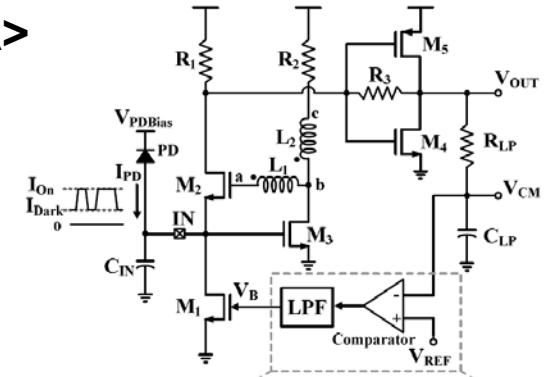


Technology	90nm CMOS	130nm SiGe
$R = R_1 \parallel R_2$	750 Ω	600 Ω
$C = C_{PD} + C_P$	140 fF	130 fF
RC BW	1.5 GHz	2.0 GHz
$\tau = RC$	105 ps	78 ps
Target Datarate	10 Gb/s (100 ps UI)	15 Gb/s (67 ps UI)

Example: 0.13um, 2010

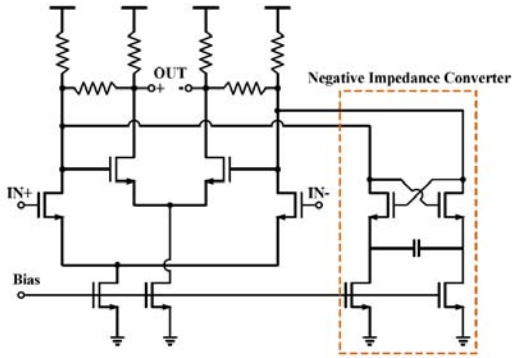
❖ 10-Gbps RGC-based TIA

<TIA>



M1	10μm/0.2μm
M2	40μm/0.13μm
M3	105μm/0.13μm
M4	19.8μm/0.13μm
M5	55.8μm/0.13μm
R1	1.13kΩ
R2	237Ω
R3	1.1kΩ
VBcom	533mV

<LA>



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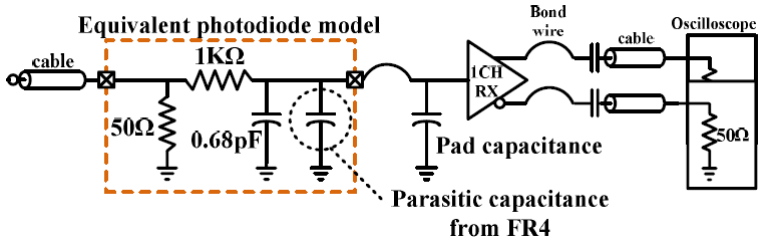

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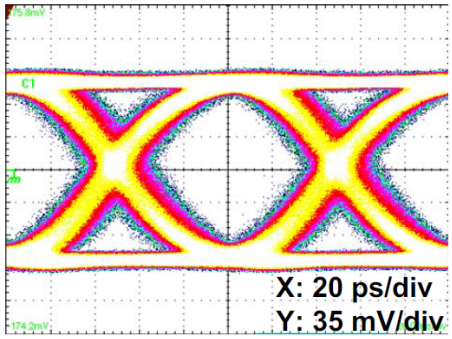
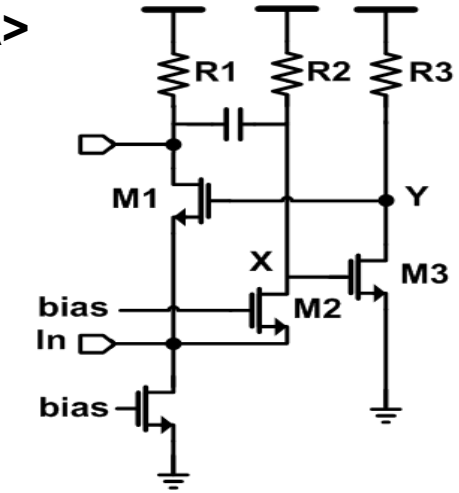


	TIA	LA
Power	5 mW	28.4 mW
Gain	58.5 dBΩ	47.5 dB

Example: 0.13um, 2011

❖ 12.5-Gbps RGC-based TIA

<TIA>



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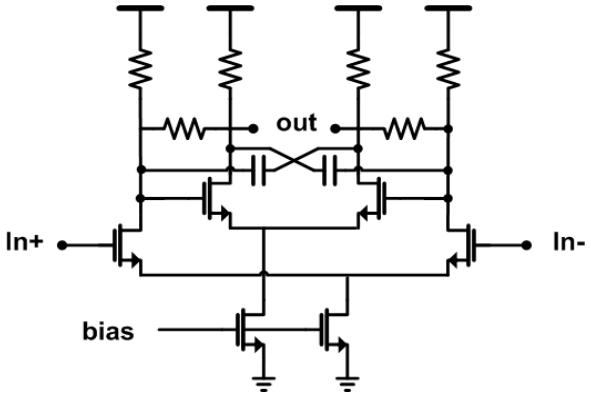

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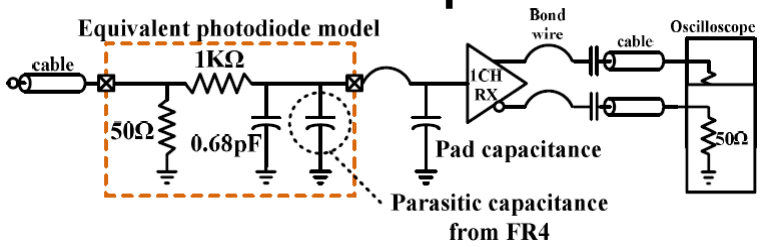

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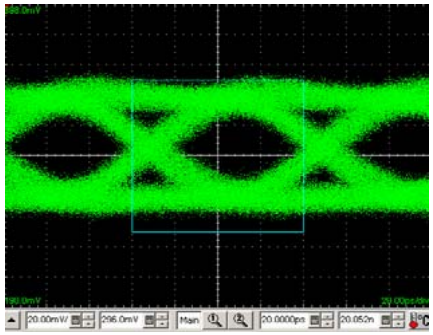
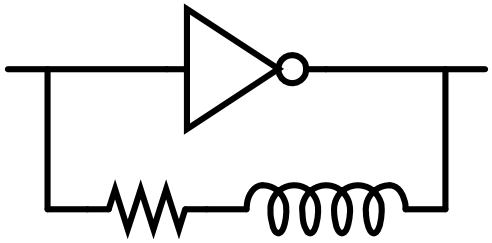


	TIA	LA
Power	2.7 mW	25.4 mW
Gain	52 dBΩ	48.4 dB

Example: 65nm, 2012

❖ 20-Gbps inverter-based TIA

<TIA>



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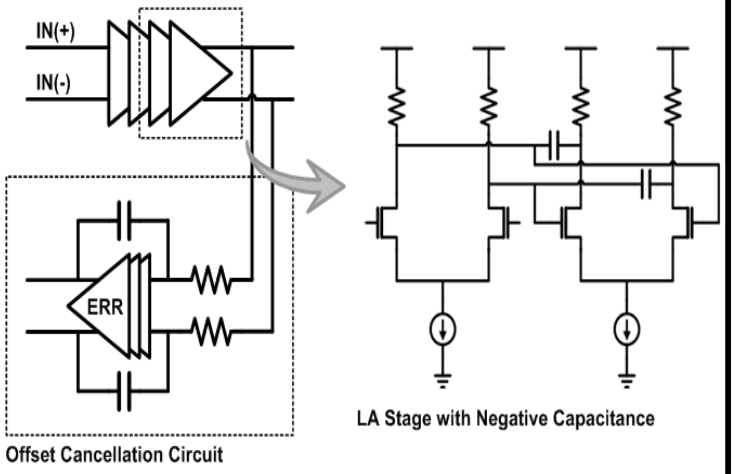

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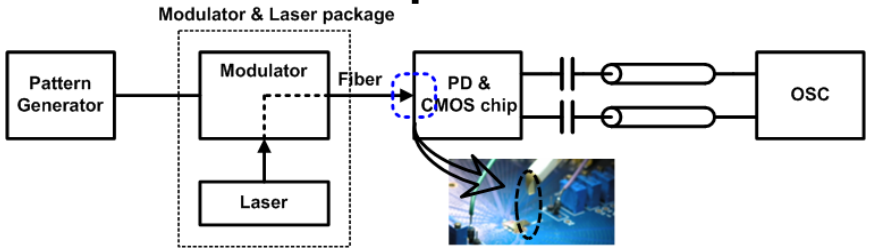

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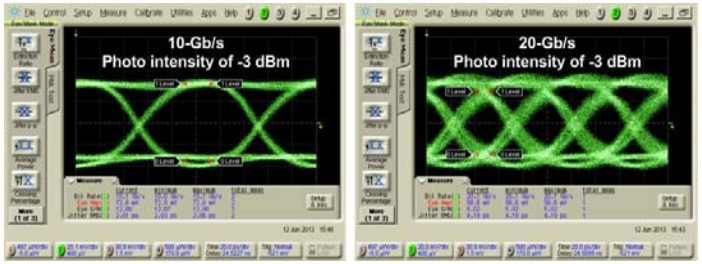
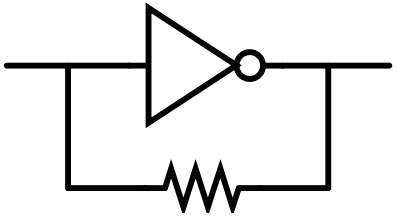


1.23 pJ/bit	TIA	LA
Power	1.3 mW	24 mW
Gain	40 dBΩ	38 dB
$I_{n,r}$	3.9 uA_{rms}	-

Example: 65nm, 2013

❖ **25-Gbps inverter-based TIA**

<TIA>



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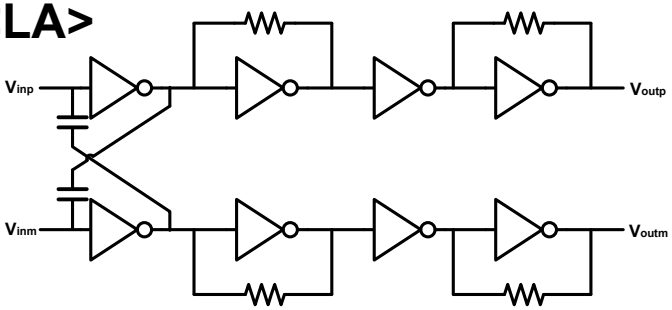
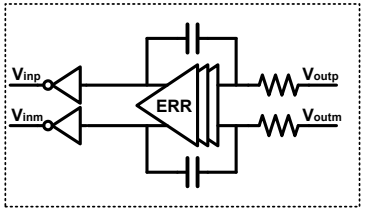
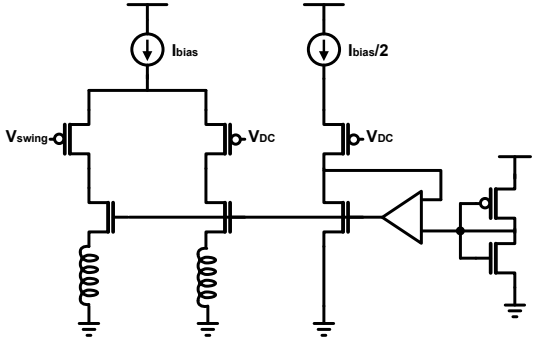
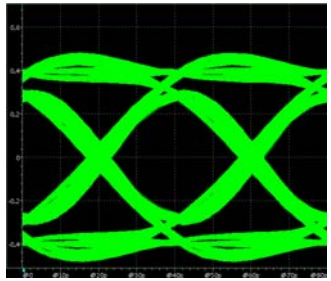




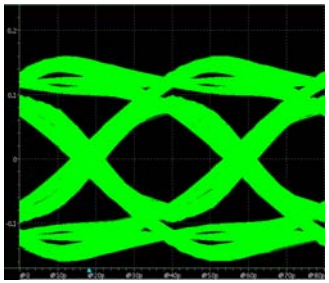
Offset Cancellation Circuit

<S2D>





<To CDR>



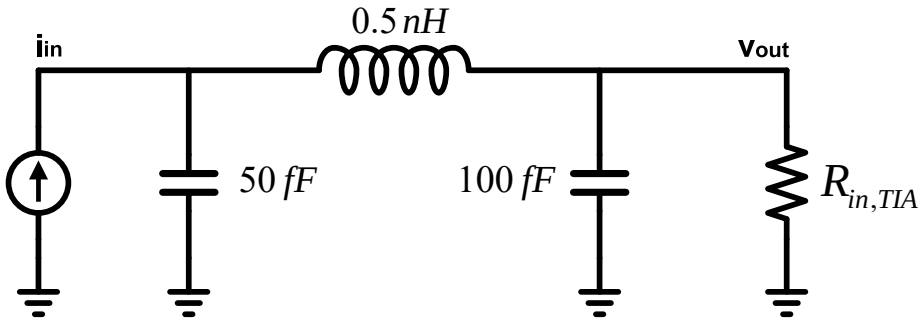
<To OSC>

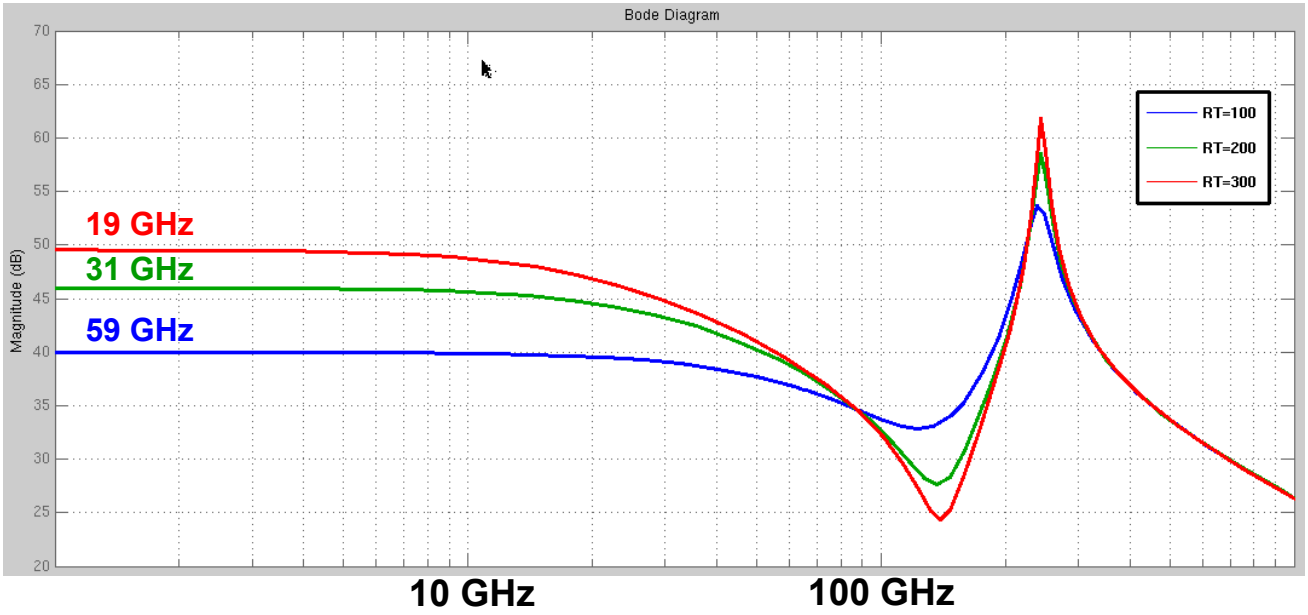
<Simulation result>

0.7 pJ/bit	TIA	LA
Power	2.1 mW	15.1 mW
Gain	41 dBΩ	30 dB
$I_{n,r}$	4 uA_{rms}	-

PD Modeling (Wire-Bonded)

- **Frequency responses for various TIA input resistances**





Topics in IC Design

8.5 Silicon Photonics

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Seoul National University
2017 Spring

What is Si Photonics?

- Photonic signals processed in Si substrate
- For waveguide, choose Silicon on Insulator (SOI)
- High density system with high bandwidth

Silicon Photonics Trends

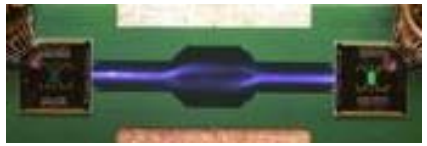
- Silicon photonics : from macro-scale to micro-scale
- Board-board level
- Chip-to-chip level
- Chip-level integration (ultimate goal)

WAN, MAN
metro, long-haul

LAN
campus, enterprise

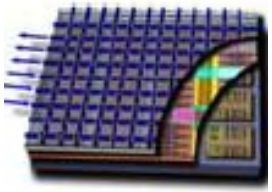
System
intra/inter-rack

Board
module-module



Module
chip-chip

IC
on-chip



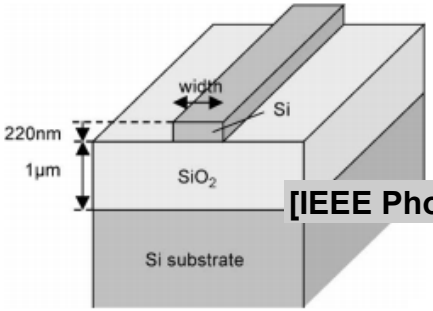
Increasing integration of optics

1980's | 1990's | 2000's | 2014~

Silicon Photonics

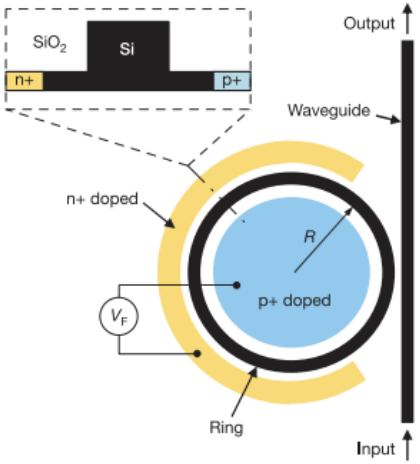
- **Keywords in silicon photonics**
  - Silicon-on-insulator (SOI)
  - Through-silicon via (TSV)
  - Flip-chip bonding

[SOI photonic wire]

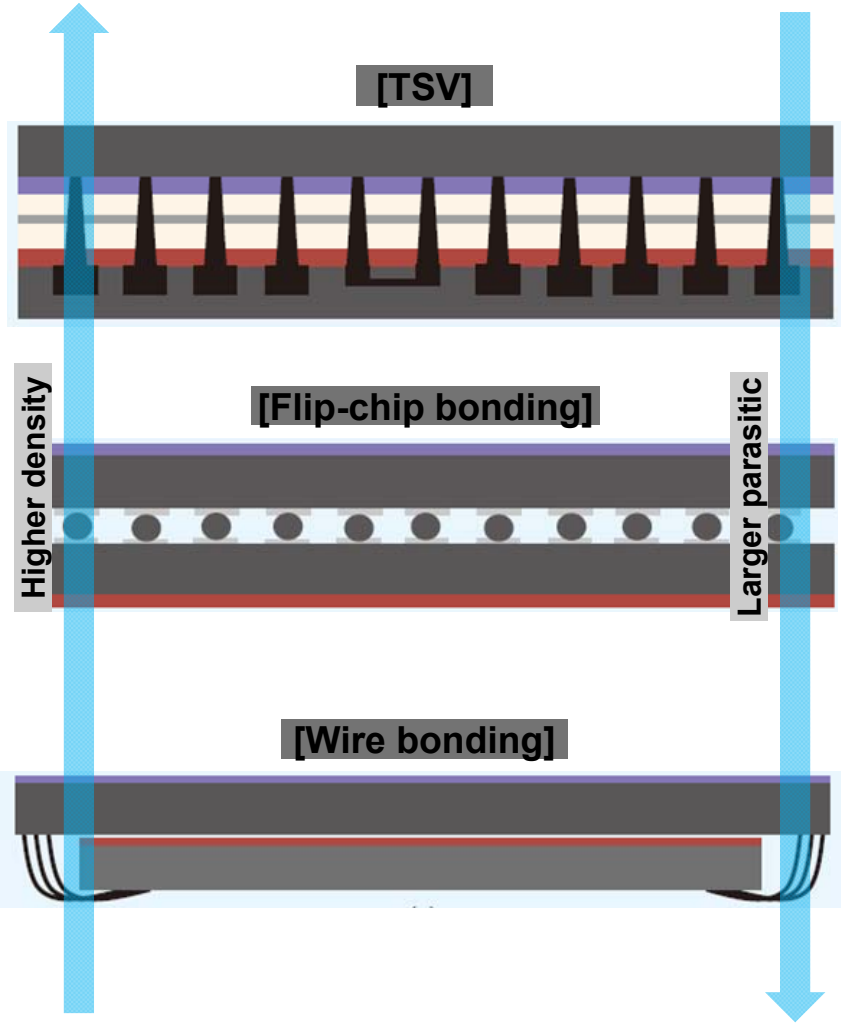


[IEEE Photon. Technol. Lett, 2004]

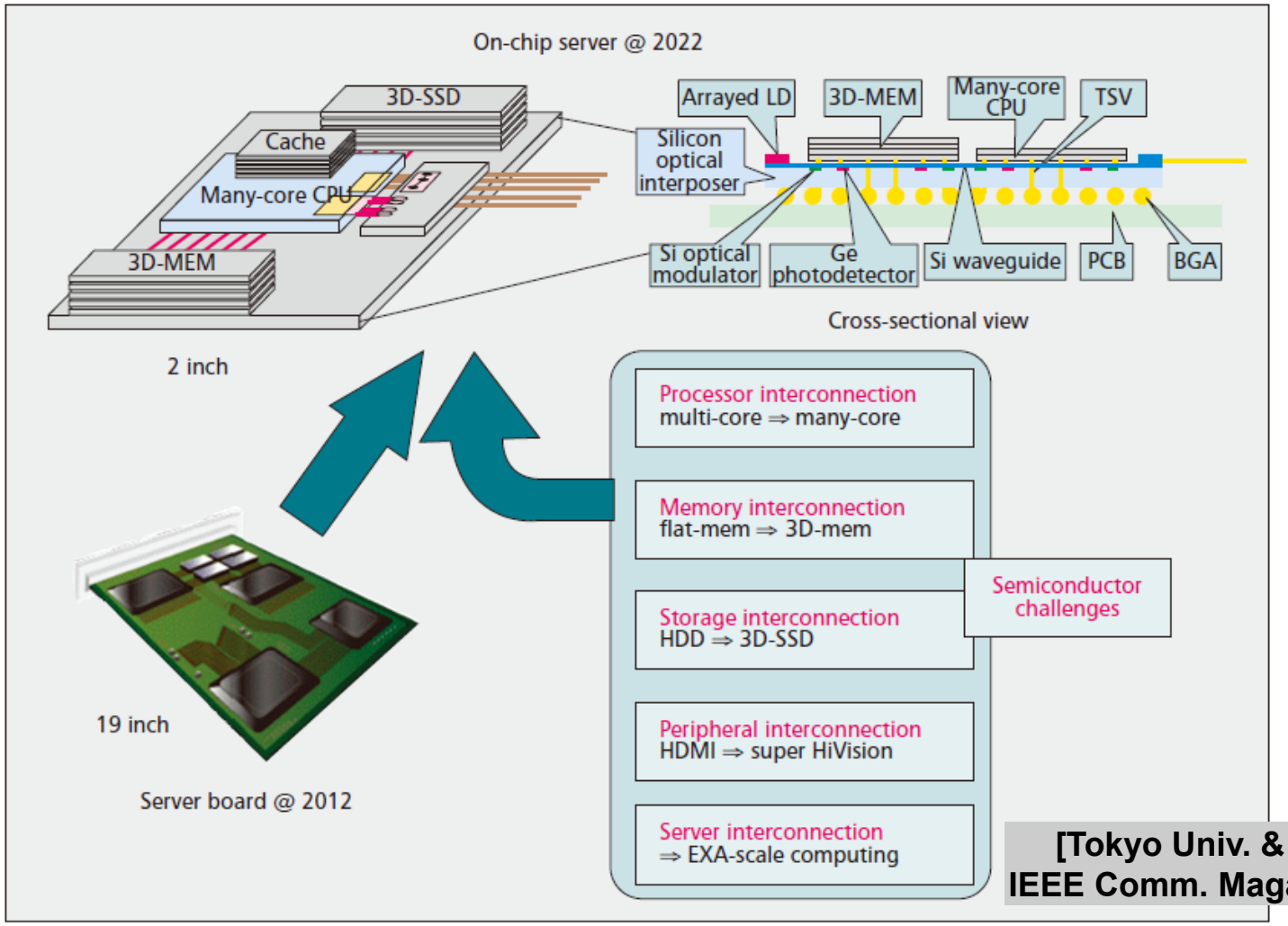
[Silicon modulator]



[Nature, 2005]



Future “On-Chip Server”

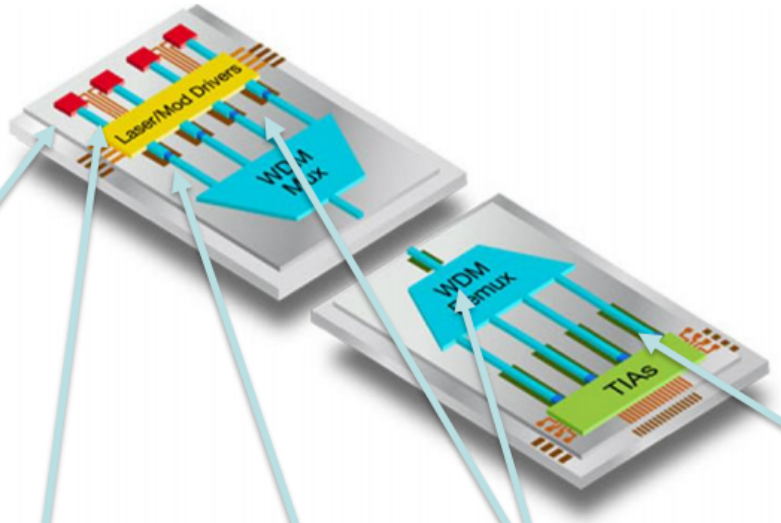


[Tokyo Univ. & PETRA, IEEE Comm. Magazine 2013]

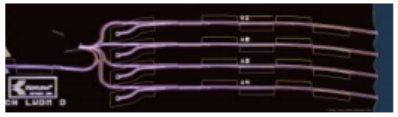
Kotura Approach

❖ **Provides WDM PICs**

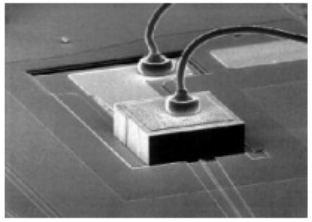
Opto-electronic integration of all components except laser eliminates dozens of piece parts



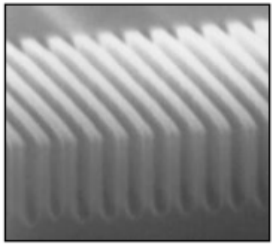
4x25 RX



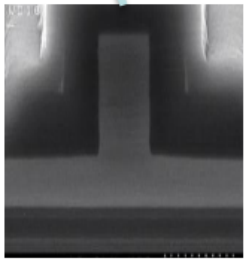
4x25 TX



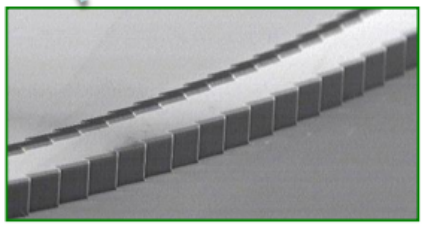
Light source



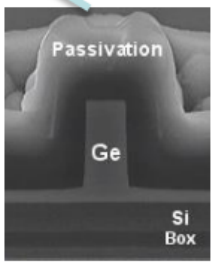
Grating



Modulator



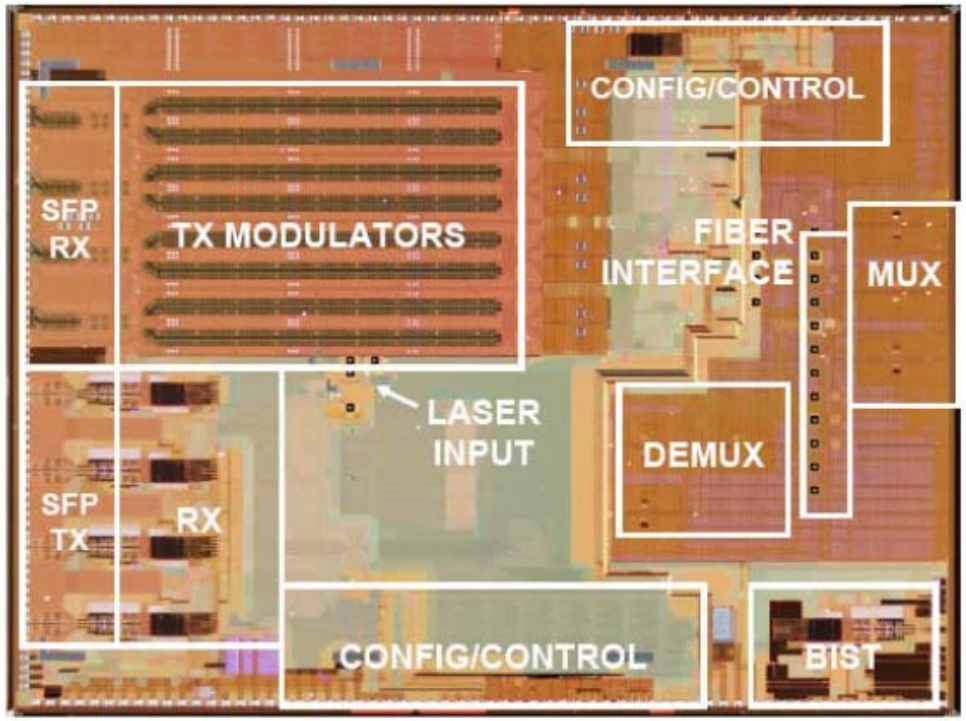
WDM Mux/Demux



Detectors

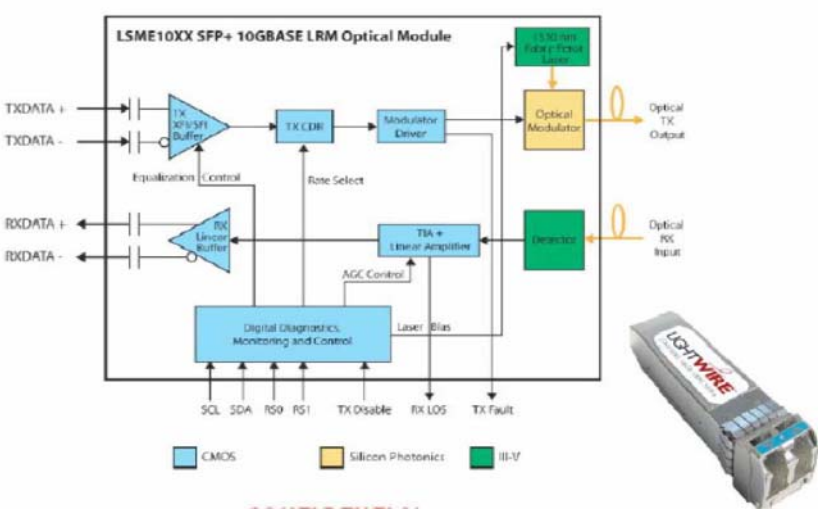
Luxtera Approach

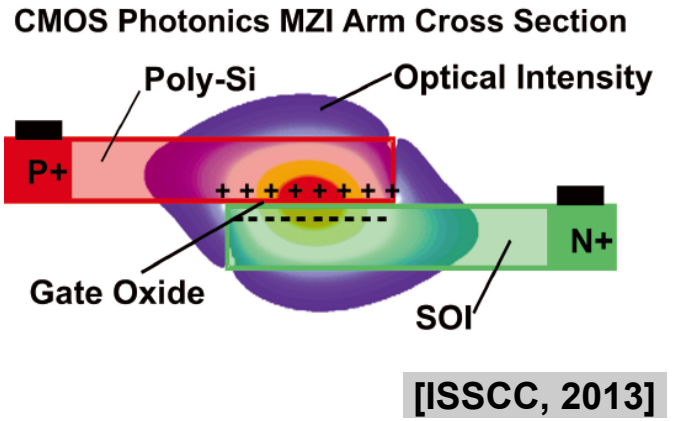
- Monolithic integration (except laser source)
- Based on SOI CMOS technology
- Ge PD compatible with silicon fabrication (epitaxial grow)
- Silicon-based modulator



Lightware Approach

- ❖ Hybrid integration of III-V laser source & PD
- ❖ CMOS photonics MZI arm cross section
  - Low-voltage operation (1.2 V)
  - High-speed operation (up to 40 Gb/s)

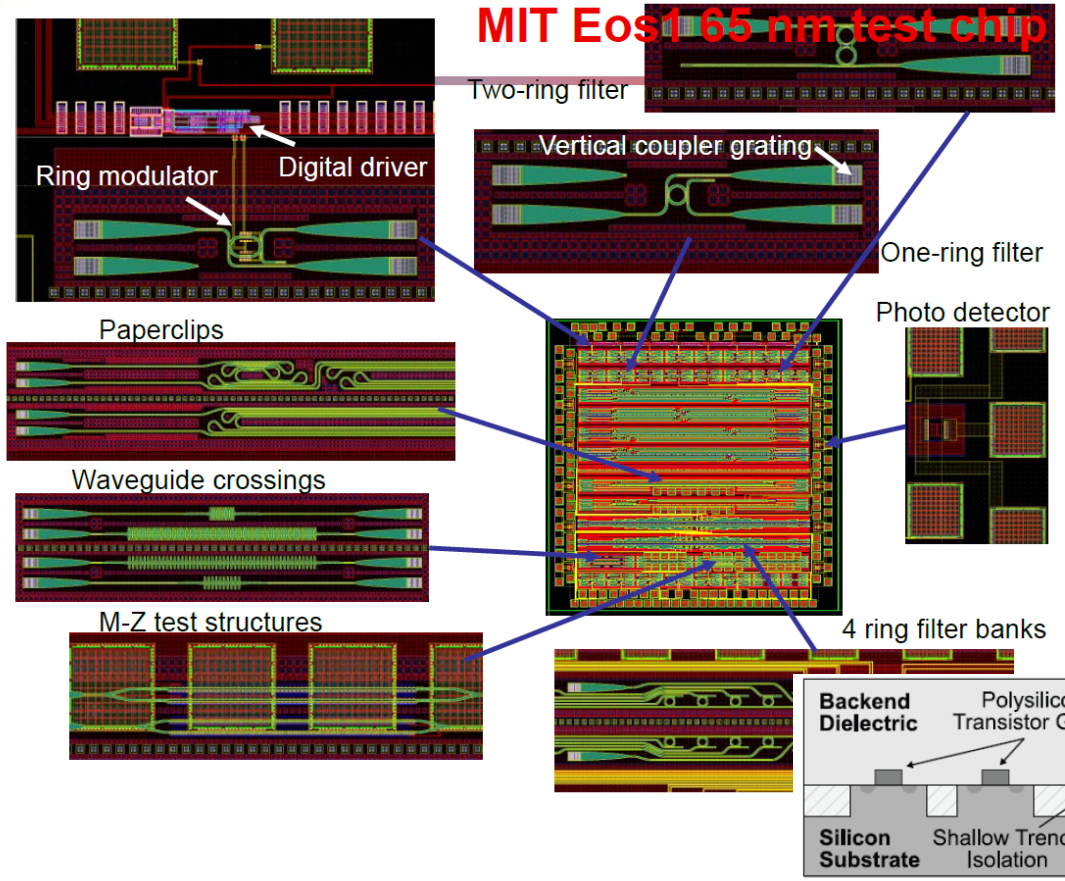


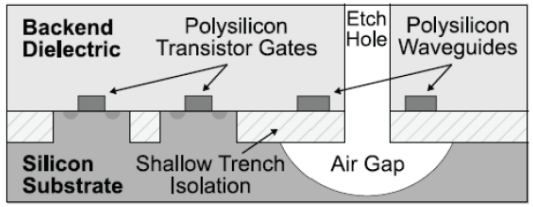


[ISSCC, 2013]

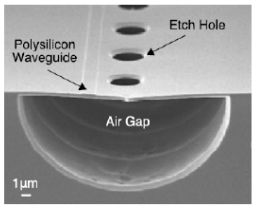
MIT Approach

- **First ever photonic chip in sub-100nm bulk CMOS technology**





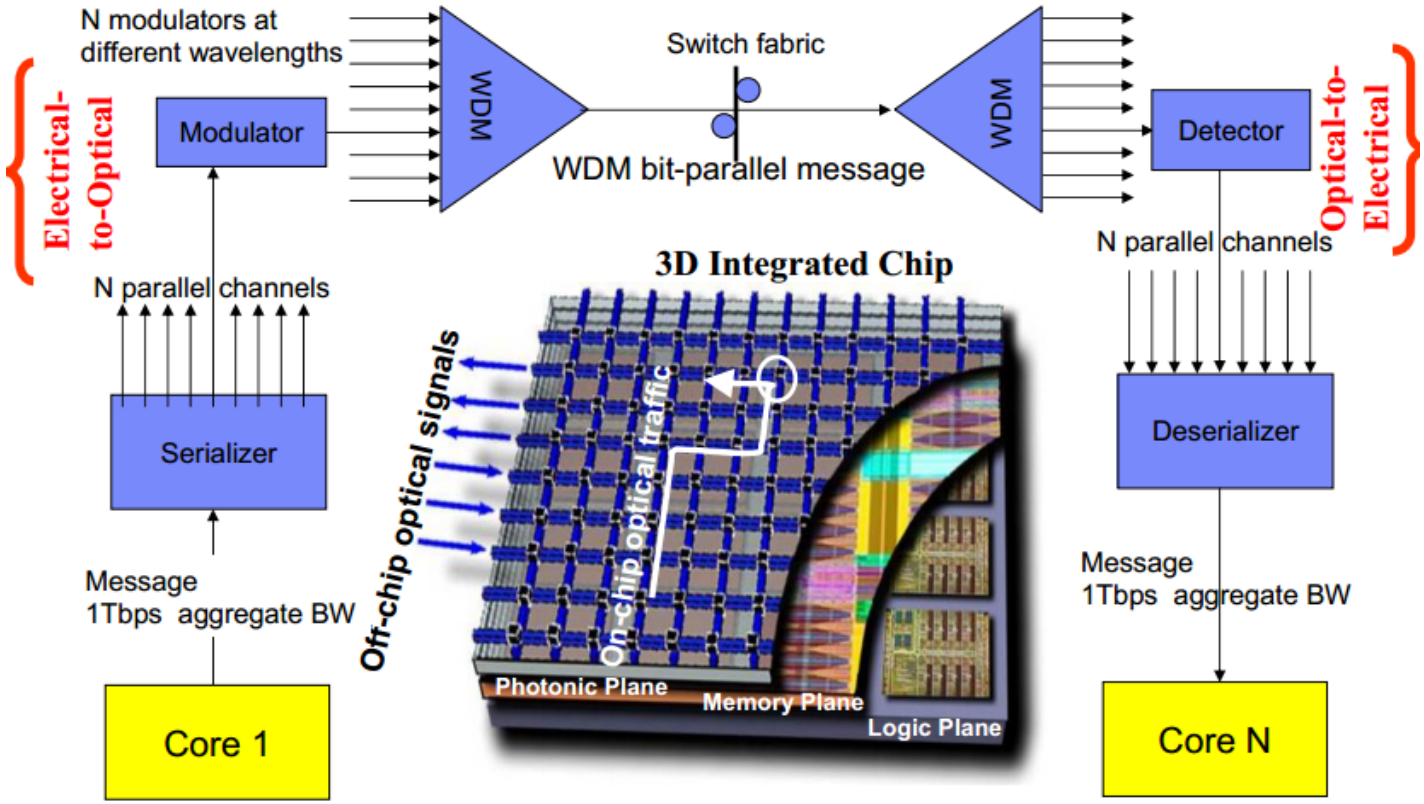
Cross-sectional view of a photonic chip



SEM image of a poly silicon waveguide

3-D Supercomputer Chip

- **Ultimate vision, circa 2020 (70Tbps optical on-chip)**

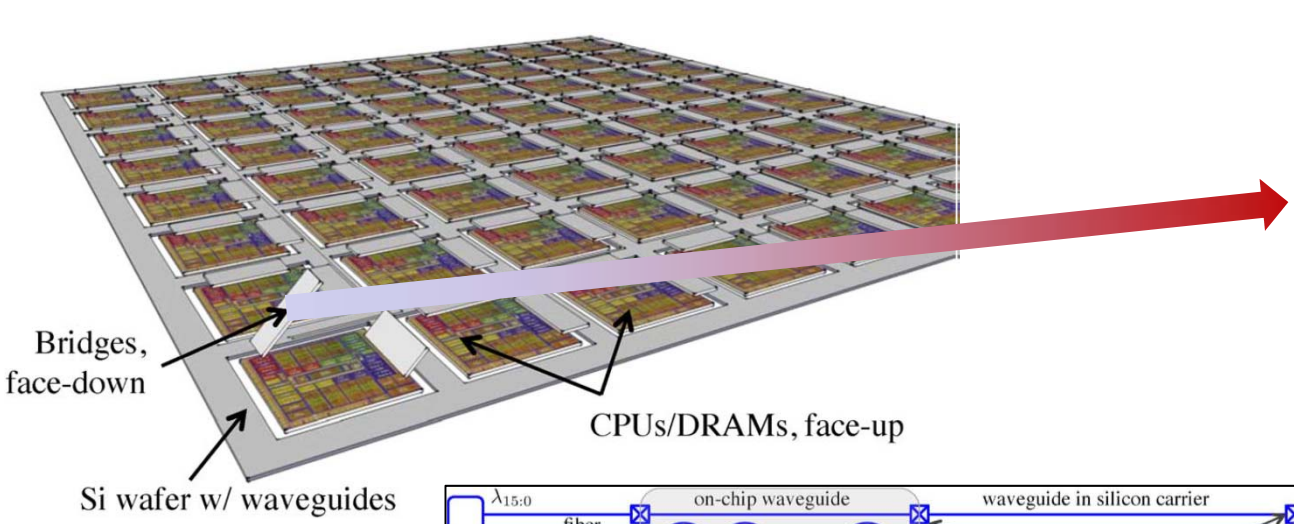


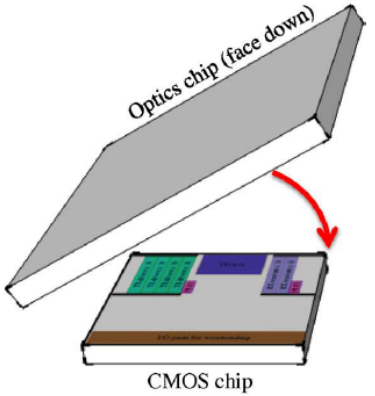
[IBM, 2008][31]

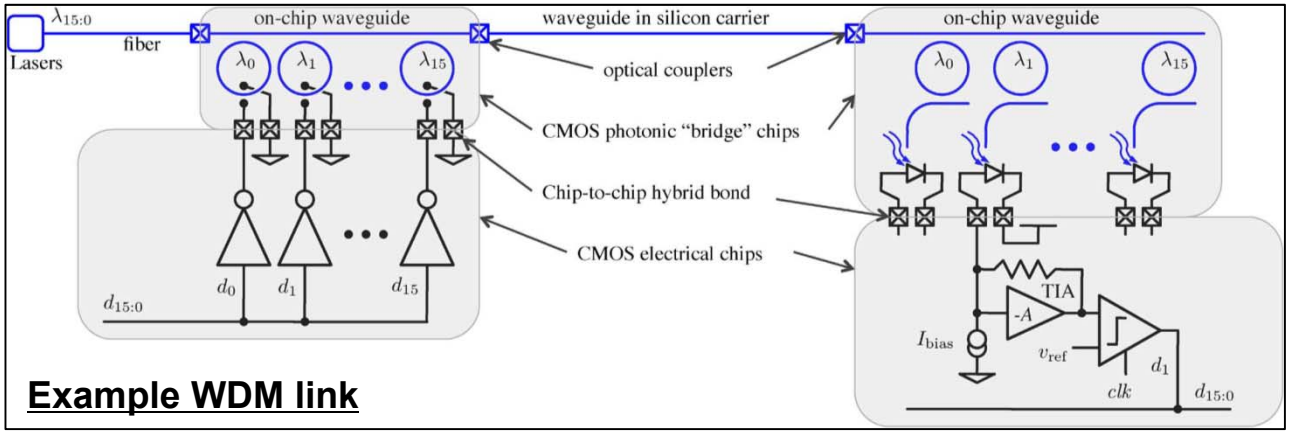
Macro-Chip

- **Envisioned 8 x 8 macro-chip**

Hybrid bonding (flip-chip)





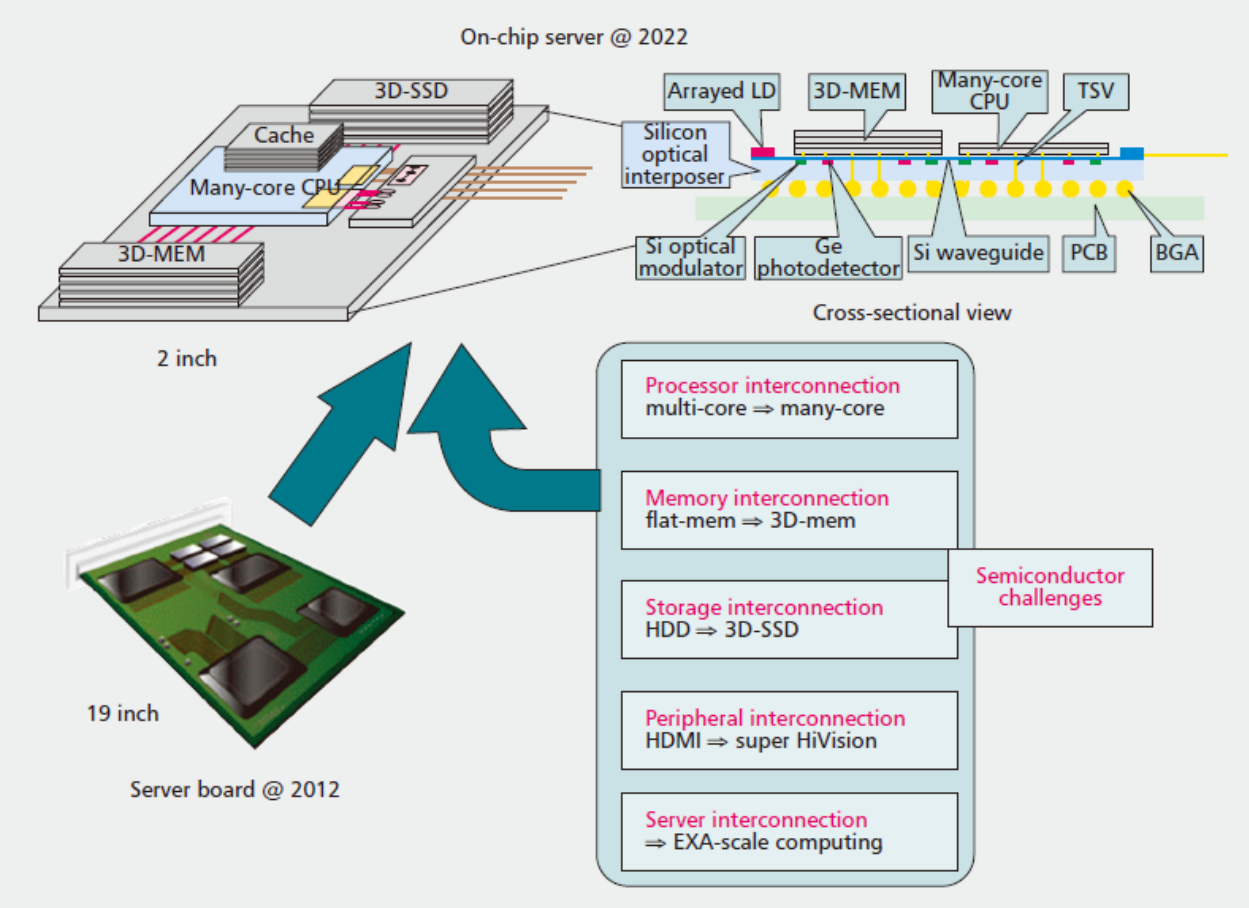


Example WDM link

[Oracle, 2012][32]

On-Chip Server

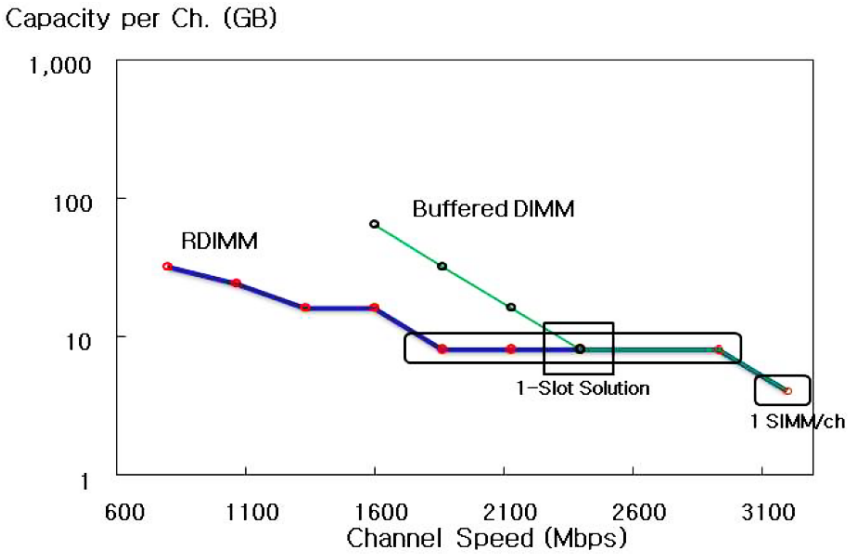
- **Optical interconnection & 3-D interconnections (TSV)**



[Tokyo Univ. & PETRA, 2013][33]

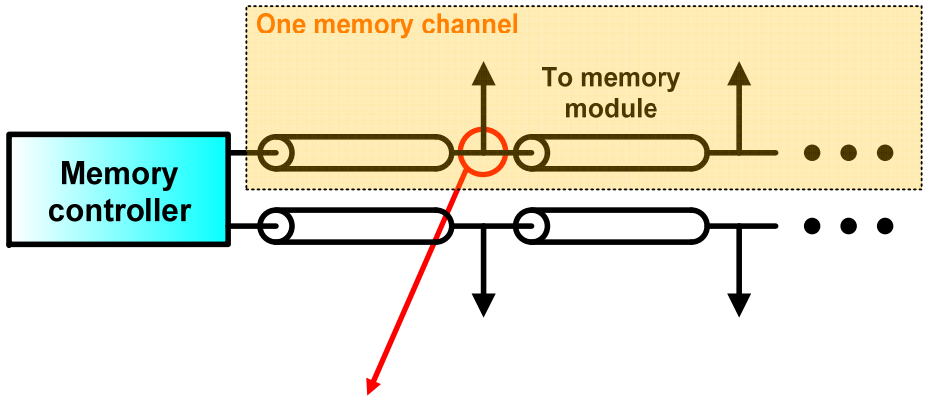
CPU-DRAM Interface

- **Electrical link : bandwidth and capacity tradeoff**



[Samsung, 2013][34]

Multi-drop bus

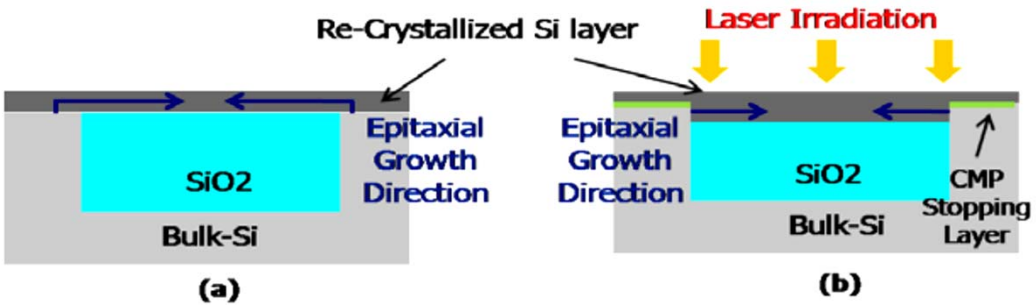


Impedance mismatch
→ degraded signal integrity @ higher data rates

- **Optical interconnection can effectively address this tradeoff !**
- **SOI-based optical platform not compatible with memory process**
- **Rather, bulk CMOS platform is suitable for optical interconnection in memory interfaces.**

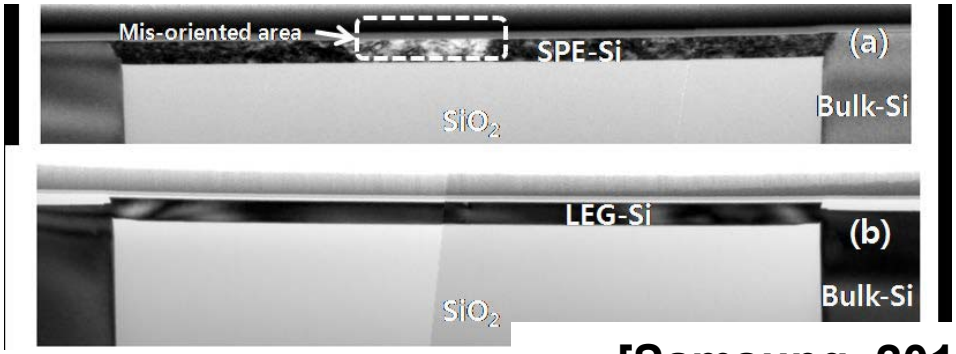
Si-Based Optical Platform

- Good crystallinity is required for low optical propagation loss
- Solid phase epitaxy (SPE): well-know method for crystallization
- Laser-induced epitaxial growth (LEG): relatively new and one of the liquid phase epitaxy (LPE) methods

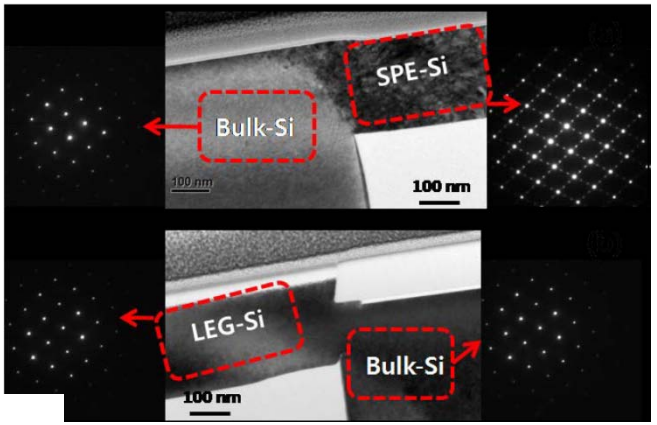


(a) SPE by hot furnace annealing
(b) LEG by high power pulsed laser

TEM image at cross setcion



High resolutionTEM image & diffraction pattern

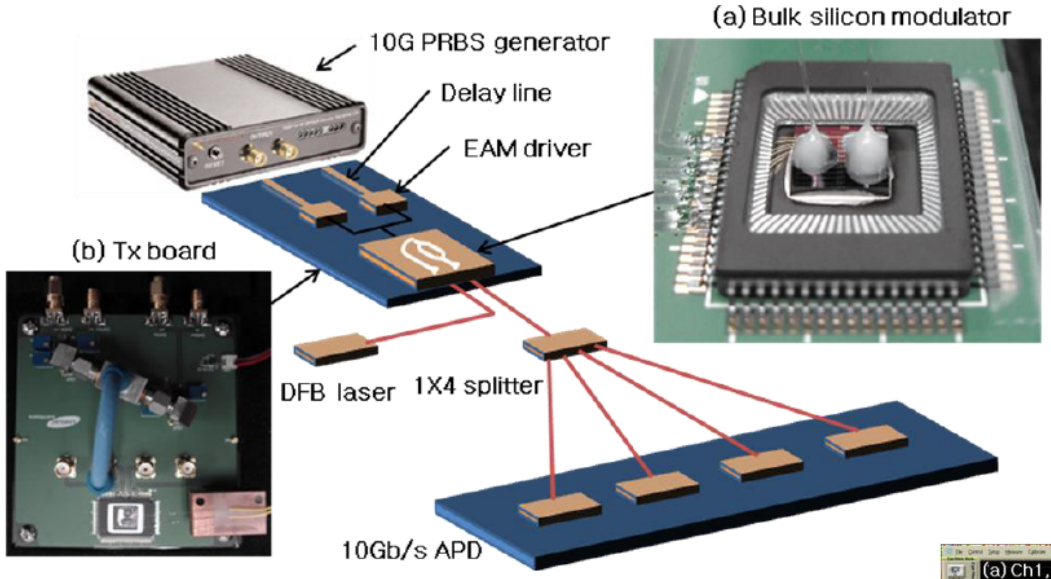


[Samsung, 2013][35]

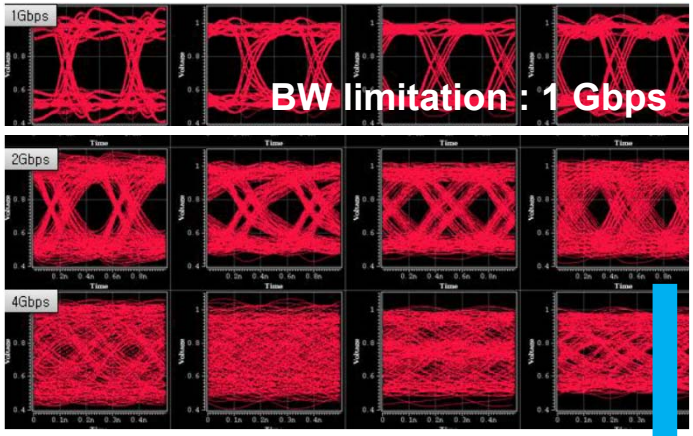
Multi-Drop Bus Memory Interface (1)

- **Bulk silicon modulator**

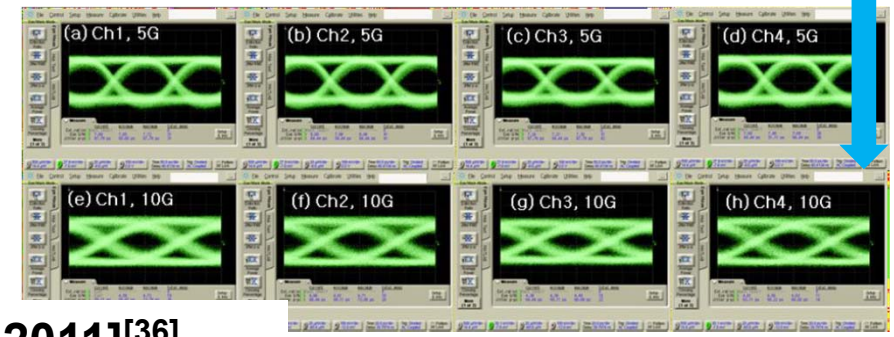
1x4 optical link configuration



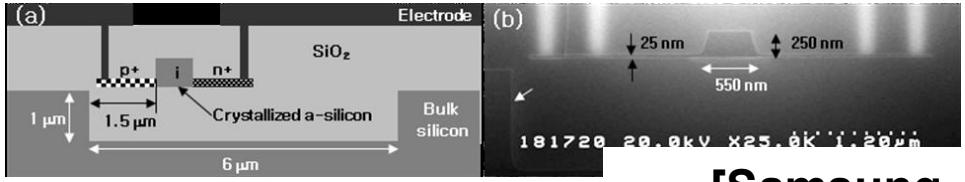
Copper-based memory bus simulation (4 DDR3 modules)



Measured eye in this work



MZI-based modulator (PIN diode)

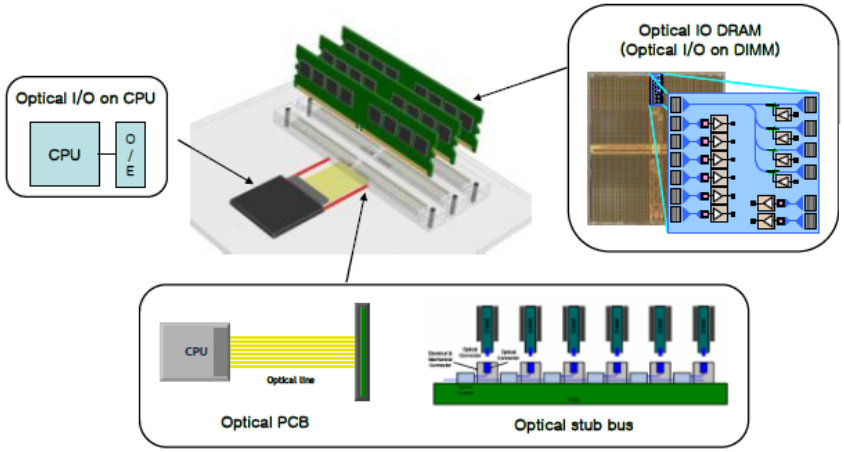


[Samsung, 2011][36]

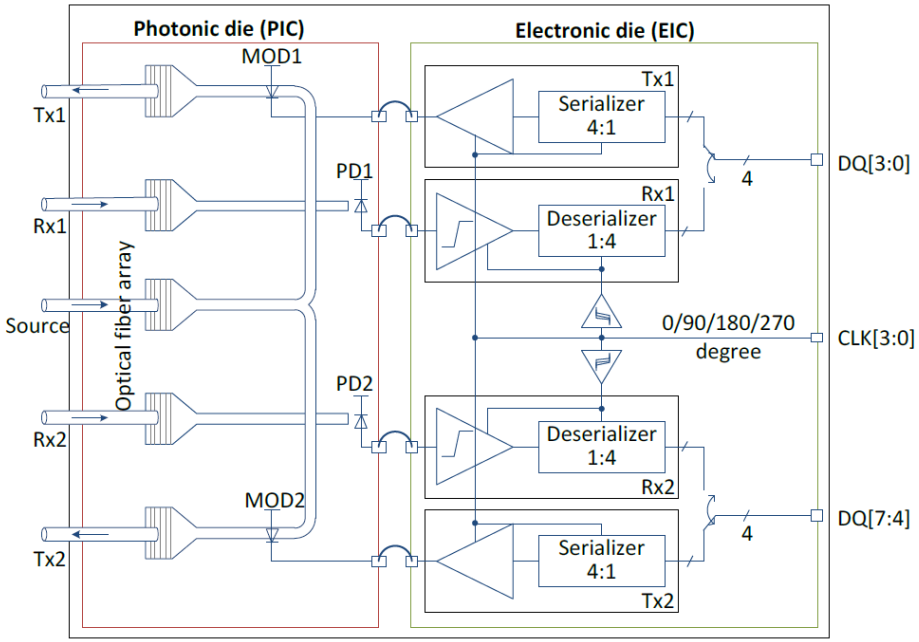
Multi-Drop Bus Memory Interface (2)

- **Hybrid integration of PIC and EIC, both from bulk Si process**

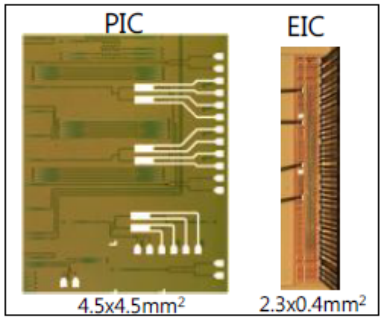
Conceptual scheme of DRAM optical interface to CPU

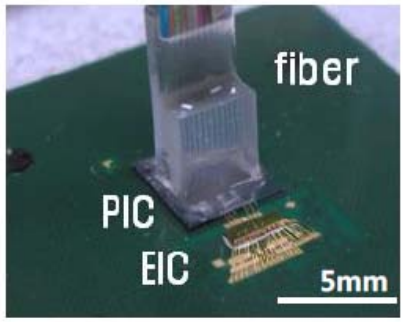


Implemented optical transceiver



Co-packaged optical transceiver chip

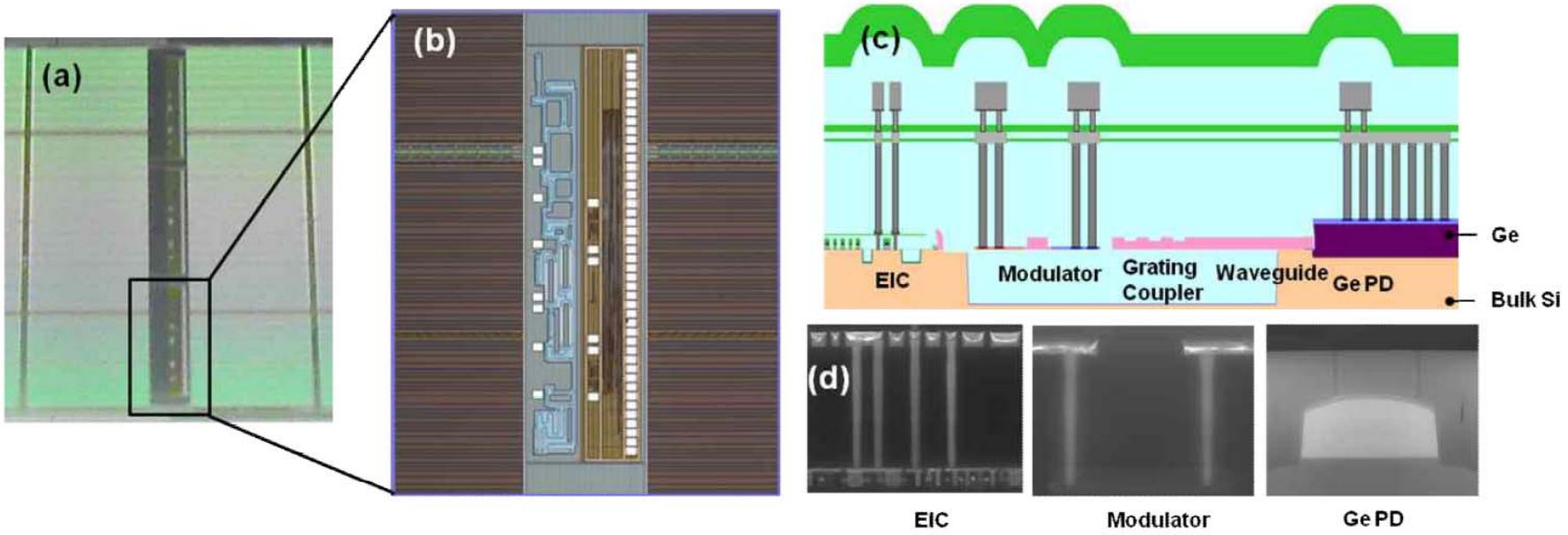




[Samsung, 2013][37]

Multi-Drop Bus Memory Interface (3)

- **Monolithic integration of PIC and EIC : EPIC**

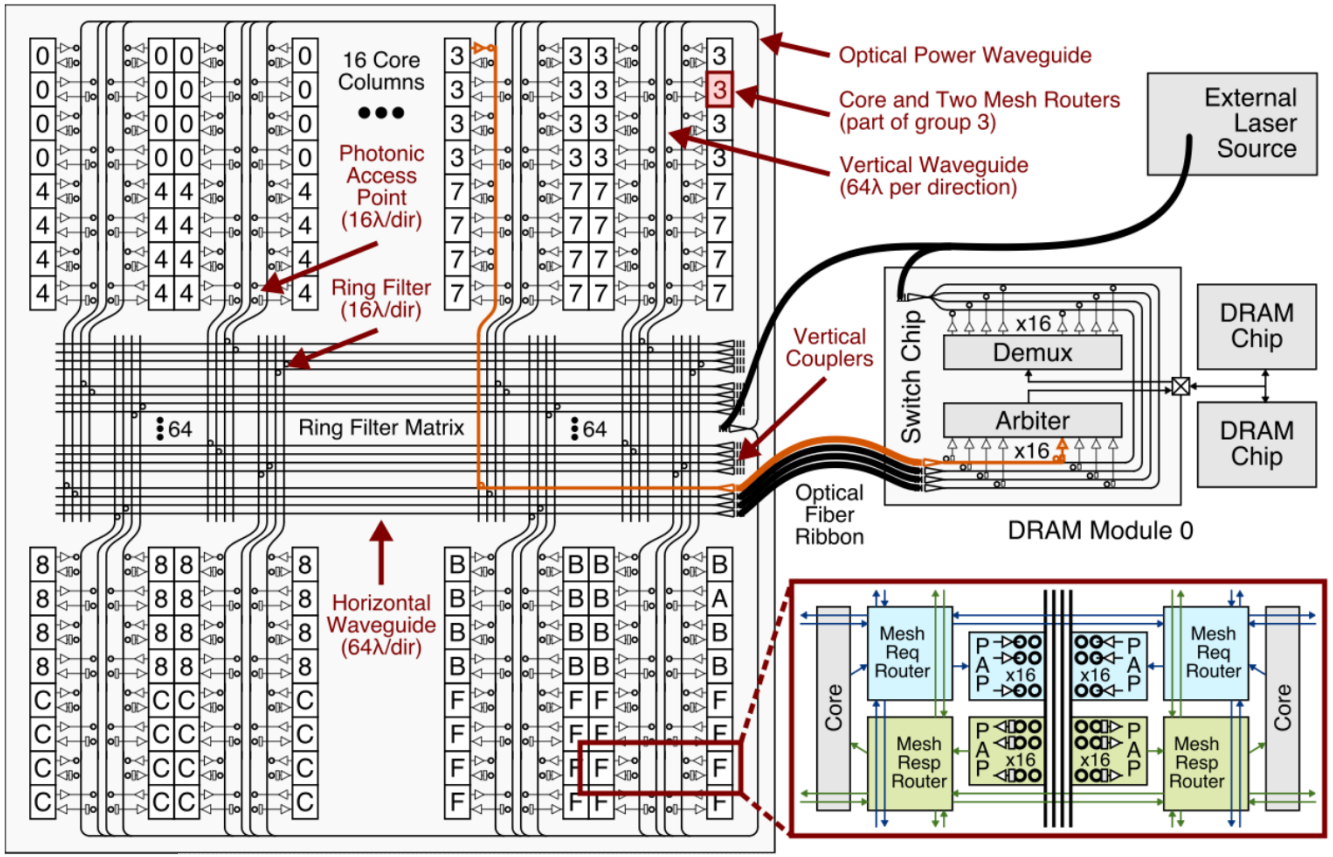


(a) EPIC layout using a DRAM periphery section
(b) Optical microscope image of EPIC
(c) Schematic of EPIC vertical structure
(d) Scanning electro microscope (SEM) images of EIC, modulator, and Ge photodiode

[Samsung, 2013][38]

Manycore Processor Networks

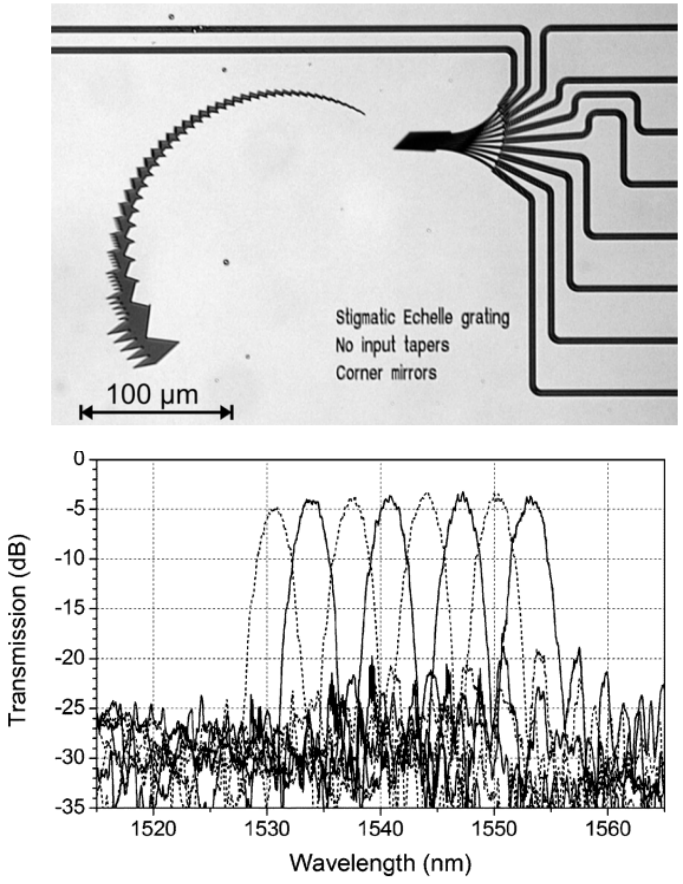
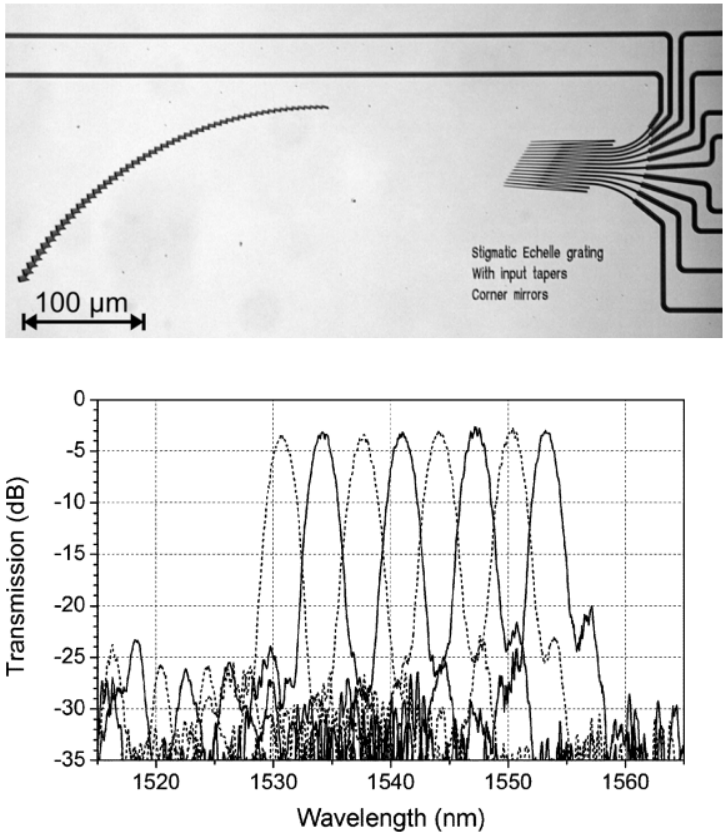
- **256 core processor with a monolithic electro-optical core-to-DRAM shared network**



[MIT & UC Berkeley, 2009][39]

State-of-the-Arts: IBM (1)

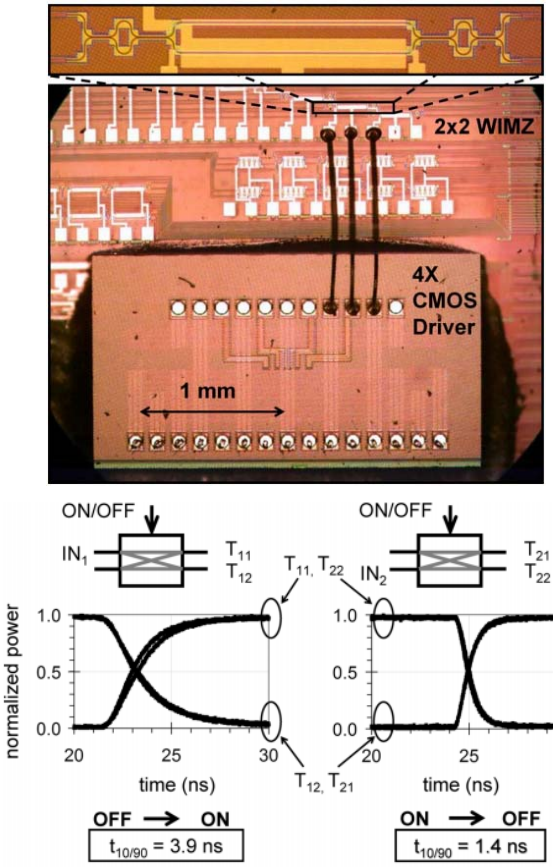
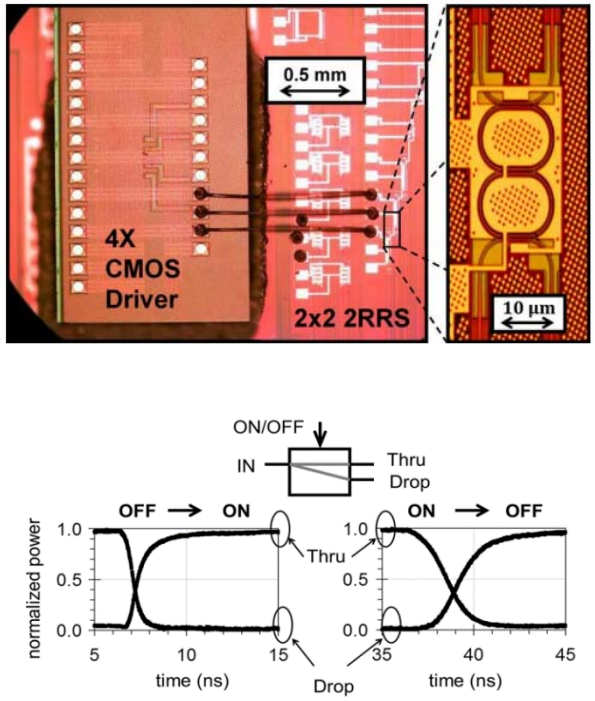
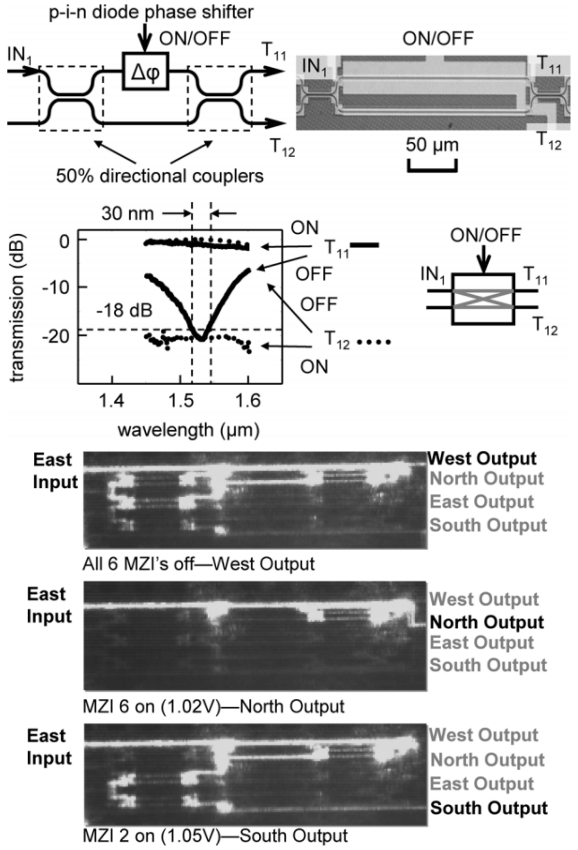
- **WDM DEMUX using Echelle grating**

Extreme echelle grating	Conservative echelle grating
	

[F. Horst et al., Photonics Technology Letters, 2009][40]

State-of-the-Arts: IBM (2)

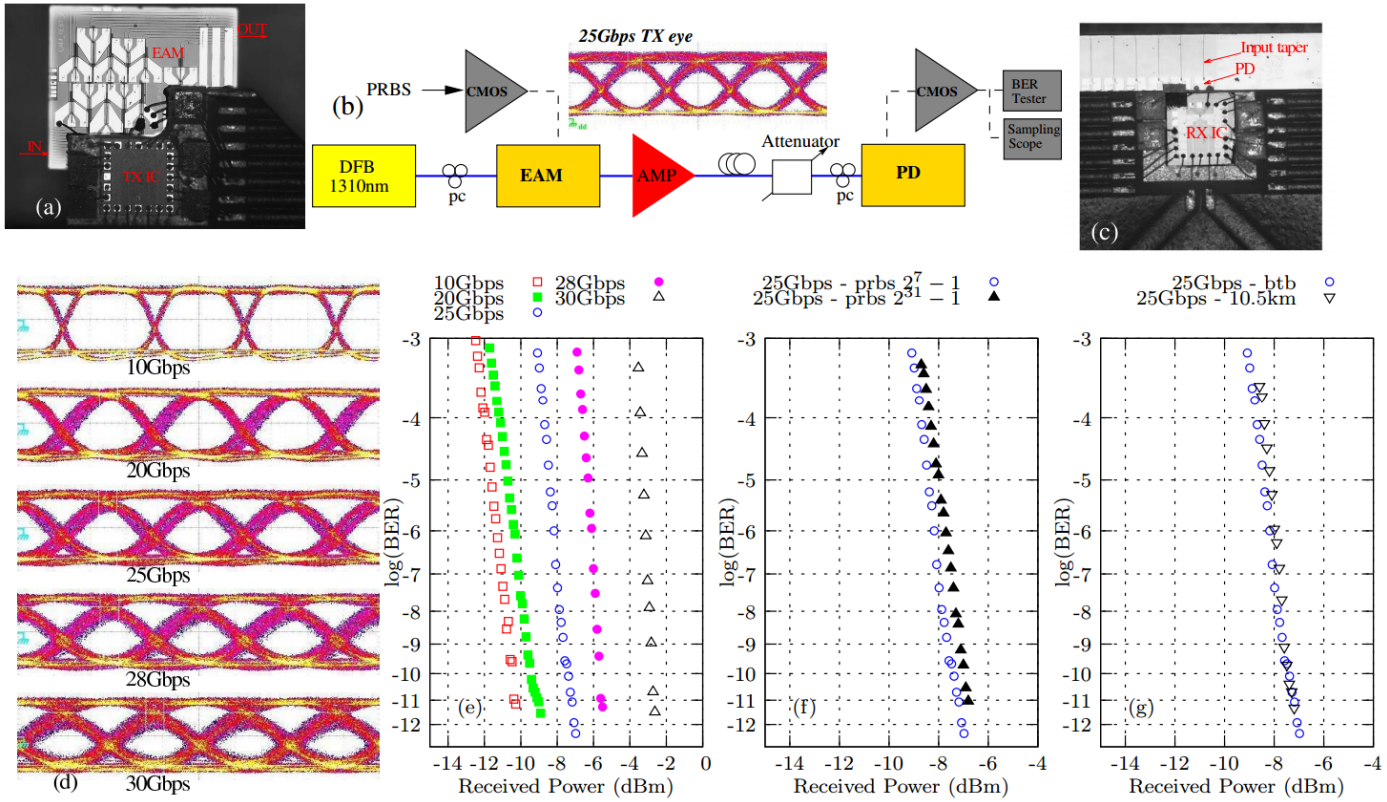
- **Comparison of Wavelength-insensitive MZ switch, 2RRS switch, MZI switch**

WIMZ switch	2RRS switch	MZI switch
		

[A. V. Rylyakov et al, JSSC, 2012][41]

State-of-the-Arts: IBM (3)

- **Optical link integrating heterogeneously III-V/silicon devices with 32nm CMOS electronics**



(a) photograph of the TX assembly

(b) experimental setup for the link also showing a TX optical eye at 25Gbps in inset

(c) photograph of the RX assembly

(d) RX output eyes

(e) sensitivity curves for different data-rates with PRBS7

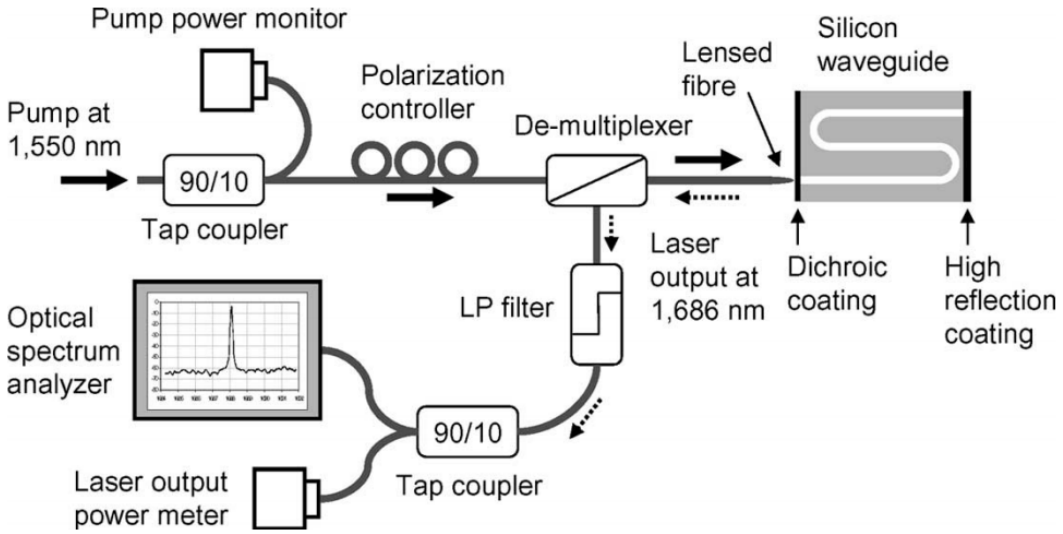
(f) PRBS patterns at 25Gbps

(g) fiber transmission lengths at 25Gbps, PRBS7

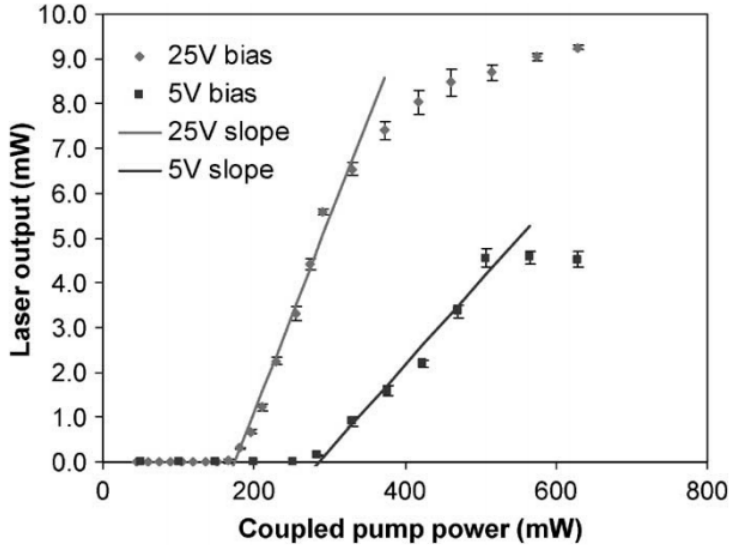
[N. Dupuis et al., OFC, 2014][42]

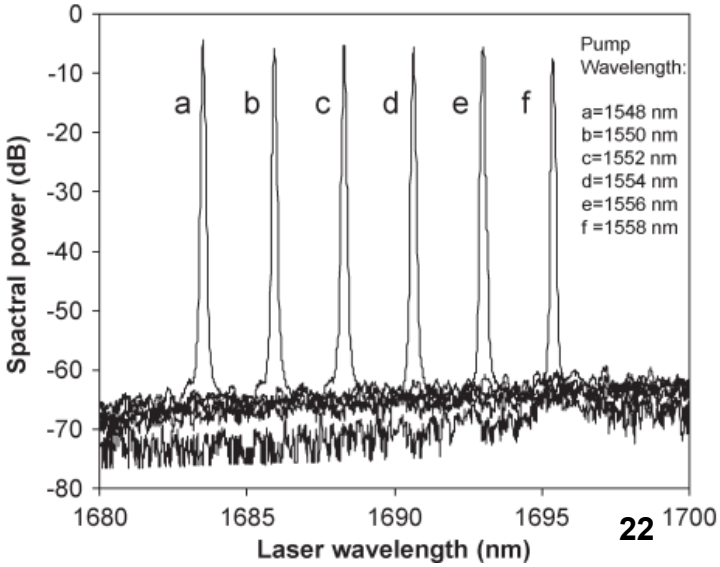
State-of-the-Arts : Intel (1)

- **Continuous-wave, all-silicon Raman laser**
- **CMOS compatible technology**
- **Nonlinear optical absorption due to the TPA-induced FCA is reduced**



[A. Liu et al., J. Lightwave Technology, 2006][43]





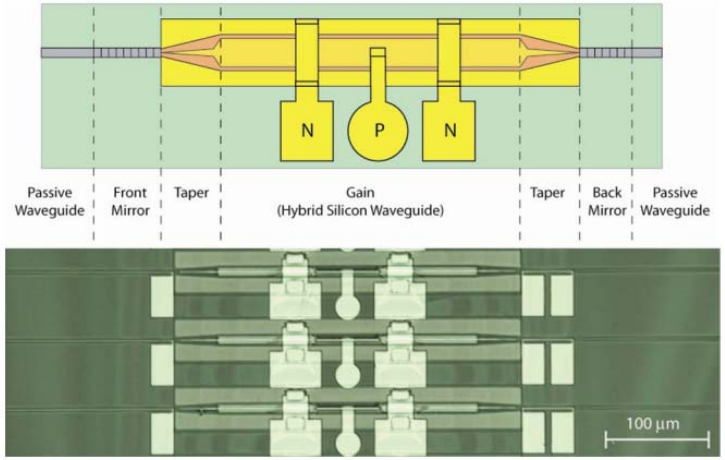
State-of-the-Arts: Intel (2)

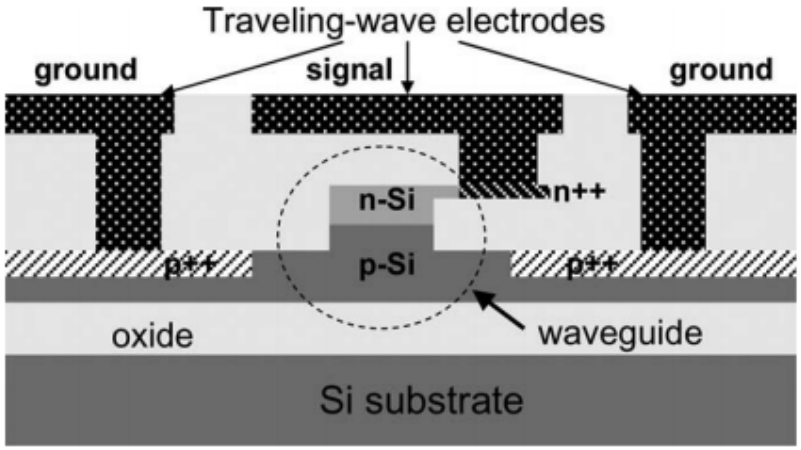
- 25Gbps * 8channel optical link
- Mach-Zehnder modulator
- MZI MUX/DEMUX

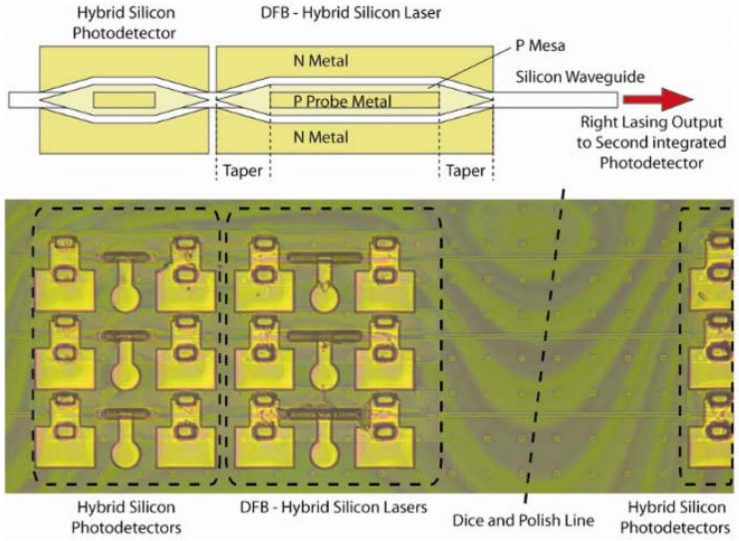
[A. Liu et al., GFP, 2008][44]

State-of-the-Arts : Intel (3)

- **Device and Integration Technology for Silicon Photonic Transmitters**
  - **Hybrid silicon platform enables on-chip lasers to be fabricated**
  - **Silicon modulators and hybrid silicon modulators**



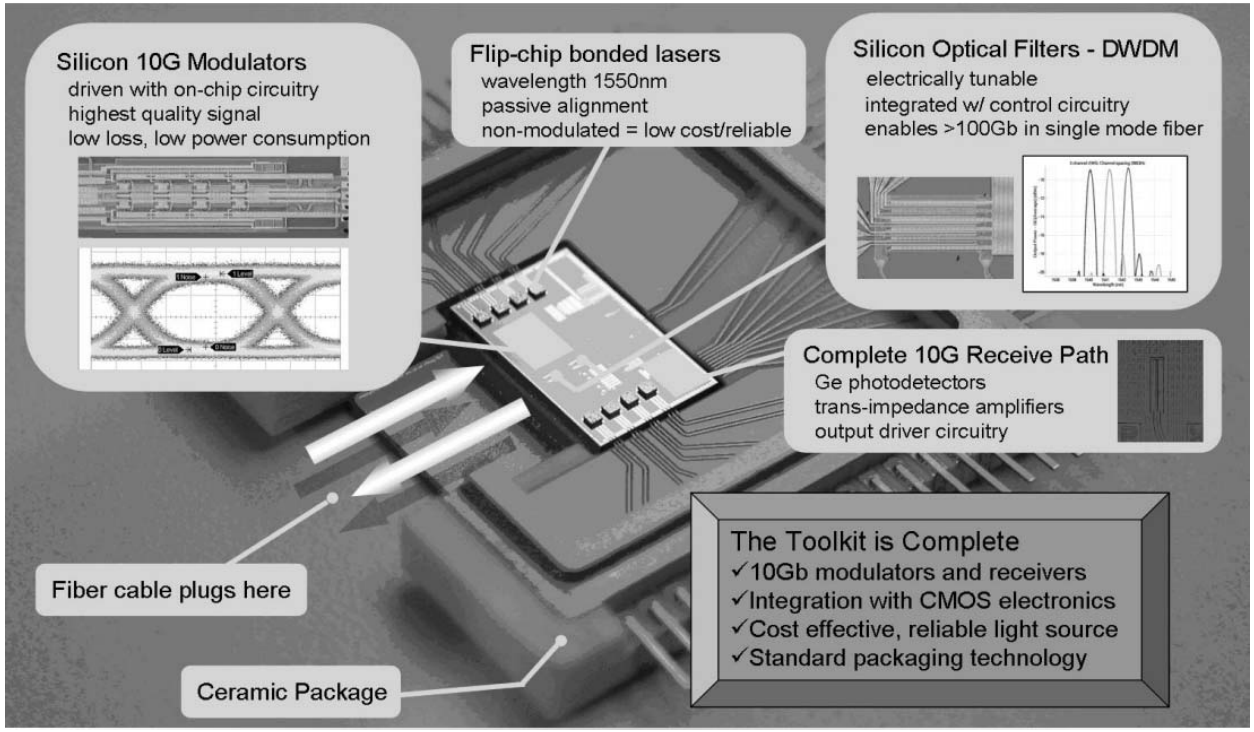




[H. Park et al., JSTQE, 2011][45]

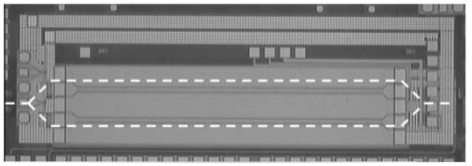
State-of-the-Arts: Luxtera (1)

- **Integrating optical communications into a CMOS platform**

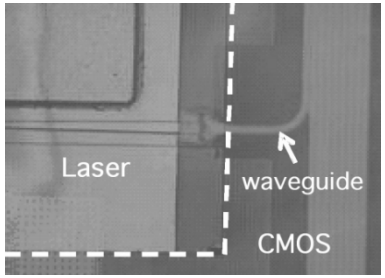


[C. Gunn, IEEE Micro, 2006][46]

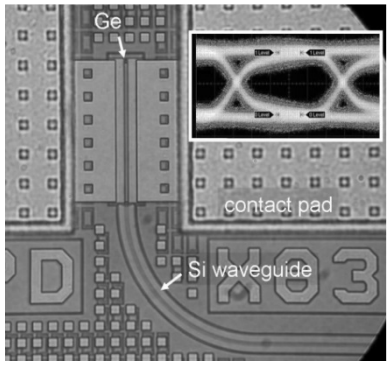
Modulator



Laser

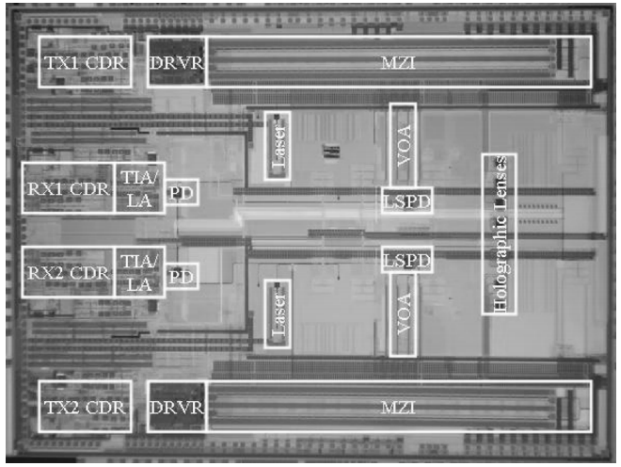


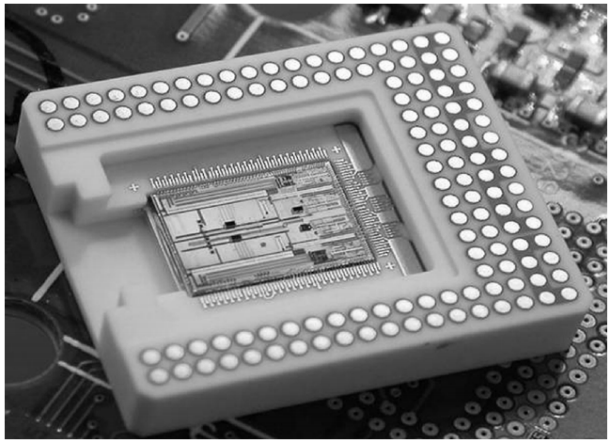
Ge photodetector

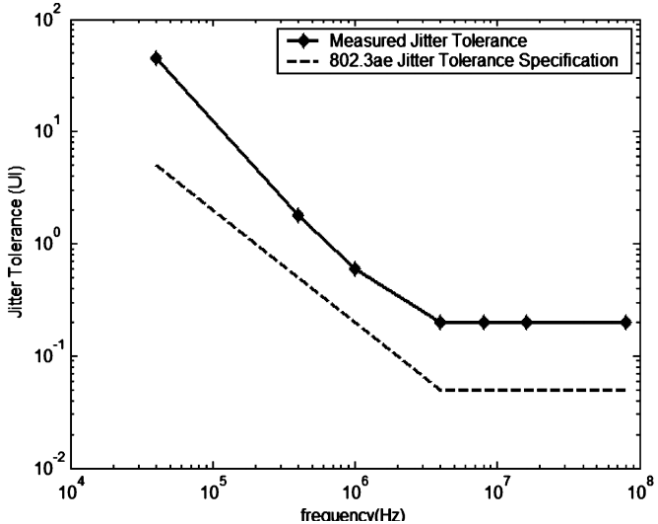


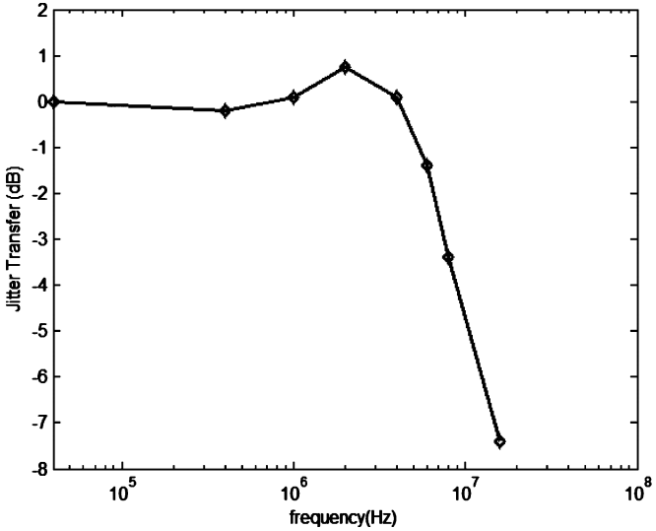
State-of-the-Arts: Luxtera (2)

- 10Gbps * 2channel optical link
- Key optical and electrical components are integrated on a single substrate using a 0.13-um CMOS SOI process





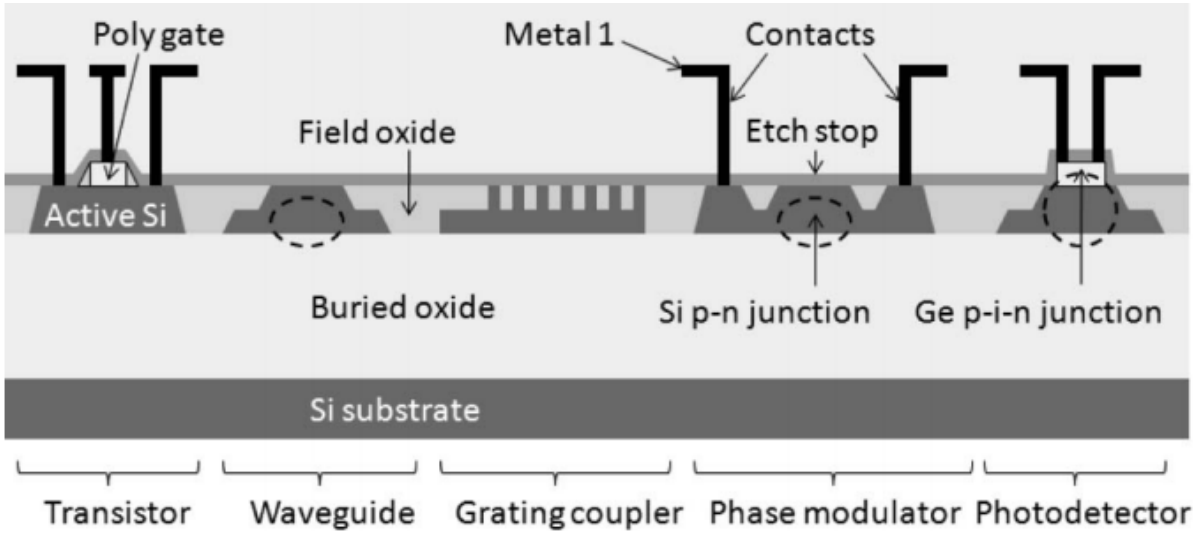


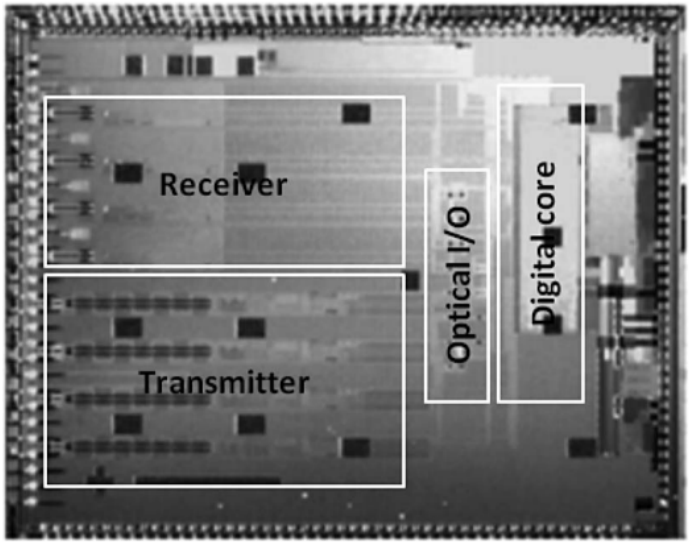


[B. Analui et al., JSSC, 2006][47]

State-of-the-Arts: Luxtera (3)

- Silicon photonics platform that allows monolithic integration with electronic circuits in a CMOS compatible process
- Monolithic integration of 4 X 10Gb/s transceiver

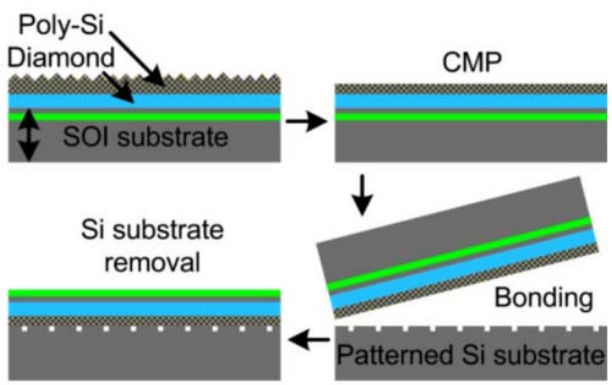


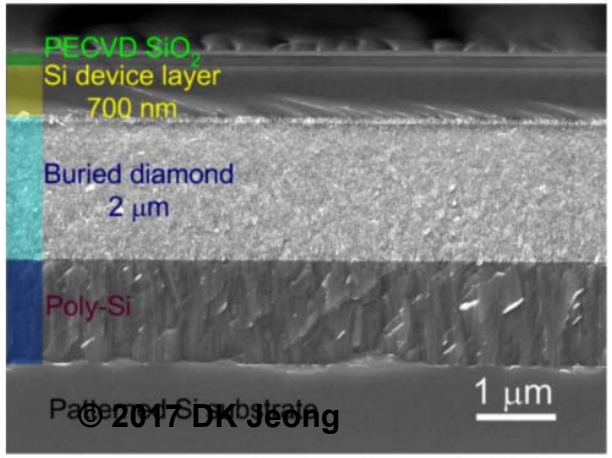


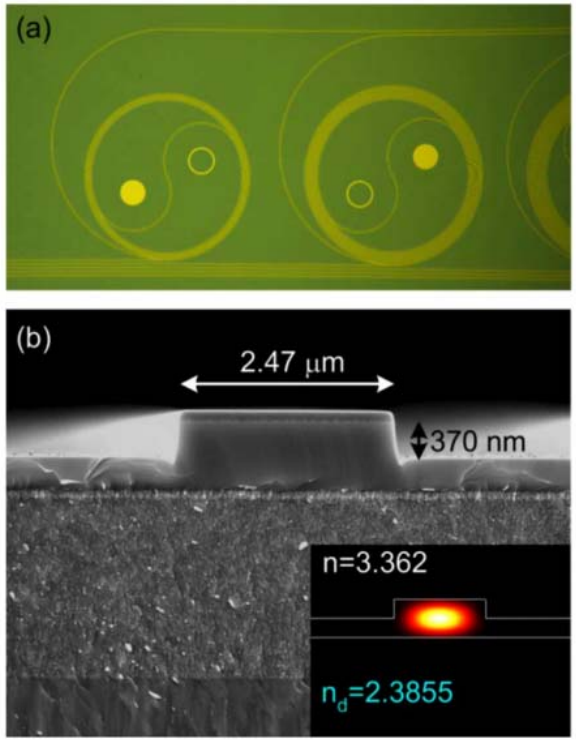
[A. Mekis et al., JSTQE, 2011][48]

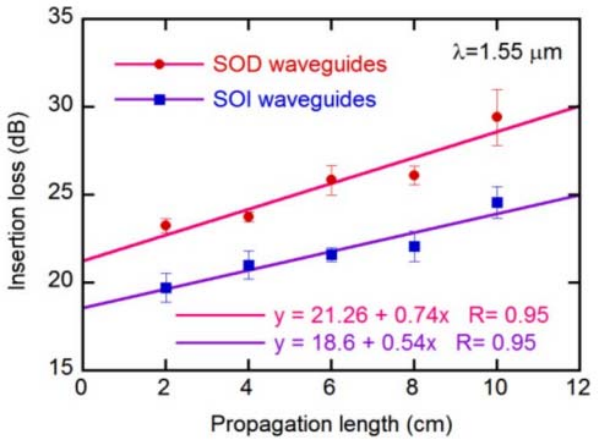
State-of-the-Arts : HP (1)

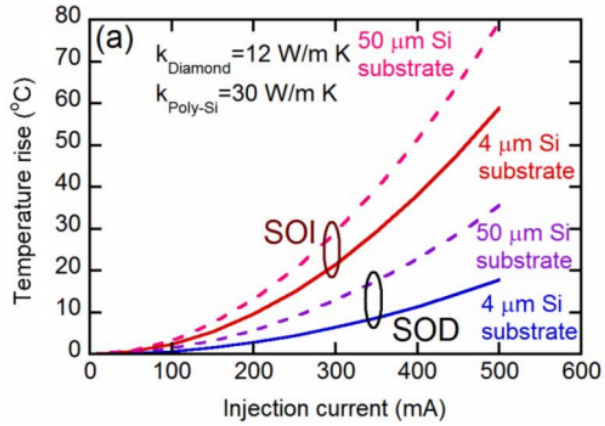
- **Waveguide on Silicon-on-diamond substrate**
- **SOD can replace SOI for photonic devices where heat needs to be extracted efficiently**







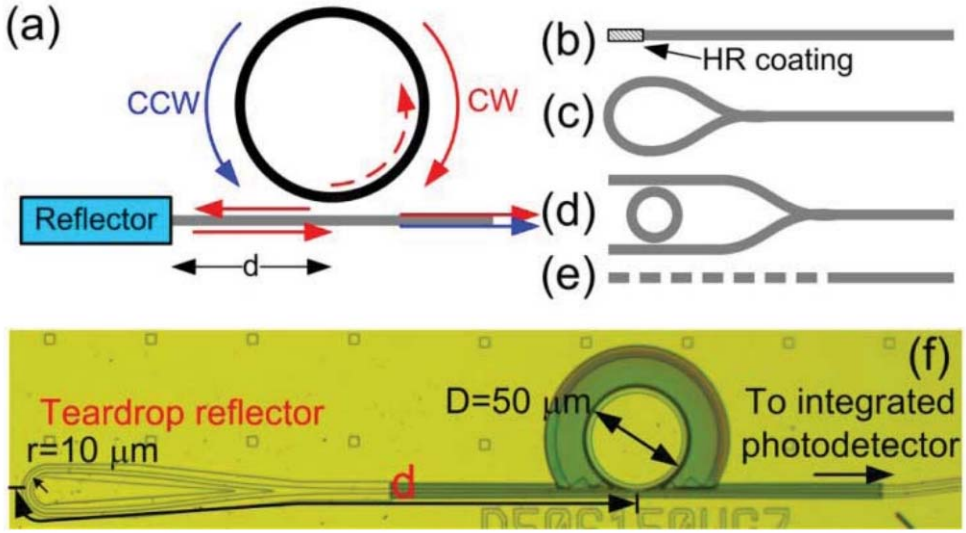




[D. Liang et al., Photonics Technology Letters, 2011][49]

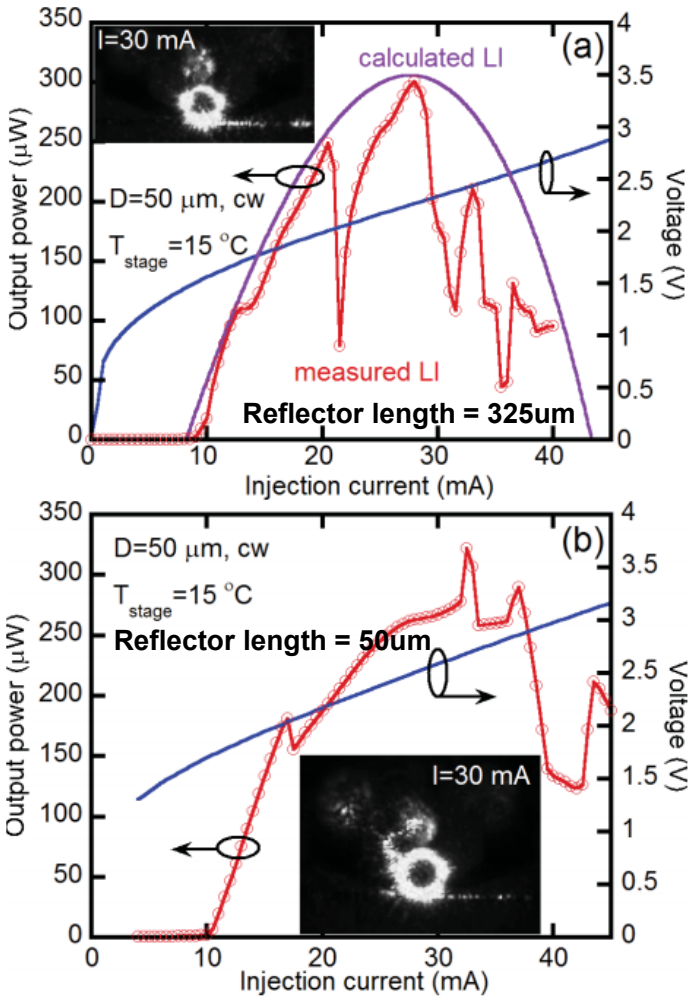
State-of-the-Arts: HP (2)

- **Study about hybrid silicon microring laser using tear drop reflector**



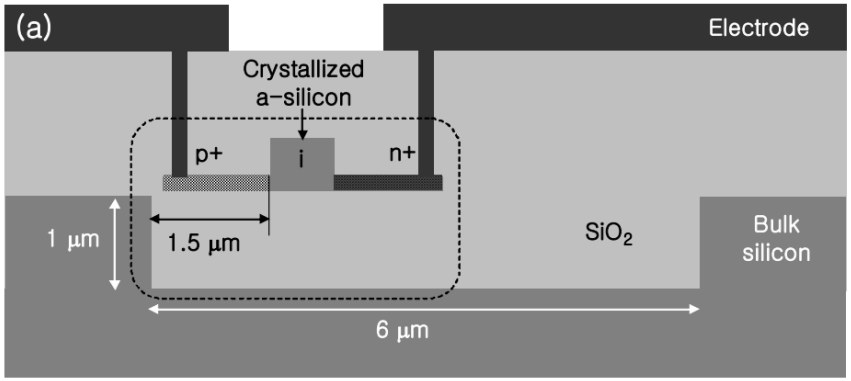
(a) Schematic of a ring laser with an external reflector integrated on the bus waveguide
(b)~(e) Schematic of various passive reflector designs
(f) Image of a fabricated hybrid silicon microring laser with tear-drop reflector

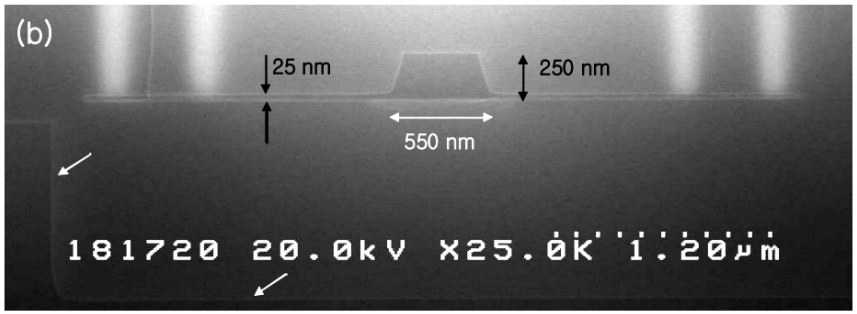
[D. Liang et al., Photonics Technology Letters, 2012][50]

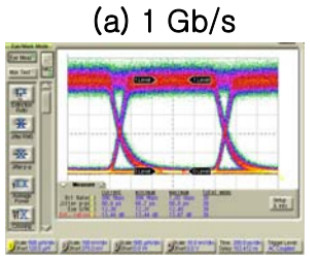


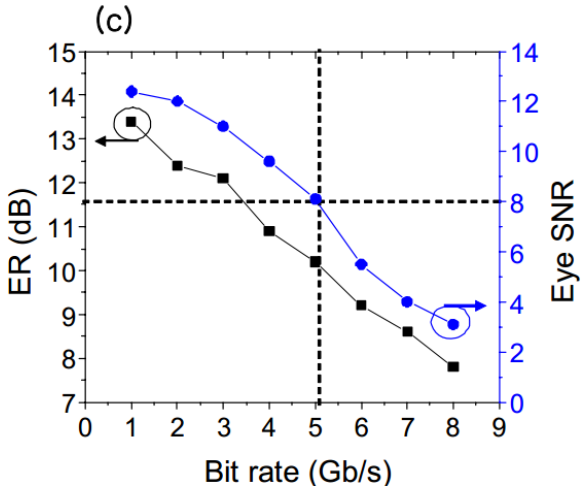
State-of-the-Arts : Samsung (1)

- **Bulk silicon MZM based on local oxide undercladding and amorphous silicon layer crystallized in the solid phase epitaxy**
- **Ultimate target : on-die integrated DRAM optical interface**





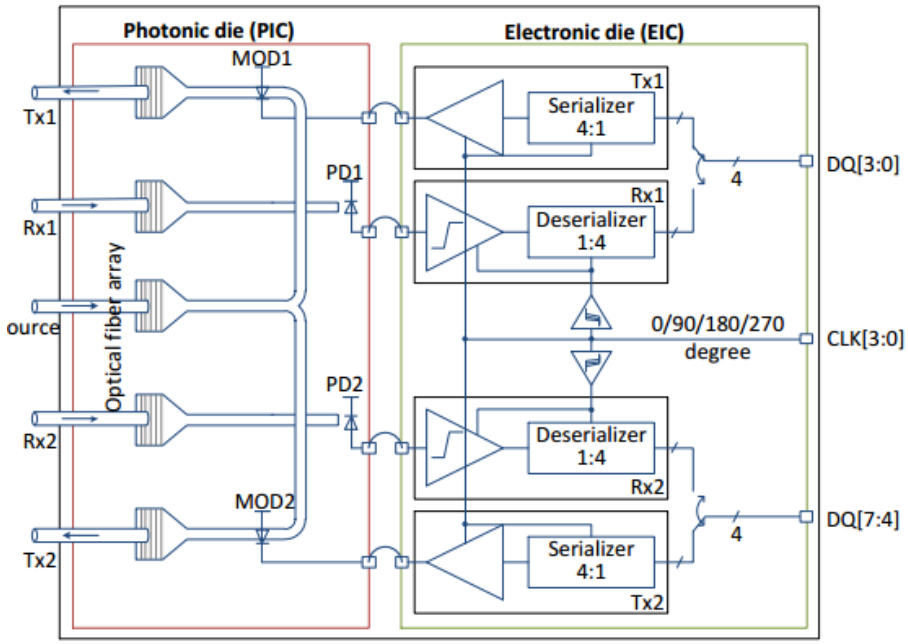


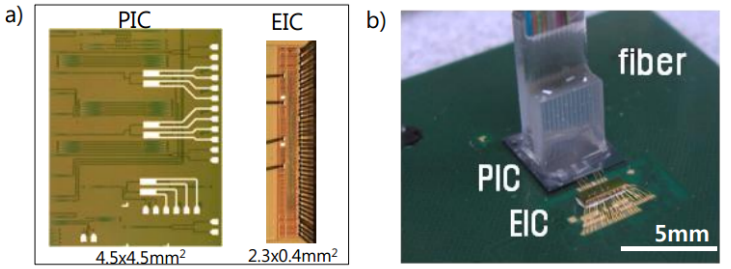


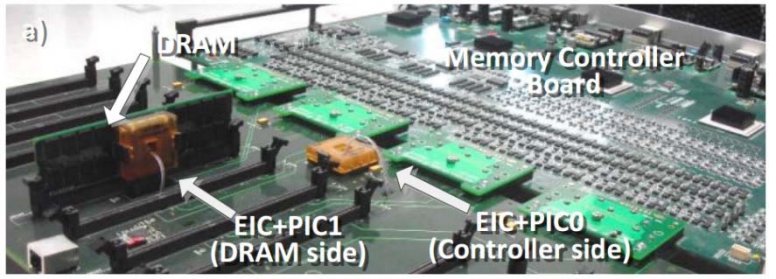
[D.J. Shin et al., GFP, 2010][51]

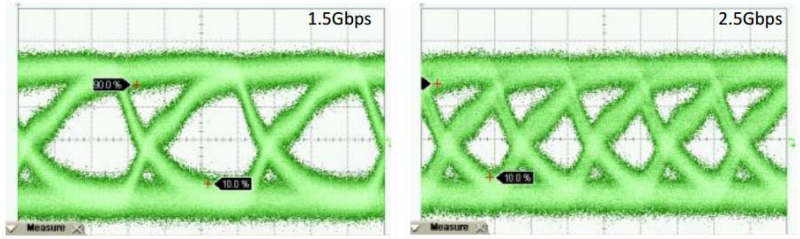
State-of-the-Arts: Samsung (2)

- Optical transceivers based on bulk-Si wafer using DRAM compatible process
- Transceiver chips are verified to work for DDR3 DRAM





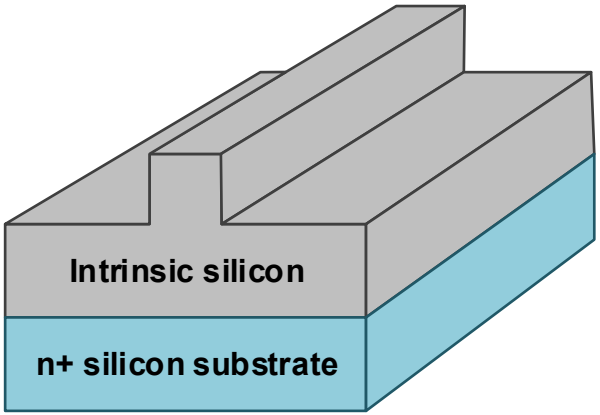




[H. Byun et al., GFP, 2013][52]

Waveguide Development

Silicon on doped silicon



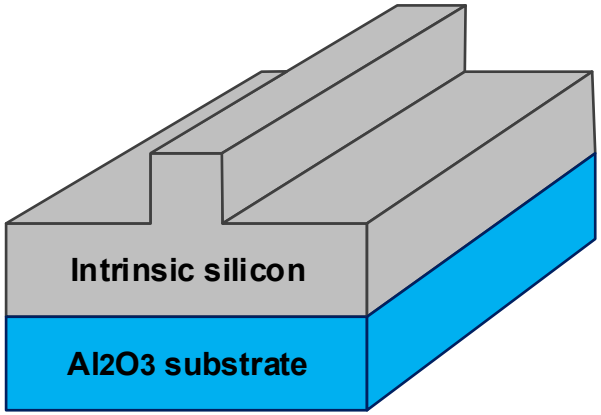
RI of intrinsic silicon = 3.5

RI difference (doping silicon) = 10^{-3}~10^{-1}

Soref & Lorenzo,

Electronics letters, 1985

Silicon on sapphire

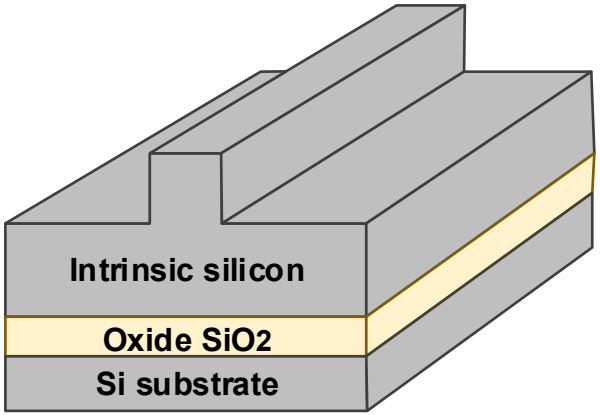


RI of sapphire = 1.76

Albares & Soref,

Proc. SPIE, 1987

Silicon on Insulator (SOI)

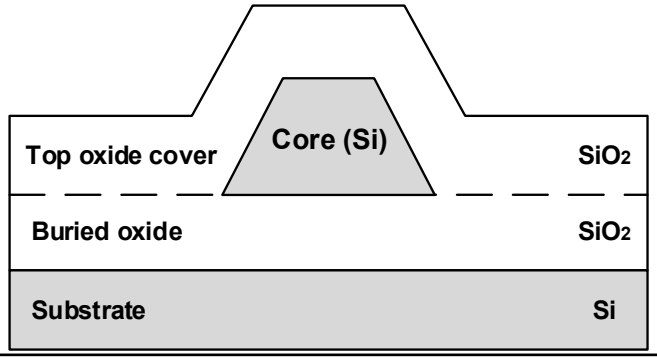
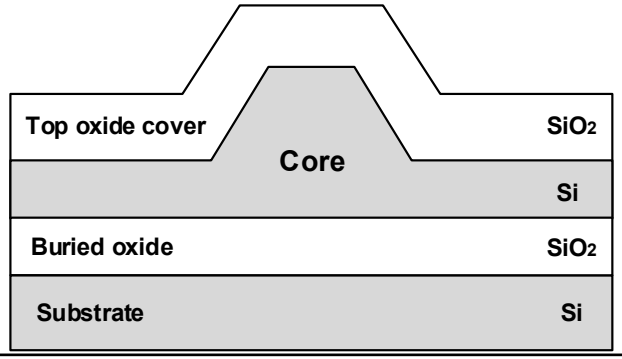
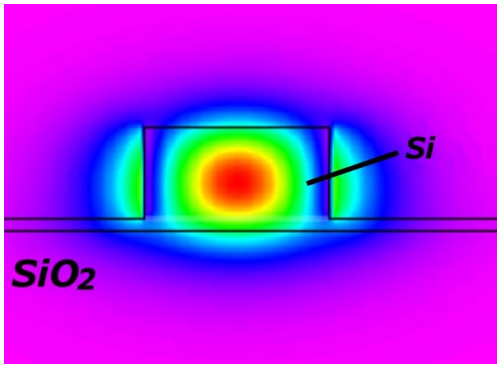
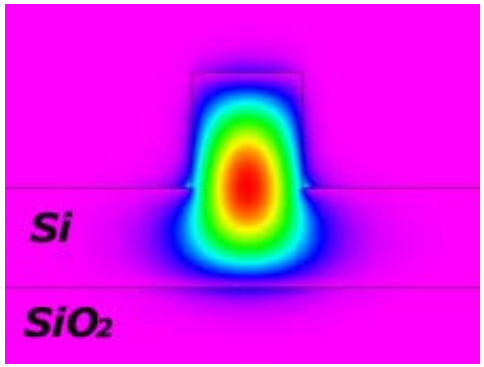


RI of silicon dioxide = 1.5

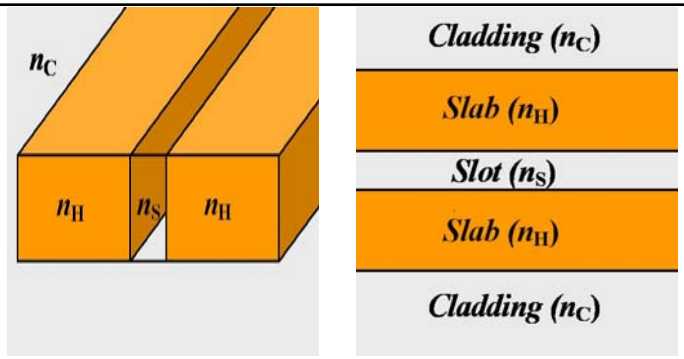
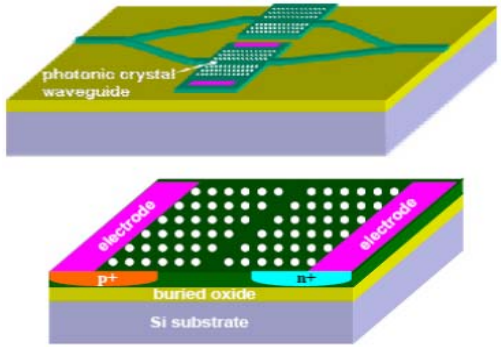
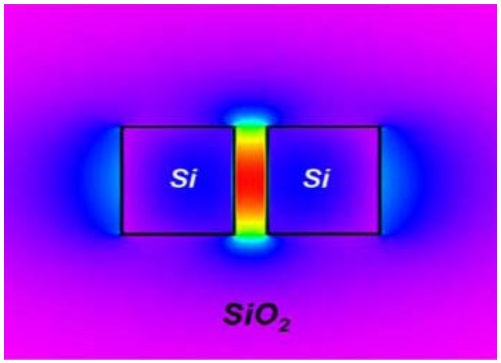
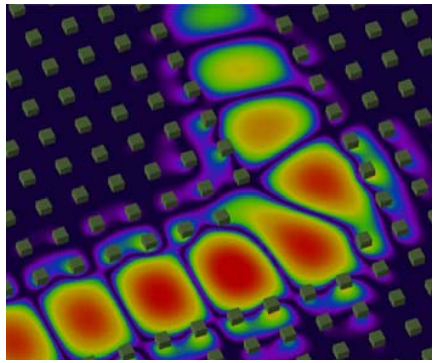
Soref & Lorenzo,

OSA Integrated Guided Wave Optics, 1989

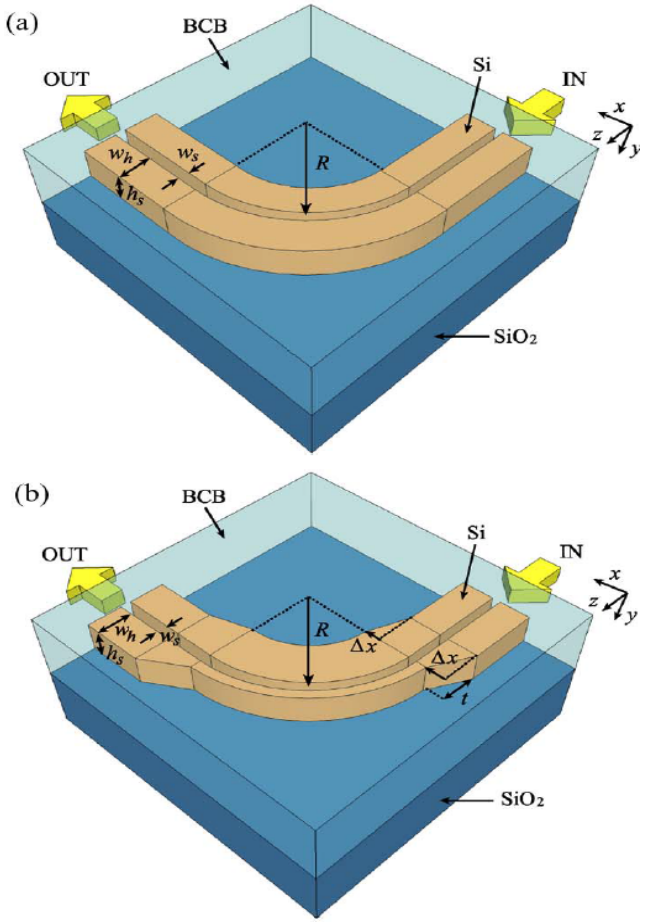
Representative SOI Waveguides

Strip waveguide	Rib / Ridge waveguide
	
	
• More compact • Higher loss, 2~3 dB/cm	• Less compact • Lower loss, 0.1 dB/cm

Representative Waveguides

Slot waveguide	Photonic crystal waveguide
	
	
• Strong light confinement in slot	• Lattices guide light

Bending, Crossing in Waveguide



[Photonics Journal Ishizaka 2013]

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Topics in IC Design

8.6 Silicon on Insulator

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2017 Spring

Contents

1. SOI vs. Bulk Silicon

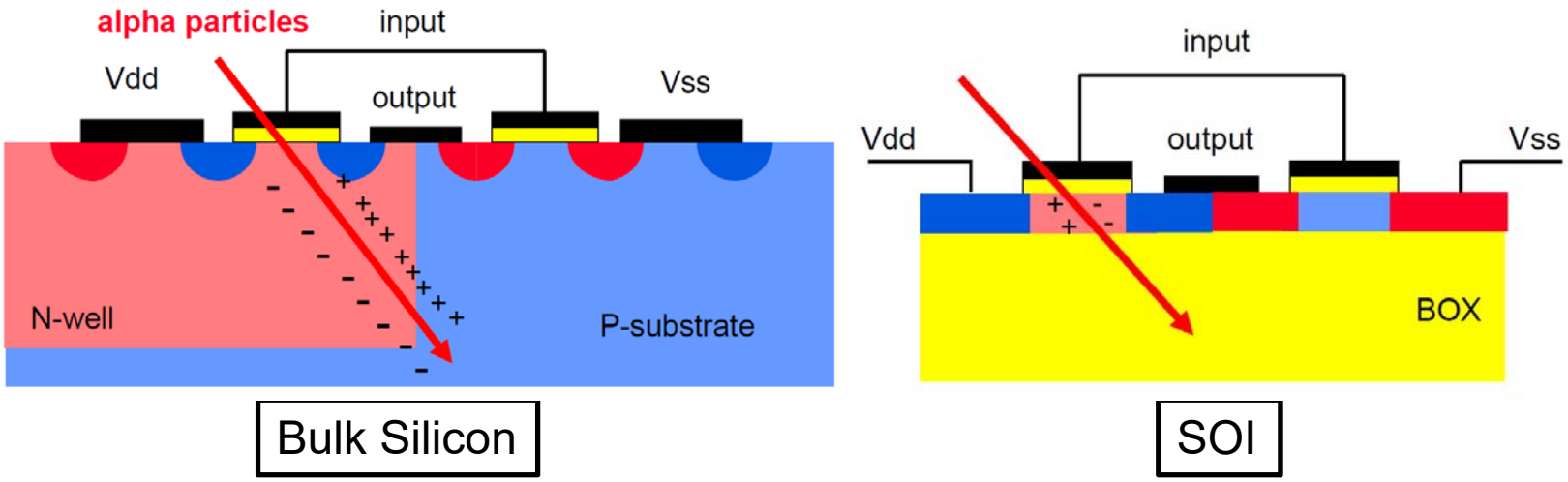
2. SOI Fabrication Process

3. Two Kinds of SOI
   - Partially Depleted SOI
   - Fully Depleted SOI

4. SOI CMOS

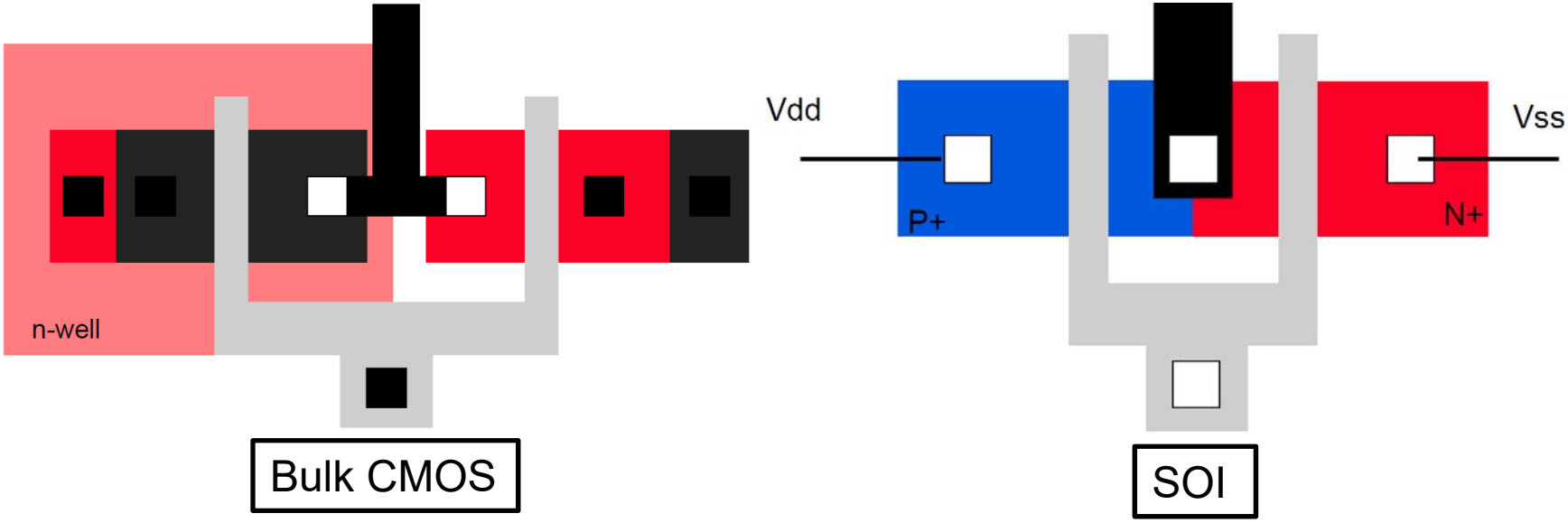
Contents

SOI vs Bulk Silicon(1)



- **Compared to Bulk Silicon,**
  - **SOI has no latchup.**
  - **SOI has low soft error rate.**
  - **High density**
  - **Low leakage current**

SOI vs Bulk Silicon(2)



- **SOI has simpler layout.**

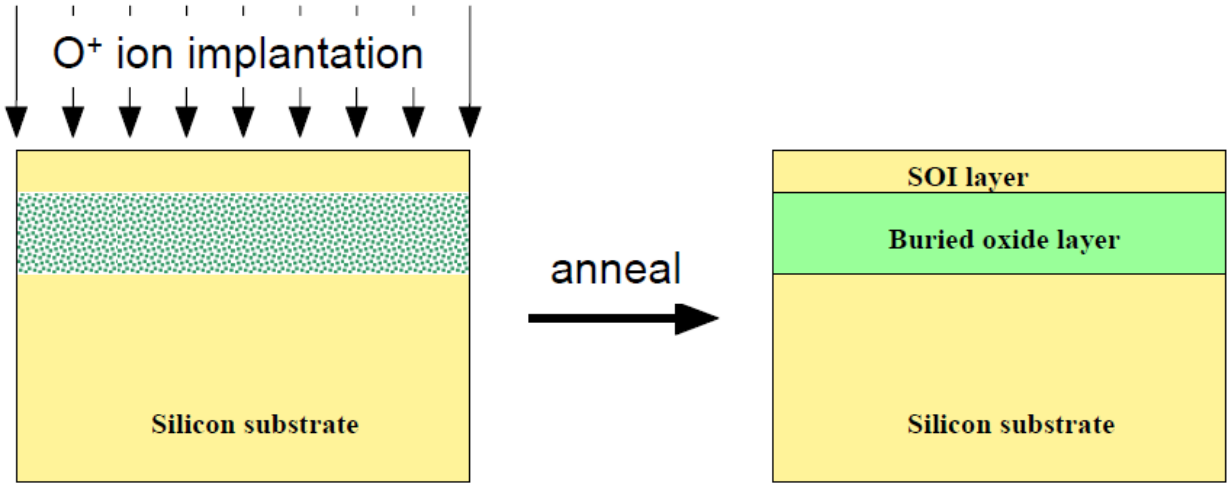
SOI vs Bulk Silicon(3)

Bulk:	*Silicon On Insulator:*
• *Higher Power than SOI*	• *Reduced Power (30-40%) vs. Bulk*
• *Moderate performance*	• *Performance 15-20% better than bulk*
• *Large xstor tubs*	• *Small xstor tubs*
• *Large capacitance*	• *Reduced capacitance*
• *High leakage current*	• *Low leakage current*
• *Moderate heat dissipation*	• *Self Heating effects*
• *Defined threshold*	• *Variable threshold (includes "kick start" effect)*
• *Lower I_D currents*	• *Higher I_D currents*

- *Bulk CMOS is beginning to experience scaling difficulties in the area of higher leakage currents as dimensions move further into the VDSM space*
- *Floating Body Effects are easily modeled with today's EDA Tools*
- *The threshold variation due to the Floating Body Effect is completely acceptable given the gains in performance benefits*

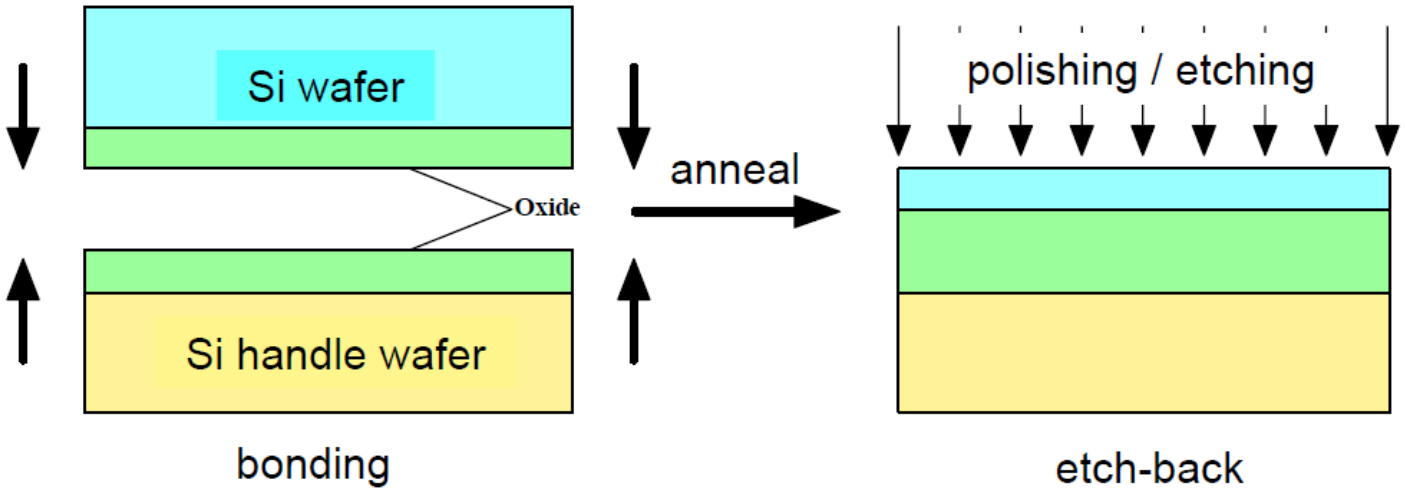
SOI Fabrication Process

- **SIMOX : Separation by ion Implantation of Oxygen**
  - **Demonstrated In 1978 by Izumi et al.**
  - **Dominant SOI technology**



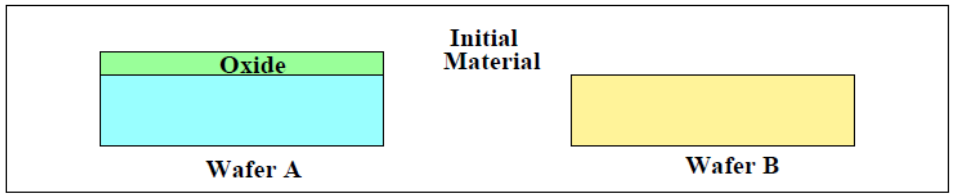
SOI Fabrication Process

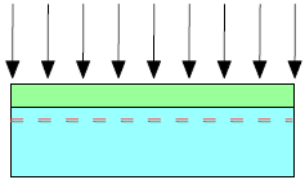
- **BESOI: Bonded and Etch-back SOI**
  - **Two oxidized wafers are bonded and annealed.**



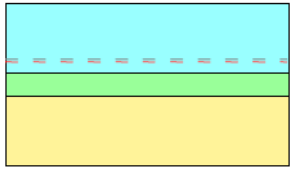
SOI Fabrication Process

- **Smart Cut**



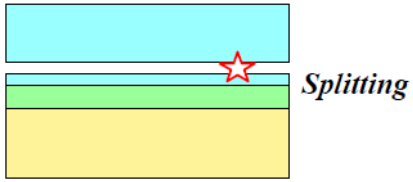


Step 1: Hydrogen implantation into wafer A

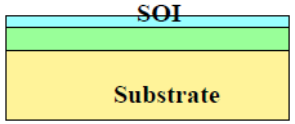


Step 2: Cleaning and bonding of wafer A and B

low temp (400-600C)
high temp (>1000C)



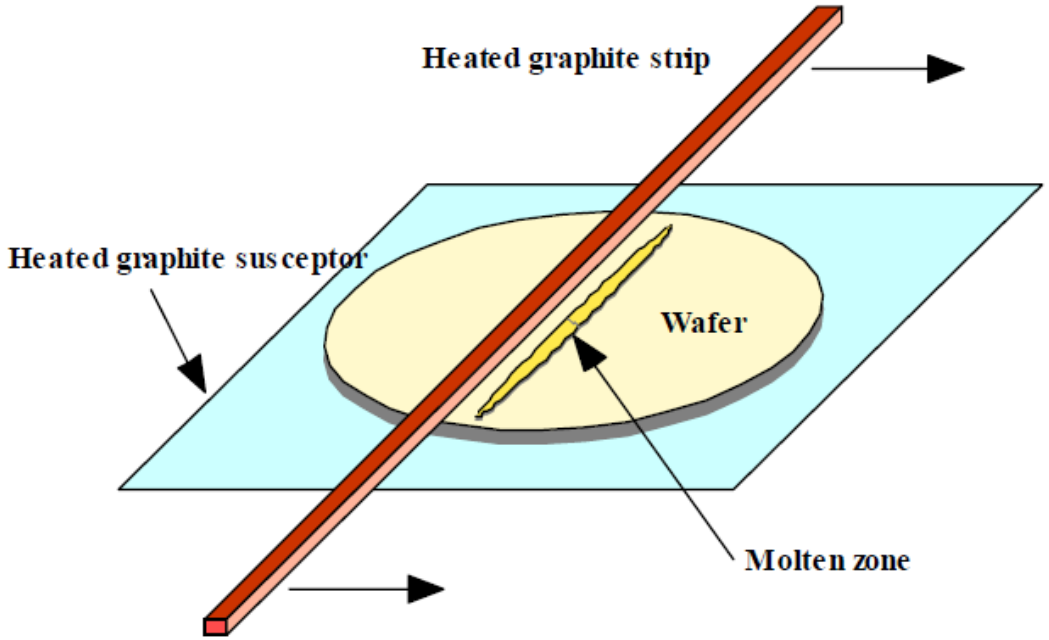
Step 3: Thermal treatment



Step 4: Touch polishing

SOI Fabrication Process

- **ZMR(Zone-Melting Recrystallization)**



Two Kinds of SOI

- **Partially Depleted SOI & Fully Depleted SOI**
  - **Partially Depleted(PD SOI)**
    - **Floating Body and Body Ties Possible**
  - **Fully Depleted(FD SOI)**
    - **No Floating Body and No Body Ties Needed.**

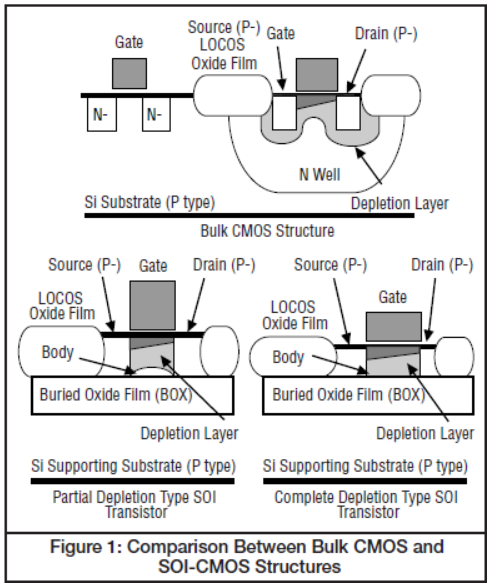
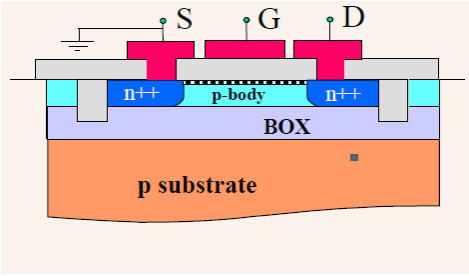
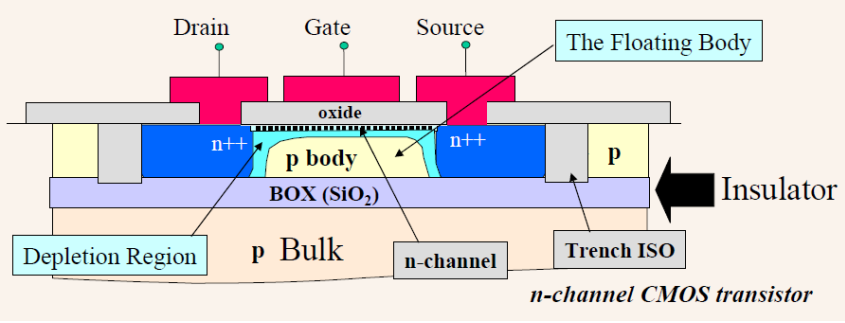


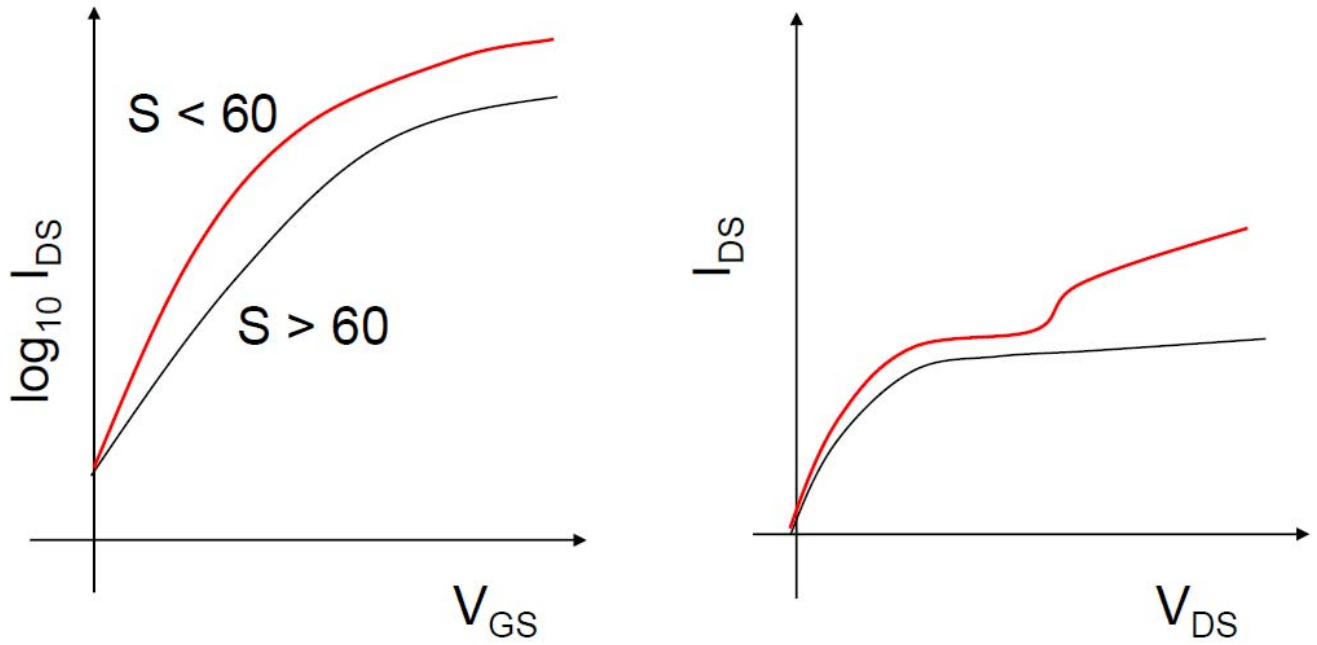
Figure 1: Comparison Between Bulk CMOS and SOI-CMOS Structures





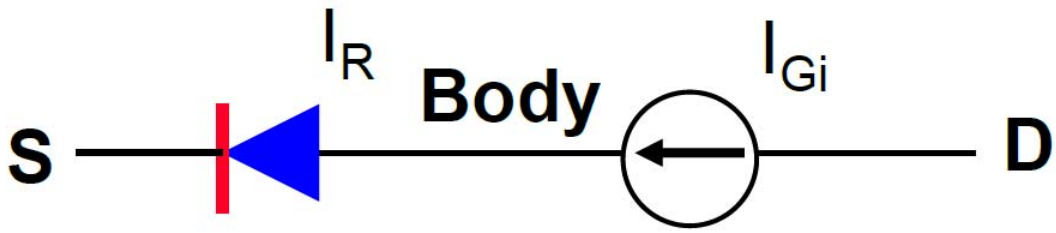
PD-SOI MOSFET(1)

- **Kink Effect**
  - **It is created due to the floating body.**



PD-SOI MOSFET(2)

- **DC Analysis**



$$I_R(V_{BS}) = I_{Gi}(V_{DS})$$

$$I_{R0} e^{qV_{bs}/kT} = (M-1) I_{CH}$$

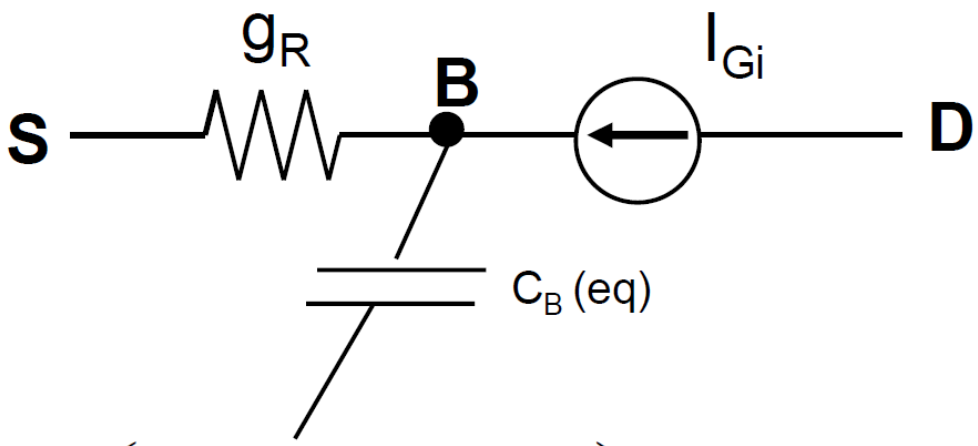
$$(M-1) \sim e^{-B/V_{DS}}$$

- thermal generation
- impact ionization
- junction tunneling
- GIDL

PD-SOI MOSFET(3)

- **AC Analysis**

Small signal ac conditions:



$$V_{bs}\left(g_D + j\omega C_B(eq)\right) = I_{Gi}(V_{DS})$$

s.s. equivalent circuit is frequency dependent!

FD-SOI MOSFET(1)

- **No Klink Effect**
  - **Can be used as normal Bulk Si.**
  - **However, it is unclear that long channel technology can be processed by FD-SOI.**

FD-SOI MOSFET(2)

- **Fully-Depleted SOI CMOS for Analog Applications**
  - **Pass Gate**
  - **Operational Amplifier**
  - **Microwave Circuit(High frequency)**

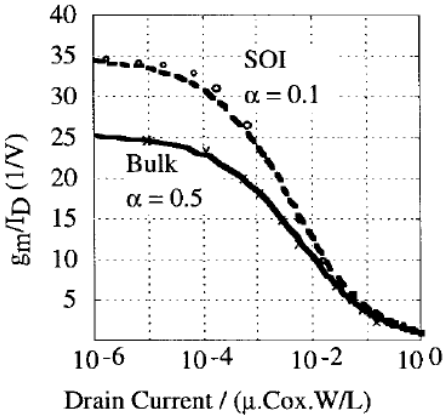


Fig. 1. g_m/I_D ratios in saturation ($V_D = 2.5$ V) for bulk ($n = 1 + \alpha = 1.5$) and FDSOI ($n = 1 + \alpha = 1.1$) MOSFET's.

TABLE II
PERFORMANCES AND CHARACTERISTICS OF MICROWAVE n-CHANNEL SOI MOSFET's: (*) T-GATE TECHNOLOGY IS USED, (◇) WITH METAL SHUNT ON THE GATE, AND (†) AT 3 GHz

SOI material	L (μm)	V_D (V)	I_D (mA)	f_T (GHz)	f_{max} (GHz)	Noise figure / Associated gain (dB) at 2GHz	Ref.
BESOI	1	-	-	-	14	5 / 6.4	35
SIMOX	1	-	-	-	11	5 / 4.4	idem
SOS	0.35	3	10	23	**56**	- / -	36
SIMOX◇	0.32	3	33	14	21	3 / 13.4	37
SIMOX◇	0.25	3	41	23.6	32	1.5 / **17.5**	38
SIMOX	0.75	**0.9**	**3**	10	11	1.5 / 9	39
SIMOX	0.75	**1**	10	12.9	**30**	- / -	40
SIMOX	0.3	2	-	-	24.3	**0.9** / 14	41
SOS*	0.5	2	**2**	**26**	**60**	1.7 / 16.3	42,43
SIMOX◇	0.2	2	125	**28.4**	46	1/15.3†	44
SIMOX	0.2	1.5	24	**34**	28	- / -	45
SOS*	0.5	2.5	-	26	**66**	**0.9 / 21**	46
BESOI	**0.14**	-	6	**40**	-	**0.8 / 17.2**	47