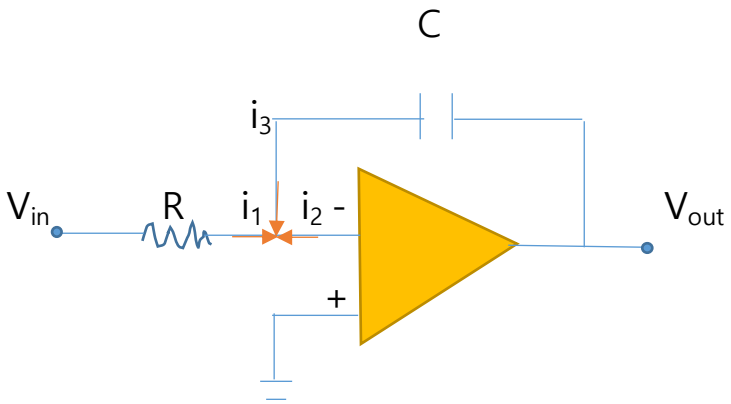
Lecture 13 : OP Amp2

9. Integrator



At Junction: $i_1+i_2+i_3=0$

$i_1=(V_{in} - V^-)/R=V_{in}/R$, $i_2=0$, $i_3=Cd(V_{out} - V^-)/dt=CdV_{out}/dt$

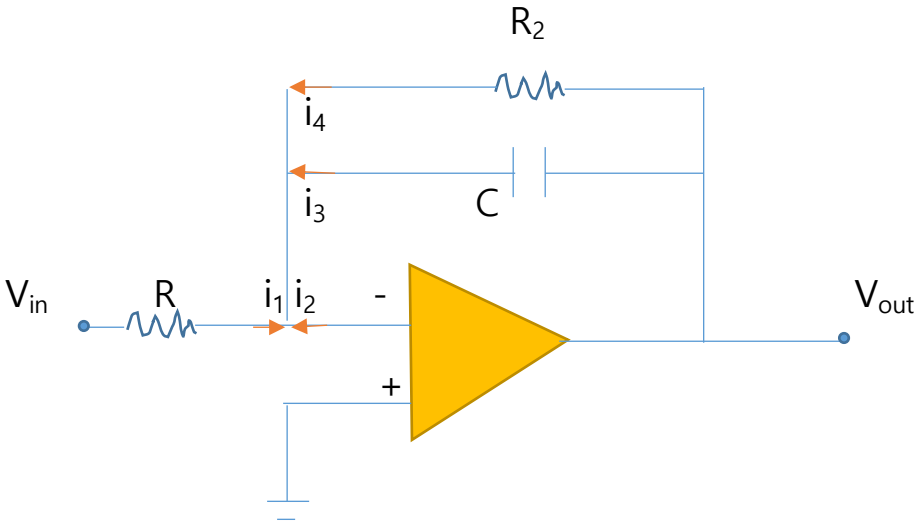
$\therefore i_1+i_2+i_3=V_{in}/R+CdV_{out}/dt=0$

$\therefore V_{out}=-\int V_{in}dt/RC$ $\therefore$Integrator

The OP Amp integrator shows better performance than the integrator using a LPF with low $\omega_{3dB}(=1/RC)$

Practically, integrator seems to saturate easily, and a large resistor R_2 parallel to capacitor can help to prevent it.

Large Resistor R_2 parallel to C can prevent the OP Amp saturation.



At Junction: $i_1+i_2+i_3+i_4=0$

$i_1=V_{in}/R$, $i_2=0$, $i_3=CdV_{out}/dt$, $i_4=V_{out}/R_2$

$i_1+i_2+i_3+i_4=V_{in}/R + CdV_{out}/dt + V_{out}/R_2=0$

Let $V=Vexp(j\omega t)$, then the above eqn becomes,

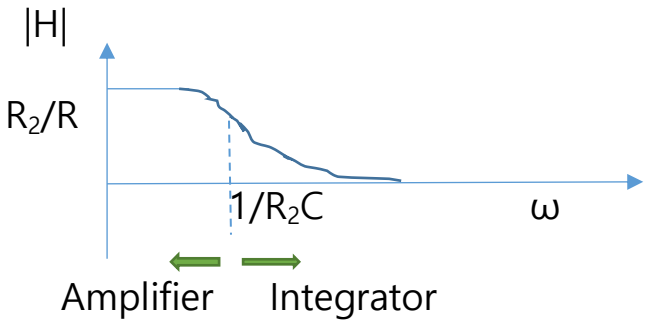
$V_{in}/R+(j\omega C+1/R_2)V_{out}=0$

$\therefore V_{out}/V_{in}=H=-(1/R)/(j\omega C+1/R_2)=-(R_2/R)/(1+j\omega R_2C)$: a kind of *LPF*

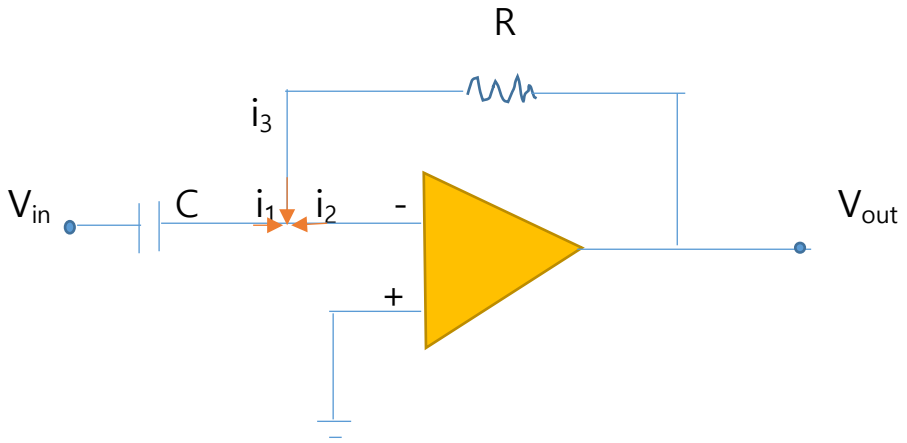
$|H|=(R_2/R)/\sqrt{\{1+(\omega R_2C)^2\}}$ and $\angle H=180^\circ - \tan^{-1}(\omega R_2C)$. Thus

$\omega \geq 1/R_2C$ then $V_{out} \fallingdotseq -\int V_{in}dt/RC$(Integrator),

$\omega \leq 1/R_2C$ then $V_{out}/V_{in} \fallingdotseq -R_2/R$(Amplifier)



10. Differentiator



At Junction: $i_1+i_2+i_3=0$

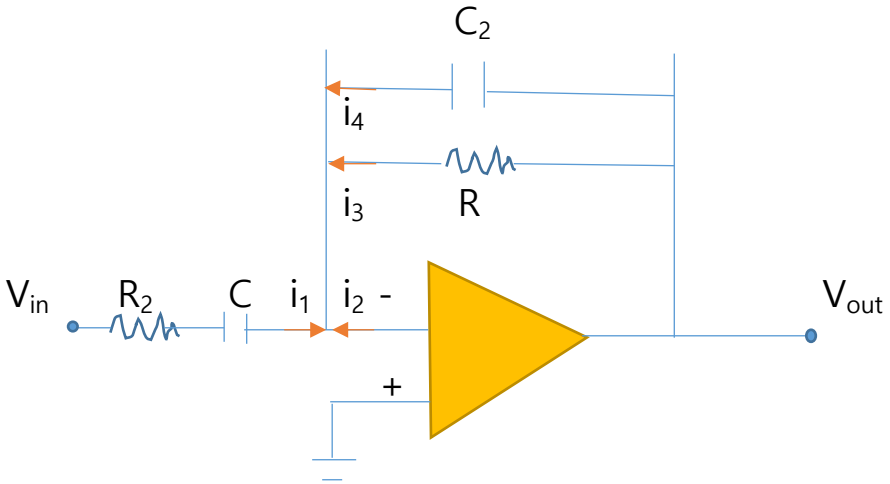
$i_1=Cd(V_{in} - V^-)/dt=CdV_{in}dt$, $i_2=0$, $i_3=(V_{out} - V^-)/R=V_{out}/R$

$\therefore i_1+i_2+i_3=CdV_{in}/dt+V_{out}/R=0$

Thus $V_{out}=-RCdV_{in}/dt$: OP Amp Differentiator

When dV_{in}/dt is very high, OP Amp also can be saturated.

Thus Roll-off function circuit can be added as follows;



At Junction: $i_1+i_2+i_3+i_4=0$

$i_1=V_{in}/(R_2+1/j\omega C)$, $i_2=0$, $i_3=V_{out}/R$, $i_4=j\omega C_2V_{out}$

$\therefore\ i_1+i_2+i_3+i_4= V_{in}/(R_2+1/j\omega C)+V_{out}\ (1/R+j\omega C_2)=0.$

Thus $V_{out}/V_{in}=H=-1/\{(R_2+1/j\omega C)(1/R+j\omega C_2)\}$

$=-j\omega RC/\{(1+j\omega R_2C)(1+j\omega RC_2)\}=-j\omega RC/\{(1-\omega^2RR_2CC_2)+j\omega(R_2C+RC_2)\}$

$\therefore|H|=\omega RC/\sqrt{\{(1-\omega^2RR_2CC_2)^2+\omega^2(R_2C+RC_2)^2\}}$

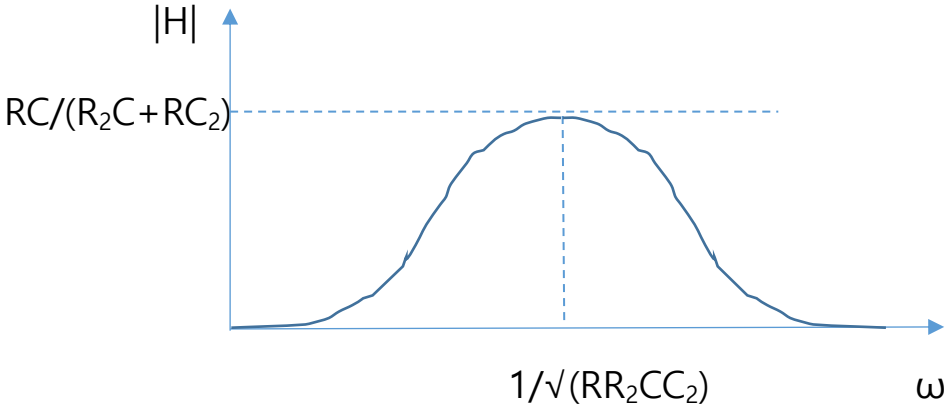
$\angle H=-90°-\tan^{-1}(\omega R_2C)-\tan^{-1}(\omega RC_2)$

If $\omega=0$ then $|H|=0$

if $\omega=1/\sqrt{RR_2CC_2}$ then $|H|=RC/(R_2C+RC_2)$

If $\omega=\infty$ then $|H|=0$

Ex) $R=100K$, $C=0.01\mu F$, $R_2=1K$, $C_2=100pF$, then $1/\sqrt{RR_2CC_2}=10^5$; $RC/(R_2C+RC_2)=50$



Differentiator ⟸

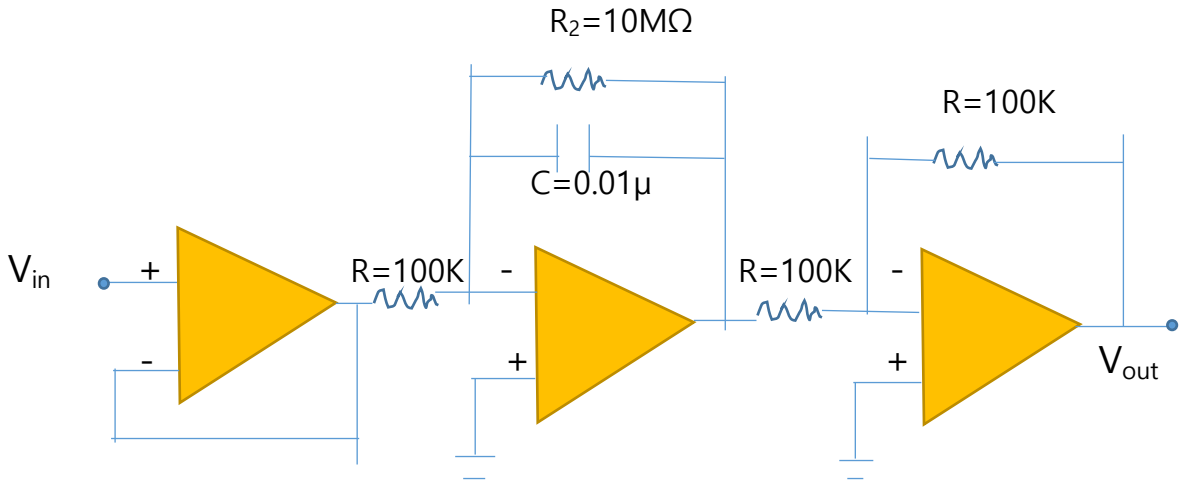
If $\omega\ll1/\sqrt{(RR_2CC_2)}$ then $H\fallingdotseq-j\omega RC=V_{out}/V_{in}$

thus $V_{out}=-j\omega RCV_{in}=-RCdV_{in}/dt$: Differentiator

The 'Roll Off' is applied to the high frequency range.

Ex) Design an OP Amp that ramps at +1V/ms with DC 1V input.

Assume the input impedance, $Z_{in} \geq 10M\Omega$, and the DC gain of 100 is considered for the saturation protection.



1) OP Amp follower is used for high $Z_{in}(\geq 10M\Omega)$,

   considering uncertain $Z_{UPSTREAM}$

2) Choose R_2 as 10MΩ much less than huge resistance ($\ll 100M\Omega$)

3) Choose R as 100KΩ that gives DC gain of 100($=R_2/R$) for saturation protection. It gives current i=1V/100KΩ=0.01mA

4) Choose C such that $i=C\Delta V/\Delta t$

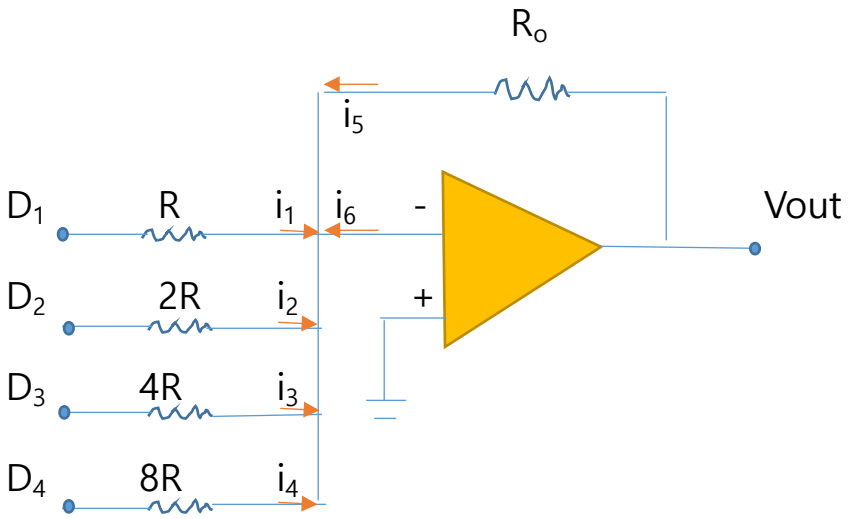
   Thus $C=i/(\Delta V/\Delta t)=(0.01E\text{-}3)/(1V/0.001s)=0.01\mu F$

5) Optionally choose the same R for the inverting amplifier

11. Digital to Analog Converter (DAC)

: To convert the Digital signal to Analog signal

(1) Binary weighed resistor method



At Junction: $i_1+i_2+i_3+i_4+i_5+i_6=0$, and $V^-=0$

$i_1=D_1/R$, $i_2=D_2/2R$, $i_3=D_3/4R$, $i_4=D_4/8R$, $i_5=V_{out}/R_o$, $i_6=0$

Thus $V_{out}=(-R_o/R)(D_1+D_2/2+D_3/4+D_4/8)$

$=(-R_o/8R)(8D_1+4D_2+2D_3+D_4)$,

where $D_i=0$ or 1 ; 0V or 5V

D_1=MSB(Most Significant Bit), D_4=LSB(Least Significant Bit)

This is the Digital to Analog conversion.

Q: Can this method be extended to the DAC of 5 or more bits?

Answer is No.

The above binary weighed resistors is practically limited to the DACs of maximum 4 bits.

Two issues for the binary weighed resistors method

Issue1: Availability and Range of Resistors

If we extend to 5 or more bits DAC, we need 16R, 32R, 64R, etc.

But the binary weighed resistors may not be easily obtained from the commercial choice such as 128R for the 8^{th} bit of DAC.

The range of OP Amp's resistor may be limited, such as 10KΩ to 100KΩ range, typically.

Issue 2: Manufacturing tolerance of commercial resistors

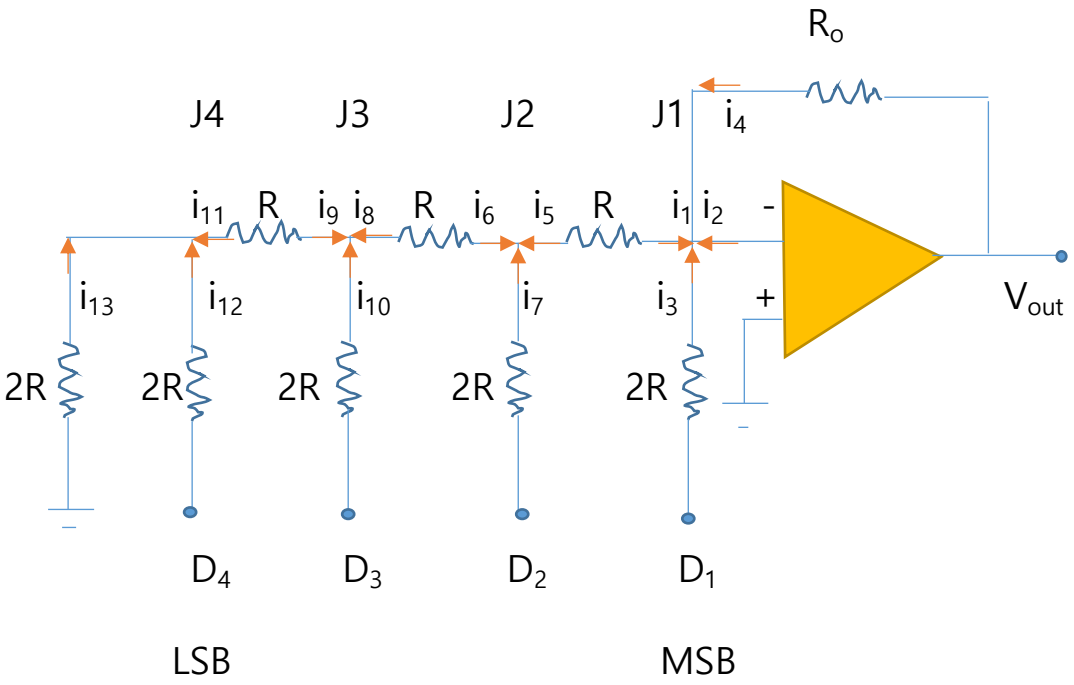
All commercial resistors may have manufacturing tolerance of about 10% from the nominal resistance. It indicates 10KΩ resistor may have resistance between 9.5KΩ and 10.5KΩ with normal specification.

For n bits of DAC, the critical situation comes when the tolerance of MSB (=0.1) is equal to the contribution of the LSB ($=1/2^{n-1}$). Thus for reliable DAC performance, $0.1 \leq 1/2^{n-1}$ is to be satisfied. Thus $n \leq 4$ and maximum 4 bits of DAC is practically accepted with the weighed resistor method.

(Q: How can we handle higher bits DAC? We may need more than 16 bits DAC in practical application. Is there any alternative method?)

(2) Ladder method or R-2R resistors method

: To DAC using R-2R resistors



Let V_1, V_2, V_3, V_4 are the voltages at the J1, J2, J3, J4 junctions, respectively.

At J4 junction: $i_{11}+i_{12}+i_{13}=0$

$(V_3-V_4)/R+(D_4-V_4)/2R+(0-V_4)/2R=0$

$\therefore 2(V_3-V_4)+(D_4-V_4)-V_4=0 \therefore 2V_3-4V_4=-D_4$ eq(1)

At J3 junction: $i_8+i_9+i_{10}=0$

$(V_2-V_3)/R+(V_4-V_3)/R+(D_3-V_3)/2R=0$

$\therefore 2(V_2-V_3)+2(V_4-V_3)+(D_3-V_3)=0 \therefore 2V_2-5V_3+2V_4=-D_3$ eq(2)

At J2 junction: $i_5+i_6+i_7=0$

$(0-V_2)/R+(V_3-V_2)/R+(D_2-V_2)/2R=0$

$\therefore 2(0-V_2)+2(V_3-V_2)+(D_2-V_2)=0 \ \therefore -5V_2+2V_3=-D_2$ eq(3)

At J1 junction: $i_1+i_2+i_3+i_4=0$

$V_2/R+0+D_1/2R+V_{out}/R_o=0$ eq(4)

From eq(3), $V_3=(5V_2-D_2)/2$

From eq(2), $V_4=(-2V_2+5V_3-D_3)/2=(-2V_2+12.5V_2-2.5D_2-D_3)/2$

$=(10.5V_2-2.5D_2-D_3)/2$

Now from eq(1), $5V_2-D_2-2(10.5V_2-2.5D_2-D_3)=-D_4$

$-16V_2+4D_2+2D_3=-D_4 \ \therefore V_2=(4D_2+2D_3+D_4)/16$

Finally from eq(4),

$V_{out}=-(R_o/R)(V_2+D_1/2)=-(R_o/R)(D_1/2+D_2/4+D_3/8+D_4/16)$

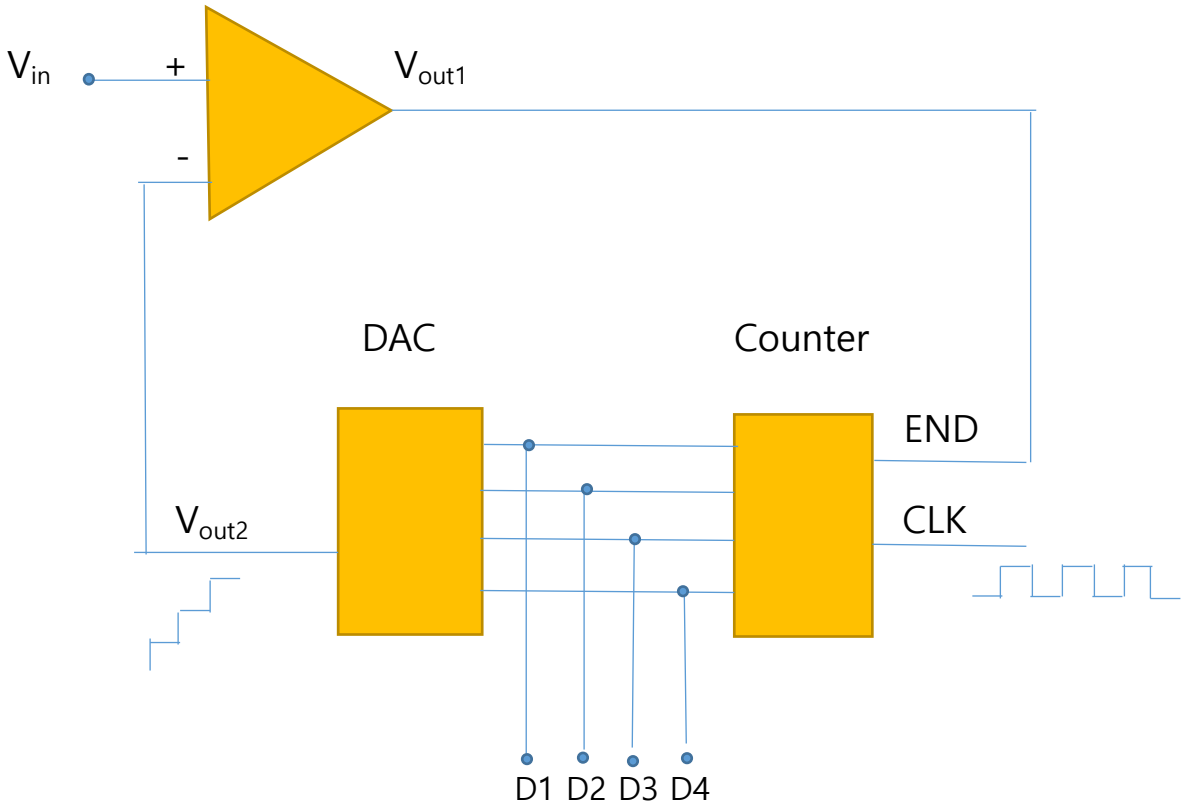
$=-(R_o/16R)(8D_1+4D_2+2D_3+D_4) \ \therefore$ 4 bit DAC

This is a very nice DAC circuit, and it can be extended to n bits of DAC, by just adding R-2R resistors, without using the troublesome binary weighed resistors.

(Q: Is this circuit free from the issue of manufacturing tolerance of resistors? A: The tolerance issue is still valid, but we can focus on the getting of R, 2R resistors of high precision grade, rather than hustle and bustle with broad range of precision resistors that may not be commercially available.)

12. Analog to Digital Converter, or ADC

: To convert from Analog to Digital, using Comparator, DAC, Counter based on *Successive Approximation*



(1) V_{in} is compared with V_{out2}

(2) if V_{in} > V_{out2} then V_{out1}=+Vcc that sends to Counter for *count-up*

otherwise V_{out1}=-Vcc that sends to Counter for *count-stop*

(3) Counter is counting-up with CLK signal

(4) DAC converts Digital to Analog, outputting V_{out2}

(5) Repeat (1) to (4)

∴ Digital (D_4, D_3, D_2, D_1) is obtained from the Analog V_{in}

Observation:

This is a 4 bit ADC consisting of OP Amp comparator, Counter, DAC, using the Successive Approximation method, and the number of bits of processing can be easily increased with the upgraded DAC and Counter accommodating increased bit numbers.

OP Amp comparator (open loop) is a very nice tool for comparison, and the digital counter is integrated together with internal/external CLK signal that is commercially available.

In order to obtain a Digital value corresponding to Analog V_{in} , it needs multiple looping-procedures until $Vout_2$ is equal or very close to V_{in} as explained, thus taking more times for processing than the simple DAC procedure.

(But it is not so much troublesome due to very high CLK speed available nowadays)