Lecture 14 : Digital Gates and Combinational Logics

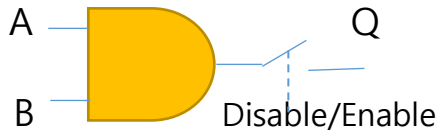
: To introduce the digital gates with combinational logics

Analog	vs	Digital
A Single line		Multiple lines
Rich analog information		Digital H/L information
Weak immunity for noise		Strong immunity for noise
Limited resource for computation		Wide resource (μP, Digital Device)

Three logic states

H=1=True=5V (for CMOS and TTL)

L=0=False=0V



Open=Disable/High-Impedance ∴ Q=[0,1,Open]

Data Width : Number of Bits for data representation

1=Bit, 4=Nibble, 8=Byte, 16=Word, 32=Long Word

∴ 1 Long Word=2 Word= 4 Bytes =8 Nibbles

Number Representation:

Binary [0,1]: $1101B=1101_2=1\cdot2^3+1\cdot2^2+1=13_{10}$

Decimal [0,1,2,3,4,5,6,7,8,9]: $36D=36_{10}$

Hexadecimal [0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F]: $3AH=3A_{16}=3\cdot16+10=58_{10}$

0=0000 1=0001 2=0010 3=0011 4=0100 5=0101 6=0110 7=0111

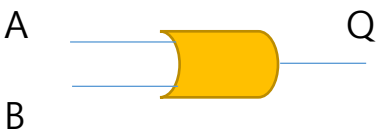
8=1000 9=1001 A=1010 B=1011 C=1100 D=1101 E=1110 F=1111

Gate and Truth Table

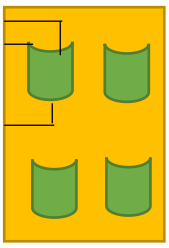
1. OR gate

: Q=A OR B = A∨B= A+B

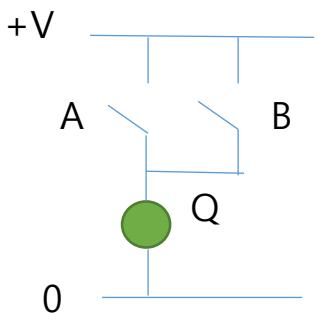
Symbol



Quad OR gate



Relay Circuit



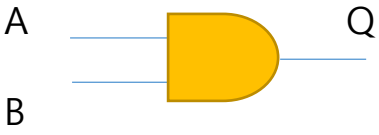
Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

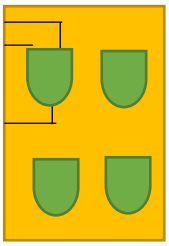
2. AND Gate

: Q=A AND B= A∧B= A·B

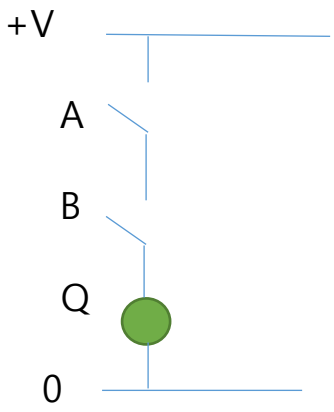
Symbol



Quad AND gate



Relay Circuit



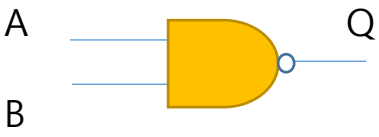
Truth Table

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

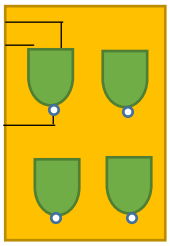
3. NAND Gate

: Q=A NAND B= Not (A∧B) = (Not A)∨(Not B)=$\underline{A}$∨$\underline{B}$=$\underline{A}$+$\underline{B}$

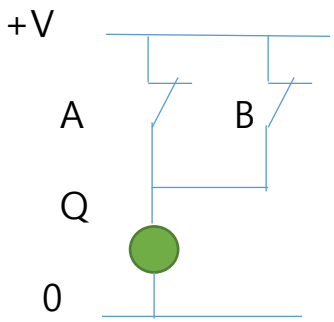
Symbol



Quad NAND gate



Relay Circuit



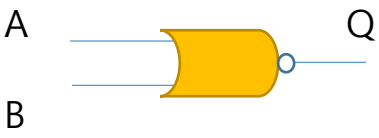
Truth Table

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

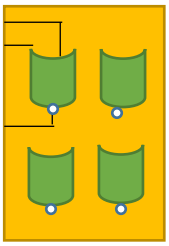
4. NOR Gate

: Q=A NOR B= Not(A OR B) = Not A ∧ Not B=$\underline{A}\wedge\underline{B}=\underline{A}\cdot\underline{B}$

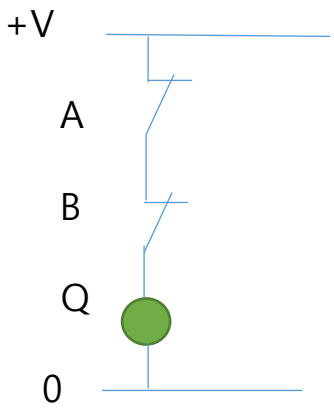
Symbol



Quad NOR gate



Relay Circuit



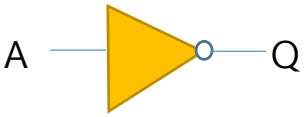
Truth Table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

5. Inverter Gate

: Q= Not A=$\underline{A}$

Symbol

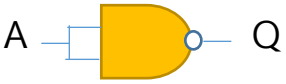


Q=Not (A∨A)

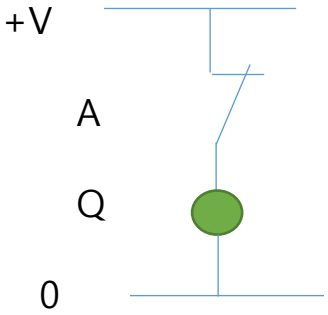
=Not A=$\underline{A}$

Q=Not (A∧A)

=Not A=$\underline{A}$



Relay Circuit



Truth Table

A	Q
0	1
1	0

5. XOR (Exclusive OR) Gate, or Digital Comparator

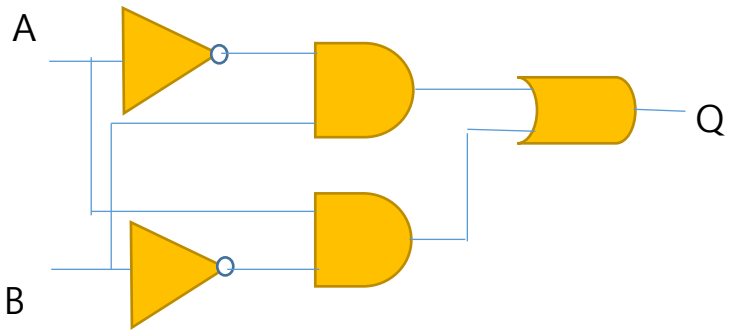
: Q=A XOR B = 1 (if A,B are different), 0 (if A,B are the same)

$=(\underline{A} \wedge B) \vee (A \wedge \underline{B})=\underline{A}\cdot B+A\cdot\underline{B}$

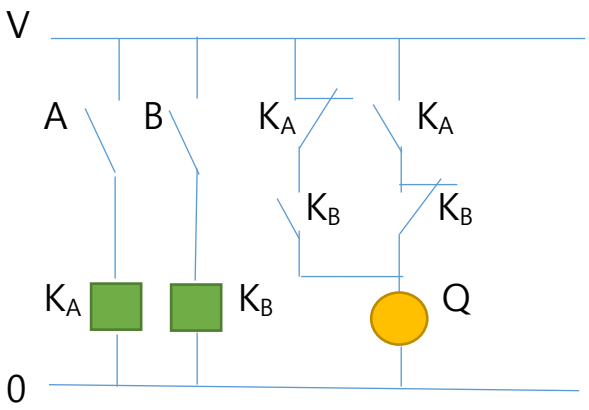
Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Combinational Logic gate



Relay Circuit

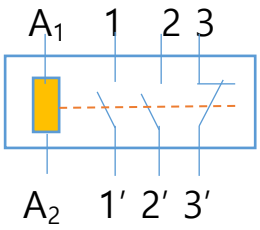


Symbol

Relay(계전기,繼電器): Electro-Magnet connected multiple switches for various functions

Source:https://theveterinarymedicine.com/General-Purpose-Relays-Power-PCB-Relay/Other-Transformers-zbtfe-582626.action

K_A or K_B



1,2: a(NO) Type, 3: b(NC) Type

Multiple points connected to magnet

NO=Normally Open, NC=Normally Closed

A_1 , A_2 : Terminal for Electro-Magnet

Functions of Relay:

(1) Switch points(접점,接點) increase; ex) one to three

(2) Voltage Change ; ex) 5V Switch to 12V Switch

(3) Switch Type conversion; ex) a Type to b Type or vice versa.

(4) Logic Function ; Logic statement execution

Logic Statement/Logic Function

: Logic statement can be converted to Logic function,

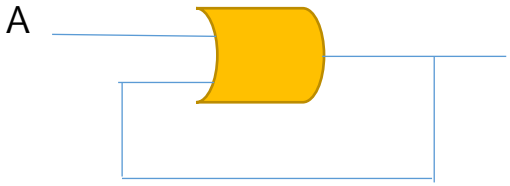
Thence the Logic circuit can be drawn accordingly,

Case1) Self-Holding Circuit

: To hold the Switch function ('ON') even when the Switch is released.

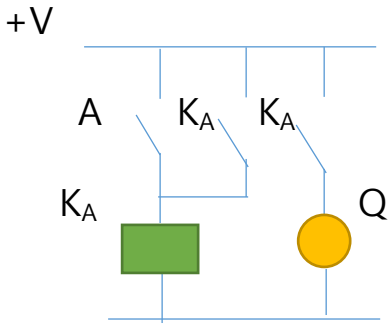
It is widely applied to M/C operation.

Logic Gate



Logic: A+Q=Q

Relay Circuit



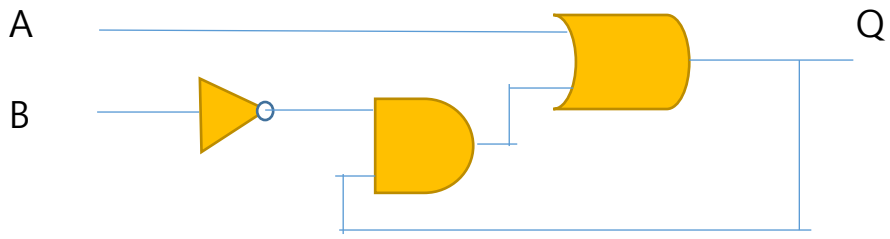
$A+K_A=K_A$ $K_A=Q$ $\therefore A+Q=Q$

For OFF function, we need a OFF S/W that is B signal, to be pressed, and there are two modes of circuit configuration: Dominant ON mode and Dominant OFF mode.

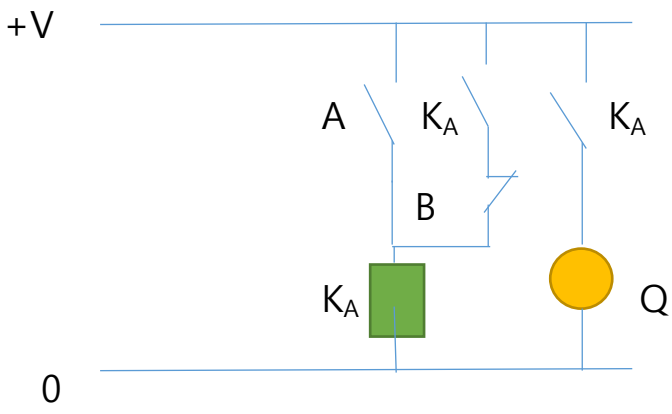
(1) Dominant ON

: To insert OFF S/W, that is B, in front of OR gate. It gives ON even when the A,B switches are pressed. Then logic function is, A + $\underline{B}$·Q=Q

Logic Gates



Relay Circuit

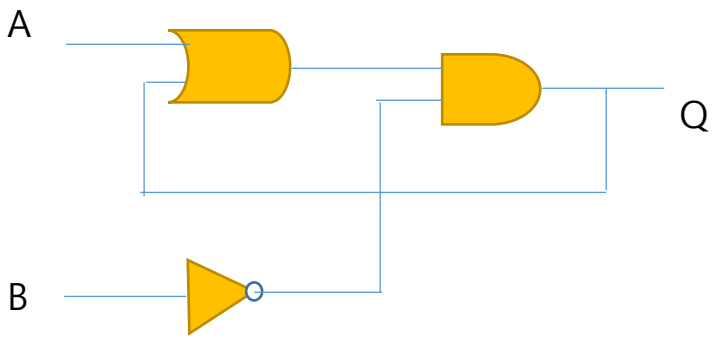


$A+K_A\cdot\underline{B}=K_A \quad K_A=Q$

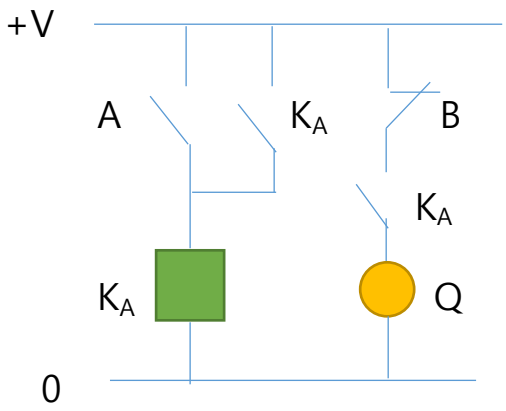
(2) Dominant OFF

:To insert OFF S/W, that is B, in front of AND gate. It gives OFF when the A,B are pressed. The logic function is, $(A+Q)\cdot\underline{B}=Q$

Logic Gates



Relay Circuit



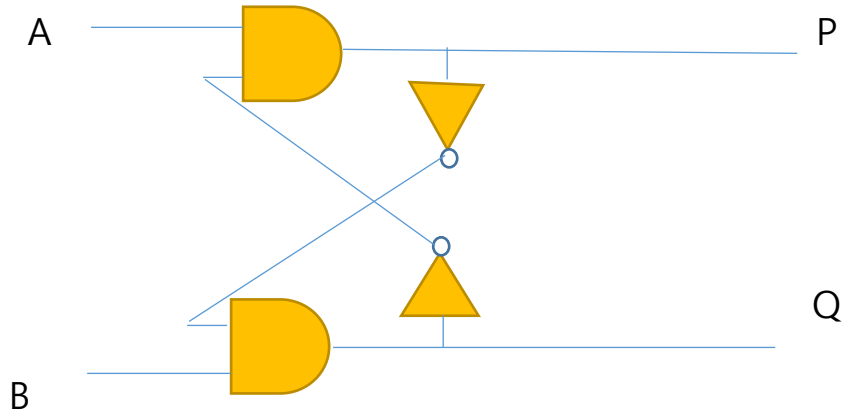
$A+K_A=K_A$ $\underline{B}\cdot K_A=Q$

Case2) Interlock Circuit (or Quiz Circuit)

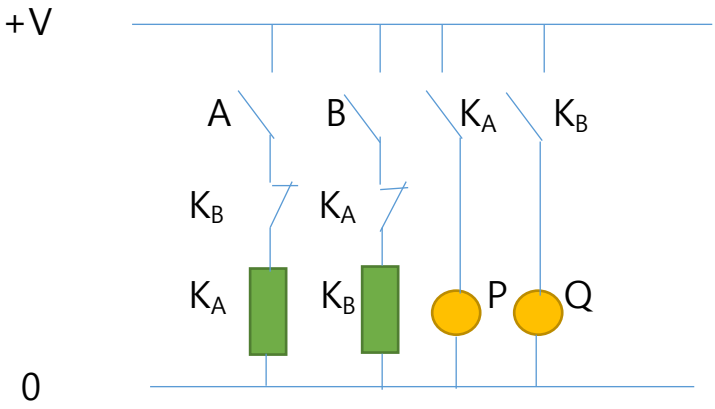
: To interlock each other, and it gives the fastest signal to pass while others are locked. Also, it is called 'Quiz Circuit'.

Logic Function: $A \cdot \underline{Q} = P$, $B \cdot \underline{P} = Q$

Logic Gates



Relay Circuit



$A \cdot \underline{K_B} = K_A$; $B \cdot \underline{K_A} = K_B$; $K_A = P$; $K_B = Q$

HW9) What about the Quiz circuit for 3 inputs ?

Karnaugh Map

: To derive Logic function from the logic statement or truth table

Step1: Make Truth table

Step2: Karnaugh Map that is to align as the sequence of only one bit change from one location to the next

Step3: Identify the 1's location on the map, and this gives the Logic function

Step 4: Verify the Karnaugh Map, by checking the Truth table

Ex) Design an Electronic Voting System of 3 inputs of (A,B,C) such that at least two inputs are 1, then output(Q) gives 1.

Truth table

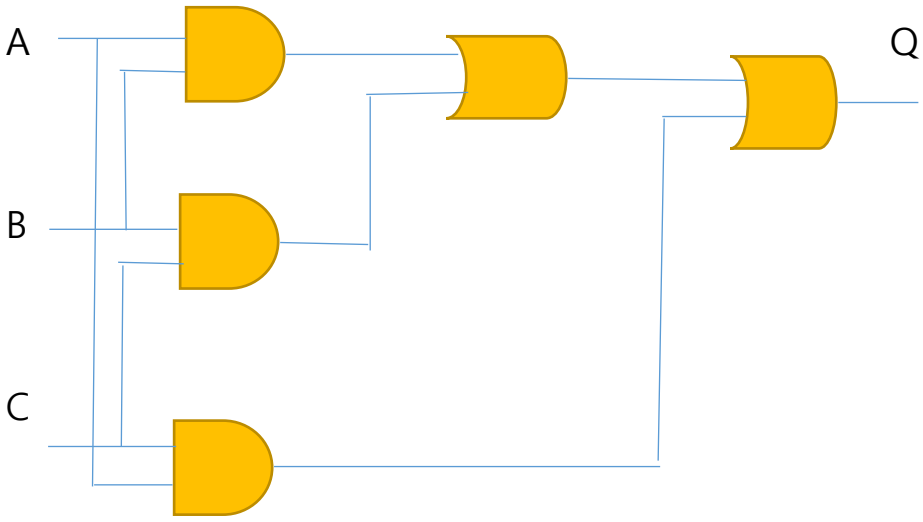
A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Karnaugh Map

C \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

∴ Logic Function : The 1's location gives Q=AB+AC+BC

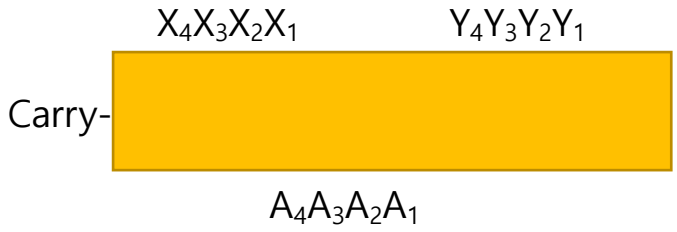
Logic Gates



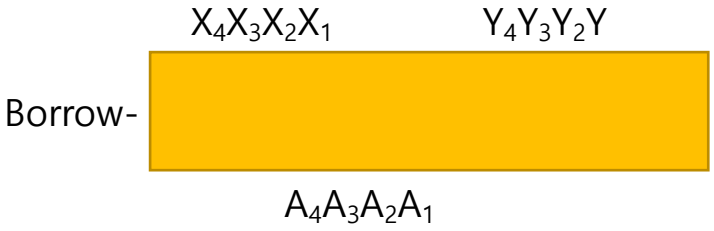
Therefore the logic gates are widely used for the logic calculation

Similarly, the arithmetic gates such as Adder, Subtractor, Multiplier, Divider gates can be used for the arithmetic calculation as follows;

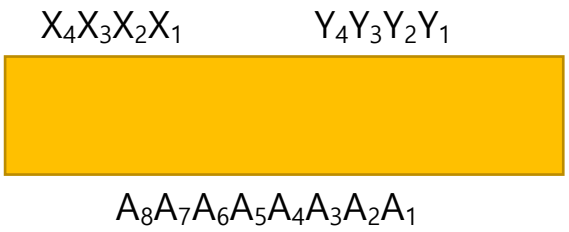
Adder Gate, X+Y=A



Subtractor Gate, X-Y=A



Multiplier Gate, X*Y=A; SHL(SHift Left) and Add



Divider Gate, X/Y=A; SHR(SHift Right) and Subtract

where quotient (lower 4bits), Remainder (higher 4bits)