Chap. 9 Advances in Microelectronics

9.2 Brief History: Moore's Law

- SSI (small scale), MSI (medium scale), VLSI (very large scale), ULSI (ultra large scale)
- Systems on a Chip (SOC)

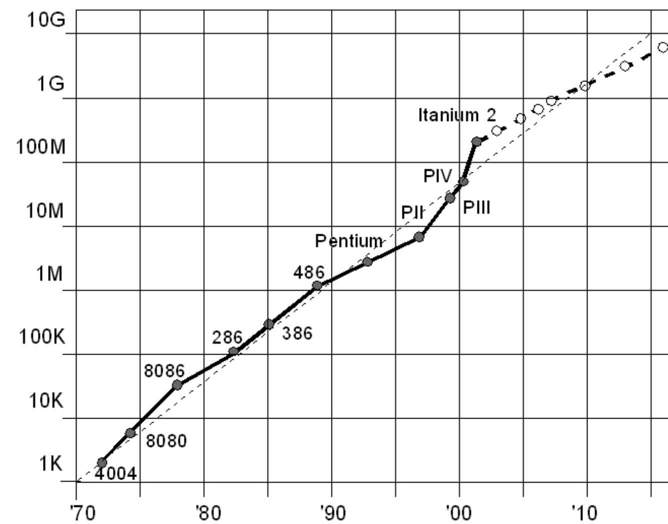

Figure 9.3. Moore's law (data points are for INTEL's microprocessors; the projections are based on the 2002 Technology Roadmap ITRS02).

- The minimum feature size

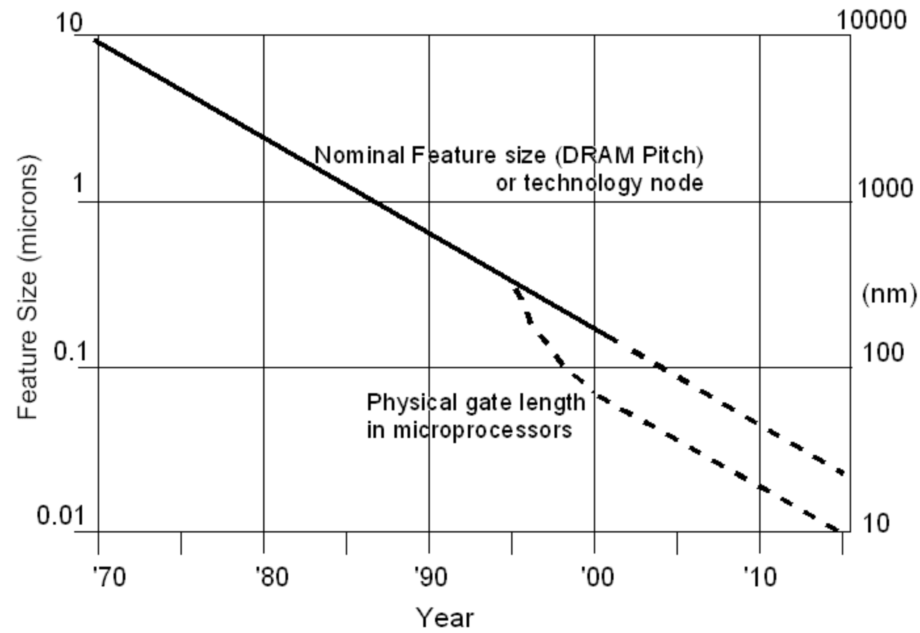

Figure 9.4. Trend of the minimum feature size (2002 Technology Roadmap ITRS02).

9.3 Basic Principles of Semiconductors

9.3.1 Semiconductor Model and Energy Band Structure

- IV column (Si, Ge) and III-V compounds (Al, Ga / P, As)

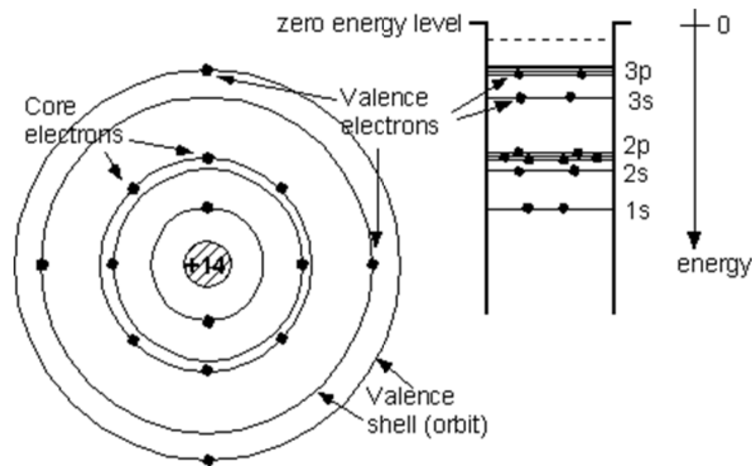

Figure 9.9. Schematic representation of the orbital model of a single silicon atom, with its 14 electrons of which the 4 valence electrons reside in the outermost shell. The energy levels are shown to the right (not to scale).

9.3.2 Charge Carriers in Semiconductors

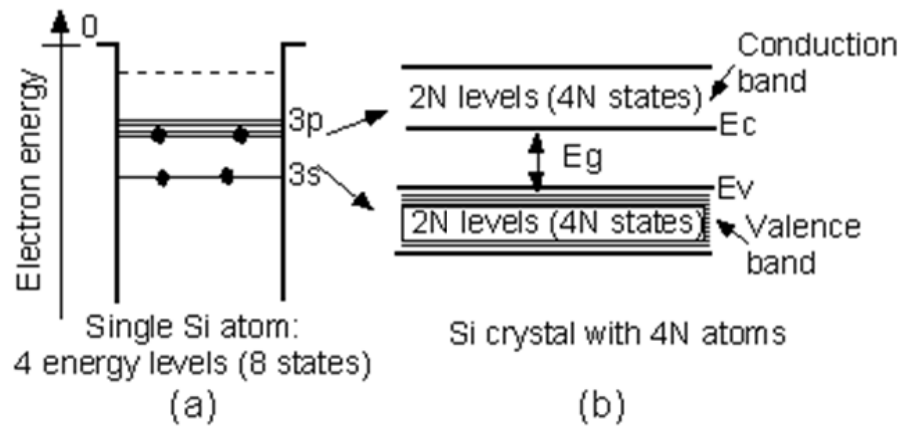

Figure 9.11. (a) Energy levels in an isolated silicon atom and (b) in a silicon crystal of N atoms, illustrating the formation of energy bands. The valence band contains 4N states and can accommodate all 4N valence electrons.

- For pure (intrinsic) semiconductors, $n = p = n_i$ and thus $np = n_i^2$

9.3.3 Extrinsic (Doped) Semiconductors

- n-type Si: *donor* concentration $N_D \approx 10^{15}\ \mathrm{cm}^{-3}$, $n = N_D + n_i$
  At room temp, $n \approx N_D$ (majority carriers)

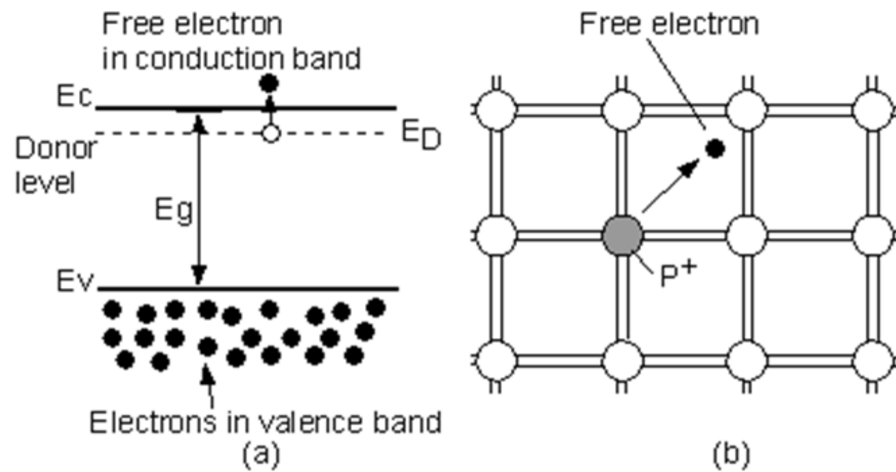

Figure 9.13. Extrinsic *n*-type silicon doped with P donor atoms. (a) Energy band diagram and (b) Bond model.

- p-type Si: *acceptor*, $p = N_A + n_i$

  At room temp, $p \approx N_A$ (majority carriers)

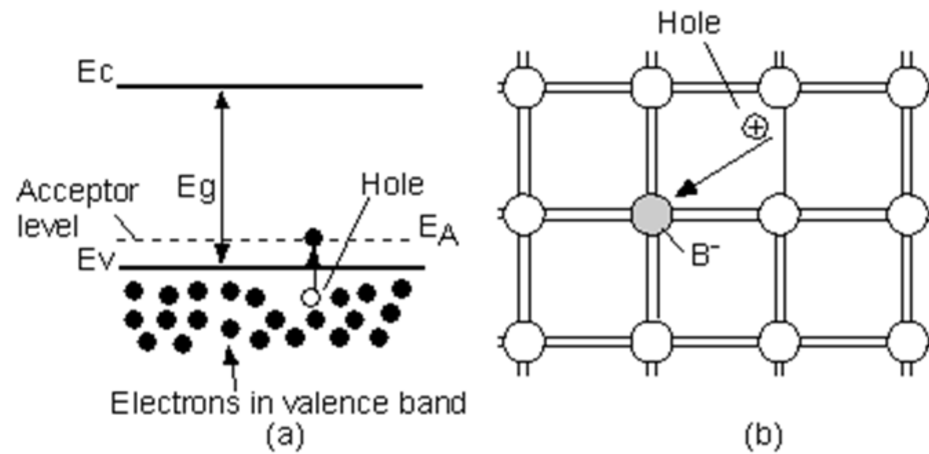

Figure 9.14. Extrinsic p-type silicon doped with B acceptor atoms. (a) Energy band diagram and (b) Bond model.

- Fermi function: $F(E)=\dfrac{1}{1+e^{(E-E_F)/kT}}$ with E_F the Fermi level, defined as the energy at which the probability of finding an electron is equal to 0.5.

(1) $F(E)\rightarrow 0 \quad \text{for} \quad E \gg E_F$ and $F(E)\rightarrow 1 \quad \text{for} \quad E \ll E_F$

(2) If the energy E of the state is a few times kT larger than the Fermi energy E_F,

$F(E) \approx e^{-(E-E_F)/kT}$; Boltzmann approximation.

$$\rightarrow \quad n=\int_{E_C}^{\infty} F(E)N(E)dE \approx N_C\, e^{-(E_C-E_F)/kT} = n_i e^{(E_F-E_i)/kT} \quad \text{and}$$

$$p=\int_{-\infty}^{E_V} [1-F(E)]N(E)dE \approx N_V\, e^{-(E_F-E_V)/kT} = n_i e^{(E_i-E_F)/kT}$$

where N(E) = the density of states and N_C (or N_V) = the effective density of states in the conduction (or valence) band.

The condition of $np=n_i^2$ is still valid!

9.4. MOS Transistor

- Long channel transistor

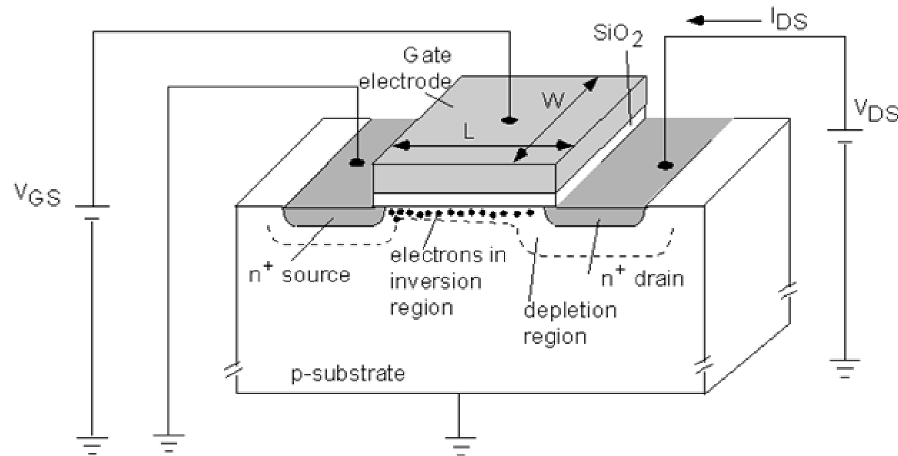

Figure 9.17. Schematic view of a n-type MOSFET.

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} \quad \text{for} \quad V_{GS} \gg V_{DS}$$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - m \frac{V_{DS}^2}{2} \right] \quad \text{for} \quad V_{GS} - V_T > V_{DS}$$

with m= body effect coeff.

- Current flow:

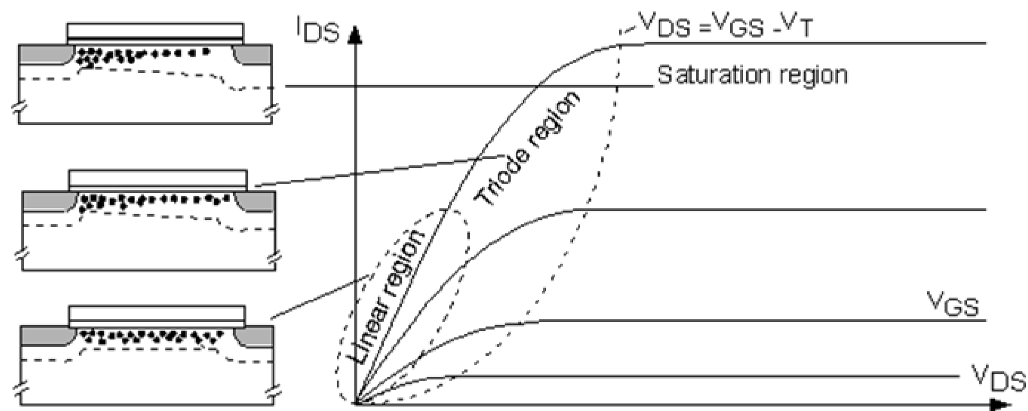

Figure 9.18. Current flow in a NMOS transistor, illustrating the three operating regions (linear, triode and saturation).

9.5. Scaling of Transistor Dimensions

- Scaling refers to reducing both horizontal and vertical dimensions by the same factor α:

TABLE 9.1. Transistor scaling assuming long channel device operation

Parameter	Multiplicative scaling factor Constant Field	Constant Voltage	Generalized Scaling
Transistor dimensions (t_{ox}, W, L, x_j)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Voltage	$1/\alpha$	1	k/α
Doping concentration (N_B)	α	α	$k\alpha$
Electric Field	1	α	k
Capacitance ($C = \varepsilon A/t$)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Current (I)	$1/\alpha$	α	k^2/α
Current per gate width (I/W)	1	α^2	k^2
Delay (CV/I)	$1/\alpha$	$1/\alpha^2$	$1/k\alpha$
Power dissipation ($P = IV$)	$1/\alpha^2$	α	k^3/α^2
Power density (P/A)	1	α^3	k^3

(Power per Area)

**Constant field scaling*: the voltage scales with the same factor as the dimensions.