Verification and Test – Verification

Verification

Verification is the process of ensuring that a design meets its specification.

- Simulation is the primary tool → should prepare test suits (i.e., a set of test patterns)

Specification coverage, which is the fraction of features in the specification that are exercised and checked by the tests.

- 100% coverage required.

Implementation coverage, which is the fraction of lines in the Verilog code that are exercised by the tests.

- For every state machine in our design, every edge between states should be traversed.

Types of tests

Ideally, require an *exhaustive* test

Practically, perform a combination of *directed* tests and *random* tests

- A *directed* test is written to cover some interesting test cases

  Example: with on clock chip, need to ensure that the clock functions properly from 23:59:59 to 00:00:00
- A *random* test uniformly samples the space of all inputs, but often samples *non-uniformly* around areas of interest.

A typical test suite may involve 10^9 or more test patterns. – definitely cannot look through all the results manually to see if they are correct.

- A common approach is to compare our design (cycle-level timing) to a higher level model (transaction-level) of the same function.

Static timing analysis

In addition to verifying that our design is functionally correct, we must also verify that it satisfies setup- and hold-time margins.

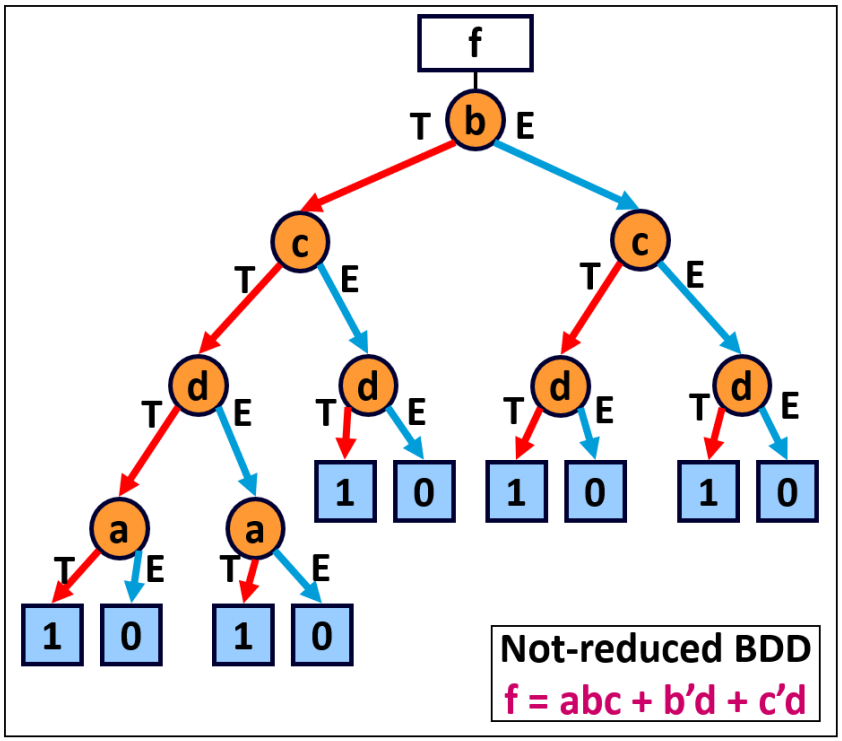
- In theory, timing verification could be performed via _____.
- In practice, it is very hard to construction a set of tests that is guaranteed to test the timing of the _____.

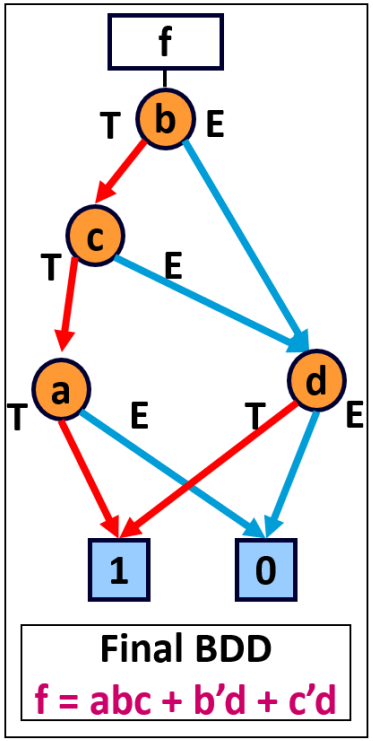
With static timing analysis, all paths are checked without the need to generate _____.

The limitation of static timing analysis is that it often report issues on paths that are guaranteed never to be used.

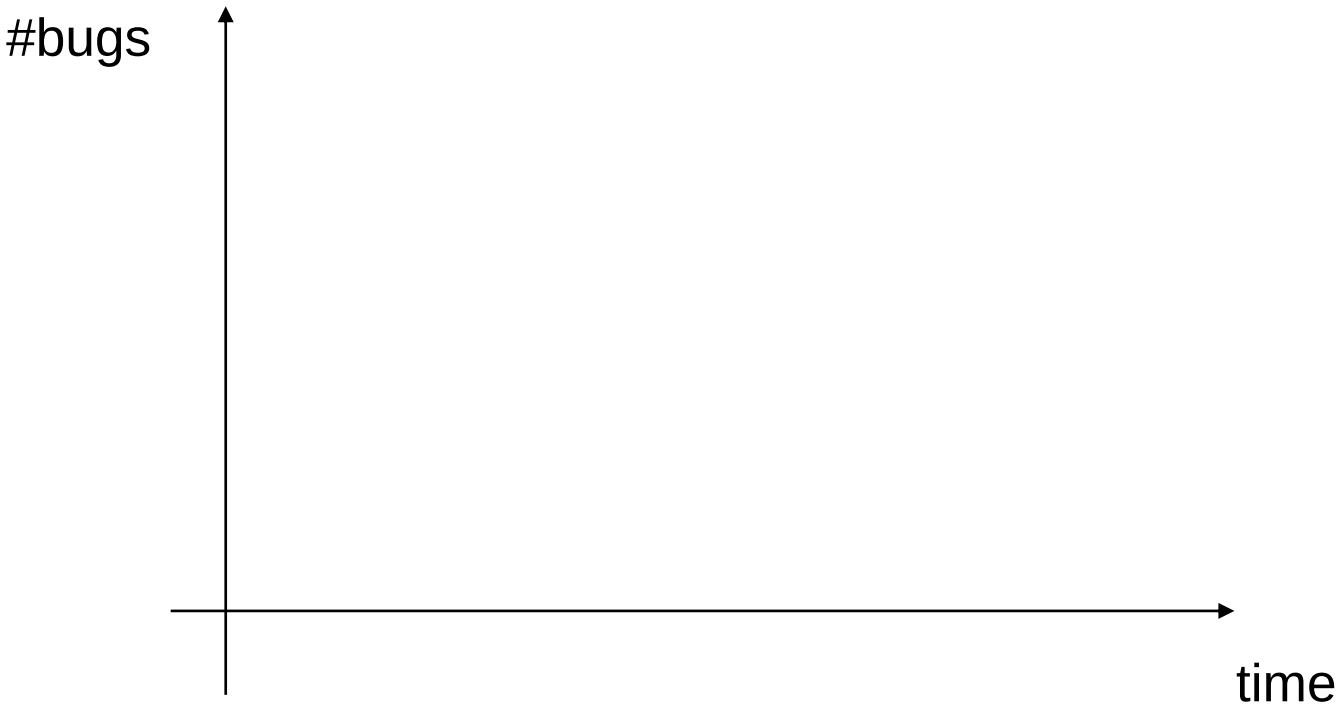
Formal verification

A technique to prove functional correctness without the need for _____.





Bug tracking



The majority of bugs are closed quickly, within one day. However, a small fraction of difficult bugs remain open for a week or more.

Summary

Design verification is the process of verifying that a design meets its specification.

- *Specification coverage* – to make sure all features of the design are correctly implemented.
- *Implementation coverage* – to ensure every line of Verilog code has been exercised.

Test is the process of verifying that a particular device has ben manufactured correctly.

- *Stuck-at fault* model – to measure the coverage of a manufacturing test
- *ATPG* for combinational logic
- *Scan chain* and *BIST*

Characterization involves testing a sample of parts to determine

- Operating envelope (Vdd, frequency)
- Critical parameters (Vth, delay, power), failure rate of a device type (aging)

Verification and Test - Test

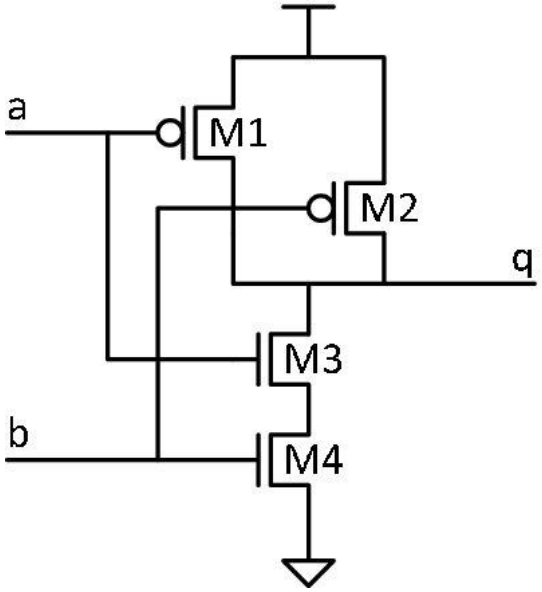
Test

Test is the process of verifying that a particular instance of a design in fact implements the design.

Needs to define potential faults (i.e., fault models)

Quick testing is essential.

Fault model: Stuck at 0/1 at q

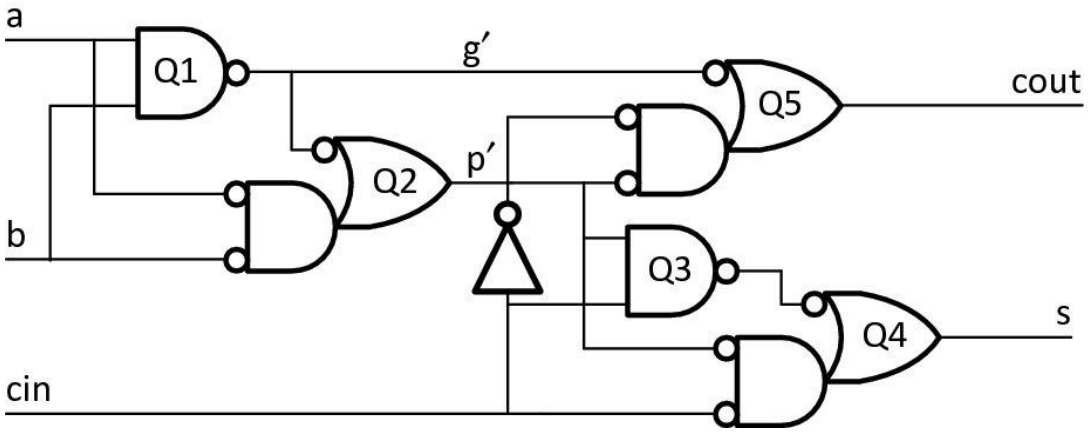


Can test stuck at 0 at q ?

Can test stuck at 0 at M1?

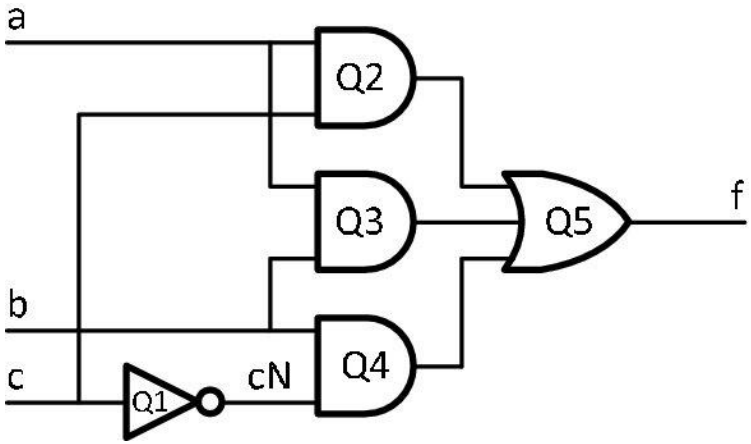
In general, good coverage of a stuck-at-fault model at gate output results in a good coverage of actual manufacturing faults.

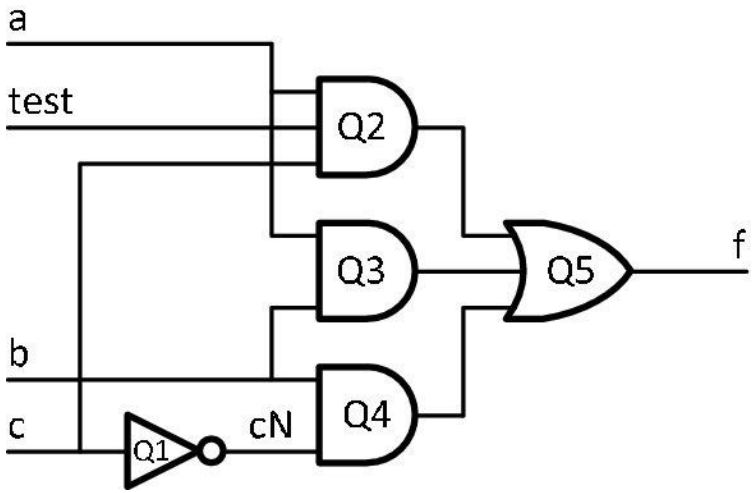
Combinational testing



a	b	cin	g'	p'	Q3	cout	s	Faults covered
0	0	0	1	1	1	0	0	g'-0, p'-0, cout-1, s-1, Q3-0
1	1	1	0	1	0	1	1	g'-1, p'-1, cout-0, s-0, Q3-1

Testing redundant logic

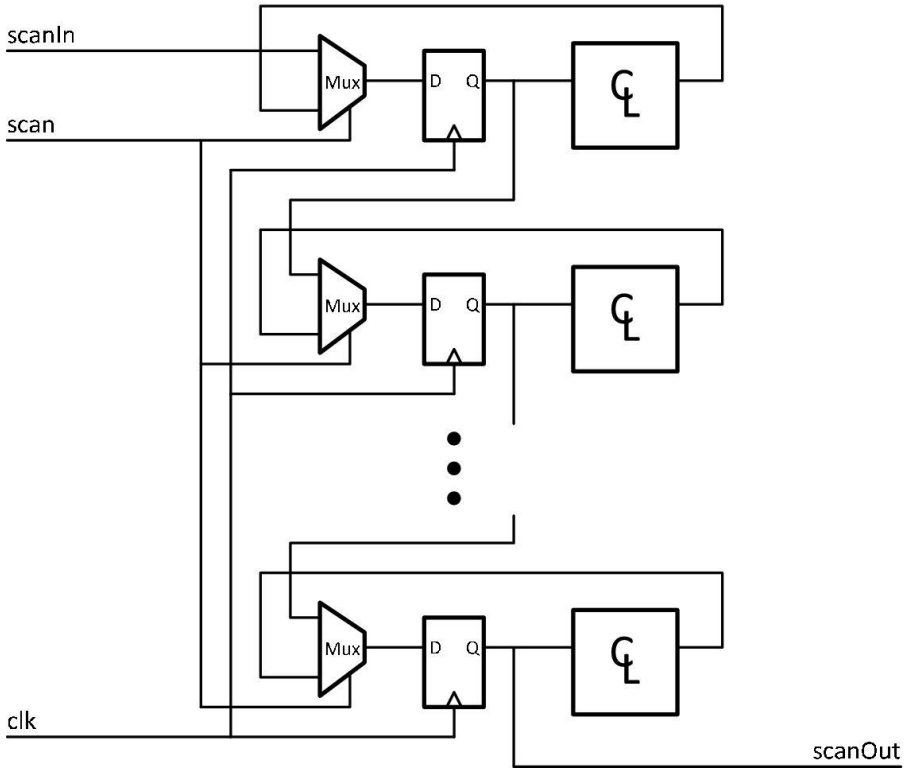




Stuck-at-0 at Q3?

Verification and Test – Design for testability

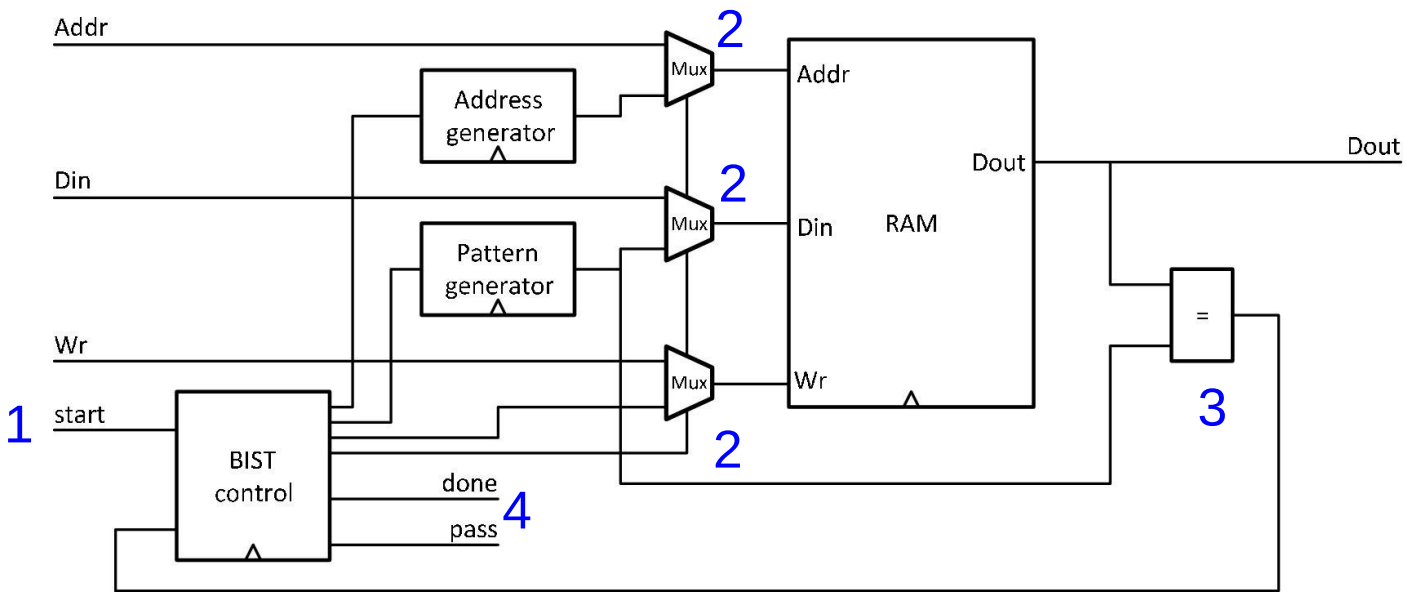
Scan



1. Scan-in
2. Run
3. Scan-out

Testing _____ logic

Built-in-self-test (BIST) for RAM

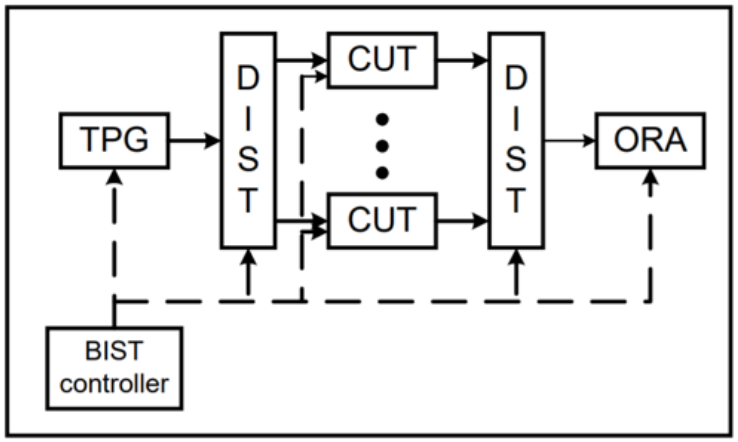


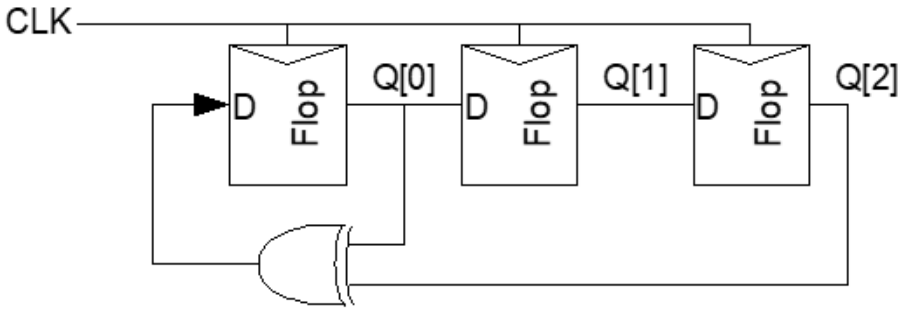
1 → 2, 3, 2, 3, ... → 4

Built-in-self-test (BIST) for logic

Another class of BIST is a pseudo-random testing of logic.

On-chip LBIST state machines generate a serious of test patterns that are scanned into registers, clocked , and then scanned out into multiple-input signature (MISR) also located on-chip.





Pseudo-random sequence generator

Characterization

Characterization tests are performed on samples of a design to determine typical and extreme parameters of the design, to determine the operating envelope of the design, and to measure the aging properties of the devices.

Note: manufacturing tests are performed on every chip produced.

- Critical parameters: V-I curve on chip's inputs and output, power consumption, critical path delay, power consumption on every operating corners.
- Accelerated-life-test: NBTI, HCI and temperature impacts
- Operating envelope: the range of supply voltage and clock frequency.

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