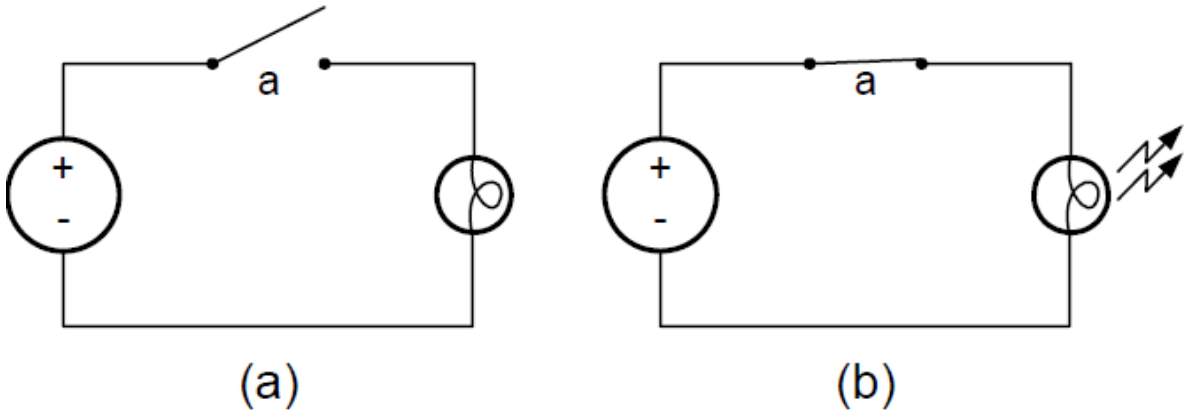
CMOS Logic Circuits – Switch model

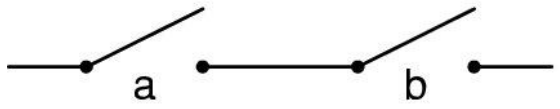
Switch Logic

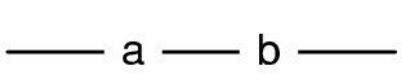
Digital systems use binary variables to represent information and switches to be controlled by the variables to process information.

Variable **a** controls a switch that connects a voltage source to a light bulb.



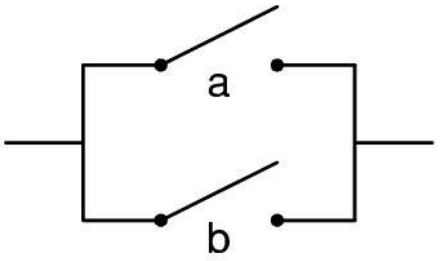
AND, OR, OR-AND Switch Networks

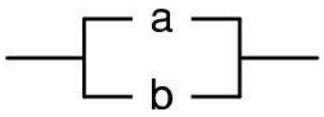




$f = a \wedge b$

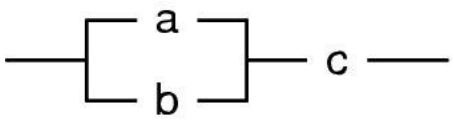
(a)





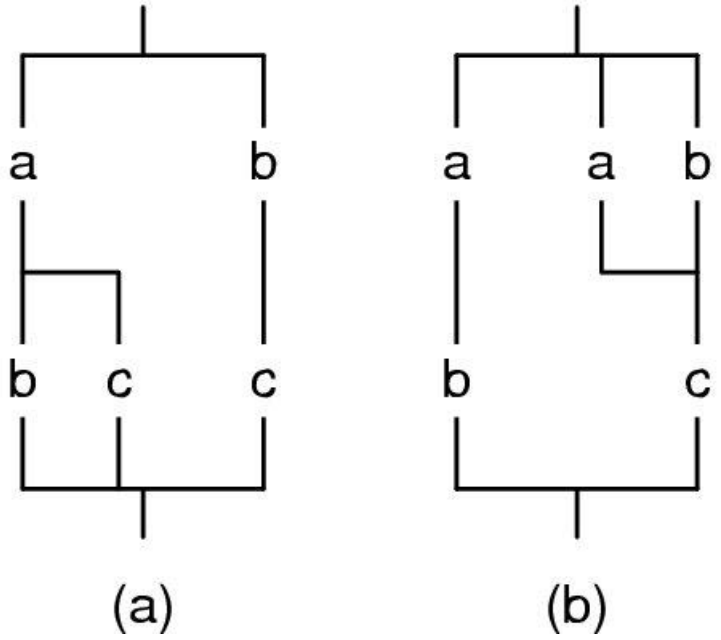
$f = a \vee b$

(b)



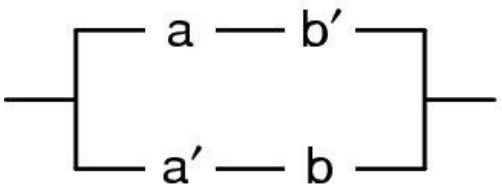
$f = (a \vee b) \wedge c$

Two switch networks of 3-input majority function

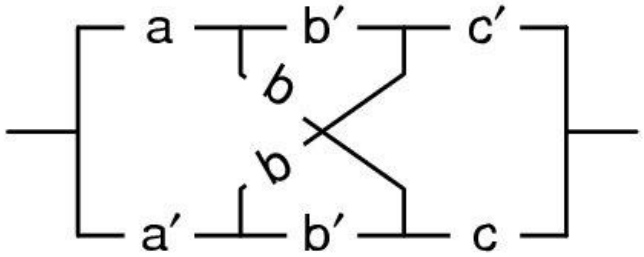


$$f = (a \wedge b) \vee (a \wedge c) \vee (b \wedge c)$$

Switch networks of XOR



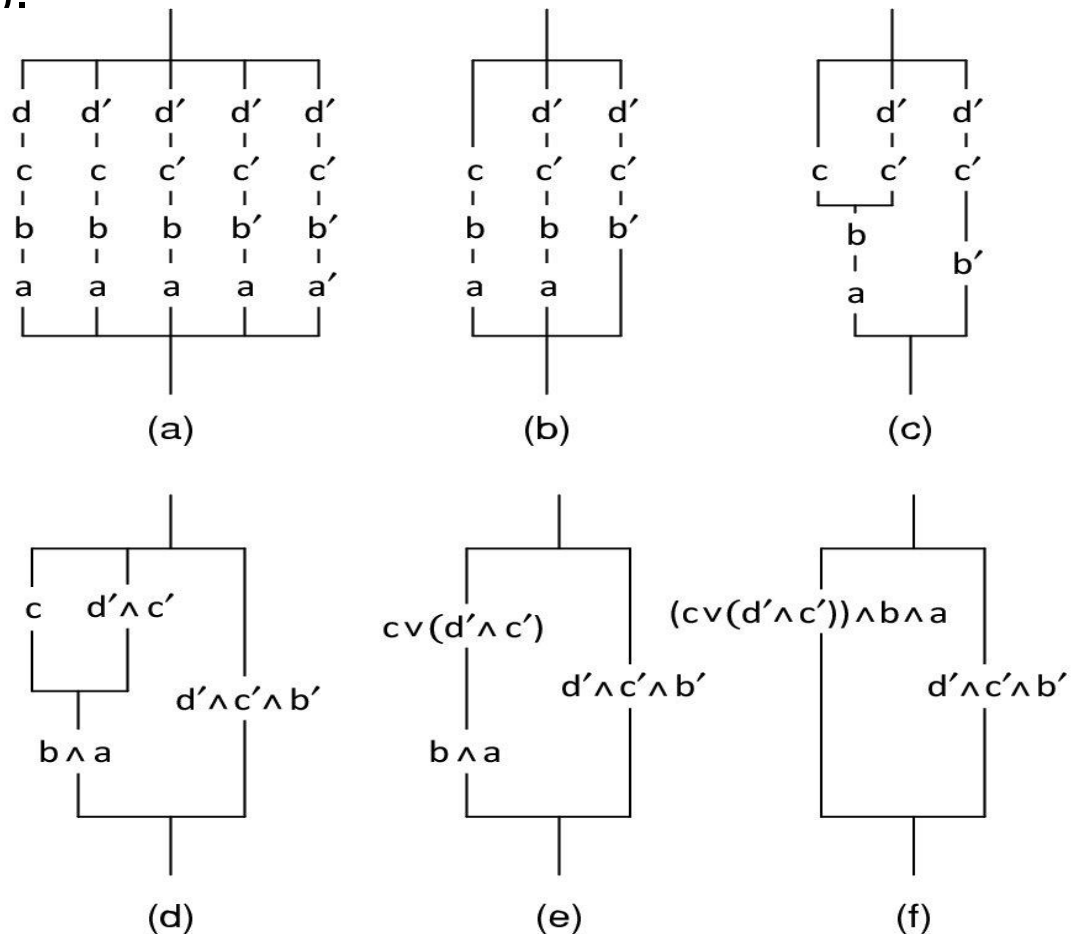
(a)



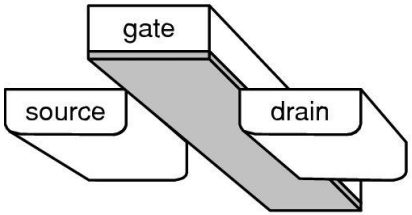
(b)

Example: Series-parallel networks

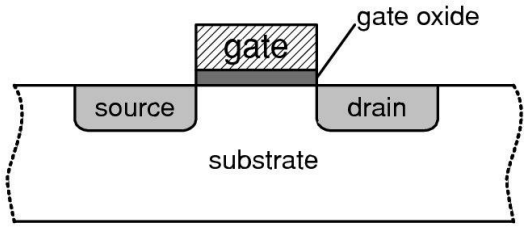
Draw and simplify a series-parallel circuit that realizes the function *f*(*d*,*c*,*b*,*a*) = 1 if *dcba* is a legal thermometer encoding (0000, 0001, 0011, 0111, or 1111).



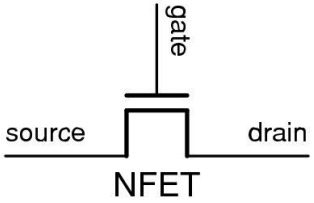
MOS Transistor 구조

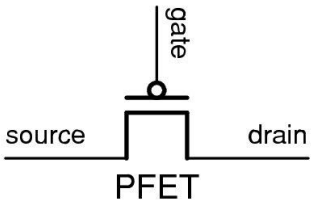


(a)

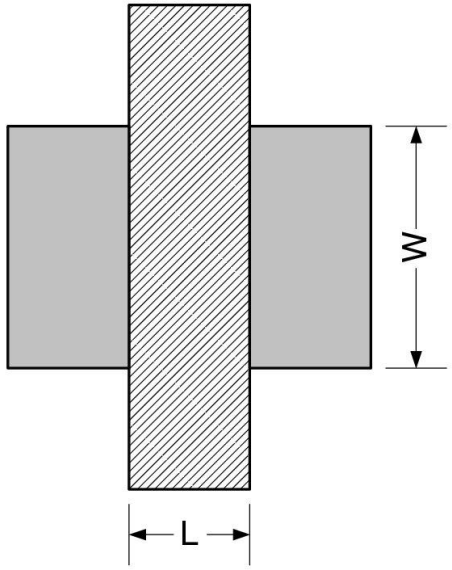


(b)



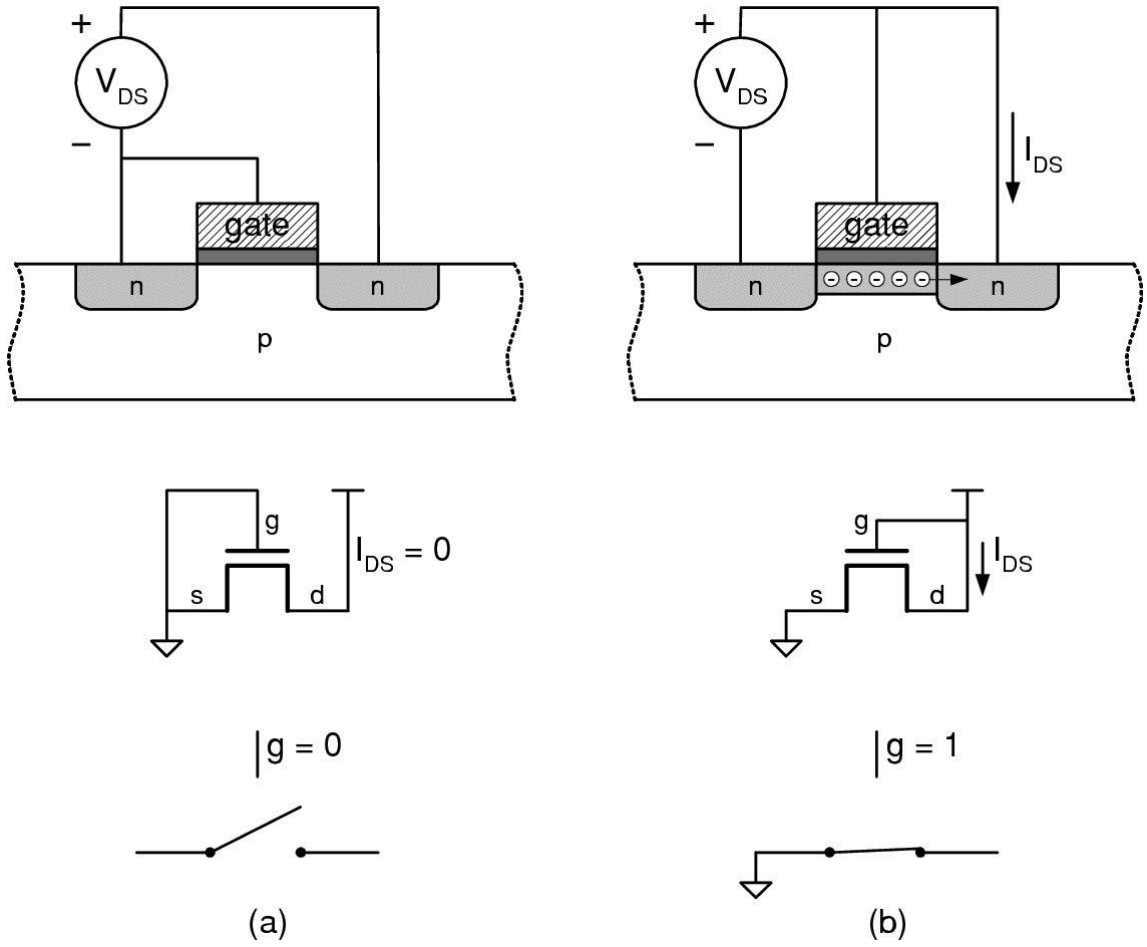


(c)

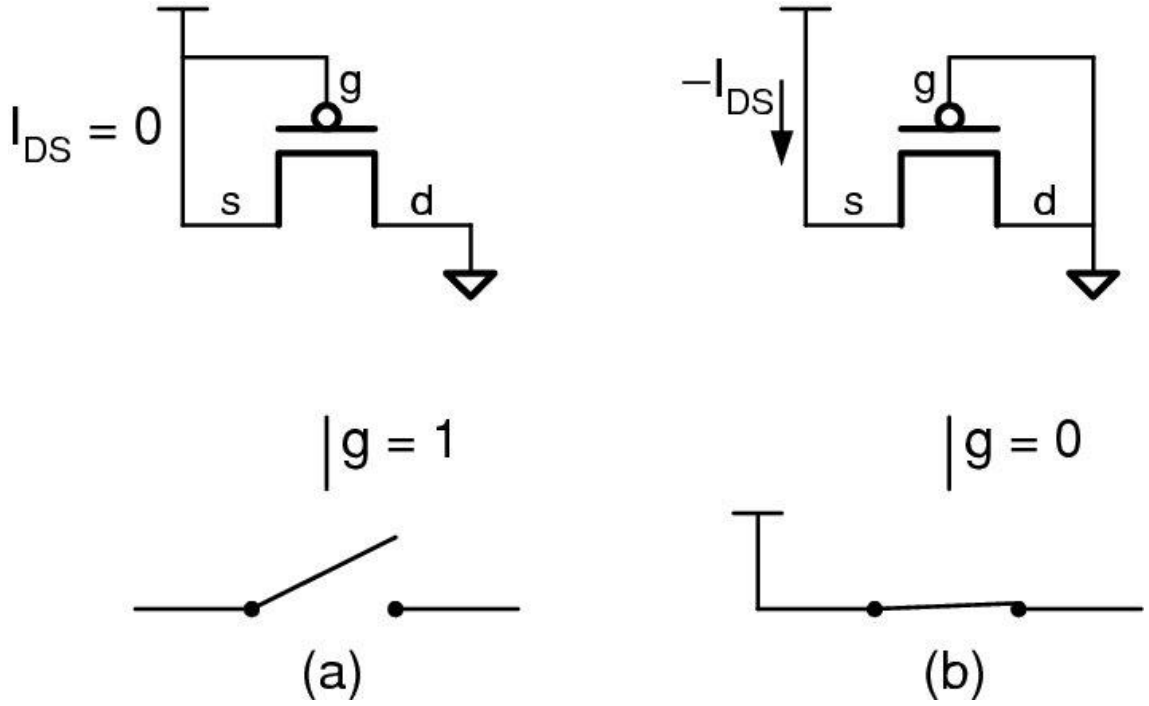


(d)

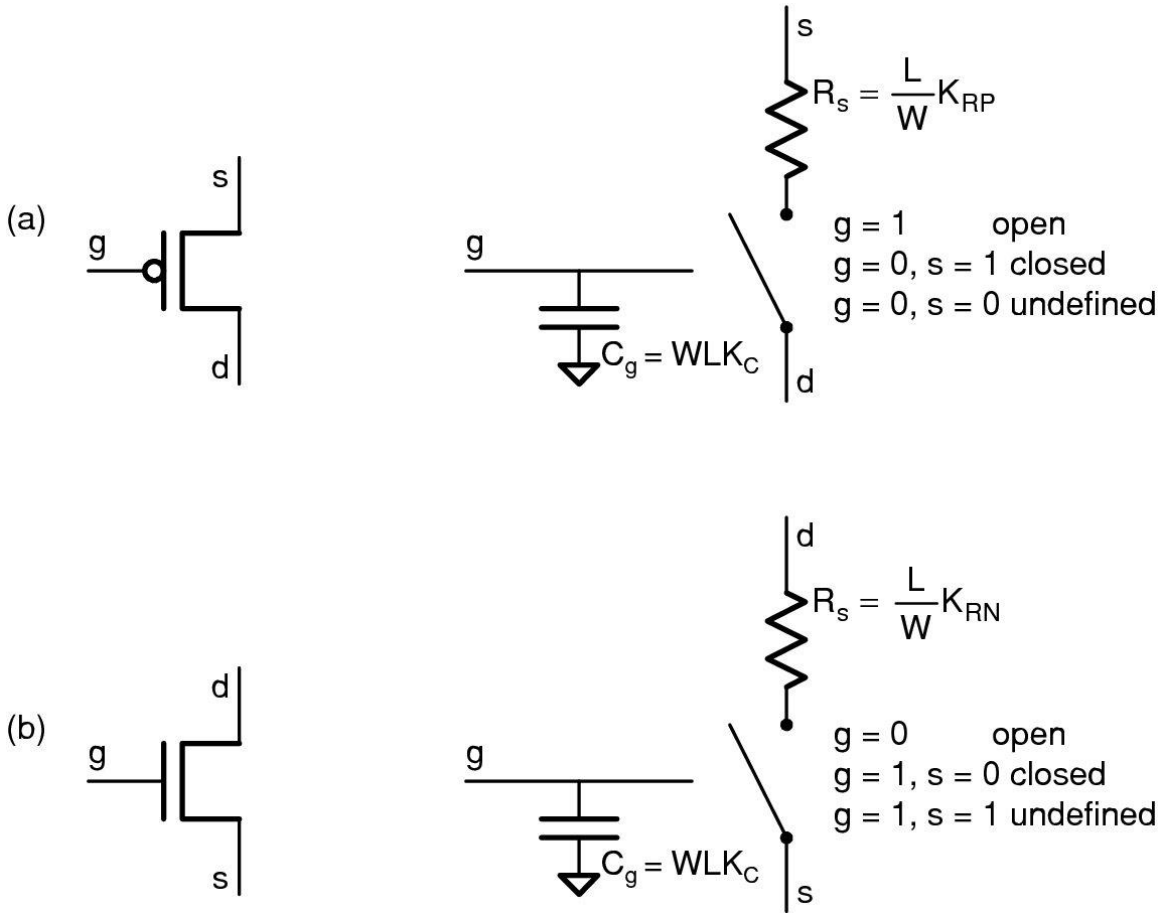
Operation of n-channel MOSFET



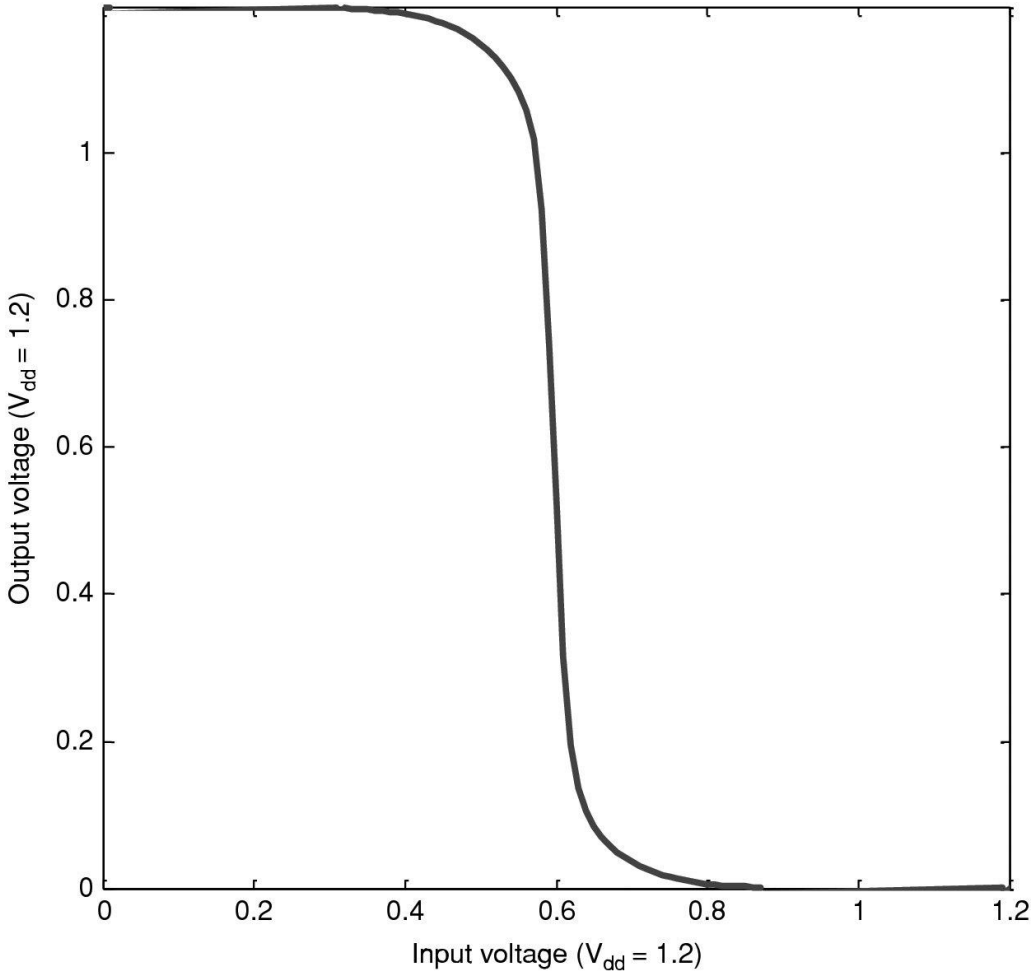
Operation of p-channel MOSFET



Electrical Model of PFET and NFET



Output voltage of an inverter as a function of input voltage



Logic circuit → Switches

Switches → MOS transistors

Logic circuit → MOS transistors

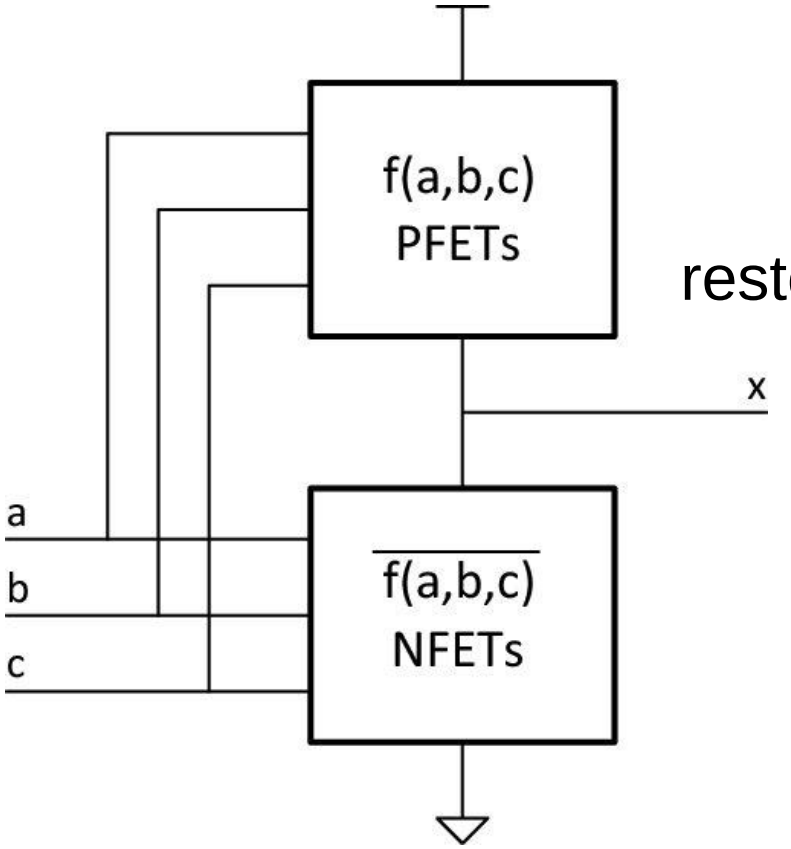
Gate with restoring output → static CMOS gate

Summary

- **Switch logic** to drive gate circuits
- **NMOS ad PMOS transistors** act as switches with restrictions
- **NMOS ad PMOS transistors have the parasitic resistance and capacitance, which affect the switching delay.**

CMOS Logic Circuits - Gates

Static CMOS Gate Circuits



restoring output

Duality?

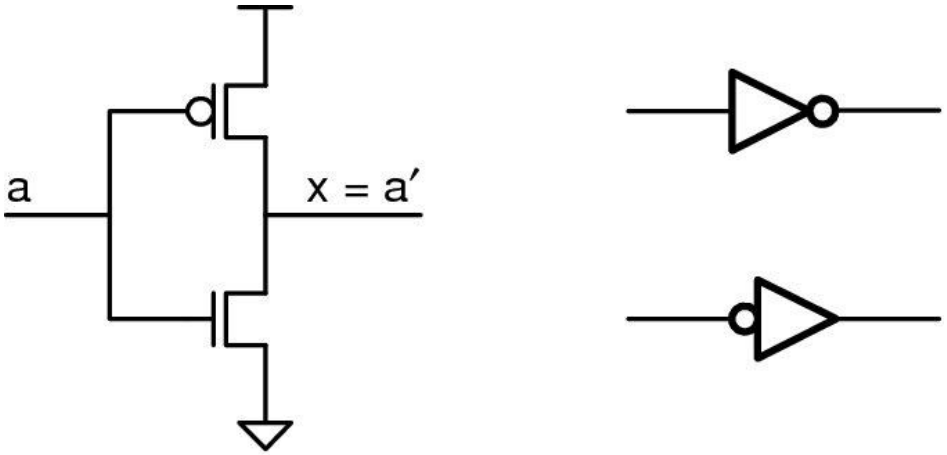
CMOS gate: Monotonic decreasing function

If the transitions on the outputs are in the opposite direction to the transitions on the inputs, it is a ***monotonic decreasing*** or inverting logic function.

If the transitions are in the same direction, it is called a *monotonic increasing* function.

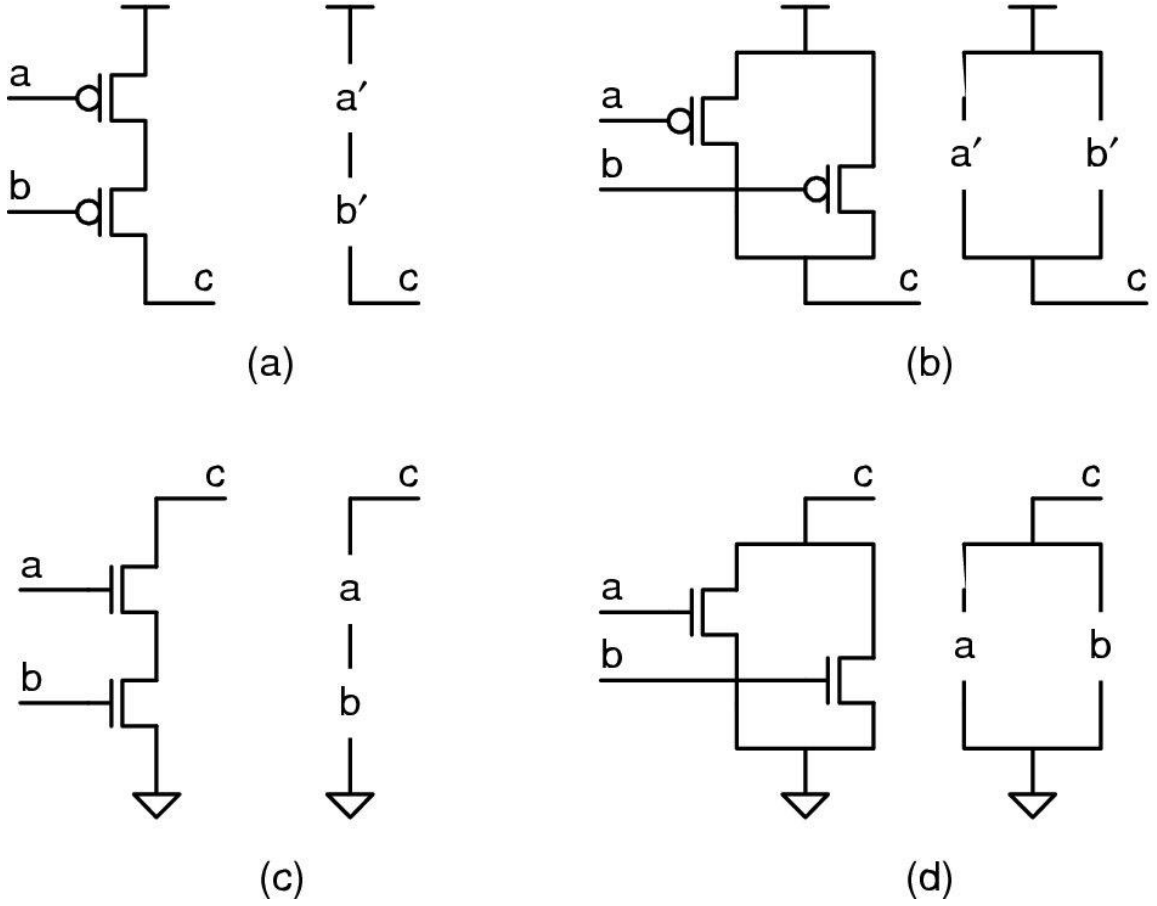
To realize a non-inverting or monotonic increasing logic function requires multiple stages of CMOS gates.

A CMOS Inverter

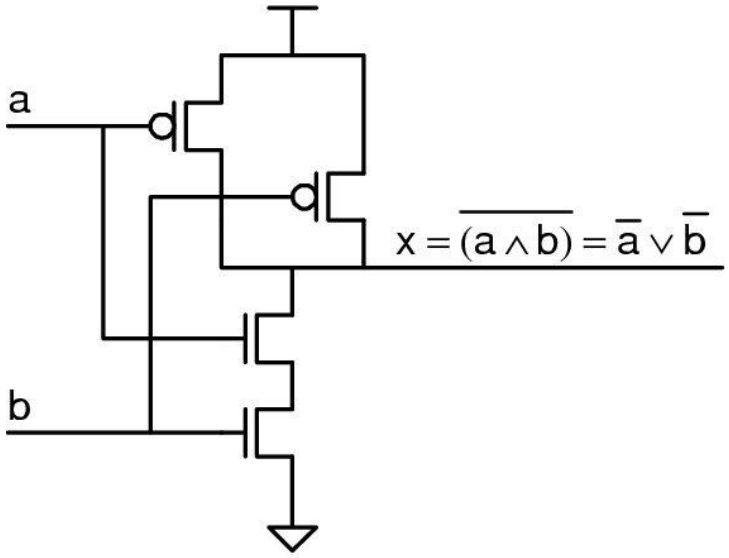


Bubble rule Where possible, signals that are output from a gate with an inversion bubble on its output shall be input to a gate with an inversion bubble on its input.

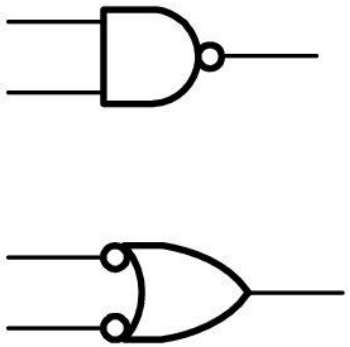
Switch networks used to realize NAND and NOR gates



A CMOS NAND

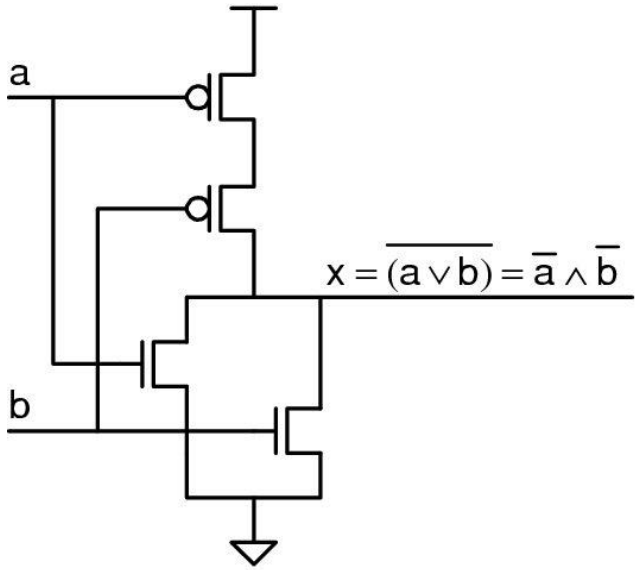


(a)

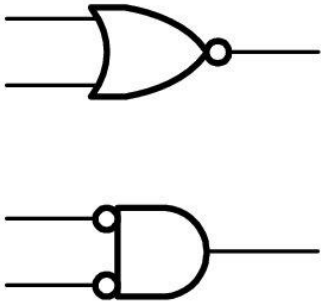


(b)

A CMOS NOR



(a)

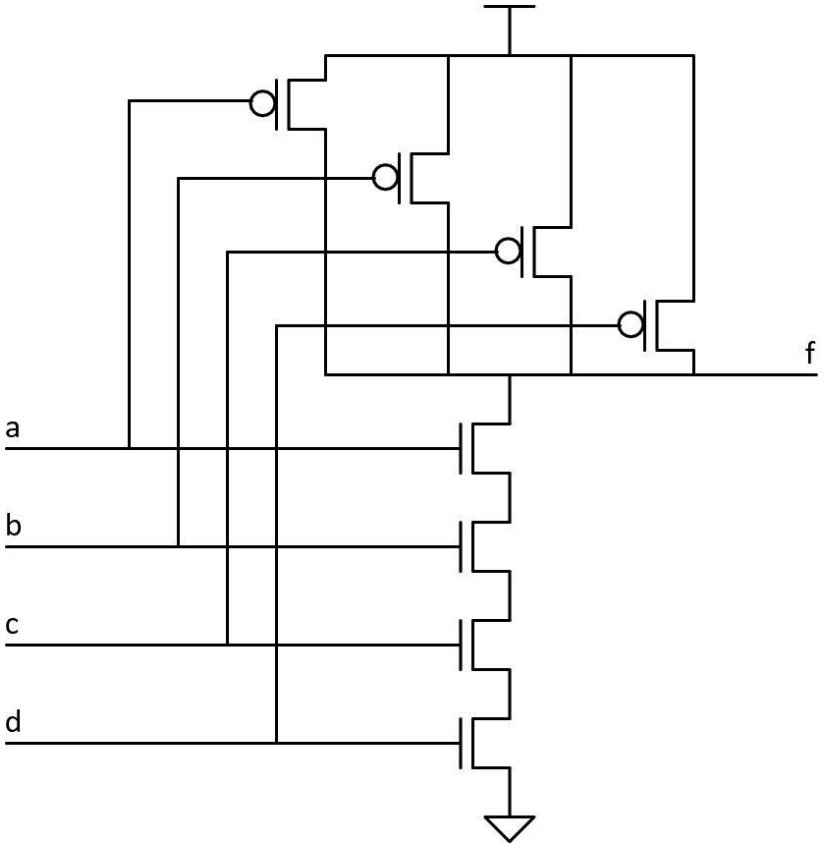


(b)

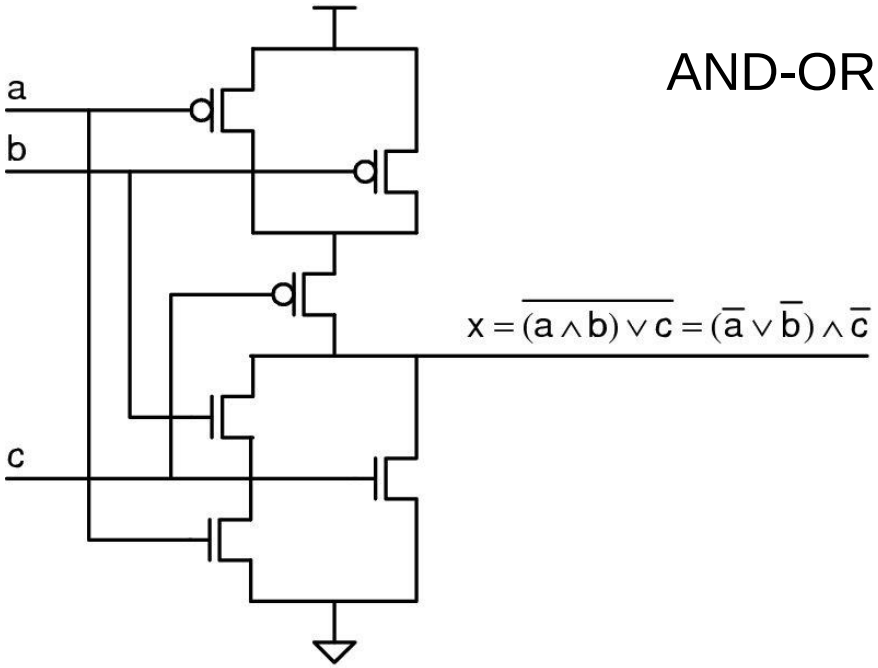
Example: Four-input static CMOS NAND

Draw the transistor-level implementation of a four-input NAND gate

f = $\overline{a \wedge b \wedge c \wedge d}$

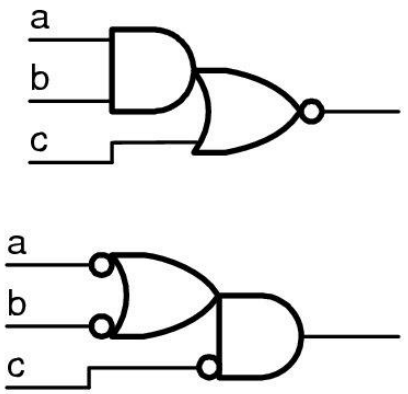


Complex Gates



(a)

AND-OR-inverter (AOI) gate



(b)

Gates built from arbitrary series-parallel (i.e., not a simple series and parallel) networks or networks that are not series-parallel.

XOR gates

Boolean equation for 2-input XOR gate?

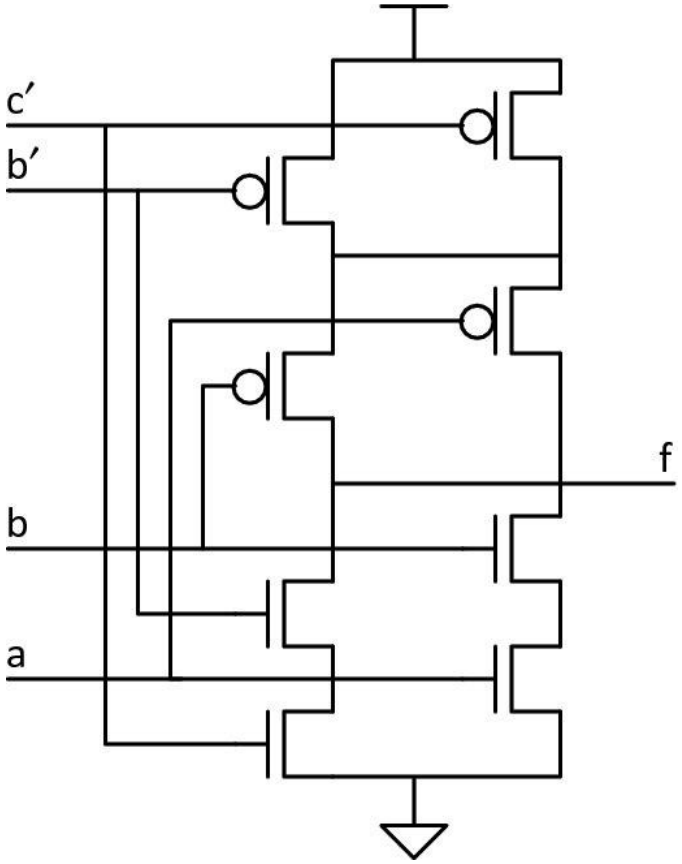
Can we build a single-stage 2-input XOR gate ?

Boolean equation for 3-input XOR gate?

Can we build a single-stage 3-input XOR gate ?

Example: CMOS gate synthesis

Draw a complex gate for $f = \overline{(\bar{c} \wedge \bar{b}) \vee (b \wedge a)}$

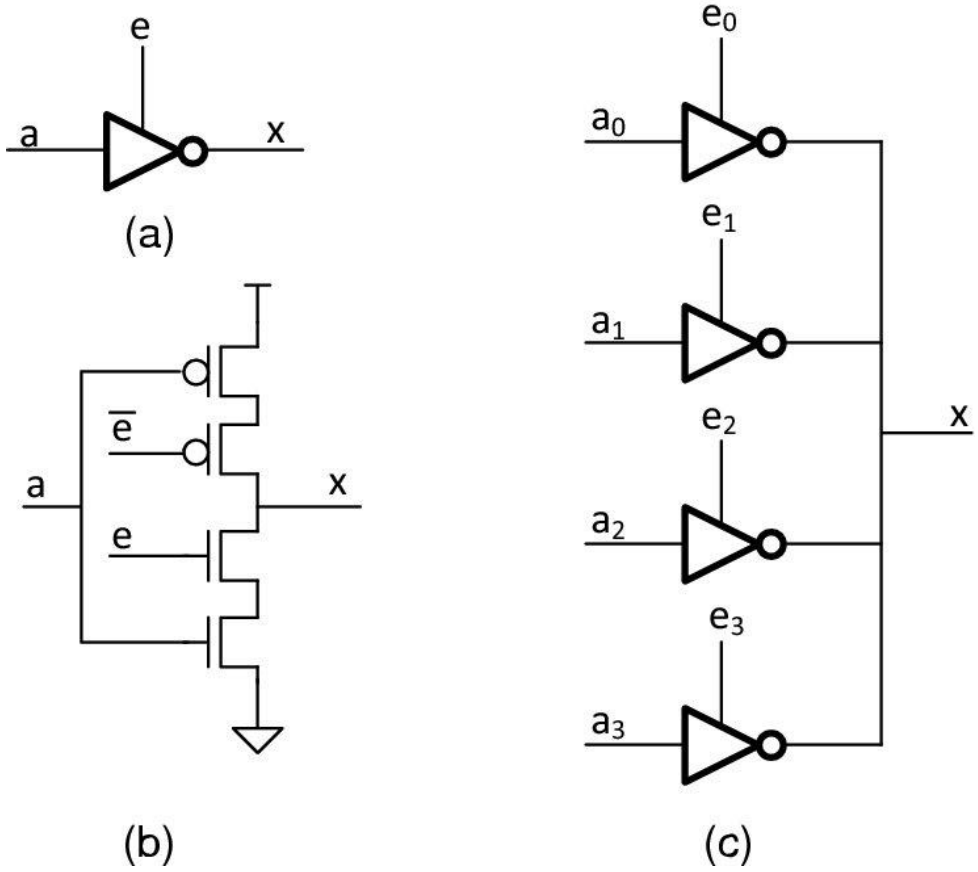


Summary

- CMOS gate circuit to implement a logic function f.
  - Pull-down NFET network to implement for f = 0.
  - Pull-up PNET network to implement for f = 1.
  - Dual network of NFET network
- Inverters, NANDs, NORs, and Complex gates
- All CMOS gates are *monotonically decreasing.*
- Multiple stages of CMOS gates are requited to build increasing or non-inverting functions.

CMOS Logic Circuits – Tri-state

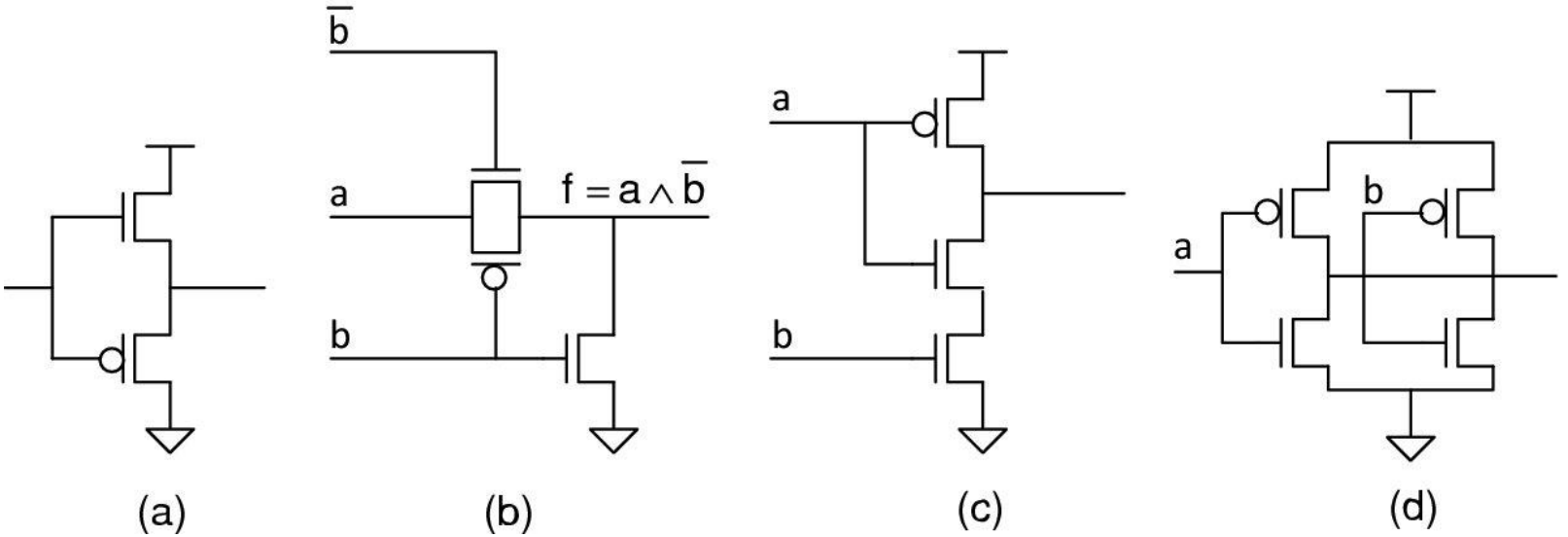
Tri-state circuit



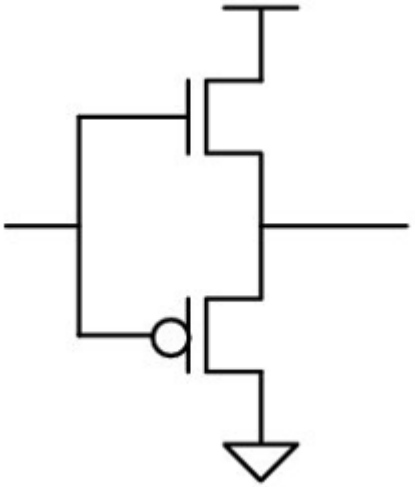
Tri-state-inverter Multiplexer using tri-state-inverters

Circuits to avoid

These are NOT static gates: do not use these circuits

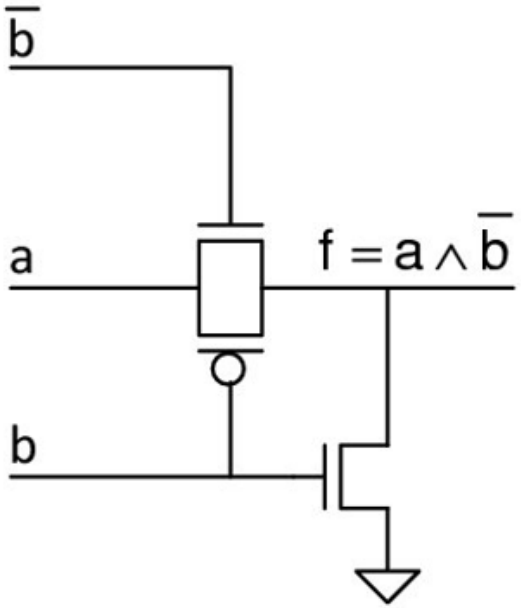


(a) Would-be-buffer



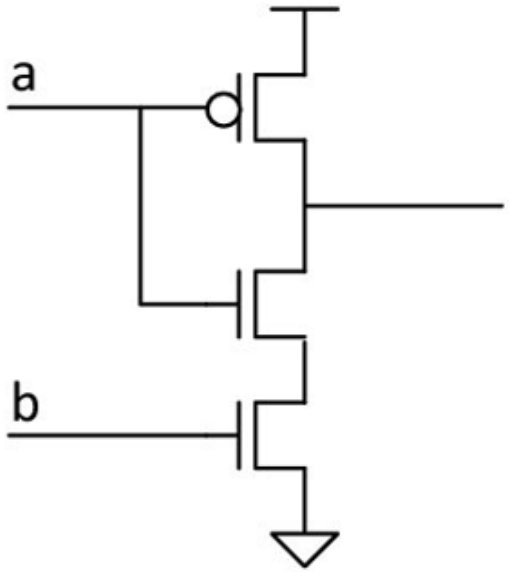
It attempts to pass 1 through NFET and a 0 through PFET.

(b) No-restoring circuit



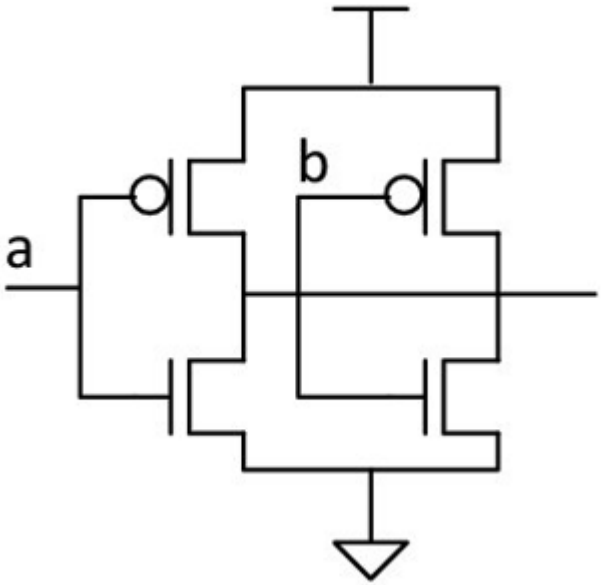
It does not restore its output. If b = 0, a noise in input a is passed directly to the output.

(c) Tri-state circuit



When a = 1 and b = 0, its output is disconnected. Due to parasitic capacitance, the previous output value will be stored for a short period of time on the output node. However, after a period, the stored charge will _____ and the output node becomes _____ value.

(d) Short circuit



Both of the pull-up and pull-down network conduct when a and b are not equal. This static current from power to ground outputs _____ value, wasting _____, and potentially _____ the chip.

Summary

- **Tri-state circuits**: Not a CMOS gate, can be in unconnected state