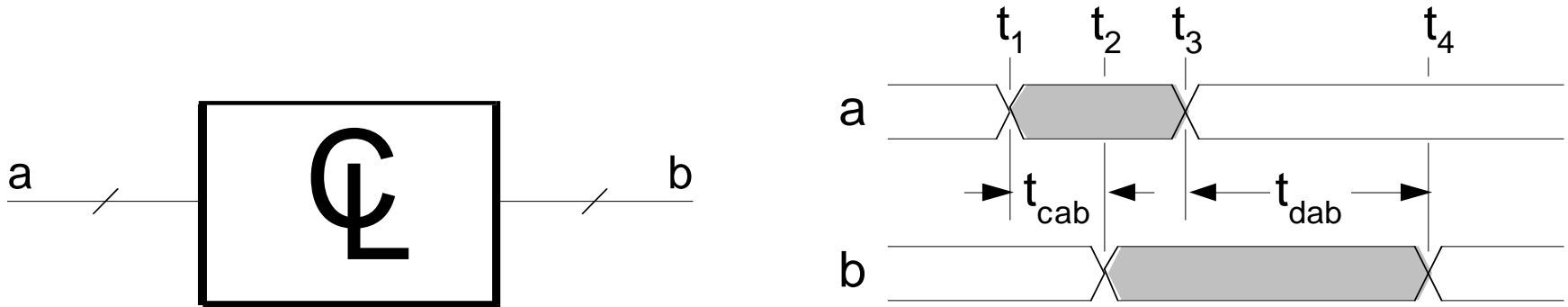

Timing Constraints – Delays

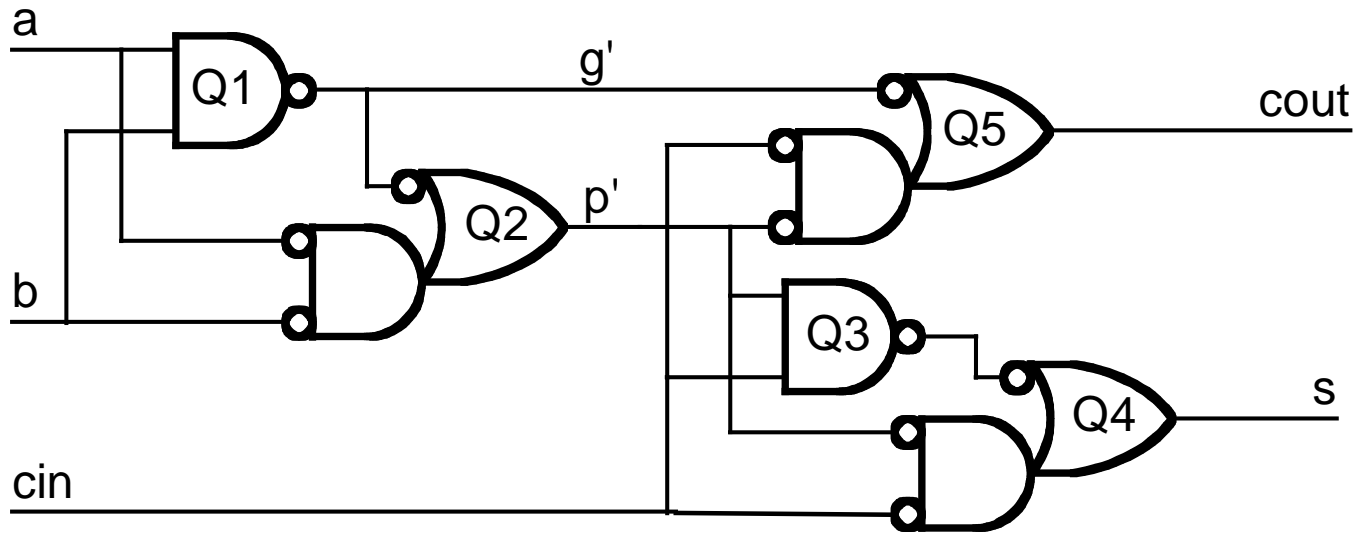
Propagation Delay and Contamination Delay

Propagation Delay – Time from last input change until last output change. (Input at steady state to output at steady state.)

Contamination Delay – Time from first input change until first output change. (Input contaminated to output contaminated)



Example: Contamination and Propagation Delay of Full Adder



Gate	Delay (ps)
Nand2	80
OAI21	120

min	a,b	cin
g'	80	-
p'	120	-
cout	200	120
U3	200	80
s	240	120

max	a,b	cin
g'	80	-
p'	200	-
cout	320	120
U3	280	80
s	400	200

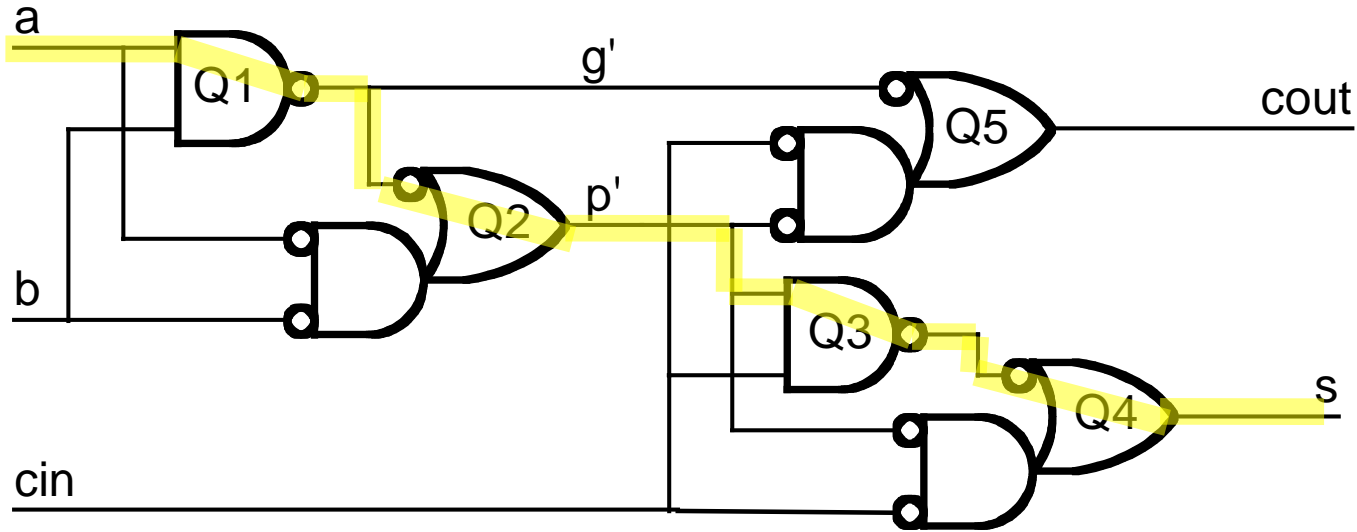
What is

t_{das}

t_{cas}

t_{dcs}

t_{ccc}



Gate	Delay (ps)
Nand2	80
OAI21	120

min	a,b	cin
g'	80	-
p'	120	-
cout	200	120
U3	200	80
s	240	120

max	a,b	cin
g'	80	-
p'	200	-
cout	320	120
U3	280	80
s	400	200

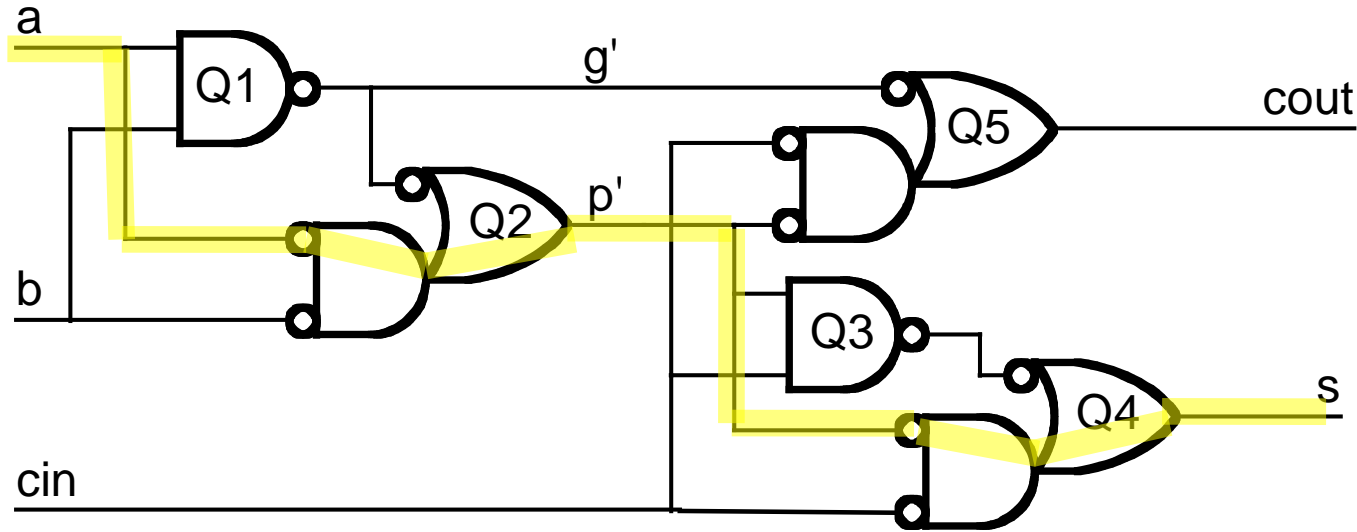
What is

t_{das}

t_{cas}

t_{dcs}

t_{ccc}



Gate	Delay (ps)
Nand2	80
OAI21	120

min	a,b	cin
<i>g'</i>	80	-
<i>p'</i>	120	-
<i>cout</i>	200	120
U3	200	80
<i>s</i>	240	120

max	a,b	cin
<i>g'</i>	80	-
<i>p'</i>	200	-
<i>cout</i>	320	120
U3	280	80
<i>s</i>	400	200

What is

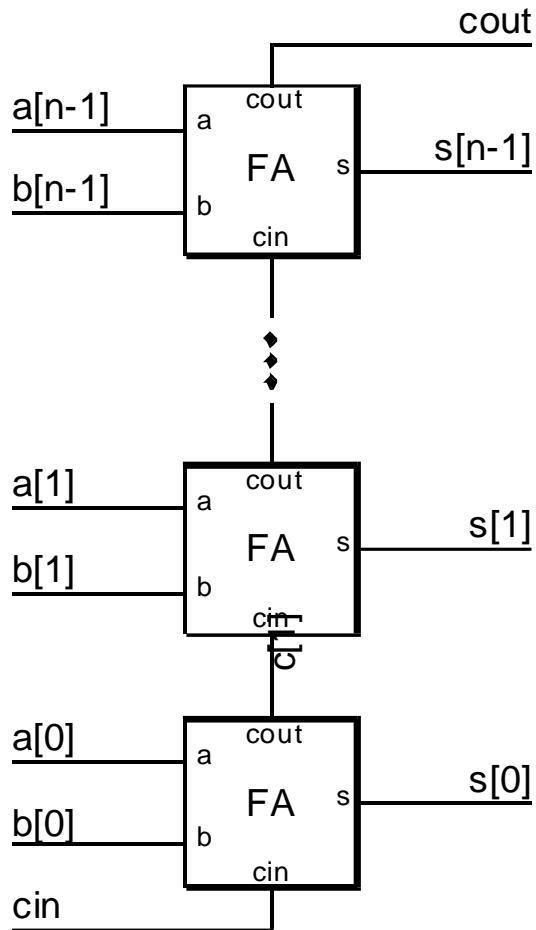
t_{das}

t_{cas}

t_{dcs}

t_{ccc}

What about an n-bit adder?



Assume delay of FA is 1

What is

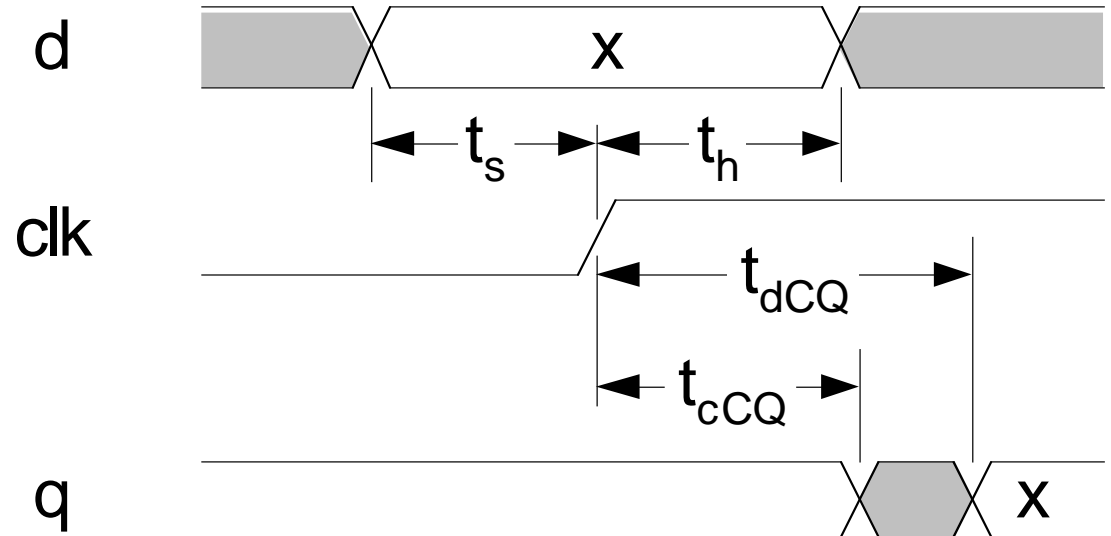
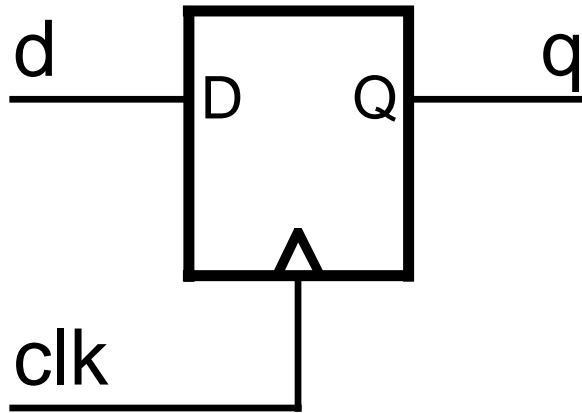
t_{das}

t_{cas}

t_{dcs}

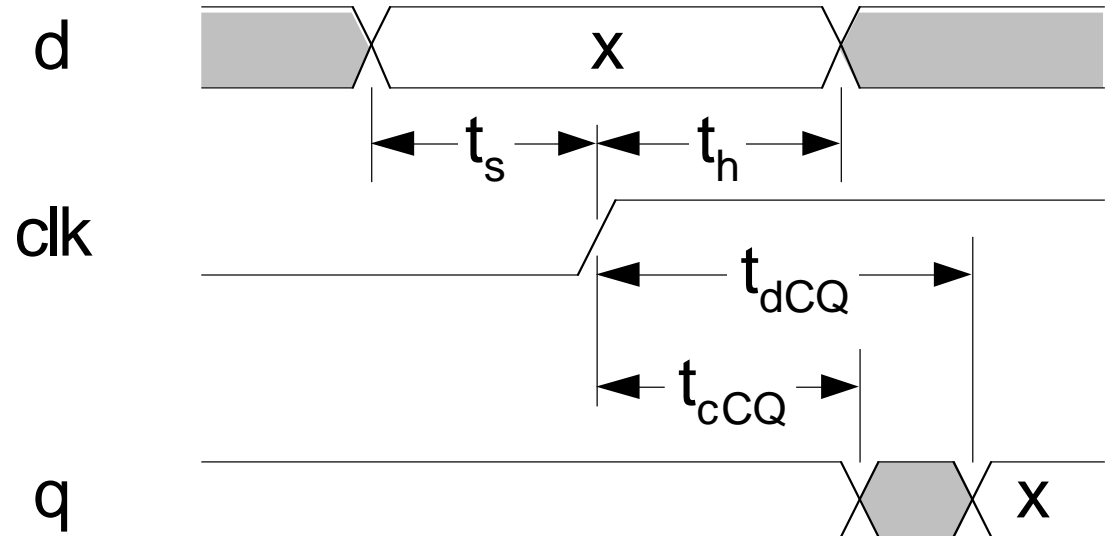
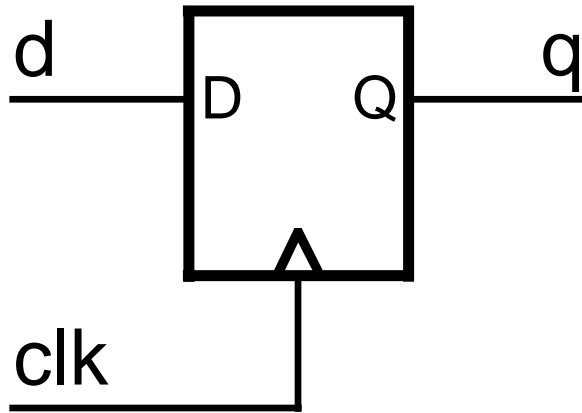
t_{ccs}

Edge-Triggered D Flip-Flop

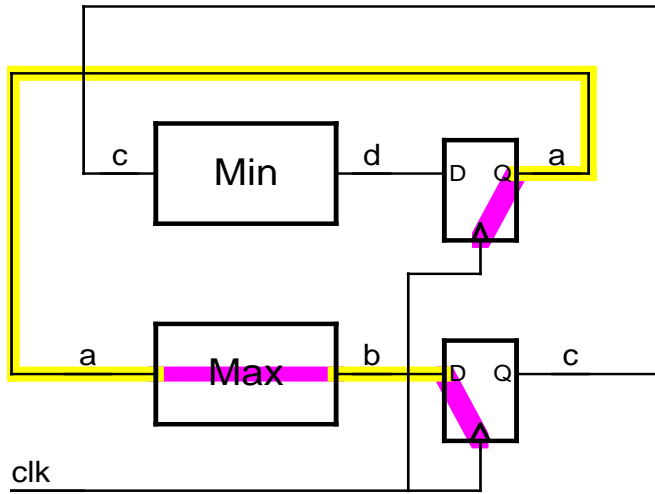


Timing Constraints – Setup and hold

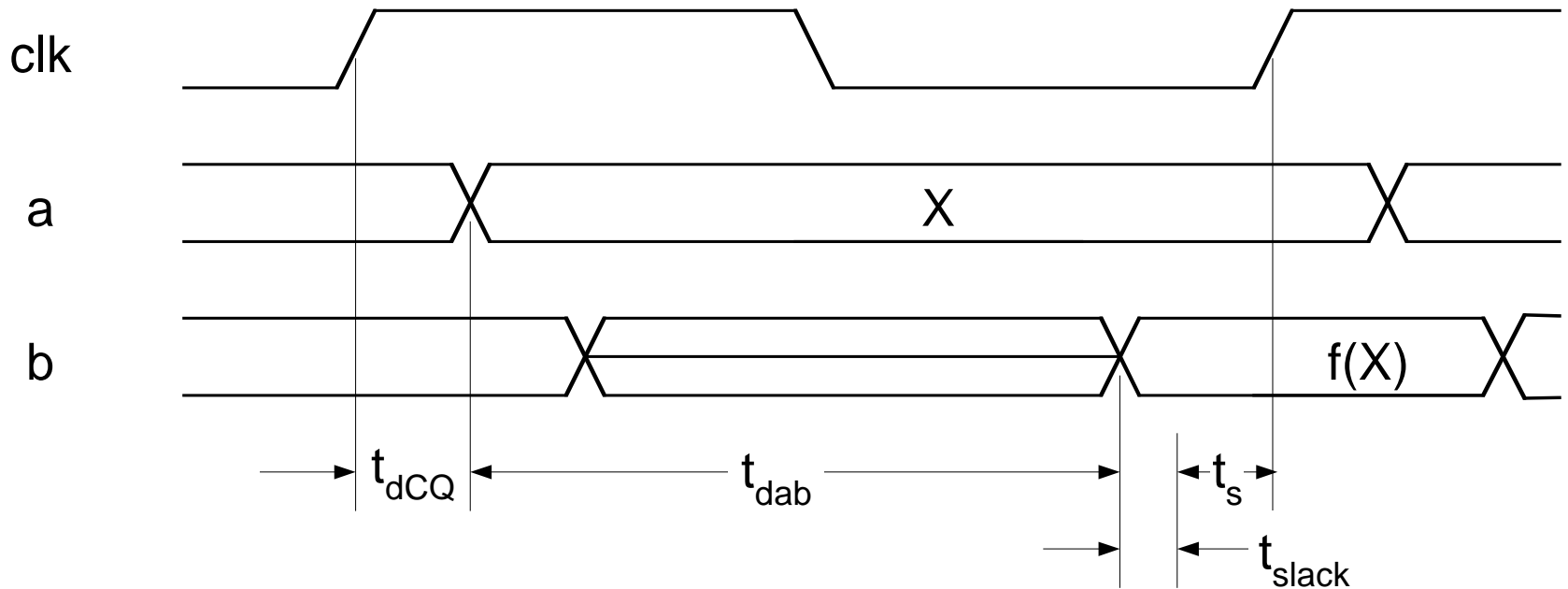
Edge-Triggered D Flip-Flop



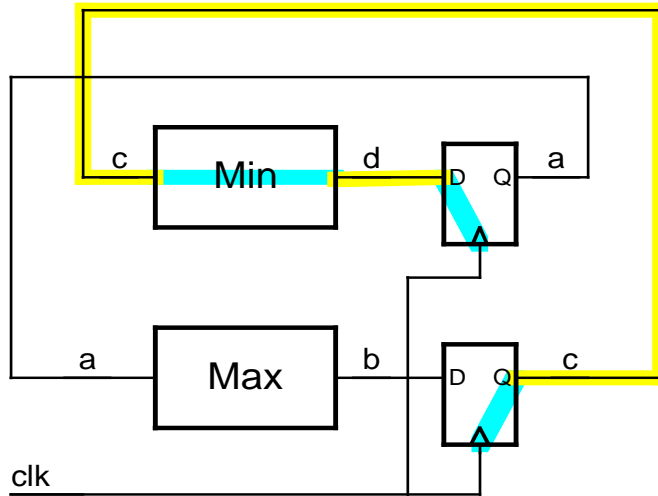
Setup Time Constraint



$$t_{cy} > t_{dCQ} + t_{dMax} + t_s$$

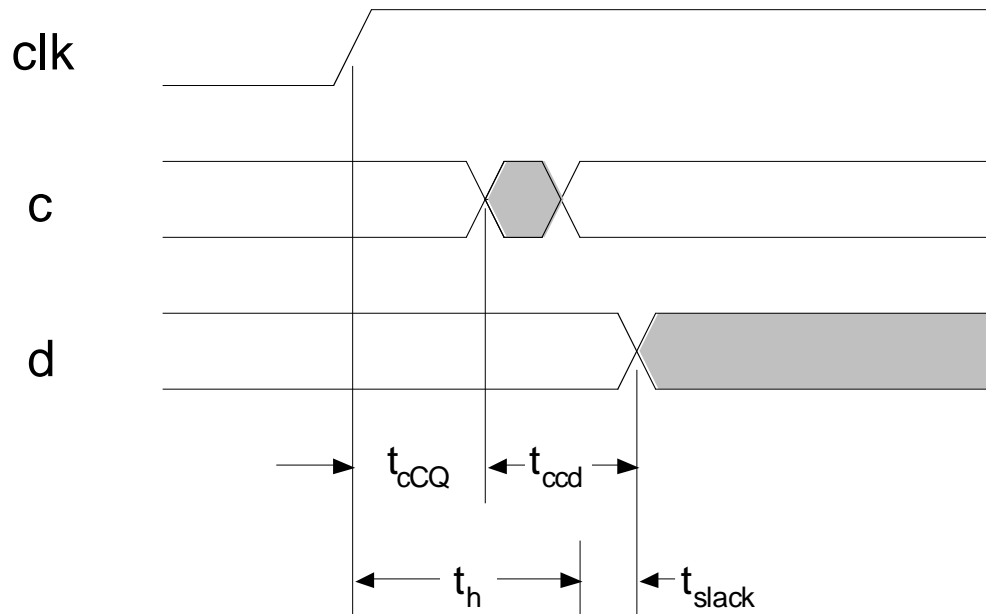


Hold Time Constraint



$$t_h < t_{cCQ} + t_{cMin}$$

Unsafe at any speed



t_{cXY} – contamination delay

t_{dXY} – propagation delay

Example

$$t_{dcQ} = t_{ccQ} = t_s = 150\text{ps}$$

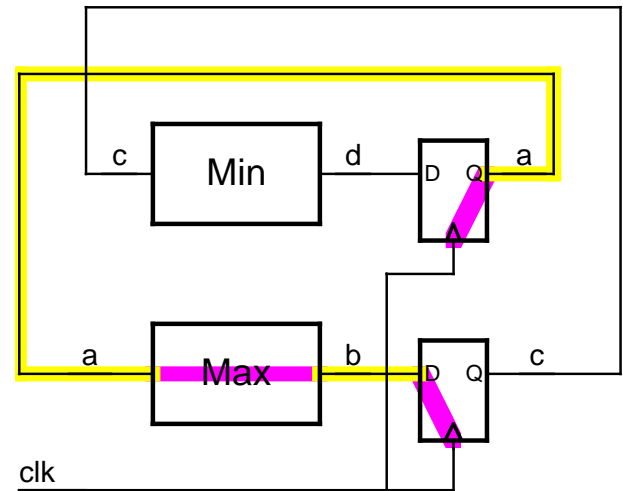
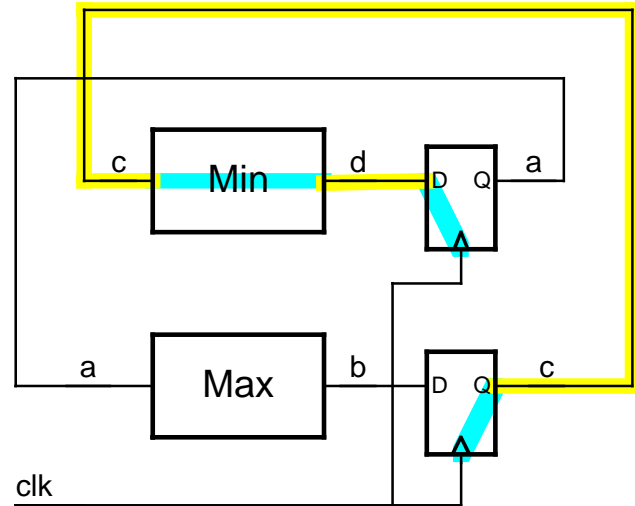
$$t_h = 250\text{ps}$$

$$t_{dMax} = 850\text{ps}$$

$$t_{cMin} = 100\text{ps}$$

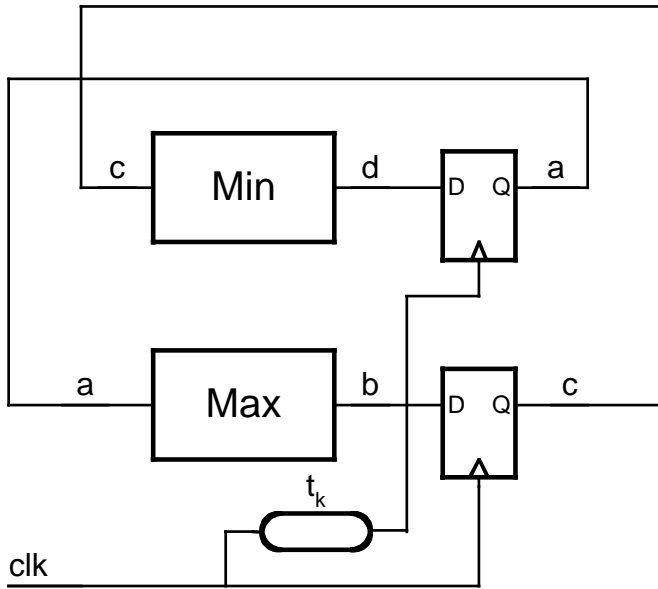
Is hold time constraint met?

What is the minimum cycle time?



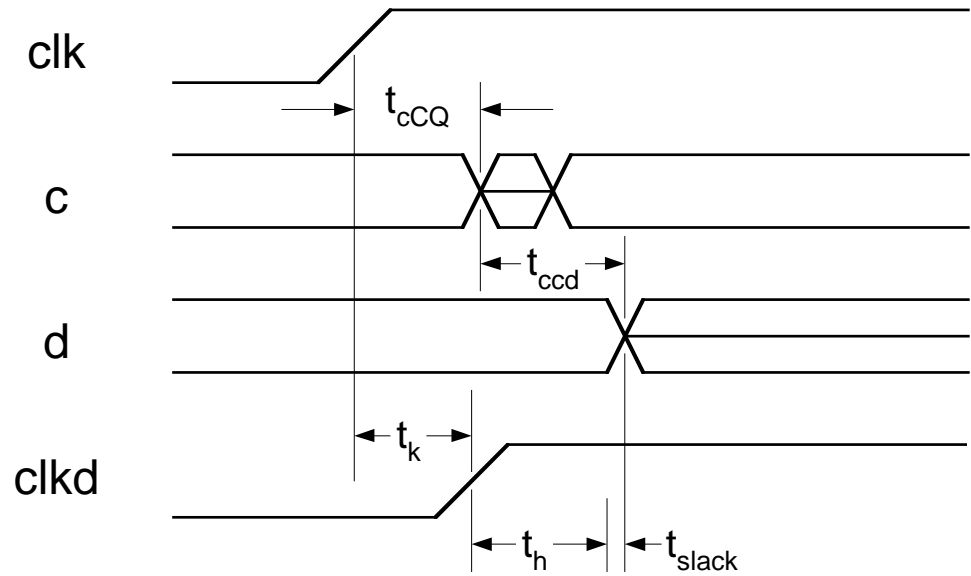
Timing Constraints – Clock skew

Clock Skew



$$t_{cy} > t_{dCQ} + t_{dMax} + t_s + t_k$$

$$t_h < t_{cCQ} + t_{cMin} - t_k$$



Example

$$t_{dCQ} = t_{cCQ} = t_s = 150\text{ps}$$

$$t_h = 250\text{ps}$$

$$t_{dMax} = 850\text{ps}$$

$$t_{cMin} = 100\text{ps}$$

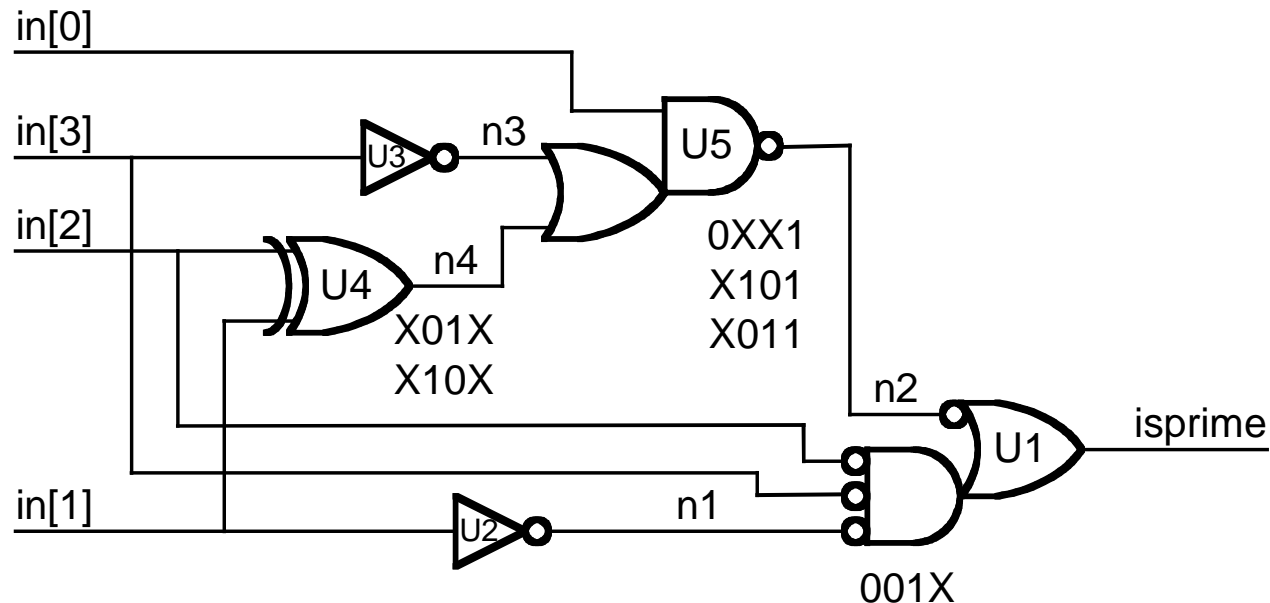
$$t_k = 100\text{ps}$$

Is hold time constraint met?

What is the minimum cycle time?

4-bit Prime or one Function in Verilog Code – Result of synthesizing description using case

```
module prime ( in, isprime );  
input  [3:0] in;  
output isprime;  
    wire n1, n2, n3, n4;  
    OAI13 U1 ( .A1(n2), .B1(n1), .B2(in[2]), .B3(in[3]), .Y(isprime) );  
    INV   U2 ( .A(in[1]), .Y(n1) );  
    INV   U3 ( .A(in[3]), .Y(n3) );  
    XOR2  U4 ( .A(in[2]), .B(in[1]), .Y(n4) );  
    OAI12 U5 ( .A1(in[0]), .B1(n3), .B2(n4), .Y(n2) );  
endmodule
```



Synthesis Reports

```

*****
Report : area
Design : prime
Version: 2003.06
Date   : Sat Oct  4 11:38:08 2003
*****

```

Library(s) Used:

```

GS30KA_W_125_1.35_CORE.db (File:
/home7imagine/from_ti/g30ka_1.3/sun5/synop
sys/lib/GS30KA_W_125_1.35_CORE.db)

```

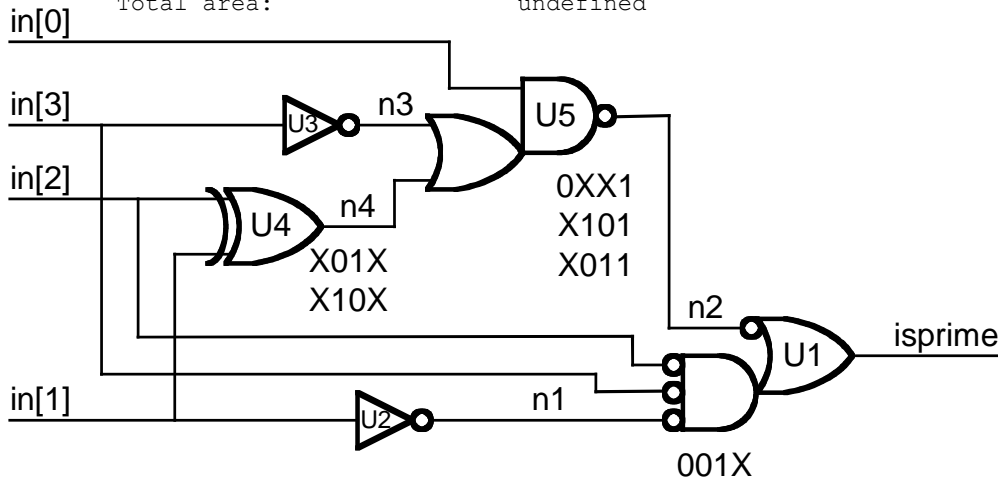
```

Number of ports:      5
Number of nets:       9
Number of cells:      5
Number of references: 4

Combinational area:   7.000000
Noncombinational area: 0.000000
Net Interconnect area: undefined (Wire load has zero
net area)

Total cell area:      7.000000
Total area:           undefined

```



```

*****
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : prime
Version: 2003.06
Date   : Sat Oct  4 11:38:08 2003
*****

```

Operating Conditions:
Wire Load Model Mode: enclosed

```

Startpoint: in[2] (input port)
Endpoint: isprime (output port)
Path Group: (none)
Path Type: max

```

Des/Clust/Port	Wire Load Model	Library	Point	Incr	Path

prime	2K 5LM	GS30KA_W_125_1.35_CORE.db			

			input external delay	0.000	0.000
			r		
			in[2] (in)	0.000	0.000
			r		
			U4/Y (EX210)	0.191	0.191
			f		
			U5/Y (BF051)	0.116	0.307
			r		
			U1/Y (BF052)	0.168	0.475
			f		
			isprime (out)	0.000	0.475
			f		
			data arrival time		0.475

			(Path is unconstrained)		

Summary

- Delays in digital systems
 - Propagation delay
 - Contamination delay
- Flip-flop timing constraints
 - Setup time (t_s)
 - Hold time (t_h)
- Cycle time determined by maximum delay
$$t_{cy} > t_{dCQ} + t_{dMax} + t_s$$
- Correct operation depends on minimum delay
$$t_h < t_{cCQ} + t_{cMin}$$
- Clock skew affects both
$$t_{cy} > t_{dCQ} + t_{dMax} + t_s + t_k$$
$$t_h < t_{cCQ} + t_{cMin} - t_k$$