Overview of NAND Flash Memory

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Content

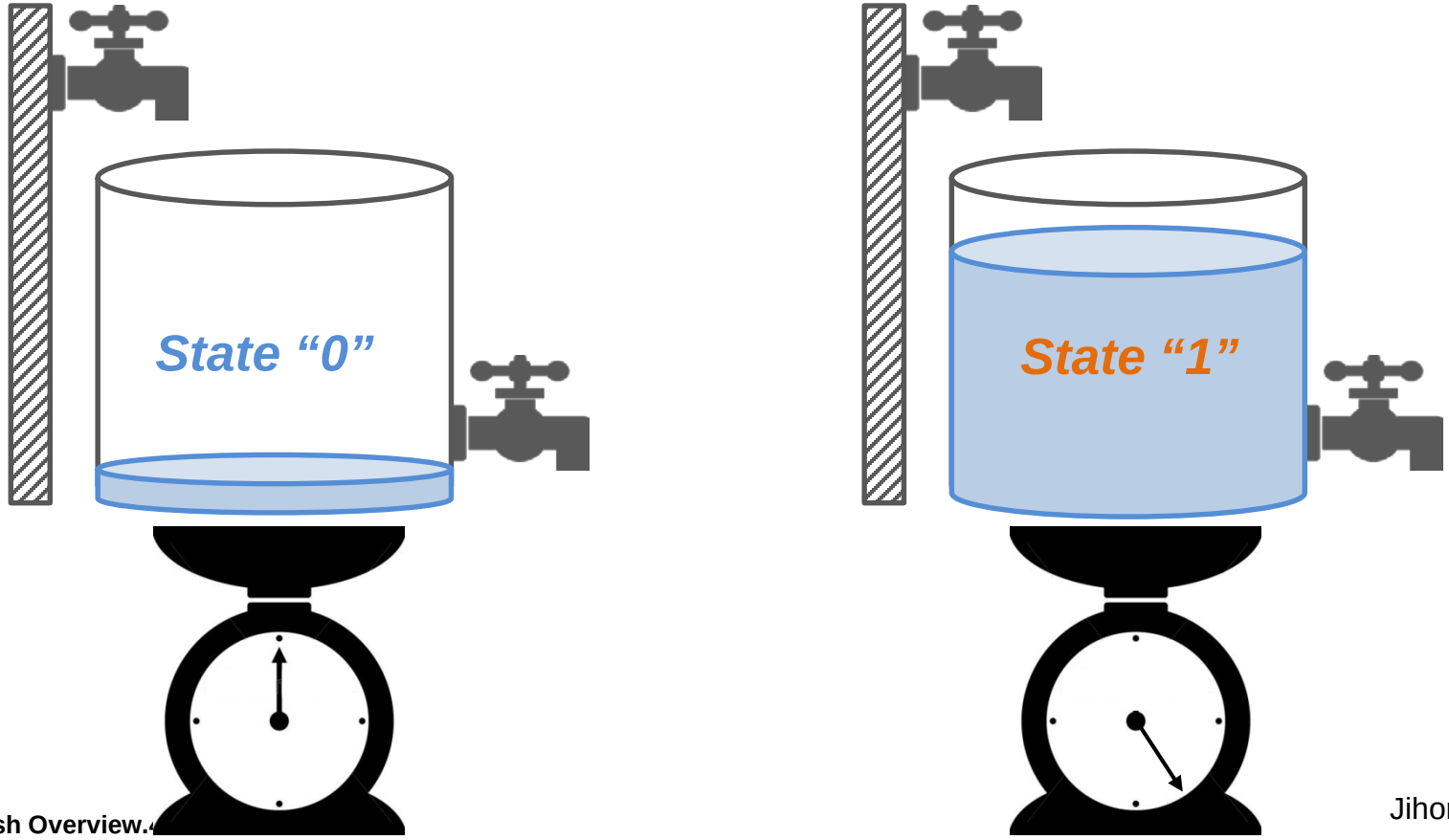
- **Overview of NAND Flash Memory**
  - What is memory?
  - What is electrical memory?
  - Memory hierarchy in MOS memory
  - What is Flash Memory?
  - NAND vs. NOR
  - NAND flash market and applications
  - HDD vs. SSD
- **Under the Hood: Internal Organization of NAND Flash Memory**
  - Chip / Plane / IO
  - Block
  - Page
  - WL / BL / SSL / GSL
  - Cell structure
  - Control block diagram

Content

- **Three Basic Operations of NAND Flash Memory**
  - Program
  - Read
  - Erase
- **Key Reliability Issues of NAND Flash Memory**
  - Endurance
  - Data retention
  - Read disturb

What is Memory?

- **Main role is to remember things for later uses.**
  - Need to some ways to store information for future references.
  - Must distinguish states stored.

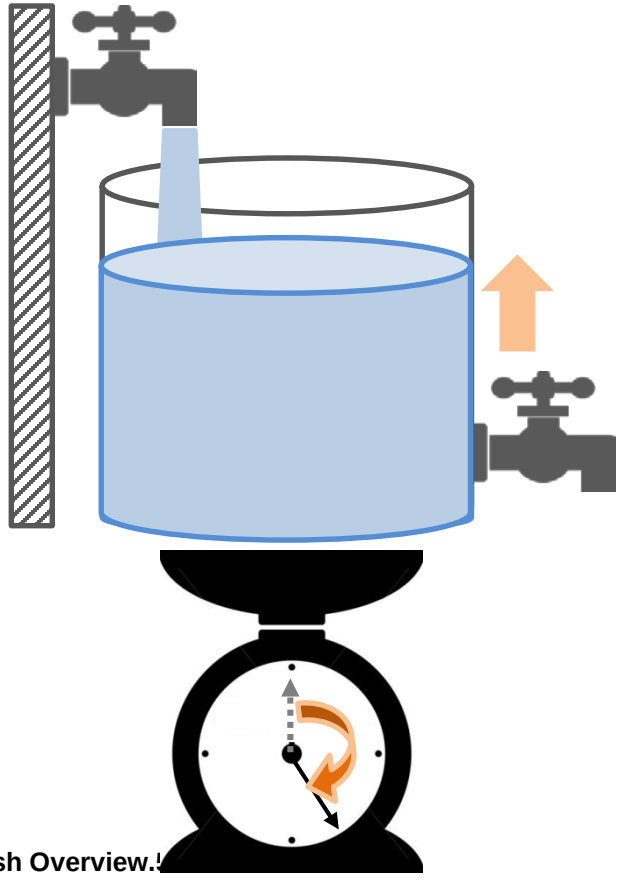


State Management Operations: Write & Erase

- **Basic State Management Operations**
  - store (write) & delete (erase) operations

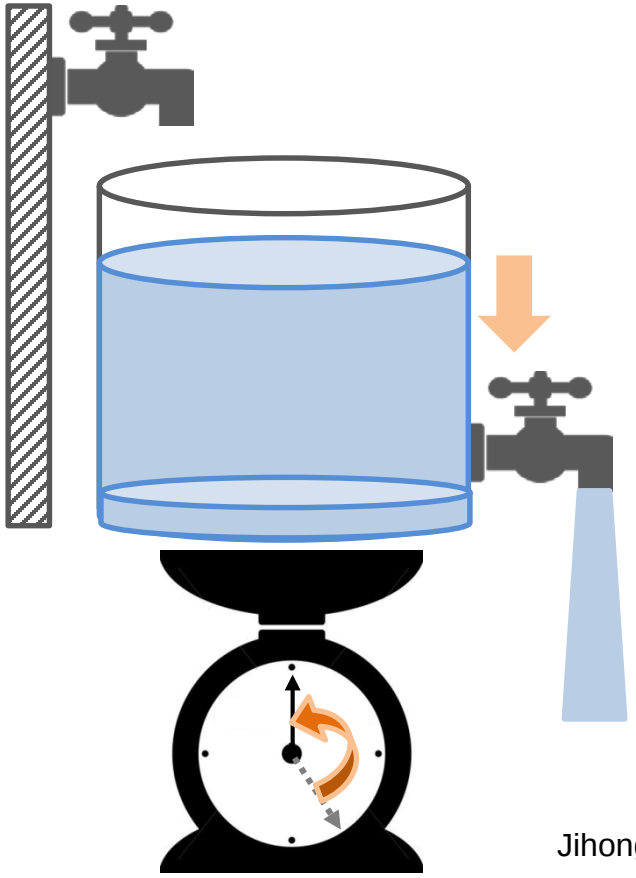
Store (Write)

State “0” → State “1”



Delete (Erase)

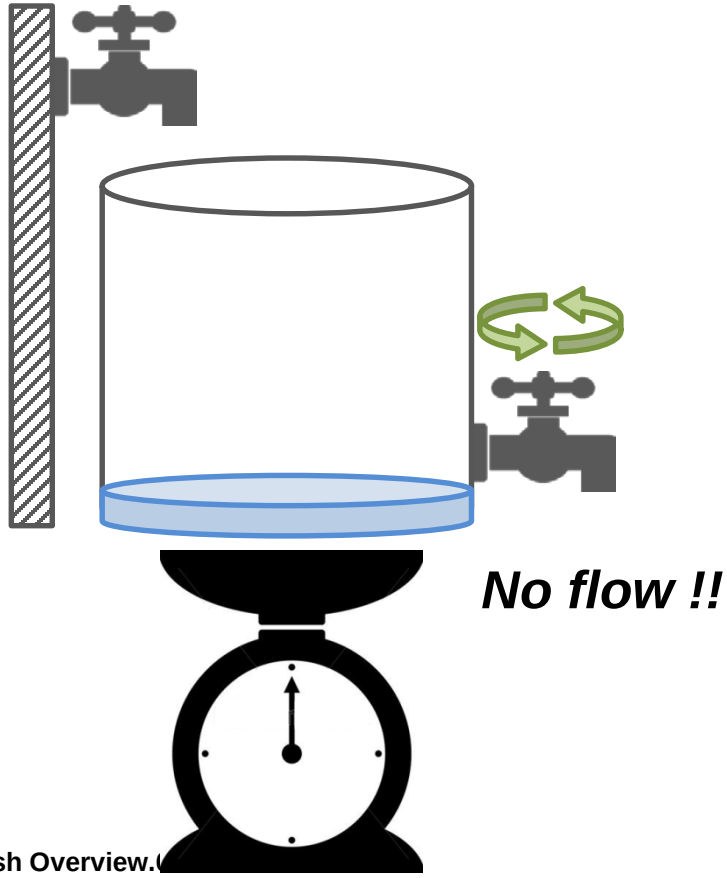
State “1” → State “0”



State Checking Operation: Read

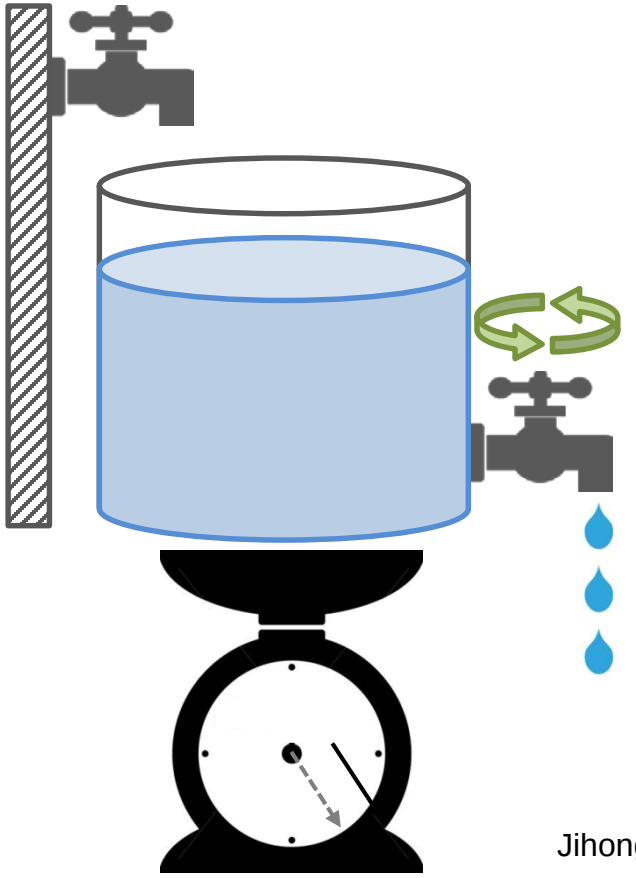
- Have to be checked (read) at desired times with no errors

Check (Read) as State "0"



No flow !!

Check (Read) as State "1"

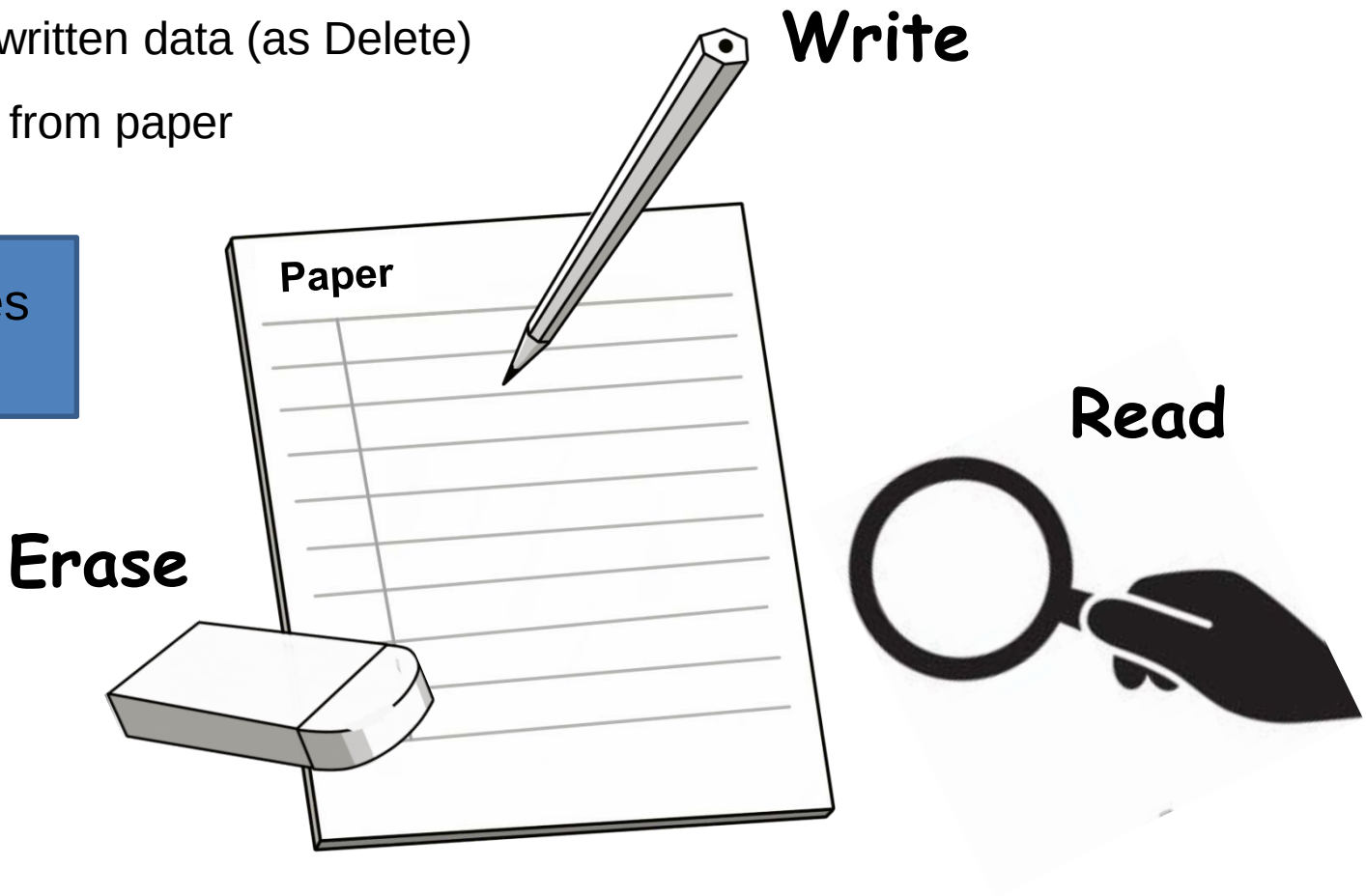


Flow !!

Example: Paper as Memory

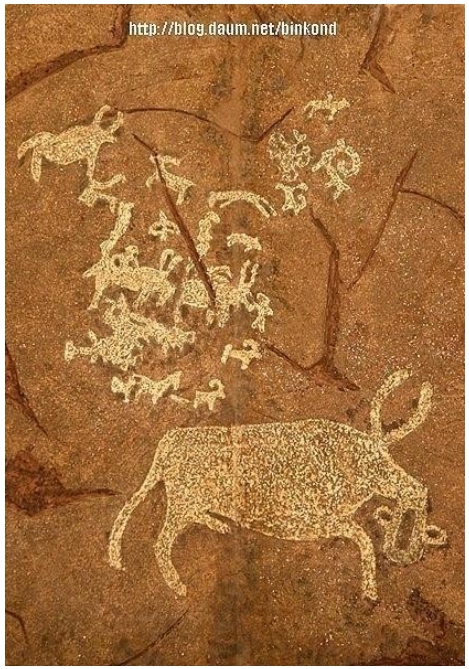
- **Very old and very popular memory**
  - Pencil writing (as Store)
  - Erase the written data (as Delete)
  - Read data from paper

No Overwrites
c.f.) DRAM



Long History of Memory

- **Since the beginning of humankind, memory has evolved continuously in various forms**
- **The 1st *"Non-Volatile Memory"* invented by Daewon Kahng in 1967 was based on the P-MOSFET and Al-gate Technology**

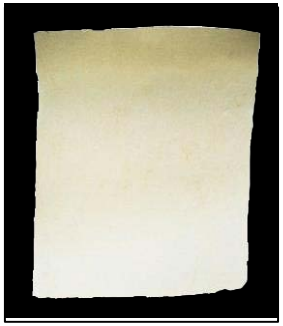


암각화 선사시대

木簡, 竹簡 (중국, 秦시대)

Magnetic (1980~)

Silicon (2002 ~)



종이 *(105*년,채윤, 後漢*)*

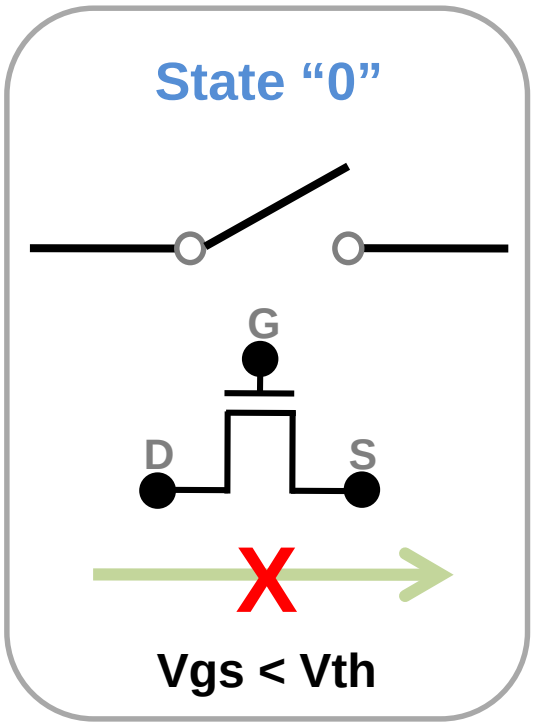
Optical Disk (1990~)

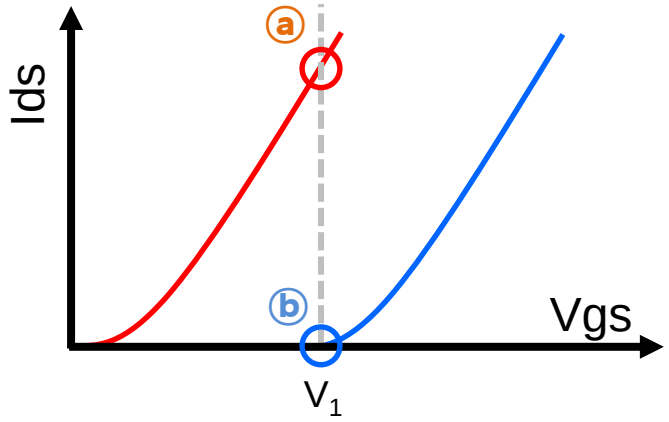
What is Electrical Memory?

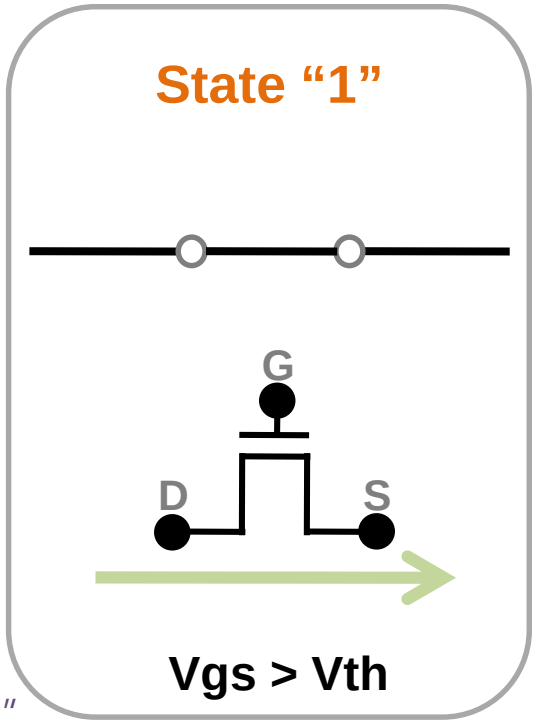
- **Store digital information by electrical operations**
  - Discrete states
    - Binary states : “0” or “1”
  - Electrically Write / Read / Erase
  - *Based on switch (i.e., transistor) on/off*

Transistor as an Electrical Switch

- Control gate voltage to turn on/off the switch.
  - Turn on → Current flow → State 1 (e.g., call it Erased)
  - Turn off → No current flow → State 0 (e.g., call it Programmed)







※ When V1 is applied to gate,

ⓐ: Vth is low → High current → State “1”

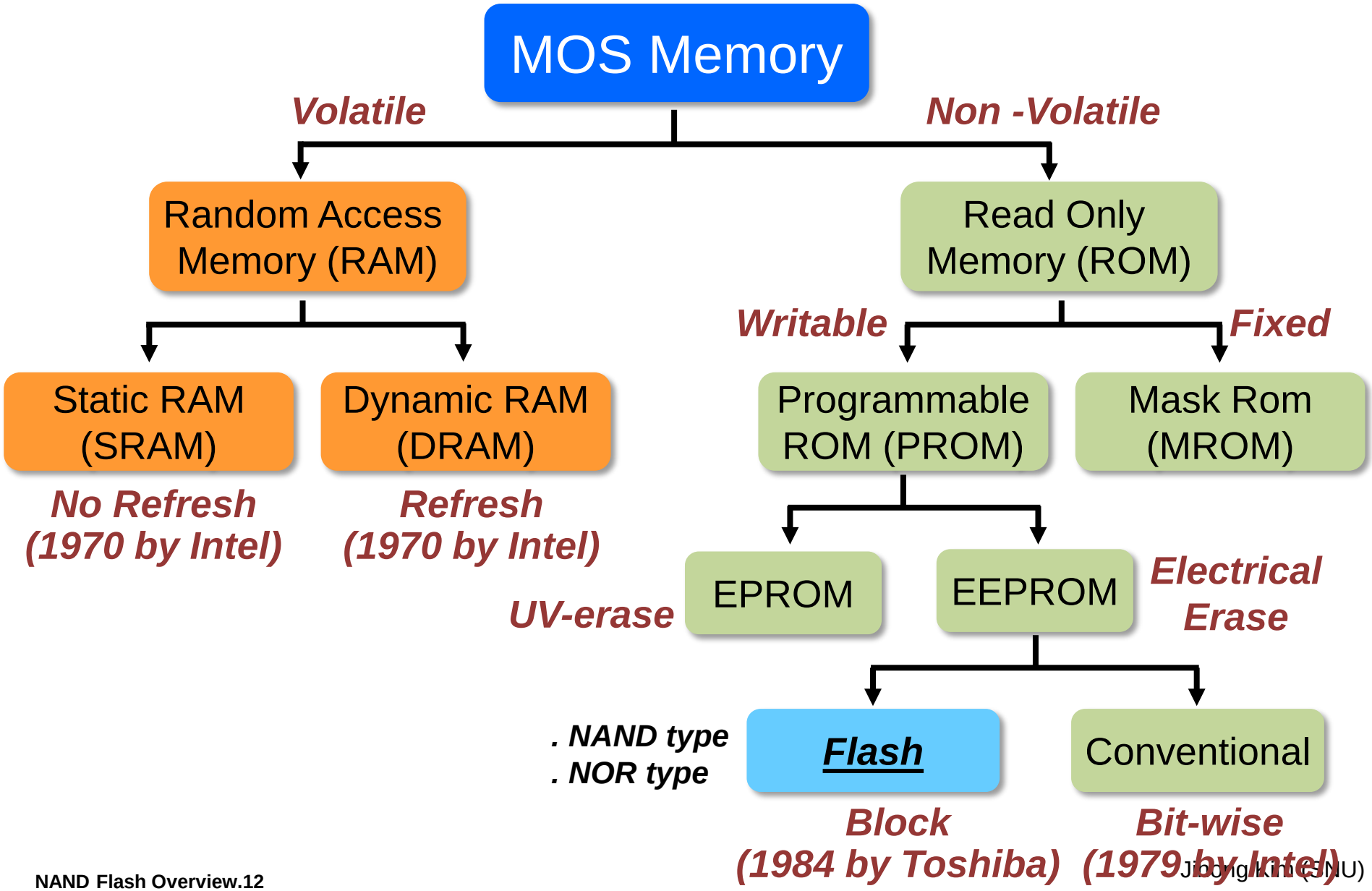
ⓑ: Vth is high → No current → State “0”

Q: Switch는 메모리는 아니나… 만약… 만약….

- **두 개의 상태를 구분은 하나 switch만으로는 새로운 데이터를 쓸 수가 없다.**

- **해결책은?**
  - 고정된 Vth 값에 대해 Vgs를 조정하니…. On/Off 구분이 가능…
  - 만약 Vth값을 변화시킬 수 있으면… 같은 Vgs에 대해서… On/Off 구분이 가능…
  - 만약 다른 상태가 다른 Vth값을 가지도록 할 수 있다면 ….

Semiconductor Memory Hierarchy (1)



Semiconductor Memory Hierarchy (2)

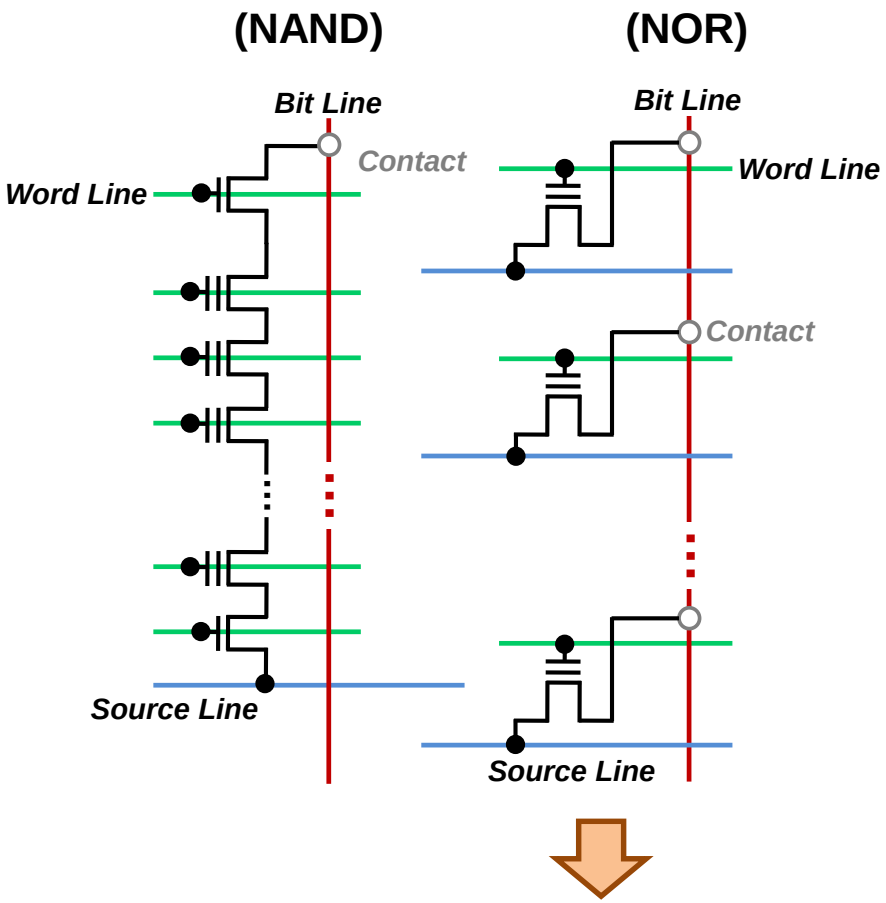
- **Volatile vs. Non-volatile**
  - Volatile : data is lost when the power is removed
  - Non-volatile : data is not lost even when the power is removed
- **Mask ROM vs. EPROM vs. EEPROM (E^2PROM)**
  - Mask ROM (Mask Programmable ROM)
    - Cell Vth is fixed at the process step → Data cannot be changed
  - EPROM (Erasable & Programmable ROM)
    - Erase is done in batch by UV, and byte program is done in off-system
  - EEPROM (Electrically Erasable & Programmable ROM)
    - Erase is done in byte electrically, and byte program is done in on-system
- **Flash (*Fast erase like camera flash*)**
  - Erase is done in batch electrically, and multi-byte program is done electrically

NAND flash vs. NOR flash (1)

- **NAND flash is the mainstream of the non-volatile memory market.**
  - Bit per cost issue

Comparison NAND vs. NOR

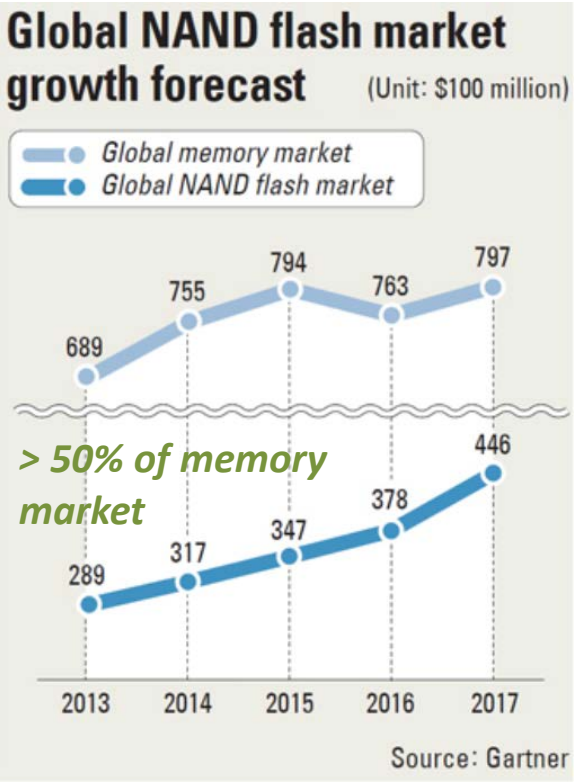
	NAND	NOR
Random Read	Slow	Fast
Program	Fast	Slow (Byte)
Erase	Fast	Slow
Life Span	10,000 ~	1,000 ~
Cost (Density)	Low (High)	High (Low)
Power	Low	High
Application	Data storage	Code storage
Example	MP3, Phone, SSD, Camera …	Phone, S/B …

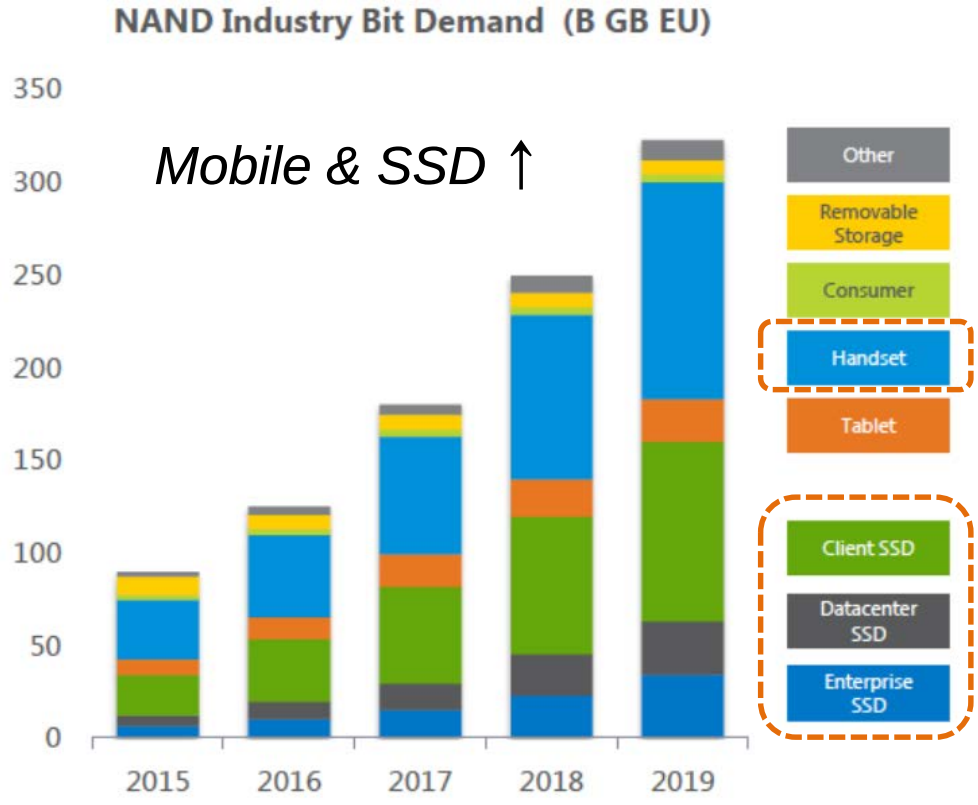


High area overhead because of contact in every cell : high cost

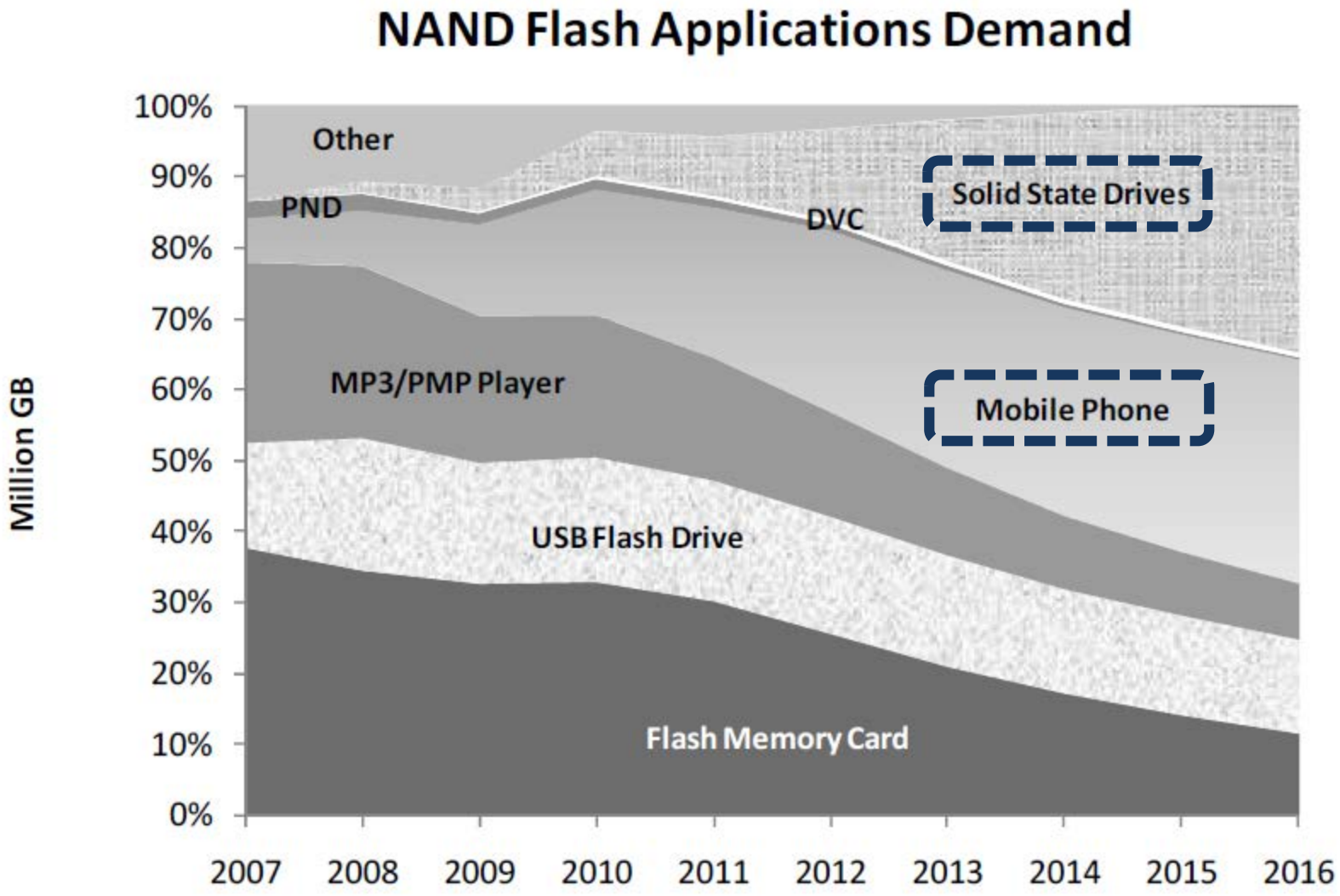
NAND Flash Market and Application

- **NAND flash market grows rapidly with explosive need for digital device (mass storage)**
  - Before 2010 : MP3, digital camera, USB, mobile phone …
  - After 2010 : SSD (Client & Enterprise), Automotive, Cloud, IoT …



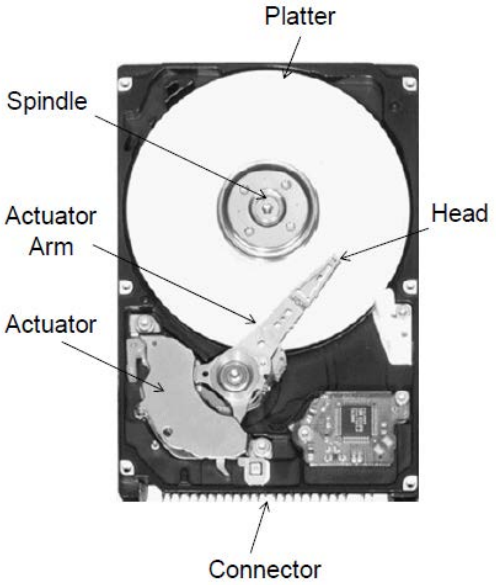


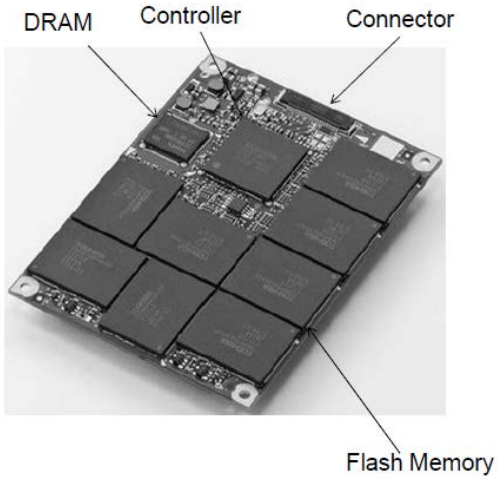
NAND Flash Market and Application



HDD vs. SSD (1)

- **SSD (Solid State Disk) is rapidly replacing with conventional magnetic disk such as HDDs in storage market**

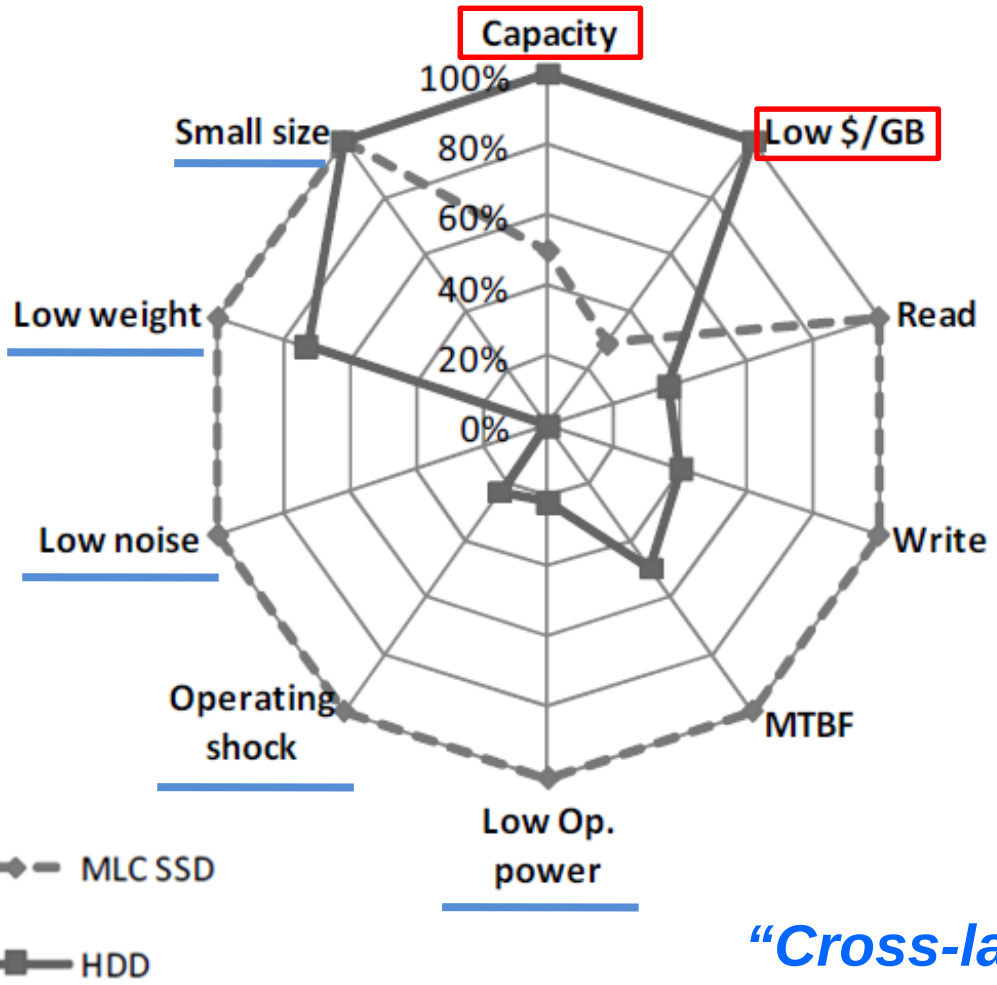




	HDD	SSD
Random access	Slow	Fast
Power	High (~4W)	Low (~1W)
Shock and Vibration	Poor	Good
MTBF	< 700,000 hour	> 2,000,000 hour
Weight	Heavier	Light
Cost	Low	***High***

HDD vs. SSD (2)

- **Capacity (= bit per cost) is drawbacks of SSDs compared with the conventional magnetic storage, HDDs**



To overcome these issues,

① **Process : Scaling down**
(more cells in the chips)

② **Circuit : Multi level cell**
(more bits in the cell)

"Trade-off relation with reliability & performance"

How to optimize ?

- Device improvement ??
- System S/W improvement ??

"Cross-layer optimization is needed"

HDD vs. SSD (3)

- **FTL (Flash Transition Layer) is introduced to solve drawbacks of SSD**
  - Mapping table
  - Wear-level , Garbage collection , Reclaim , Over-provisioning , Trim …

- ✓ Low power consumption
- ✓ Fast random access
- ✓ Shock resistance
- ✓ Small form factor

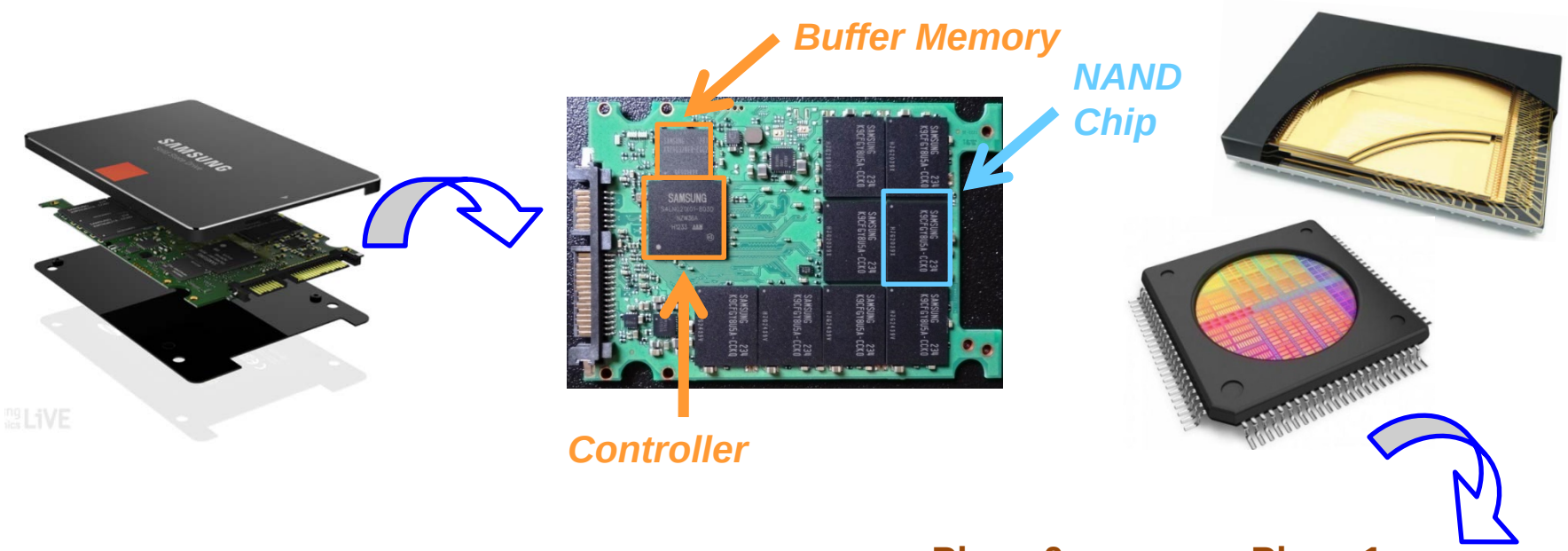
⋮

- ✓ ***Low density***

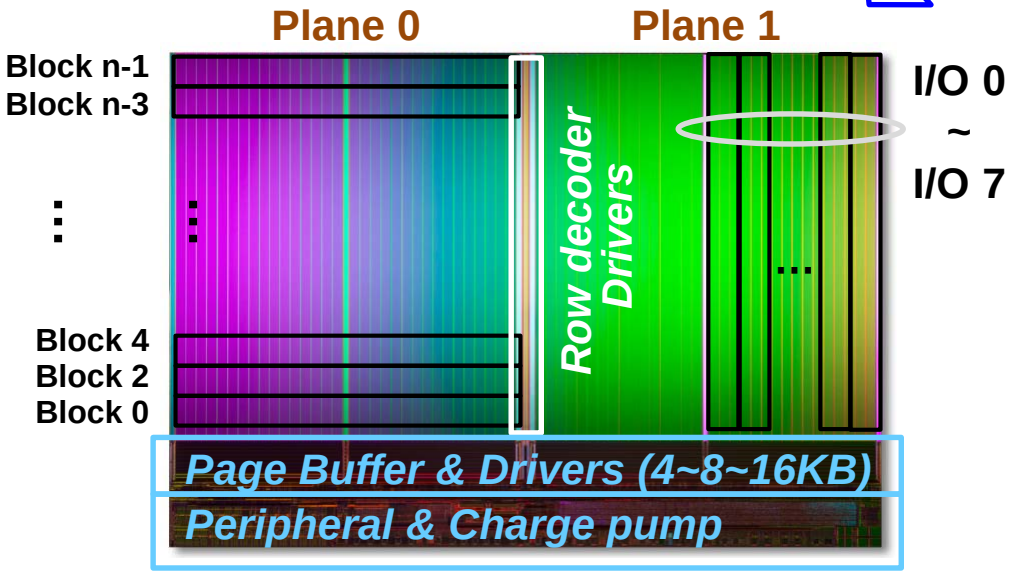
  (high bit per cost)
- ✓ Limited lifetime
- ✓ Out-of-place update

  (Erase before write)

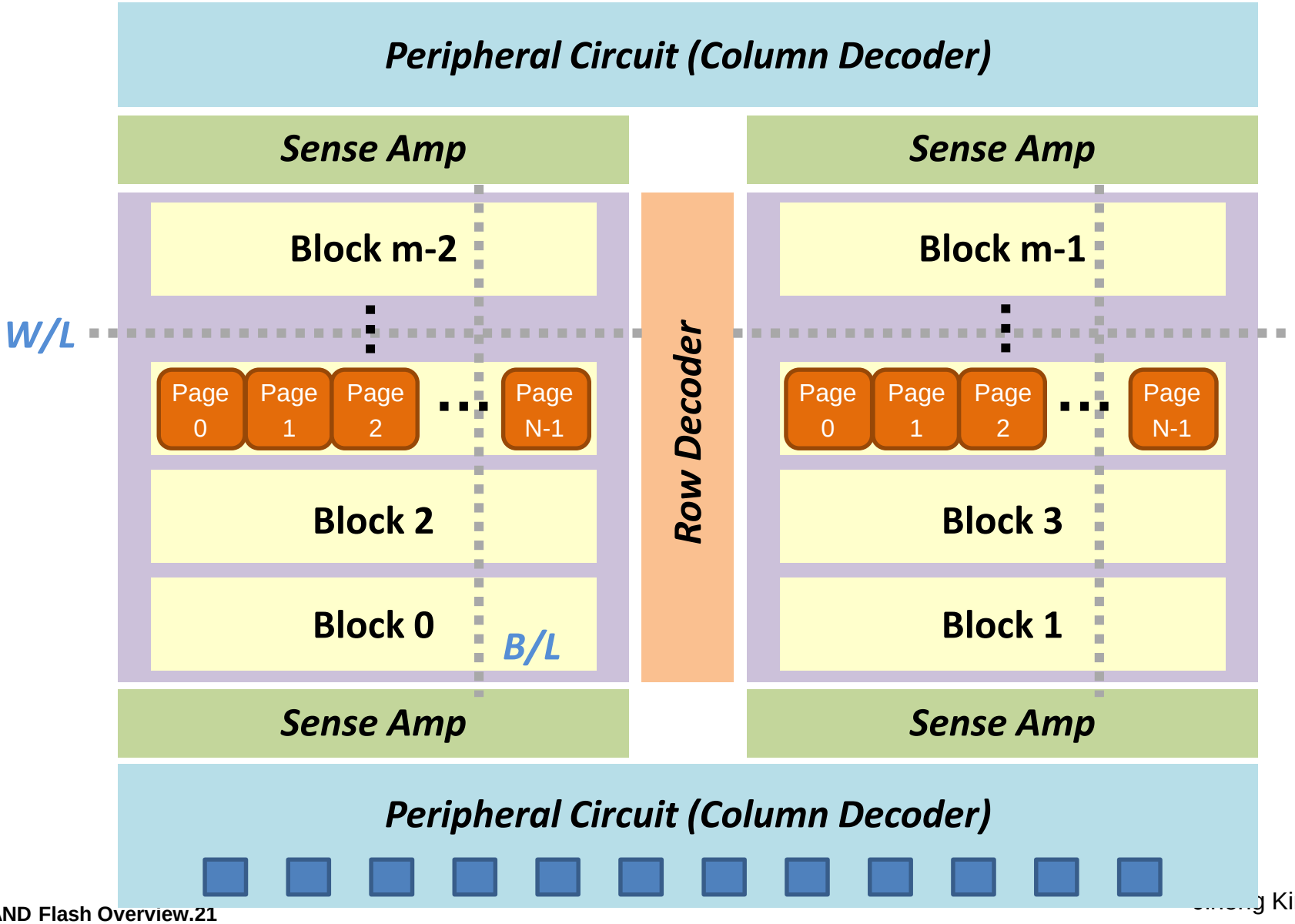
NAND Flash Architecture



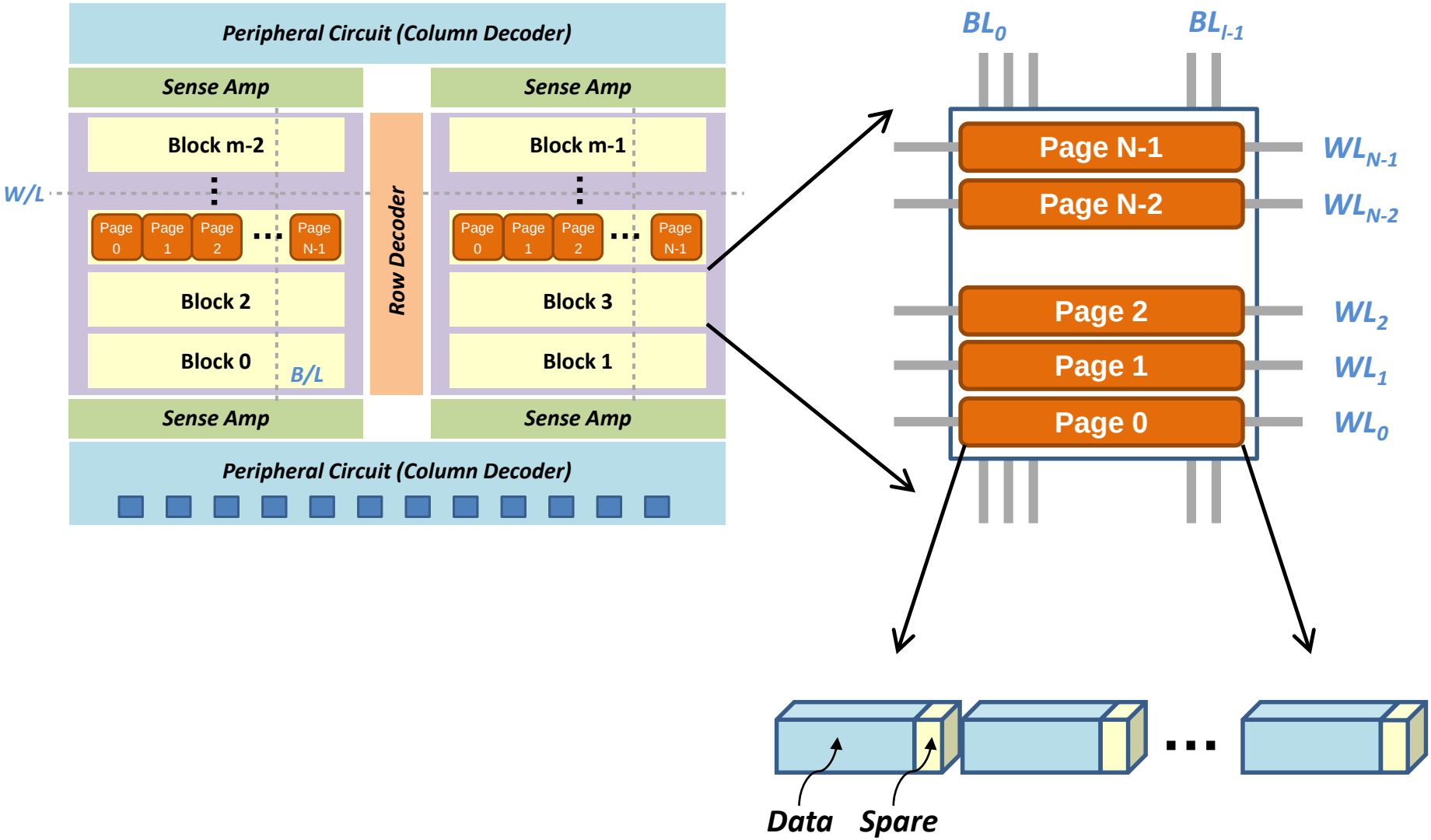
- ✓ Plane : unit of multi operation
- ✓ Planes consist of multiple blocks in the row direction
  (SLC : 64 pages / MLC : 128 pages)
- ✓ Planes consists of 8ea I/O group in the column direction



NAND Flash Architecture

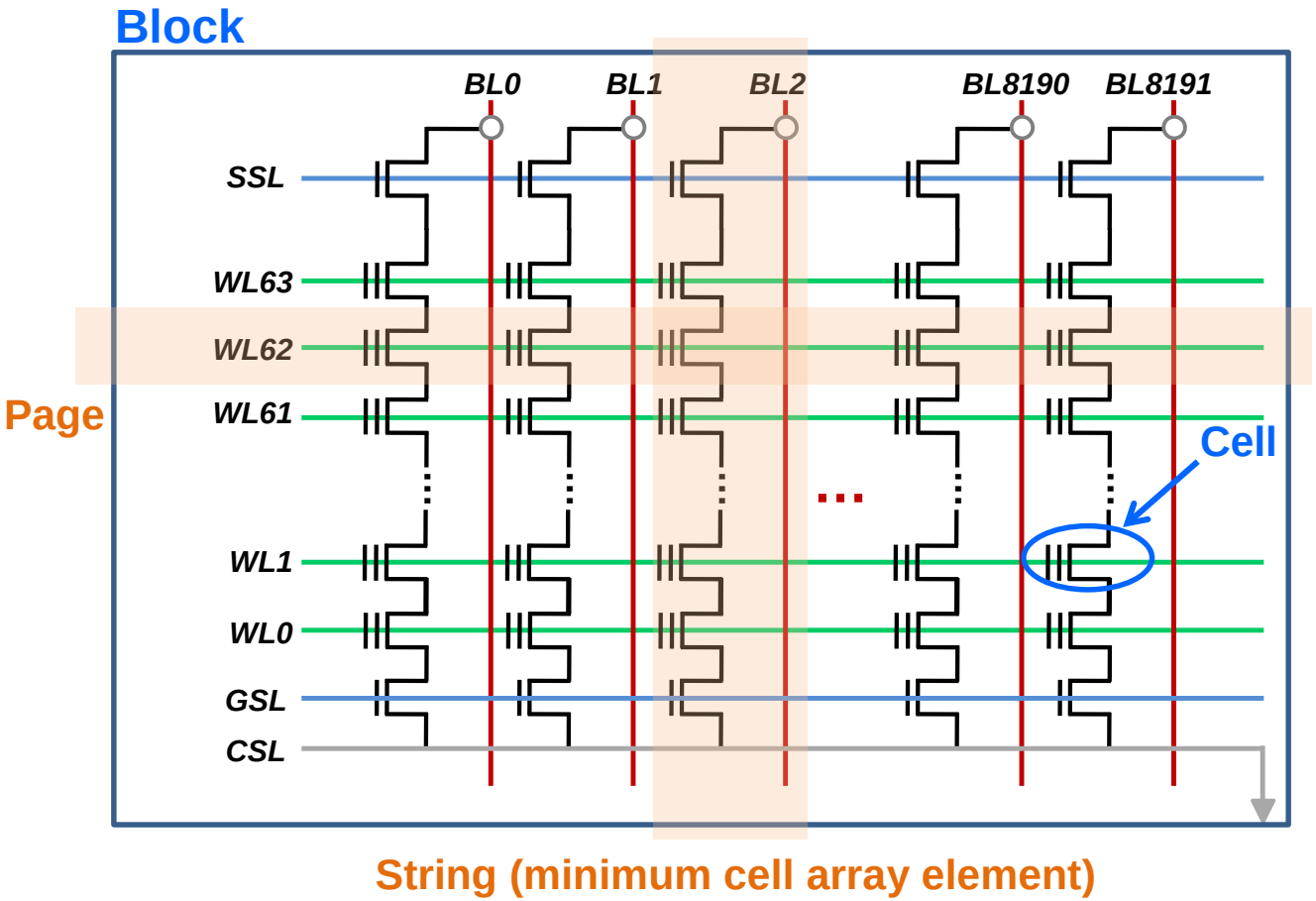


NAND Flash Architecture



NAND Flash Architecture

- **NAND flash is divided into blocks, and block consists of pages**
  - Block is basic unit of erase operation
  - Page is basic unit of program and read operation



(Example)

. SLC

. 64 WLs = 64 page

. 8K BLs

. 8ea I/O = 8KB = page size

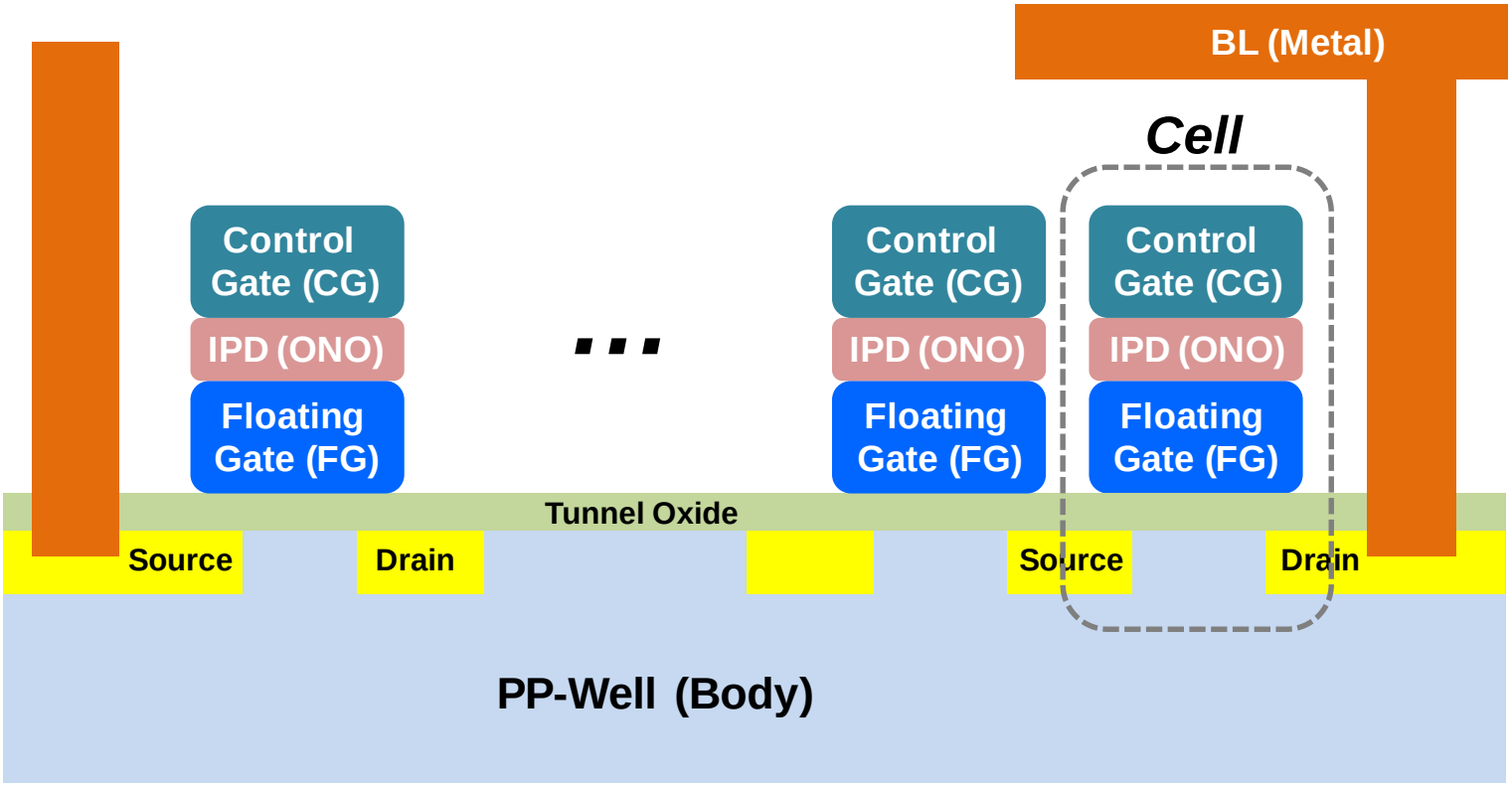
. 8192 blocks

Total density

= 64 (page) x 8192 (BL)
x 8192 (block) x 2 (MLC)
x 8 (I/O)
= 64Gbit (8GB) NAND

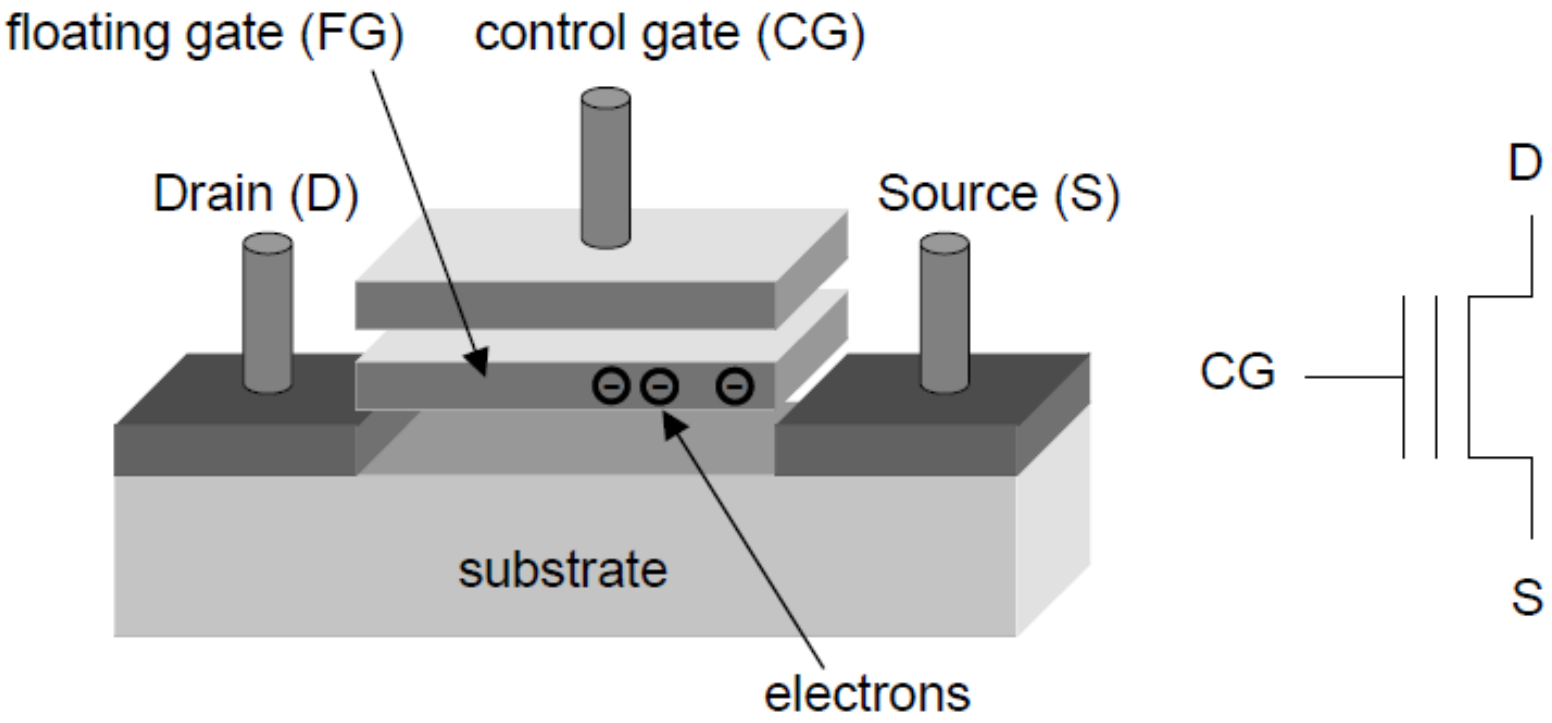
NAND Flash Architecture

- **Cell is the minimum storage unit of NAND flash**
  - Electrons can be injected (ejected) into (out of) the FG through tunnel oxide with electric field across tunnel oxide
  - Cell Vth changes depending on the amount of charge in floating gate (FG)



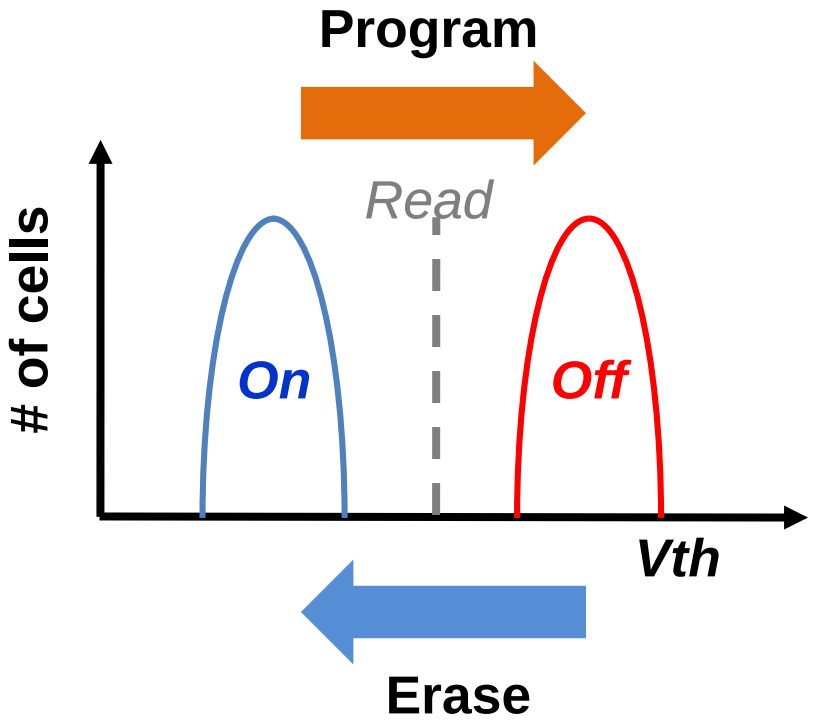
NAND Flash Architecture

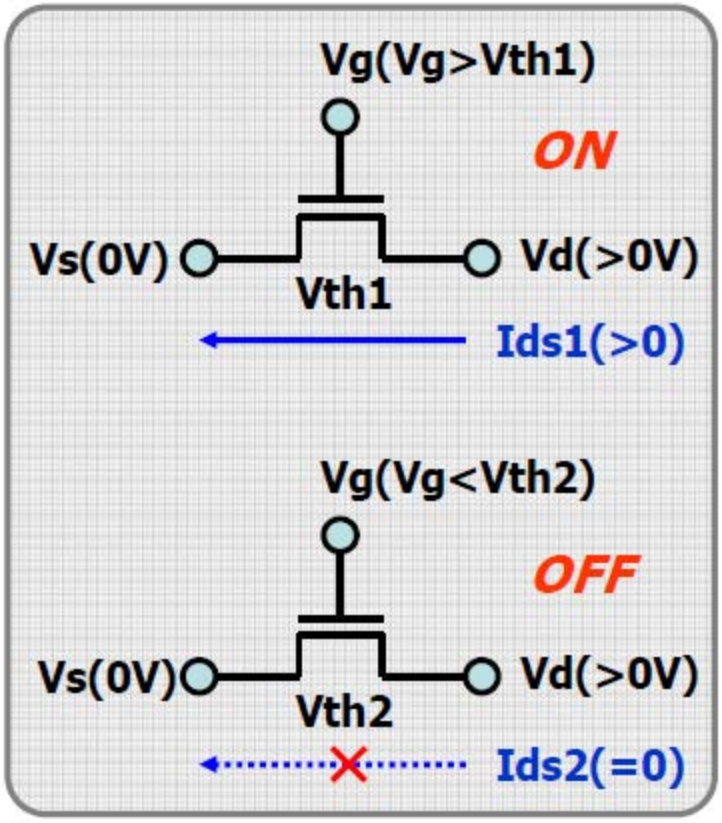
- **Floating gate memory cell and its schematic symbol**
  - Floating gate is isolated by IPD (Inter Poly Dielectric, ONO)
  - *Isolated FG can store the charge even when the power is off*
  - Floating gate architecture is major difference with normal MOSFET



NAND Operation – Overview

- **Write & Read binary data to a NAND flash cell**
  - Data “0” → Program → Shift cell Vth to high → Off state → No current flow
  - Data “1” → Erase → Shift cell Vth to low → On State → Current flow

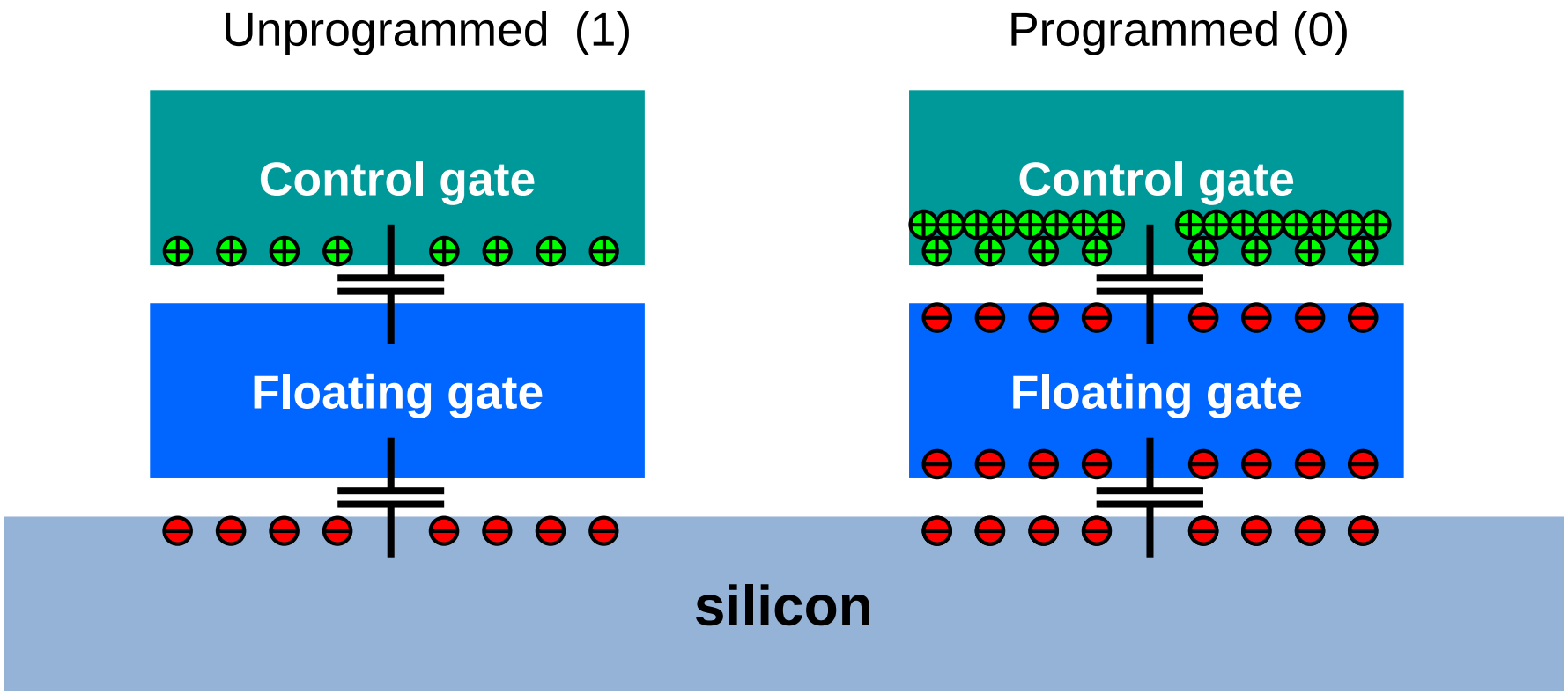




✓ *Read : Check the current flow*

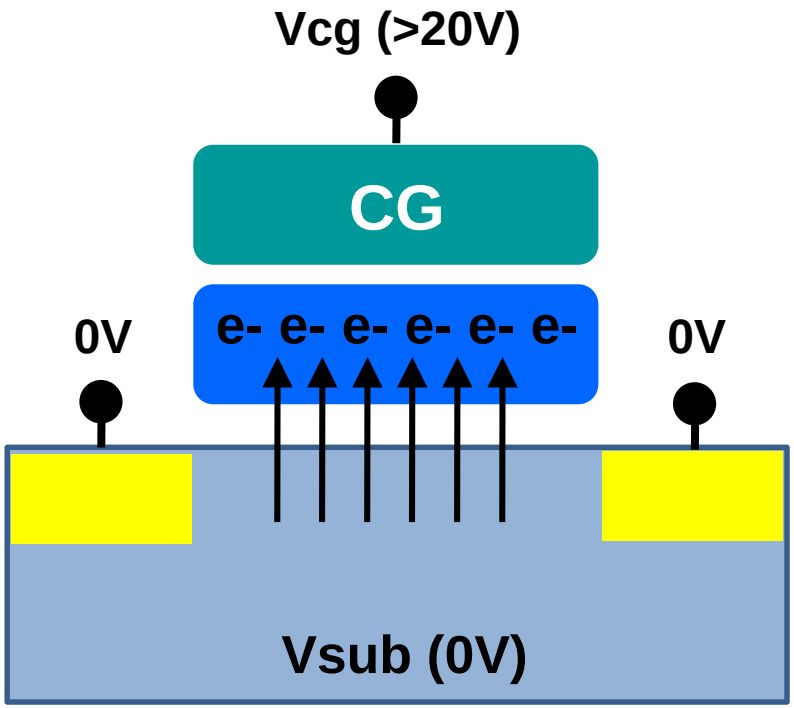
NAND Operation – Overview

- **To obtain the same channel charge, the programmed gate needs a higher control gate (CG) voltage than the unprogrammed gate**



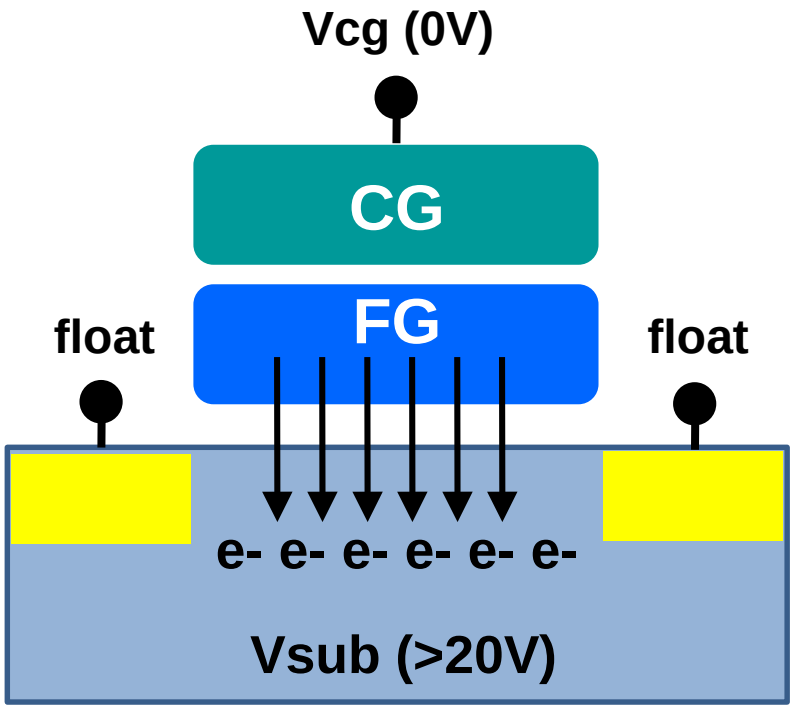
NAND Operation – Program

- **High voltage at control gate transfers electron from substrate to floating gate by F-N tunneling**



Program : FN tunneling

Off cell → Data “0”

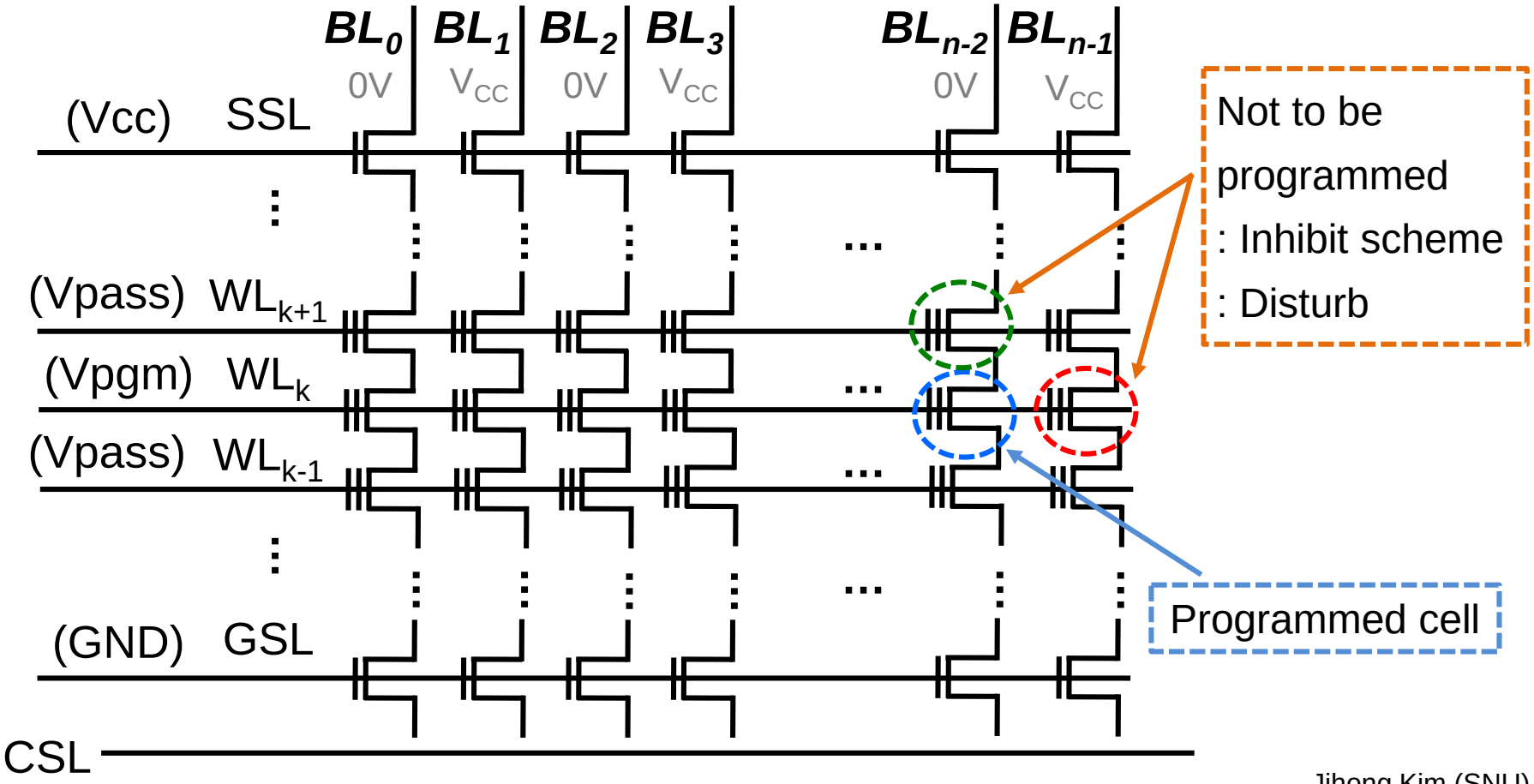


Erase : FN tunneling

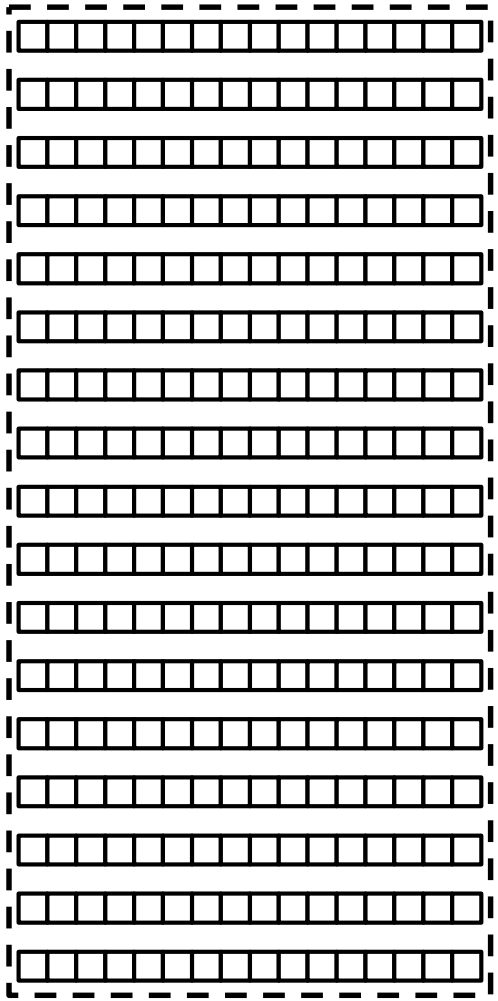
On cell → Data “1”

NAND Operation – Basic Bias Condition

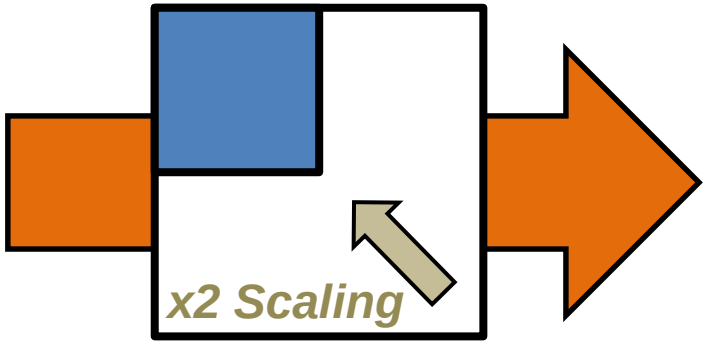
- **Selected WL : high program voltage (Vpgm) enough to FN tunneling**
- **Unselected WL : medium pass voltage (Vpass) not to FN tunneling**



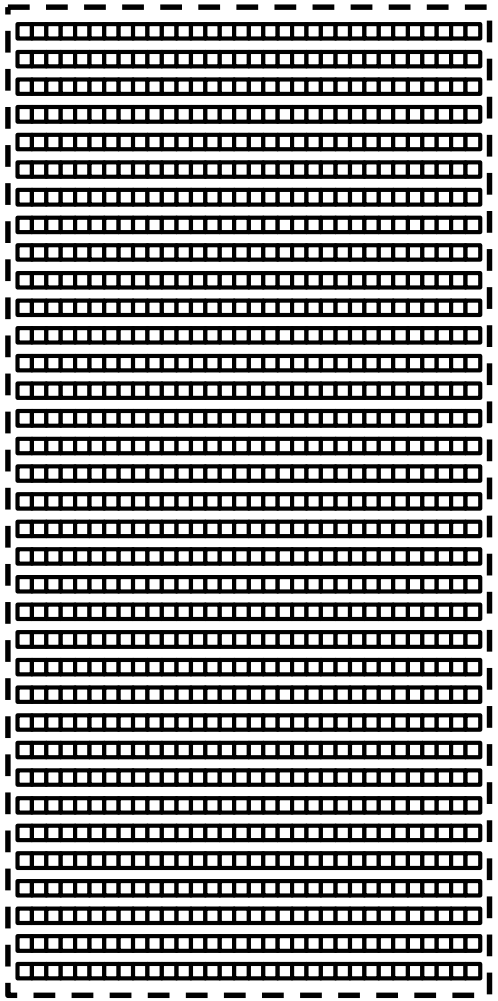
Increasing NAND Capacity: Scaling



NAND Block



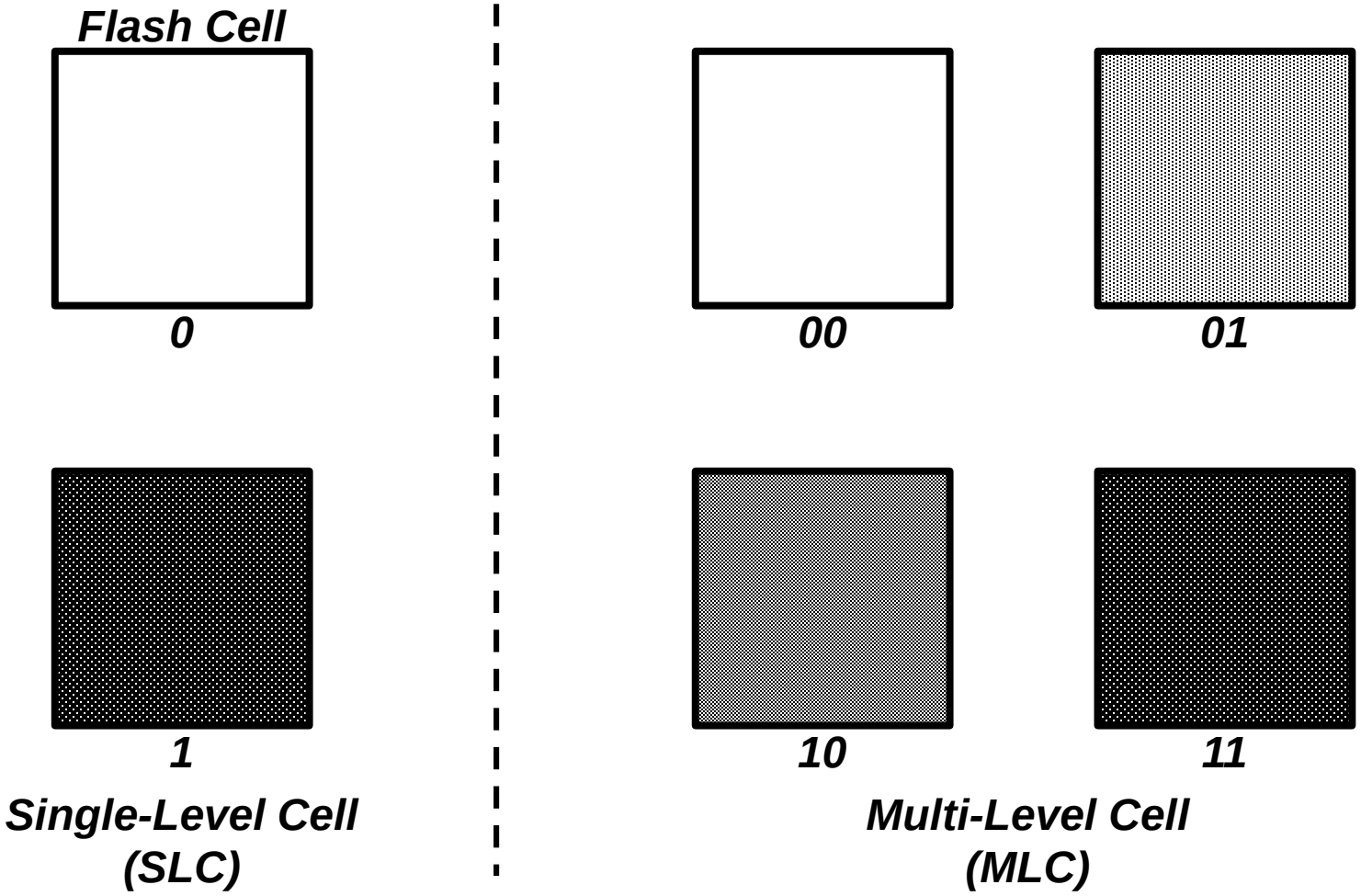
Flash Cell



Scale-Downed Block

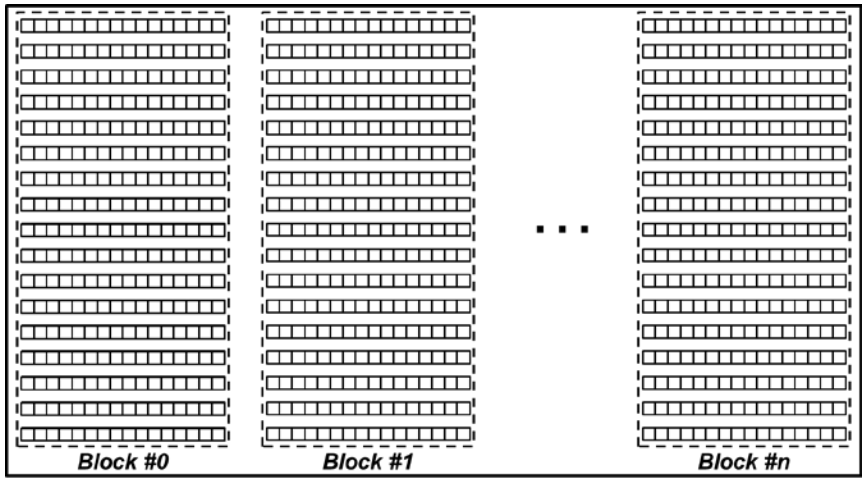
***x4* more cells in the same-sized block!**

Increasing NAND Capacity: Multi Leveling

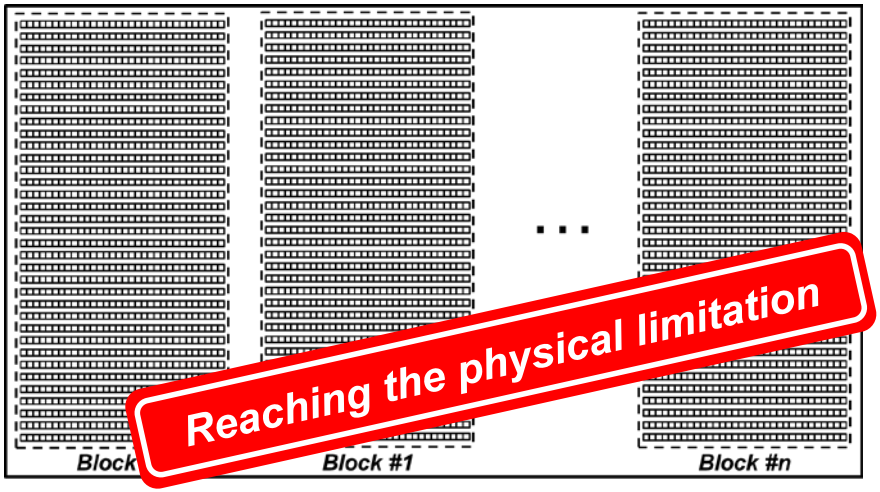


x2 more data in the same-sized cell!

3D NAND Flash Memory

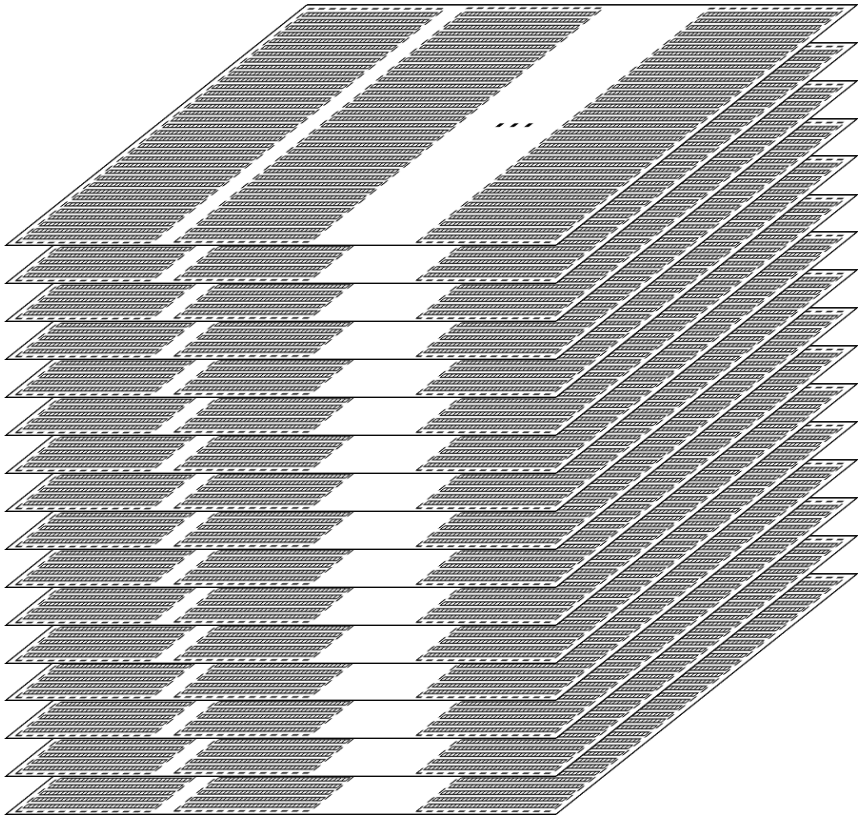


Shrinking processes, multi-leveling



<Scaling down in the planar NAND>

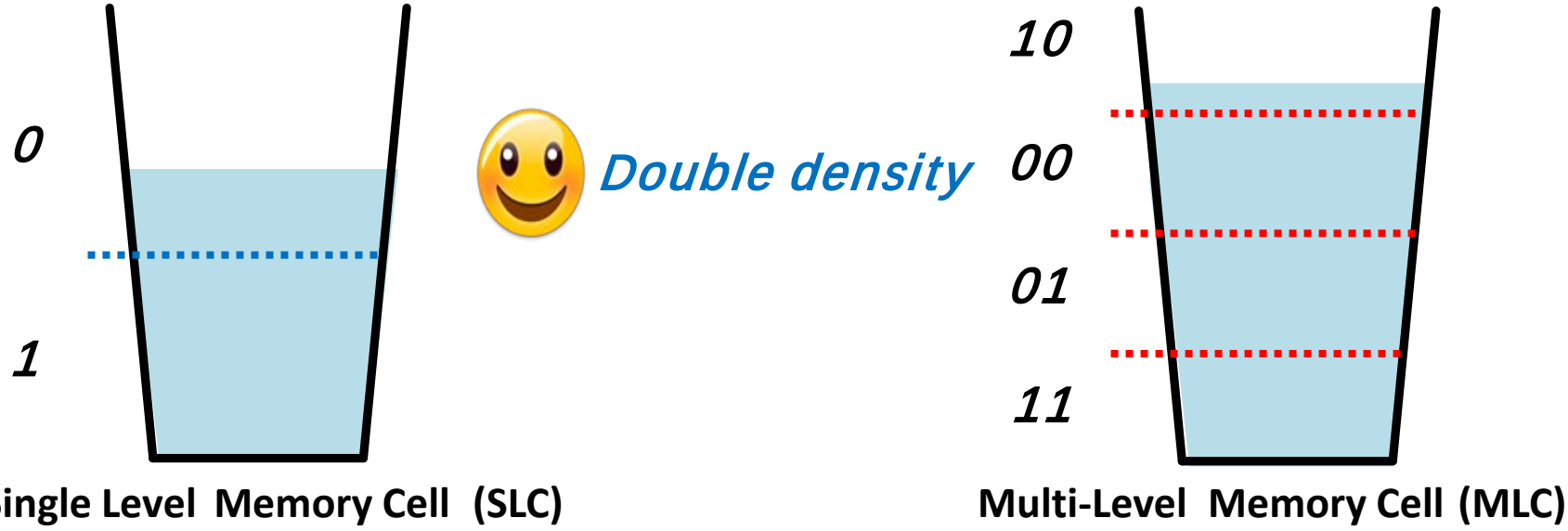
x16 more cells in the same area



<3D NAND flash memory>

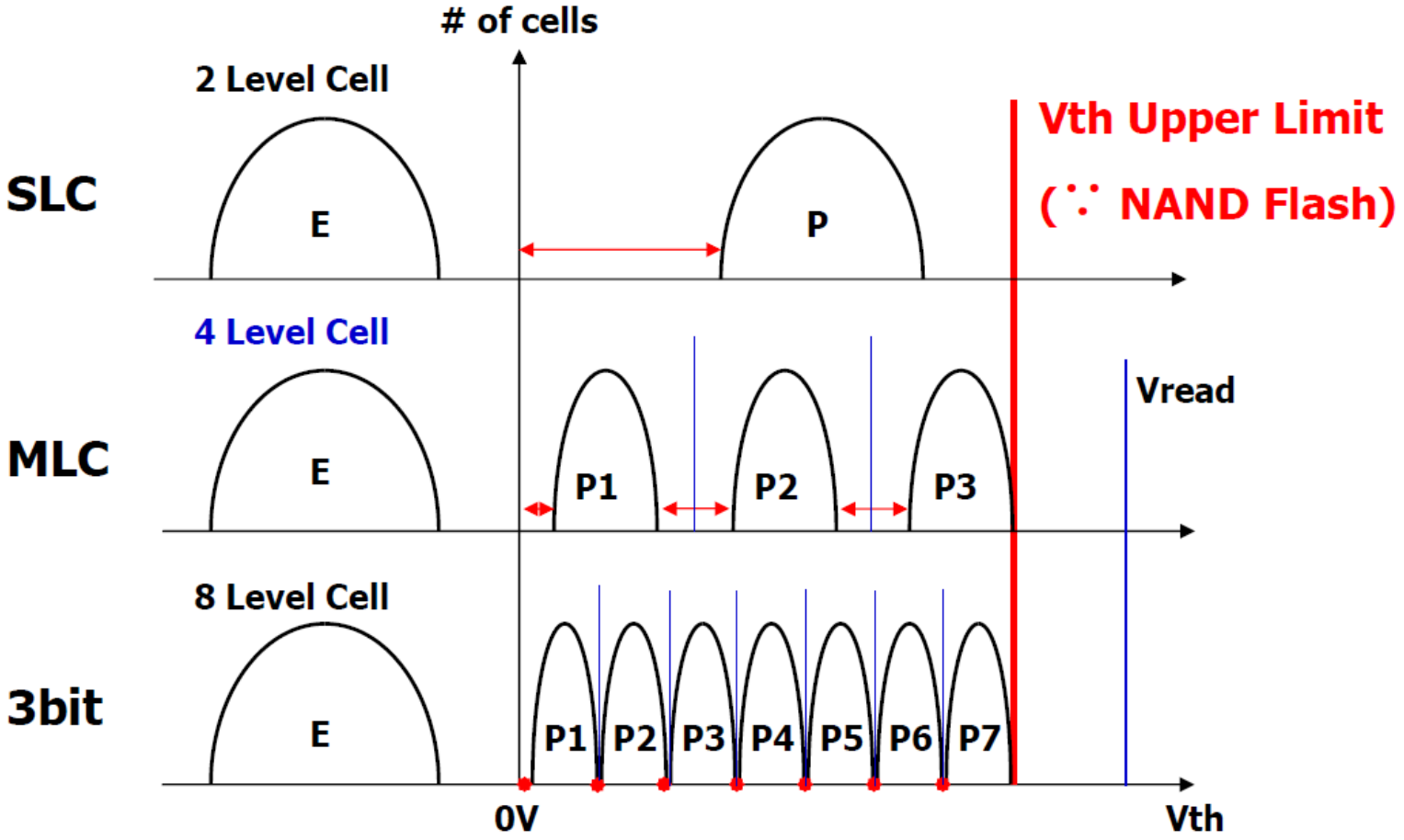
NAND Operation – SLC vs. MLC (1)

- **Good for high capacity**
- **Bad for performance and reliability**

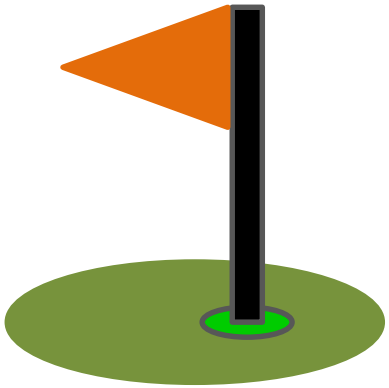


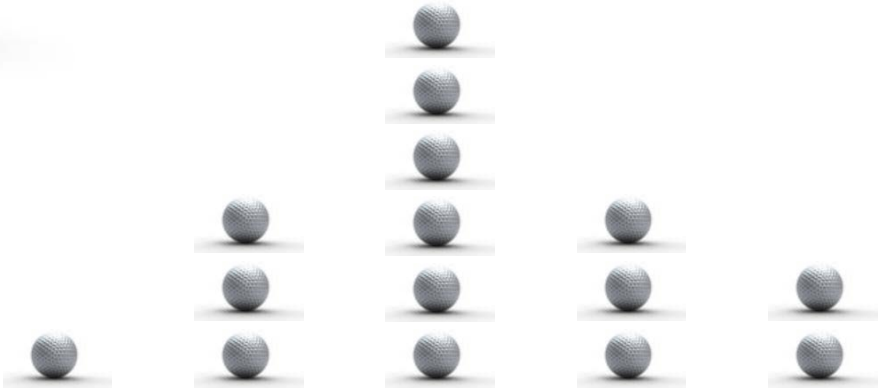
NAND Operation – SLC vs. MLC (2)

- **In order to reduce the bit per cost (or acquire the high capacity), multi-level cell technology is introduced**



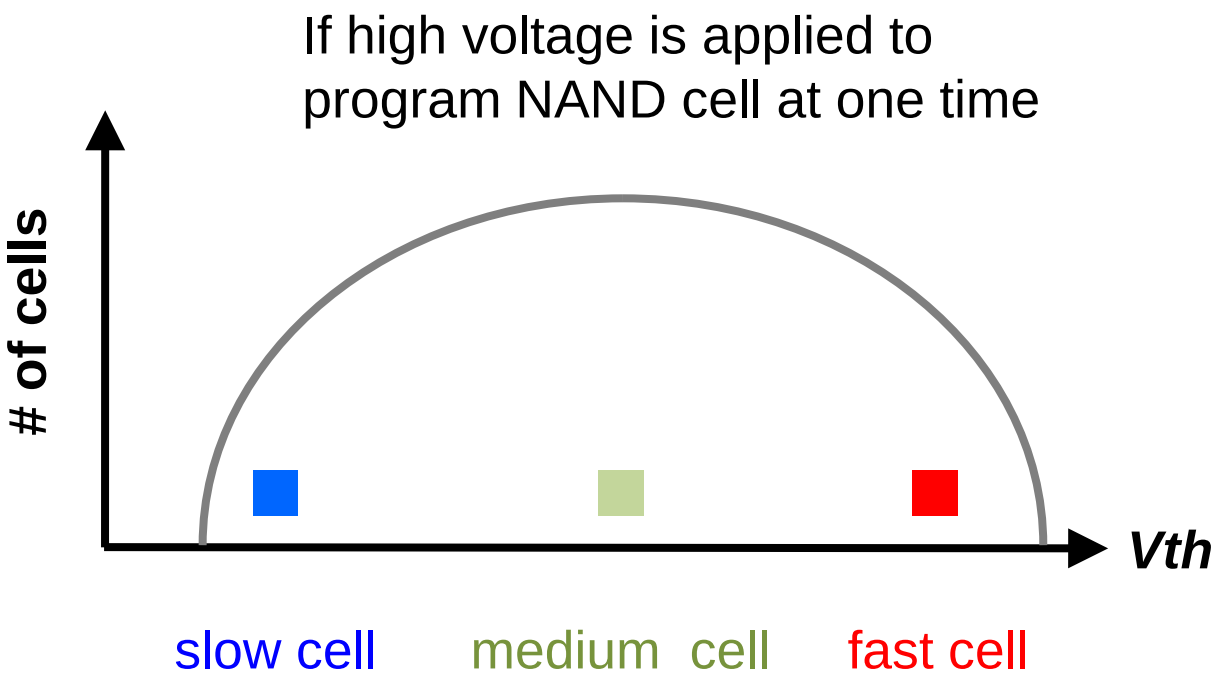
ISPP ?





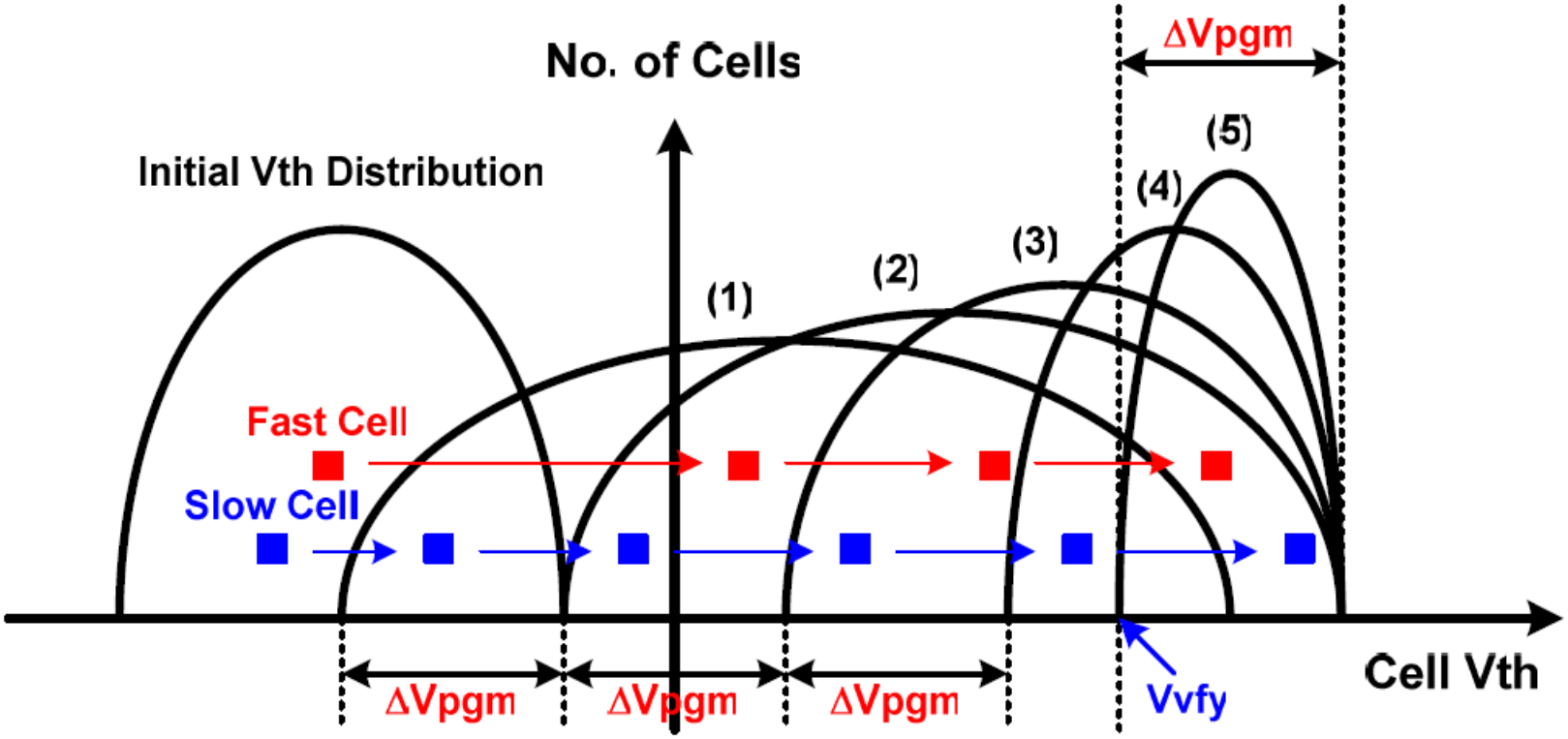
NAND Operation – ISPP (1)

- **The difference in cell speed due to the process variation makes difficult to control the cell Vth distribution**



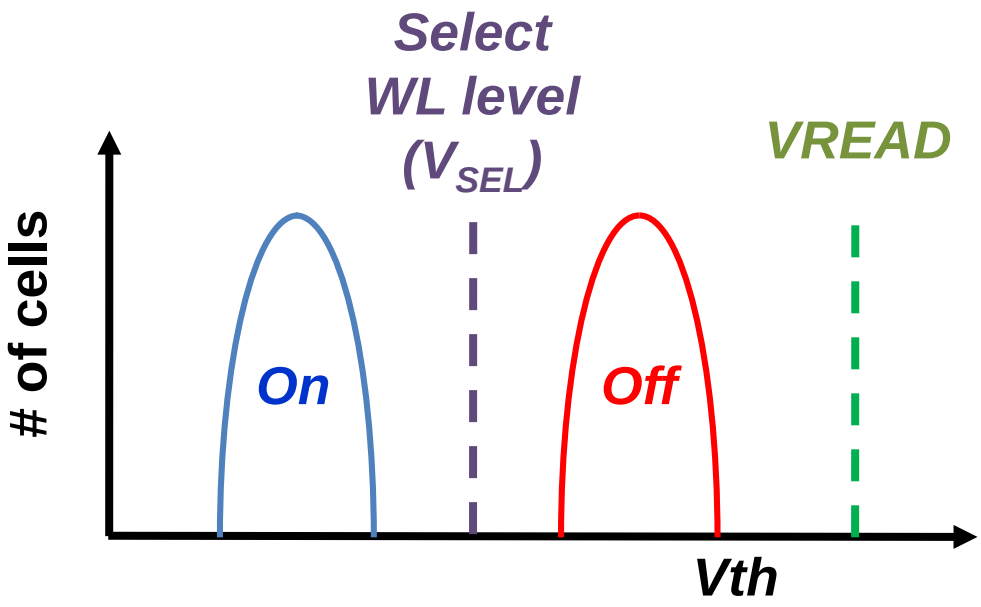
NAND Operation – ISPP (2)

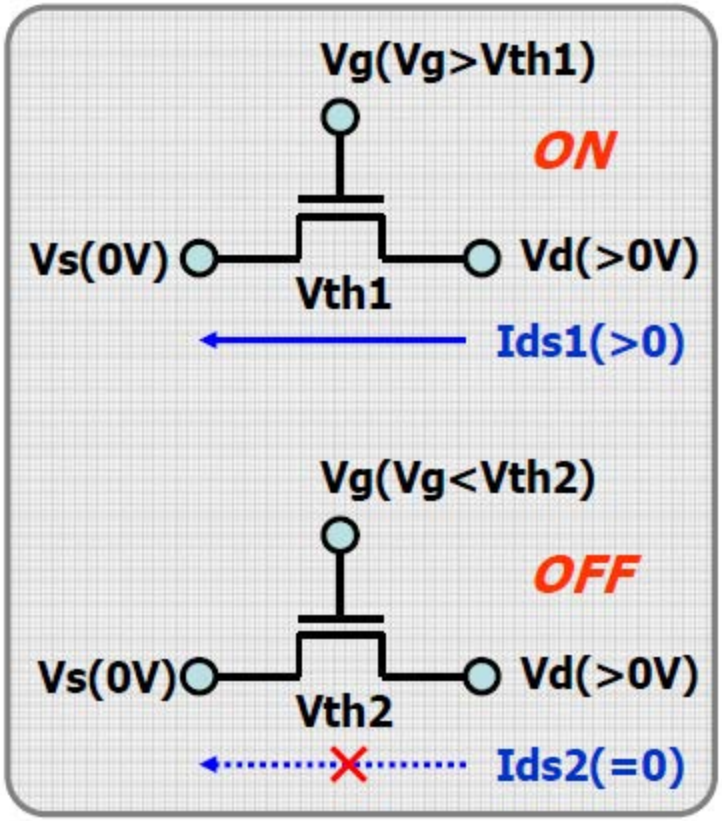
- **How to control the cell Vth : Incremental Step Program Pulse**
  - Cell Vth width control using repeated program operation
  - The smaller ISPP, the smaller cell Vth width (the lower BER)
  - The smaller ISPP, the larger program loop (the larger program latency)



NAND Operation – Read

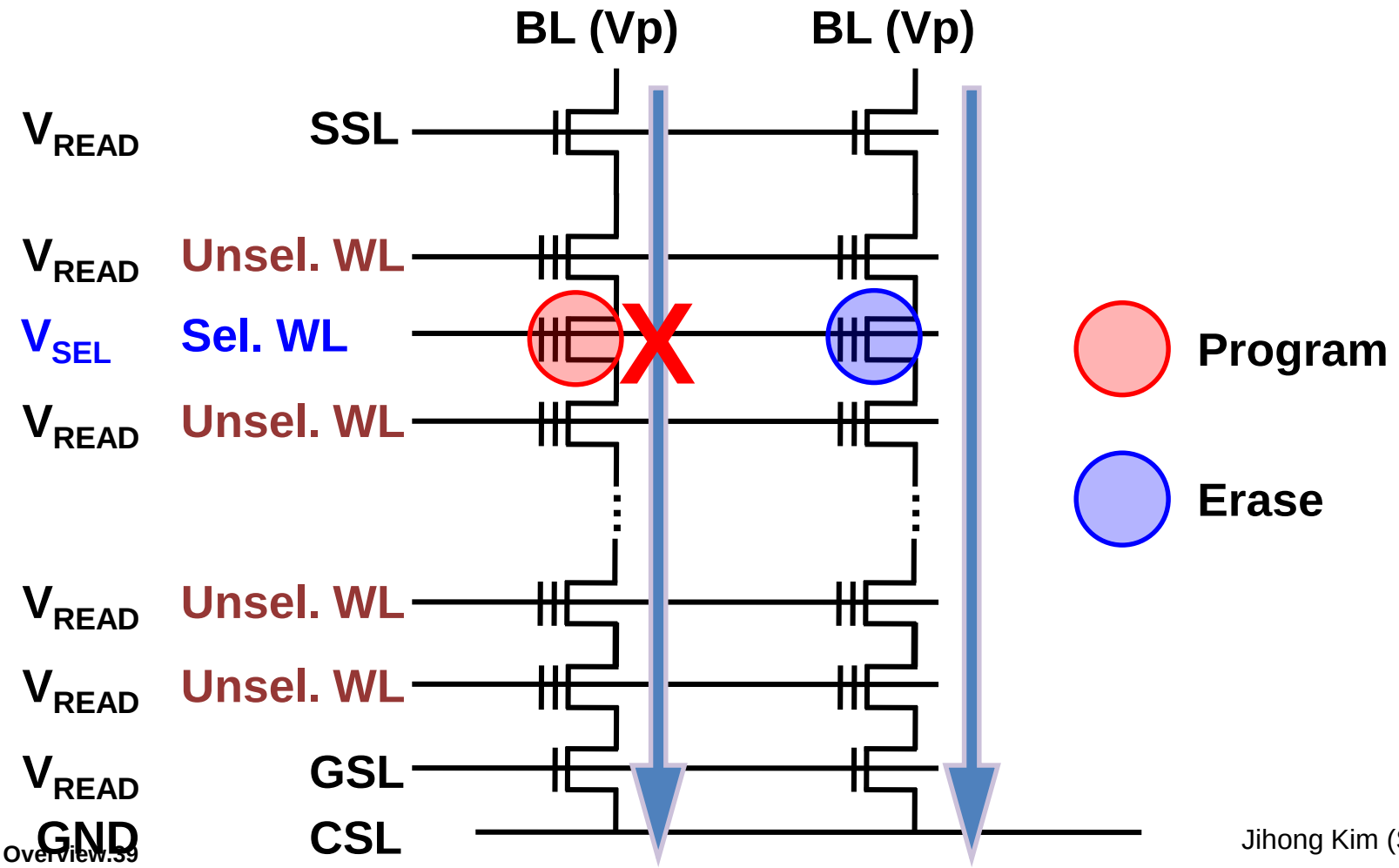
- **Check the current flow of the string**
  - V_{SEL} > cell Vth → Cell transistor is turn-on → Current flow → Cell data is “1”
  - V_{SEL} < cell Vth → Cell transistor is turn-off → No current flow → Cell data is “0”





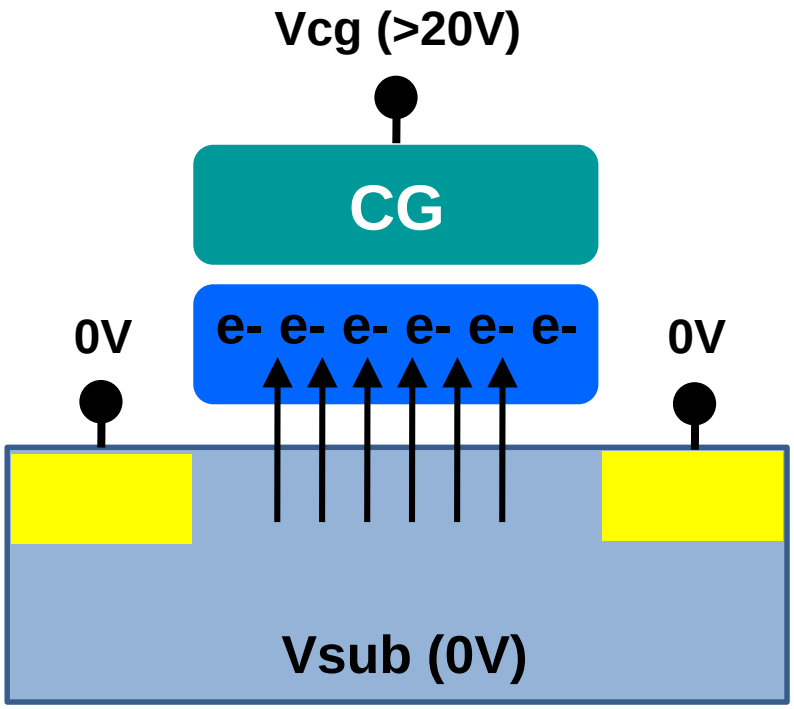
NAND Operation – Bias Condition

- **Select WL : target voltage**
- **Unselect WL : high enough to turn on the unselect cell in a string**



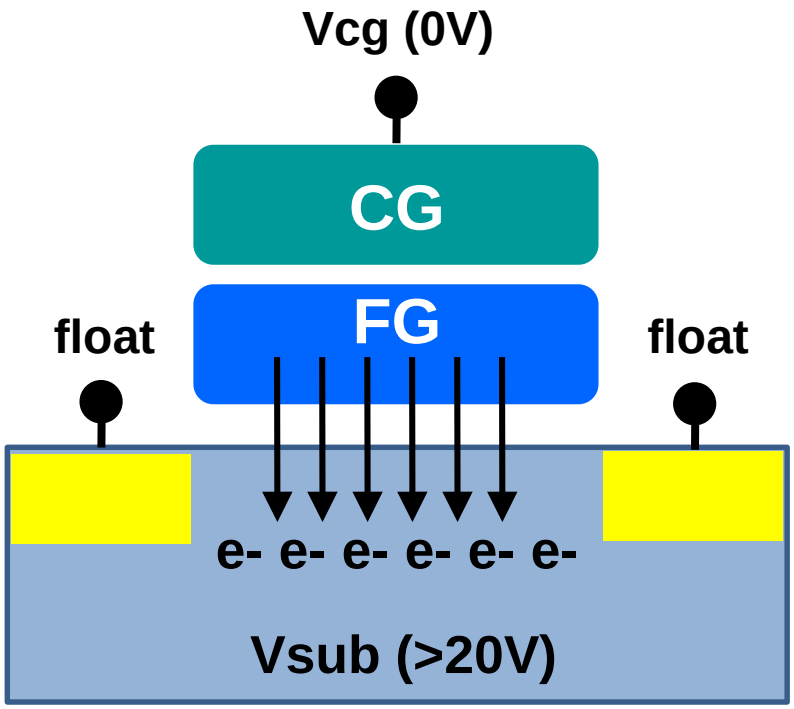
NAND Operation – Erase

- **High voltage at substrate transfers electron from FG to substrate by F-N tunneling**



Program : FN tunneling

Off cell → Data “0”

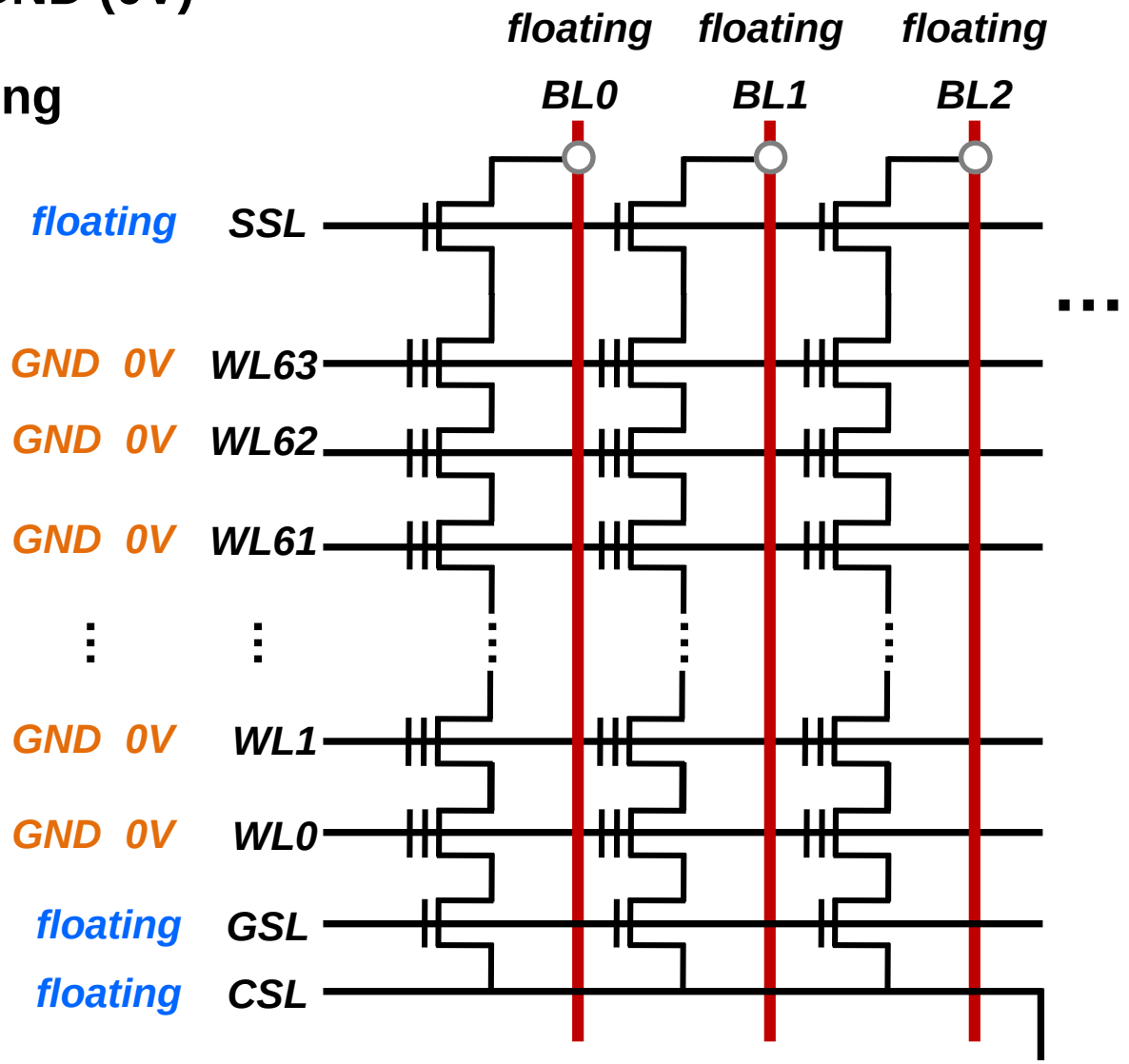


Erase : FN tunneling

On cell → Data “1”

NAND Operation – Bias Condition

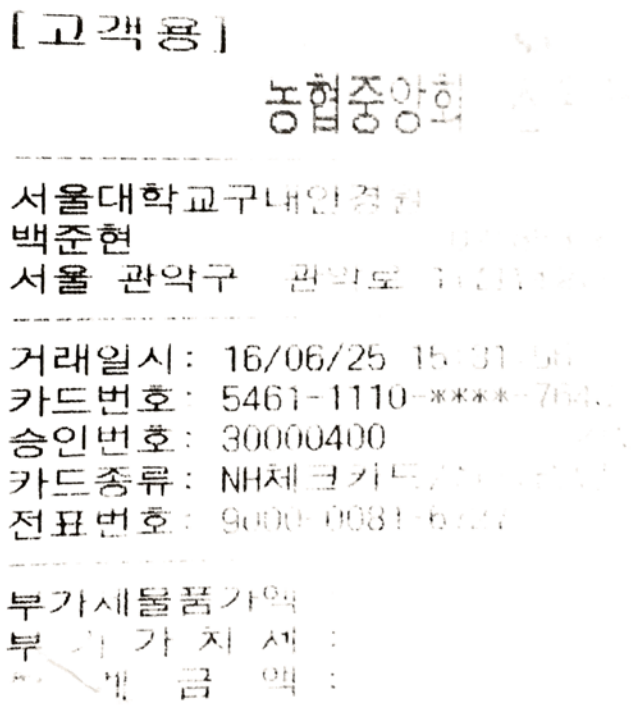
- All cells in a string : GND (0V)
- GSL / SSL / BL : floating
- Bulk : Erase voltage



Key Reliability Issues in Flash Memory

- Flash memory must maintain the integrity of the stored data. The key concerns are:
  - Data Retention
  - NAND Endurance
  - Read Disturbs

Data Retention


[고객용]

농협중앙회

서울대학교구내안경점
백준현
서울 관악구

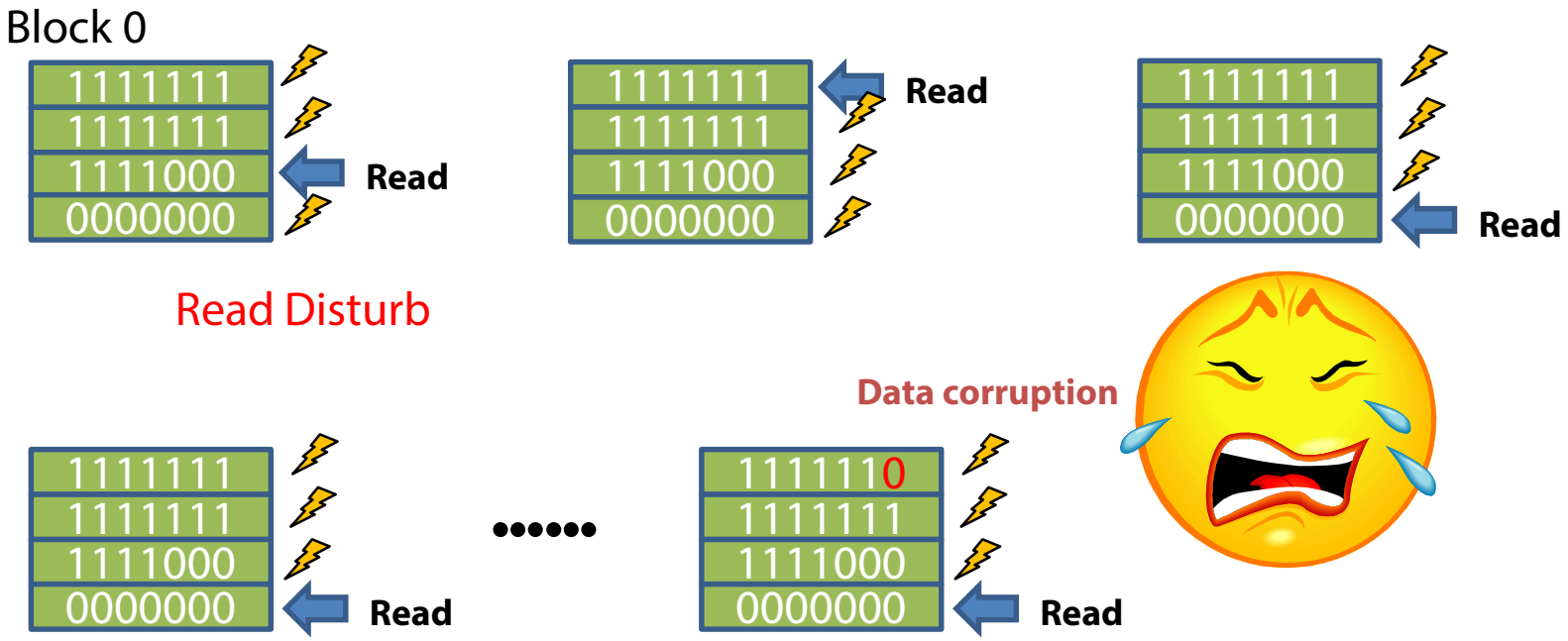
거래일시: 16/06/25
카드번호: 5461-1110-****-
승인번호: 30000400
카드종류: NH체크카드
전표번호:

부가세물품가액
부 가 가 치 세 :
[illegible] 금 액 :

1 Year at 30 ˚C?

Read Disturb Problem

- Read disturb occurs when a page is read in a block



The maximum read count between successive erasures is limited.

NAND Flash Reliability

Endurance

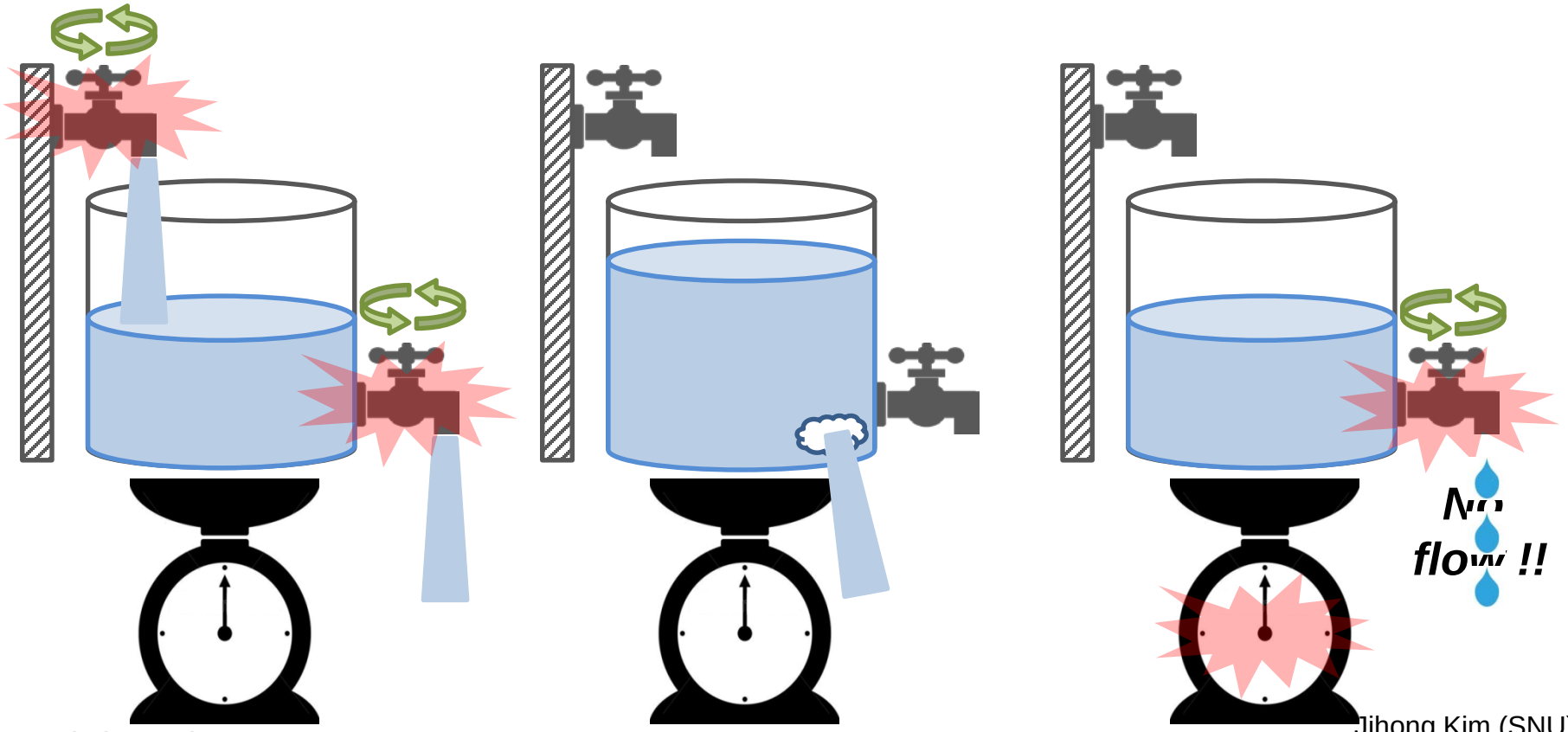
A limited number of program/erase operations

Retention

Data loss by leakage

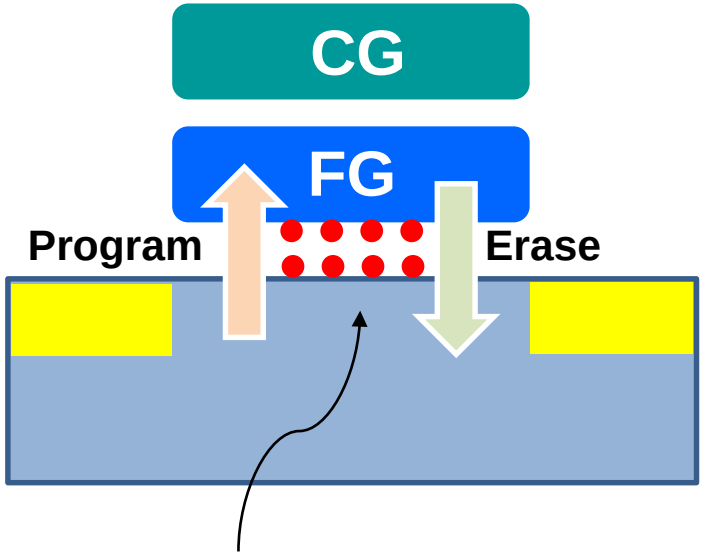
Read Disturb

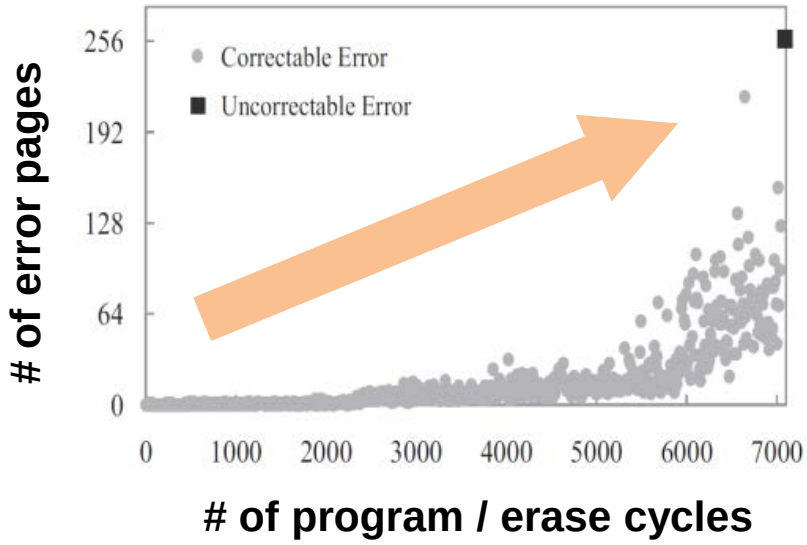
A limited number of read operations



NAND Flash Reliability – Endurance

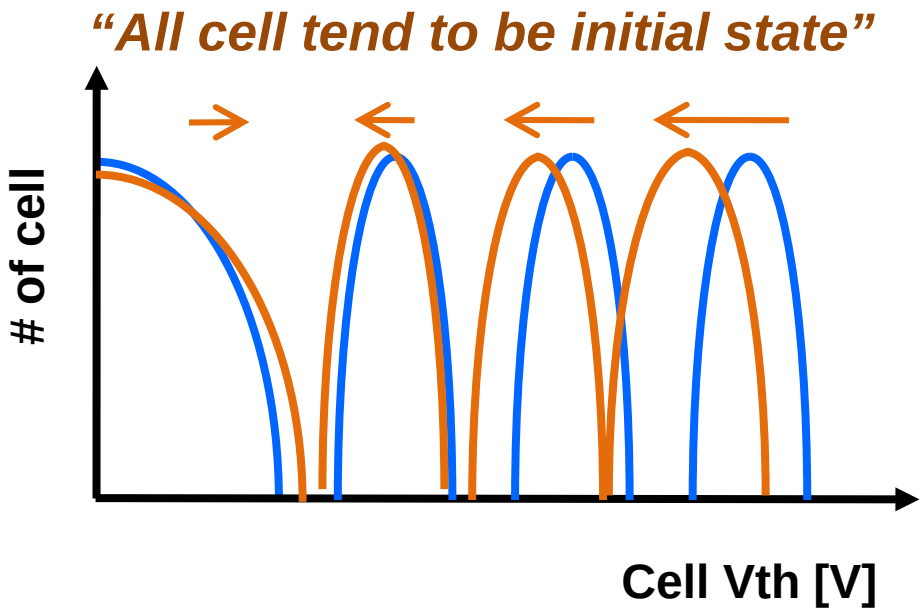
- **Repeated program & erase operations wear-out NAND flash because of tunnel oxide degradation**
  - High voltage in program & erase operation give a damage to tunnel oxide, and then increase interface and oxide trap density
  - The larger number of P/E cycles, the higher BER (Bit error rate)
  - Tunnel oxide damage accelerates the reliability degradation, for example retention error and read disturb error

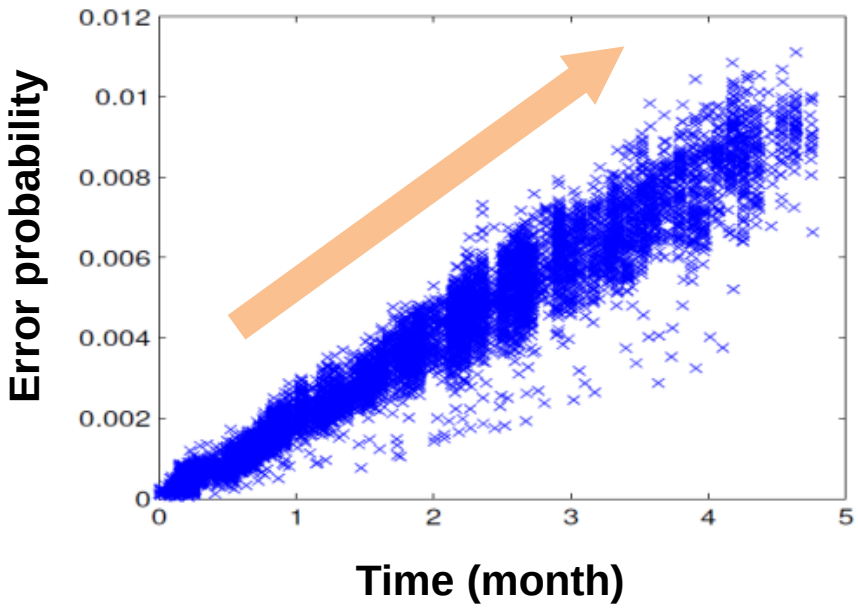




NAND Flash Reliability – Retention

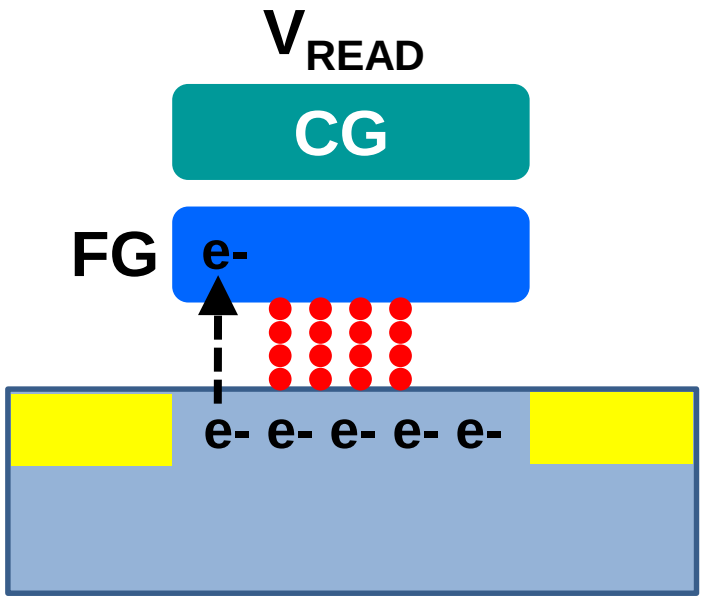
- **The retention concept is the ability of a memory to keep a stored information over time with no biases applied**
  - Thermal stress (= high ambient temperature) leads to charge loss which means cell Vth shift to lower state
  - Charge loss causes an increase in BER, eventually read failures
  - The higher cell Vth, the larger charge loss

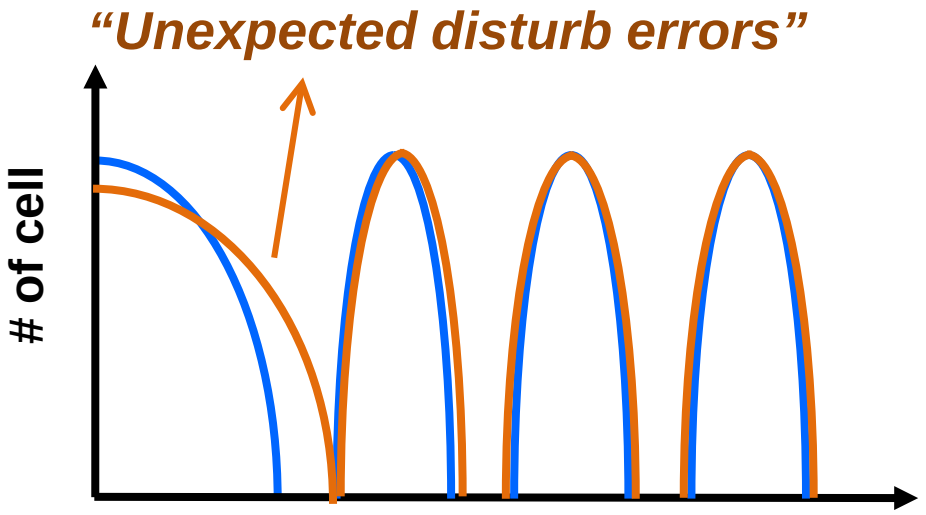




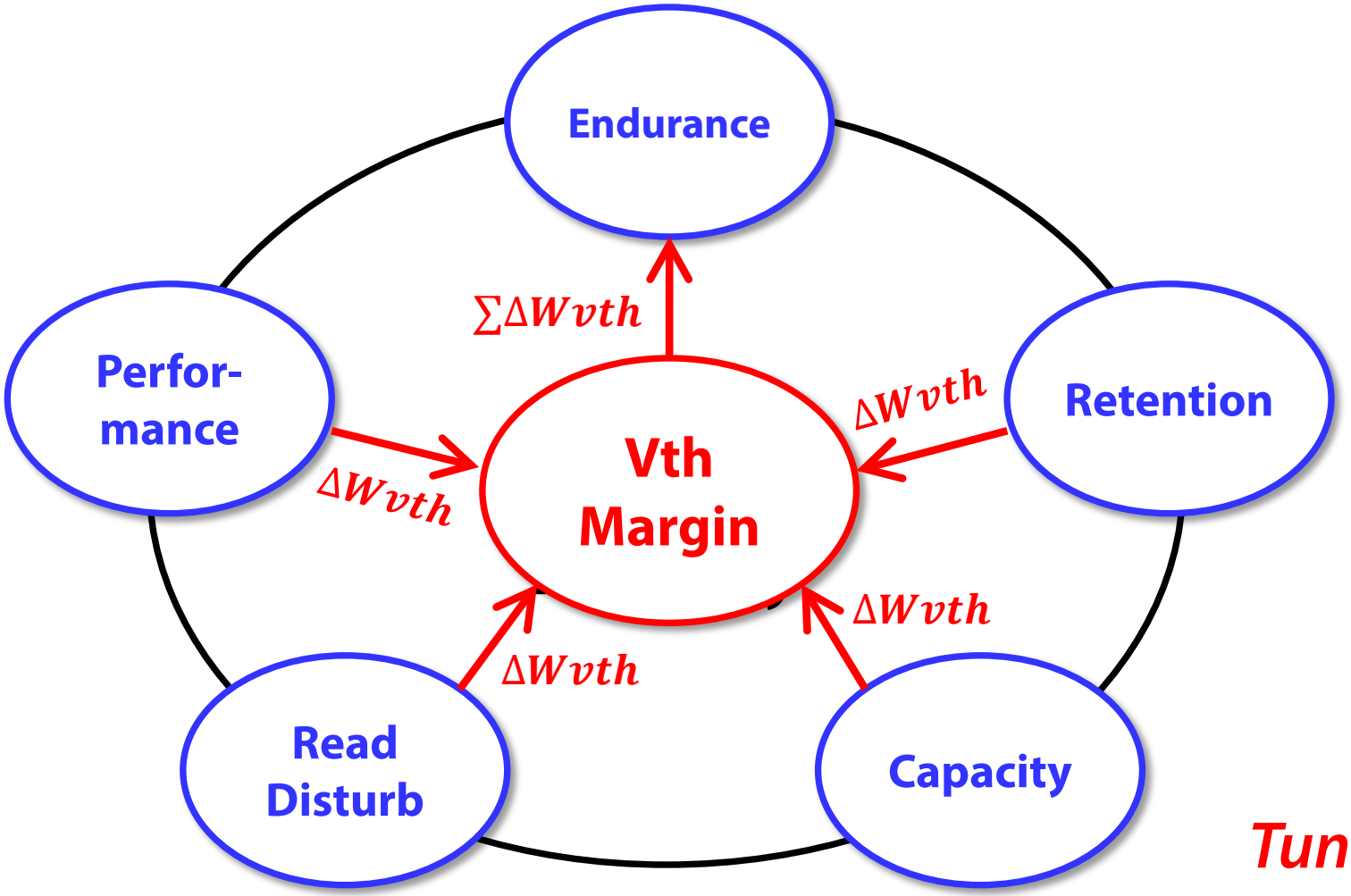
NAND Flash Reliability – Read Disturb

- **Read disturb is an unexpected soft-program phenomenon due to repeated read operations**
  - V_{READ} (6~7V) which is applied to unselect W/L's in read operation can cause a soft-programming.
  - Read stress increases with the read voltage and read operation time
  - As P/E cycles increase, read disturb errors are accelerated





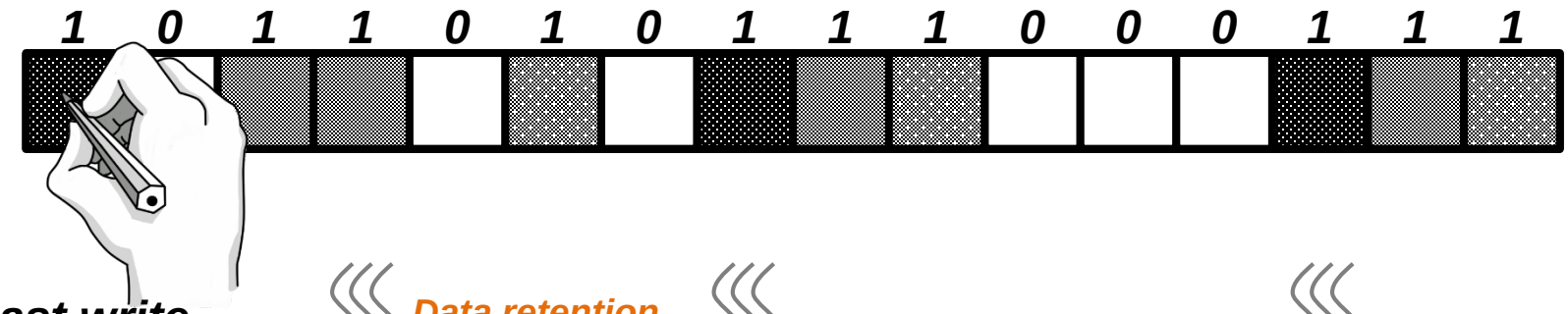
NAND Flash Trade-Off Overview



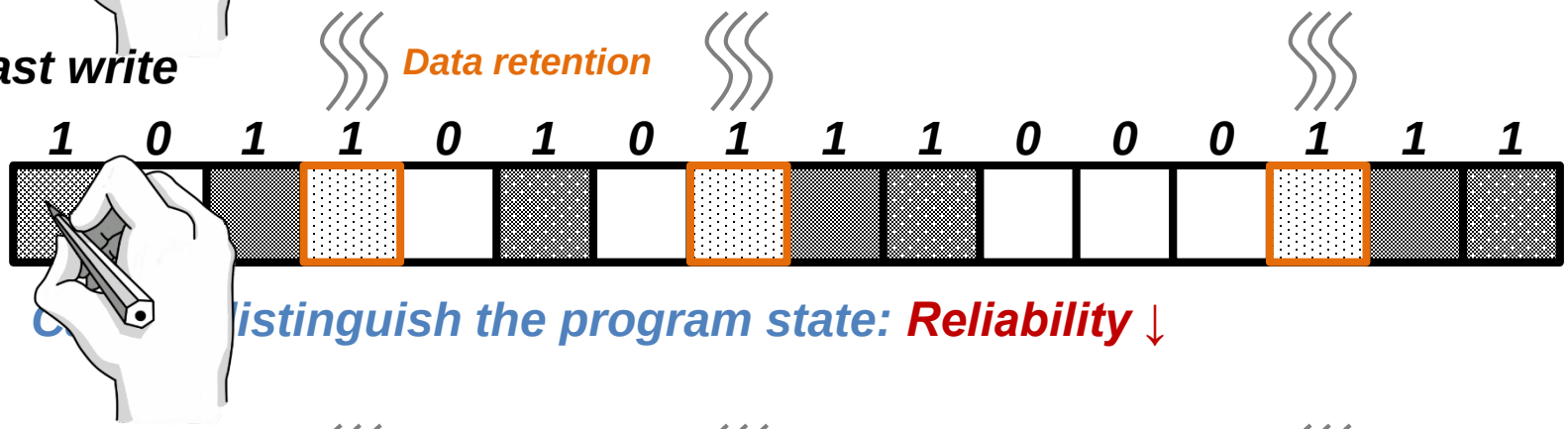
Tuning Control

Write Performance vs. Retention

Normal write

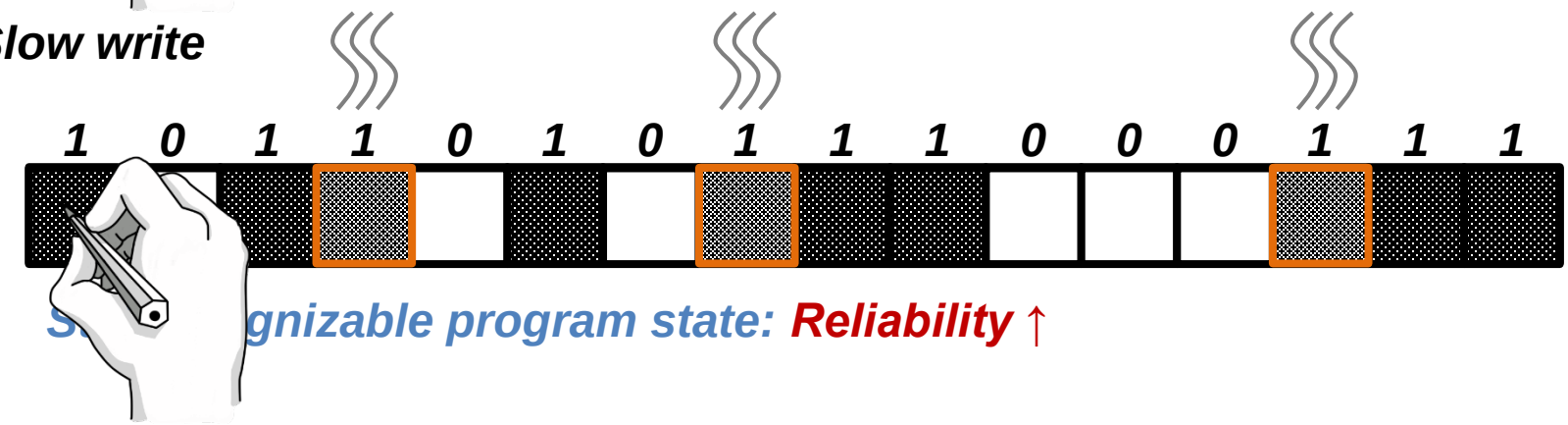


Fast write



C istinguish the program state: Reliability ↓

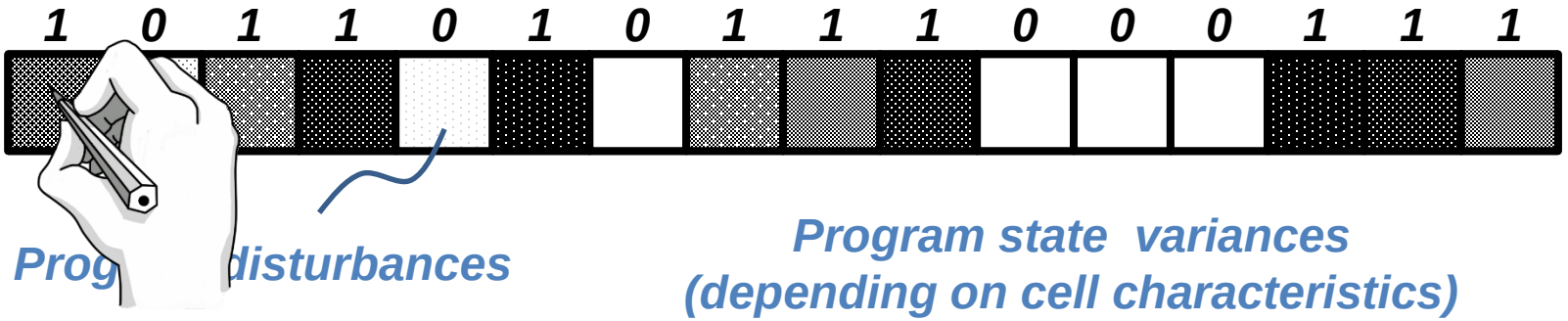
Slow write



S gnizable program state: Reliability ↑

Capacity vs. Write Performance

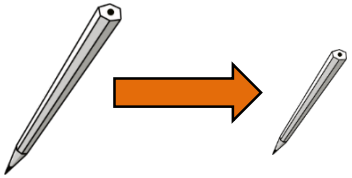
What happens in a NAND page-write



Prog disturbances

Program state variances
(depending on cell characteristics)

With shrunk processes and multi-leveling



1) Precise voltage control for smaller grids

2) Multi-step writing
(e.g., ISPP – Incremental Step Pulse Program)