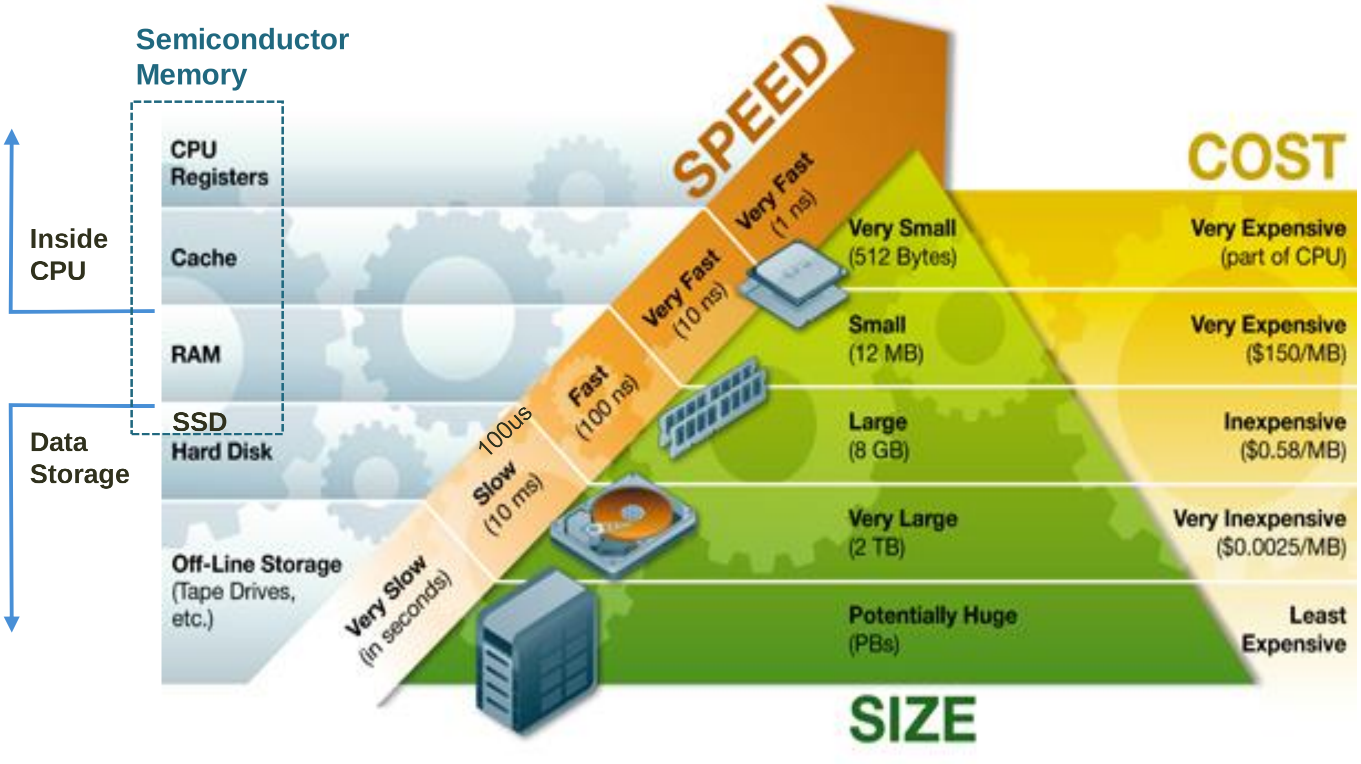
Memory Types & Hierarchy



source : www.ts.avnet.com

Memory types and strong points

- SRAM : Speed
- DRAM : Speed/Cost
- NAND : Cost

- **Requirements of memory device**
  - Fast Write / Read Speed
  - High Write / Read Throughput
  - Random Access
  - Non-volatility
  - Low Power Consumption
  - Low Cost / High Density

Single memory type cannot cover all the requirements

Memory performance comparison chart

Volatility	Volatile		Non-Volatile				
	SRAM	**DRAM**	**NAND**	**FeRAM**	**MRAM**	**PRAM**	**ReRAM**
Cell Size(F^2)	150~200	~8	≤ 2	30~80	20~40 $^{(a)}$ ~8 $^{(b)}$	~4 ≤2 (3D stack)	≤ 2
Read Time	~1ns	~30ns	~50us	~70ns	< 30ns	~30ns	30ns~1us
Write Time	~1ns	~30ns	~1ms	~70ns	< 30ns	~500ns	30ns~1us
Endurance	$> 10^{15}$	$> 10^{15}$	10^5	10^{12}	$> 10^{15}$	10^7	$> 10^7$
Byte Operation	O	O	X	O	O	O	O
Commercialized	-	1970 Intel	1989 Toshiba	2006 Fujizsu / Ramtron	2006 $^{(a)}$ Freescale	2010 Samsung 2015 Intel / Micron	Under Research

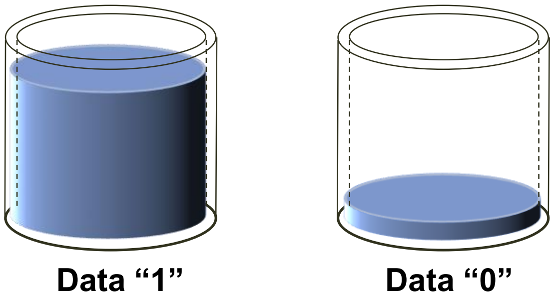
(a) : Field Switching MRAM
(b) : STT-MRAM

Each memory has its own strength

→ Cannot be easily replaced by others

Classification - Operating principles

Capacitor Based



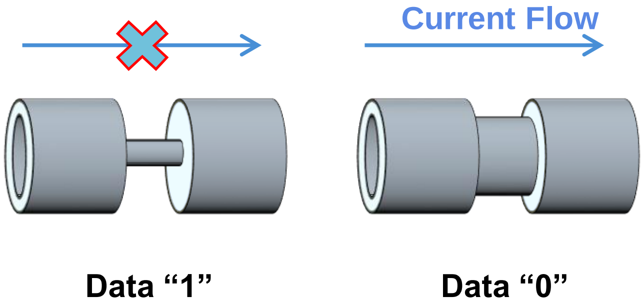
- **DRAM**
- **SRAM**
- **Flash**

Difficult to increase memory density (scaling device size)

- Capacitance (Bottle volume) ↓

→ Signal strength ↓

Resistor Based



- **PRAM (Phase-change Memory)**
- **MRAM (Magnetic Memory)**
- **RRAM (Resistive Memory)**

Advantages to increasing density

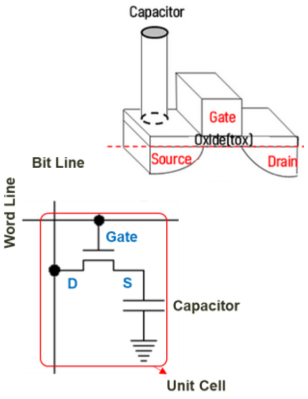
- Signal strength is insensitive to device size

Classification

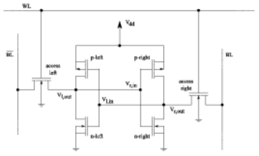
Volatile | **Non-Volatile**

Capacitor Based

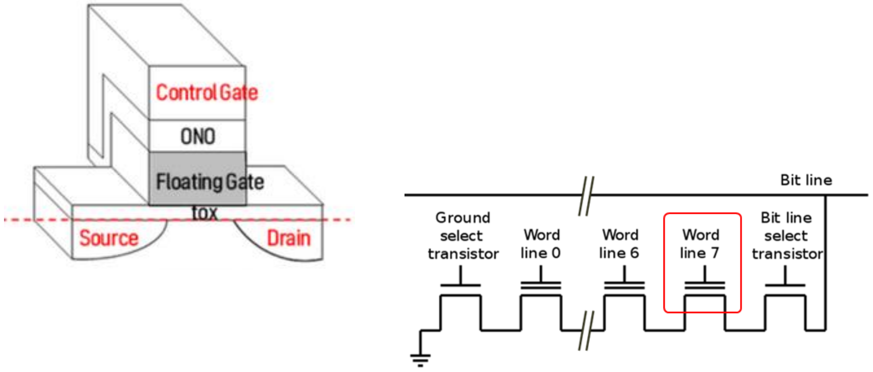
DRAM



SRAM

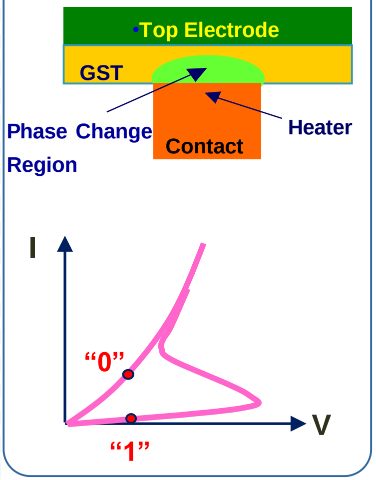


FLASH

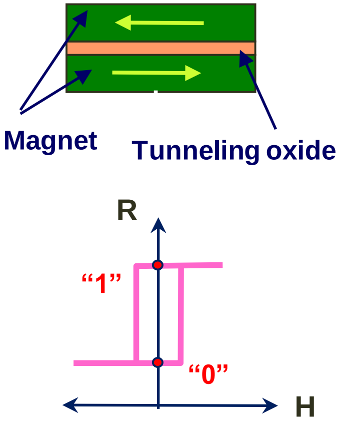


Resistor Based

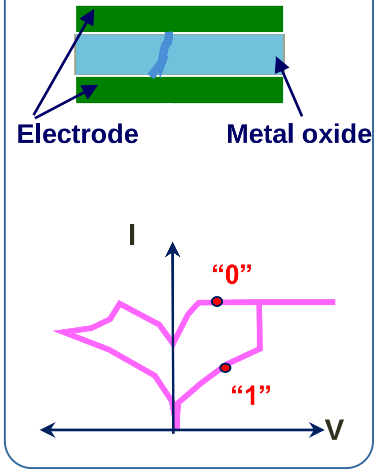
PRAM



MRAM

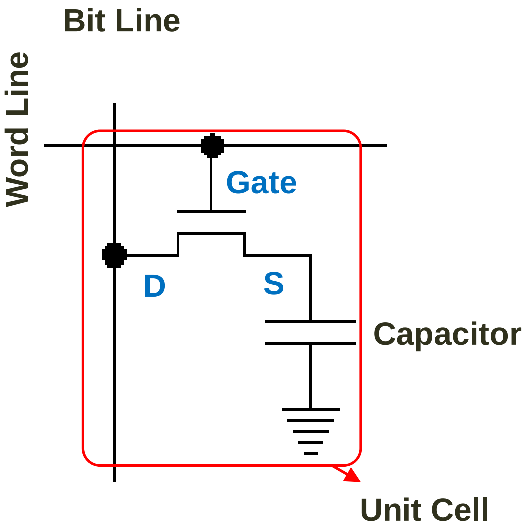


RRAM

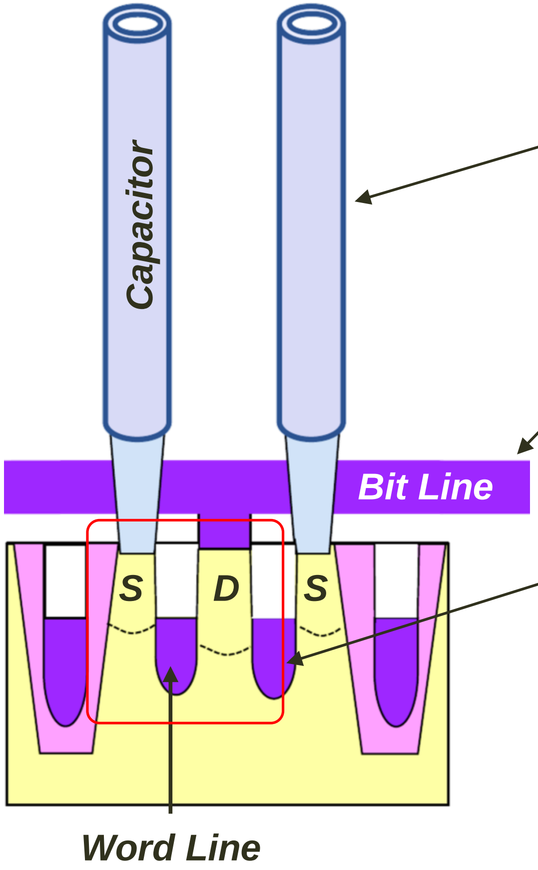


DRAM

1 Transistor + 1 Capacitor



S : Source
D : Drain



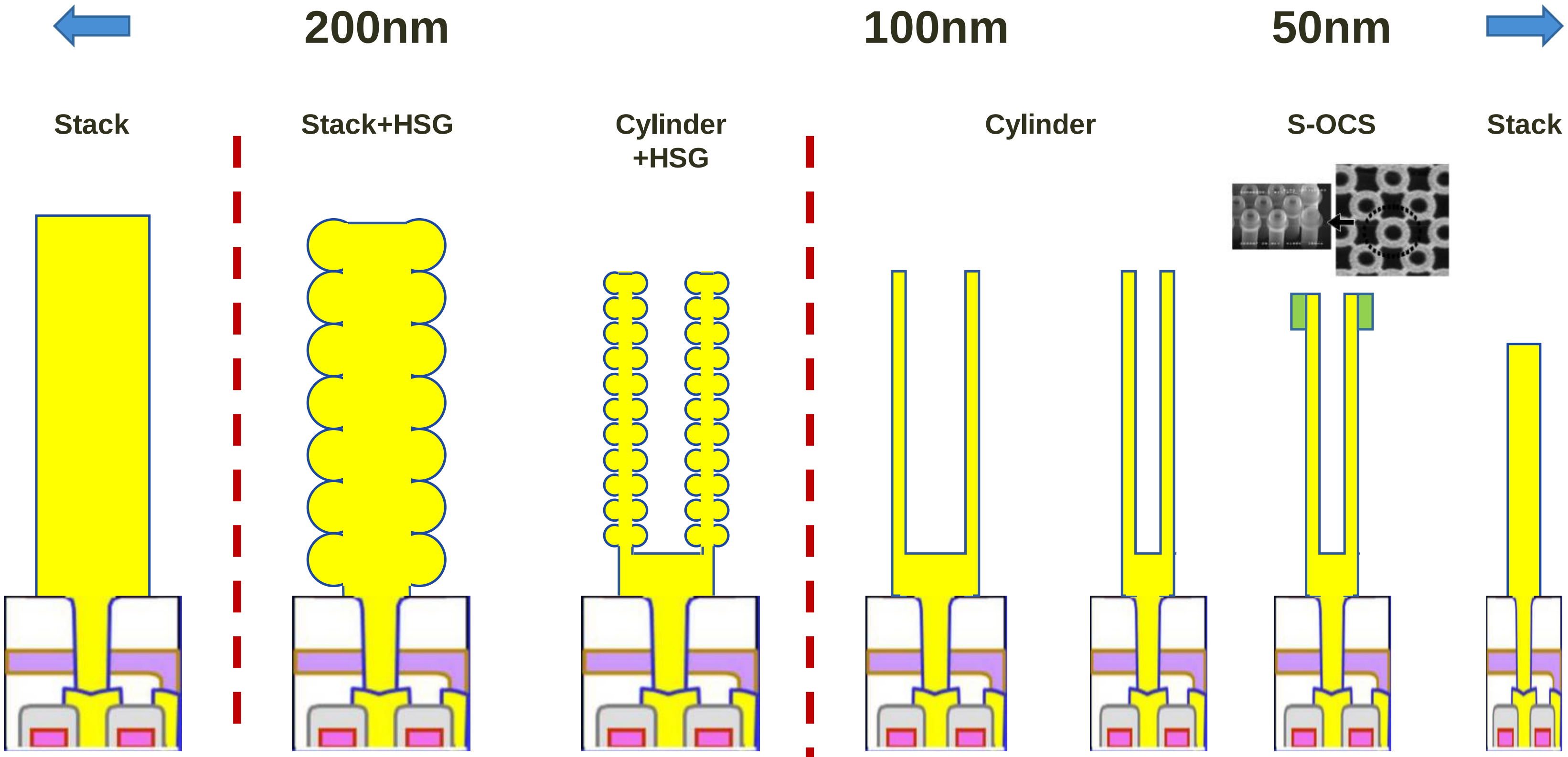
Capacitor
The location where charge is stored. Composed of Storage Node, Dielectric, and Plate node triple structure.

Bit Line
Data I/O line

Cell Transistor + Word Line
Transferring charge between capacitor and bit line to store / read data

Charged capacitor representing data ‘1’ and an uncharged capacitor ‘0’

DRAM – evolution of capacitor



200nm 100nm 50nm

Stack | **Stack+HSG** | **Cylinder +HSG** | **Cylinder** | **S-OCS** | **Stack**

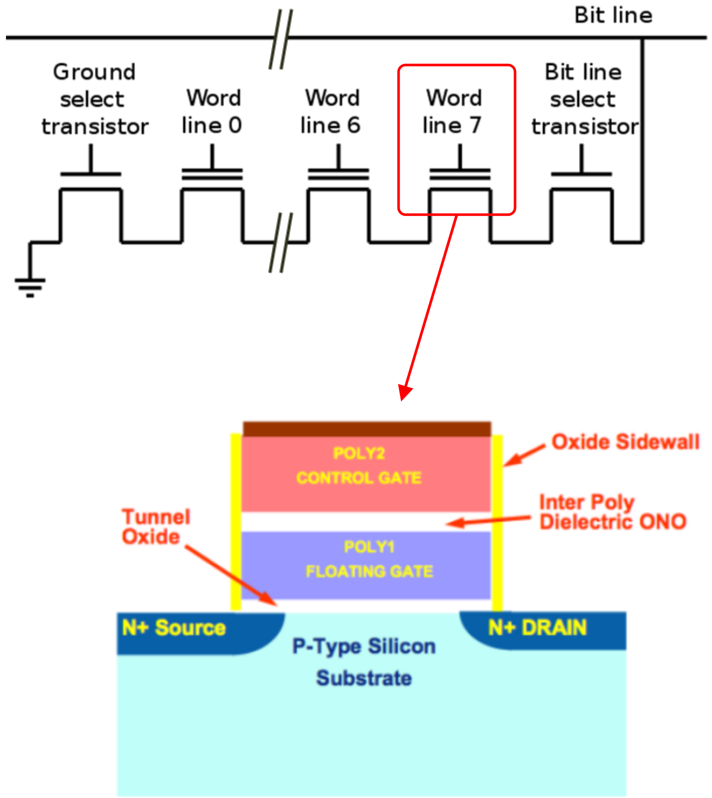
SiO_2 / Si_3N_4 → **Al_2O_3, Ta_2O_5, HfO_2** → **HfO_2, ZrO_2, $SrTiO_3$** →

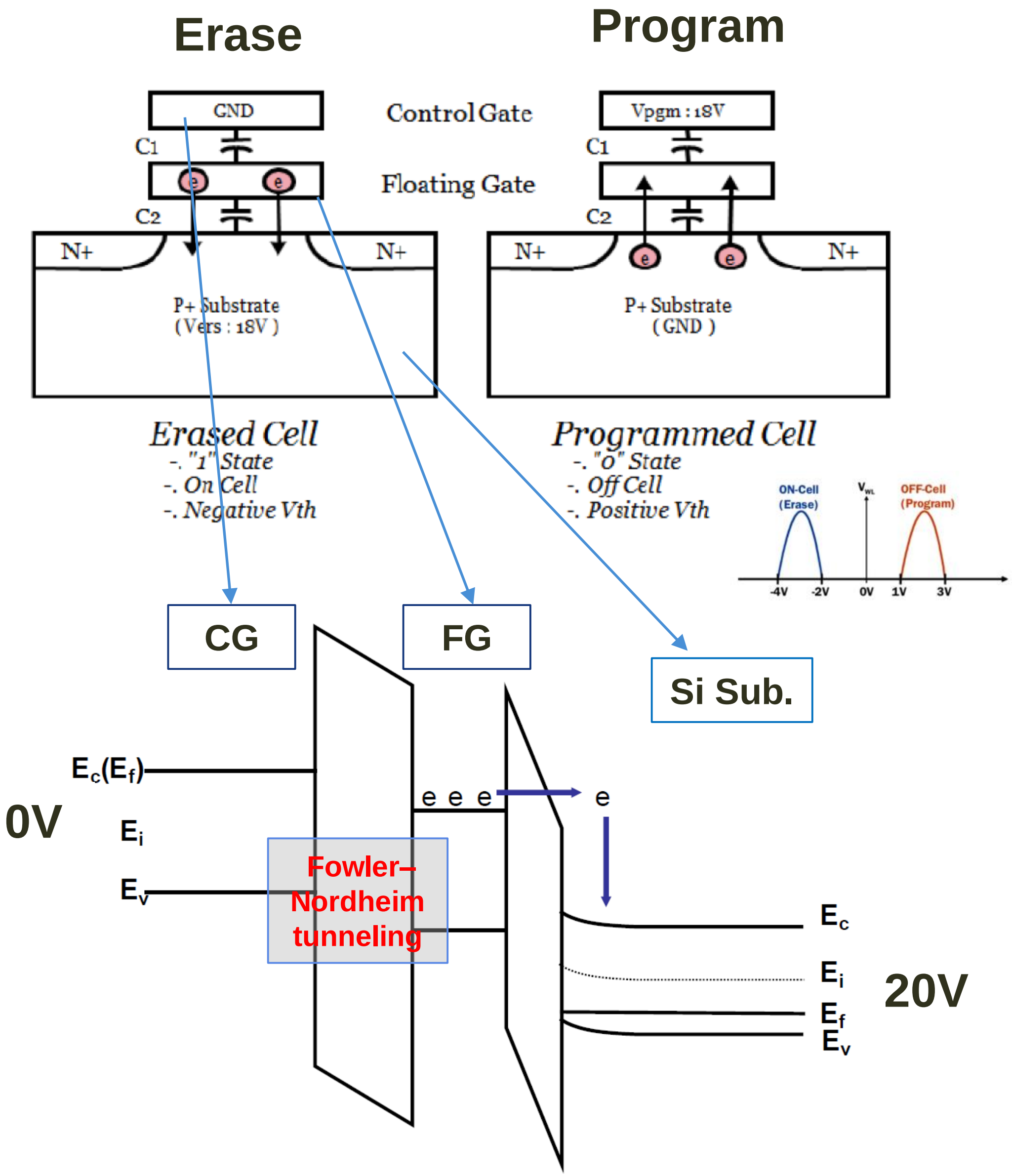
Low-k & Complex Structure

High-k & Simple Structure

*** HSG : Hemi-Spherical Grain**

Flash



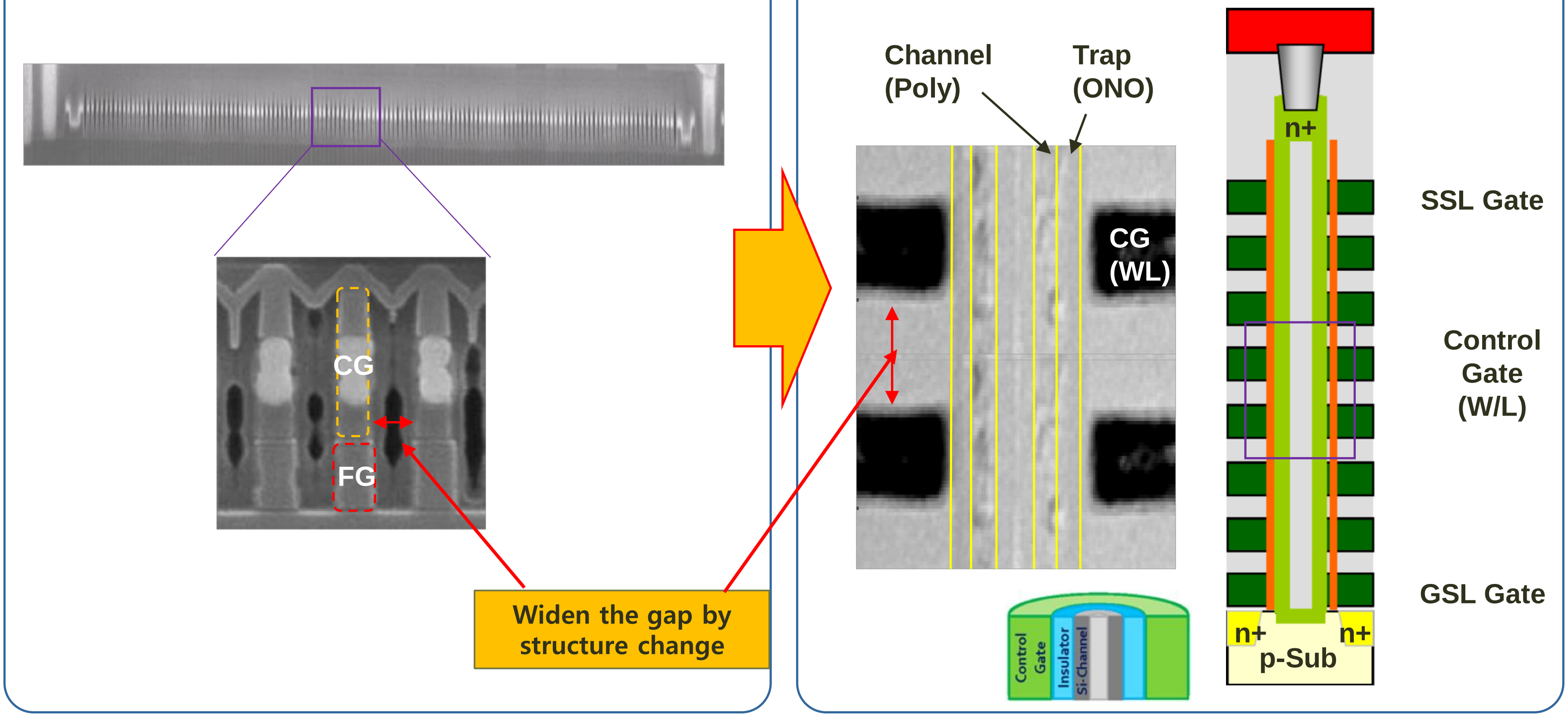


Use F-N tunneling to ‘trap’ electron at Floating Gate

Flash – nowadays

2D NAND → 3D NAND
Floating Poly Gate → Charge Trap Flash (CTF) Technology

2D NAND **3D NAND**



- Bit growth : Cell dimension decreased by 3D stacking → Overcomes scaling issue
- High program performance : Decreased interference between cells
- Low power consumption

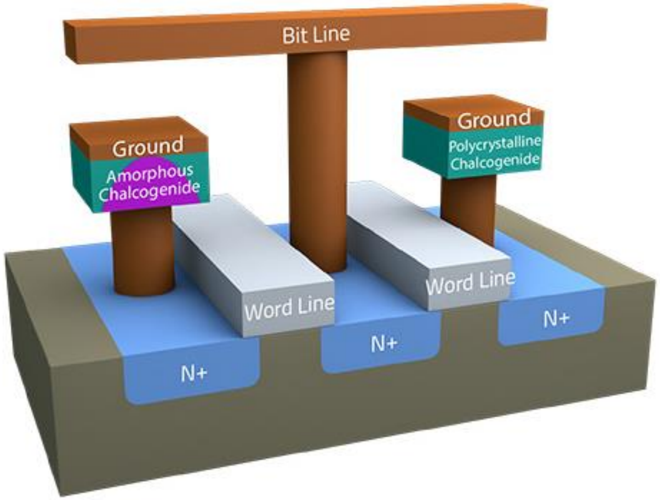
source : samsungsemiconstory.com

PcRAM (Phase-change RAM)

Reversible phase change of chalcogenide material

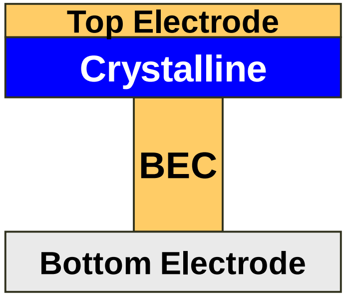
(Crystalline ⇔ Amorphous)

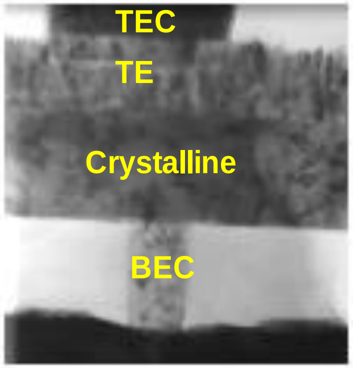
- Writing : Current heating
- Reading : Resistance change



Low resistance

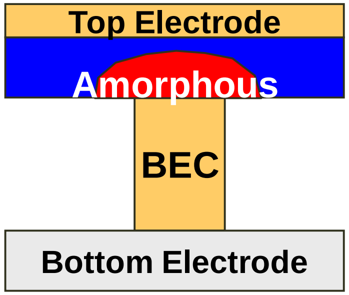
SET state : “0”

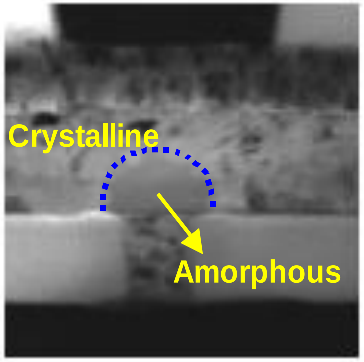




High resistance

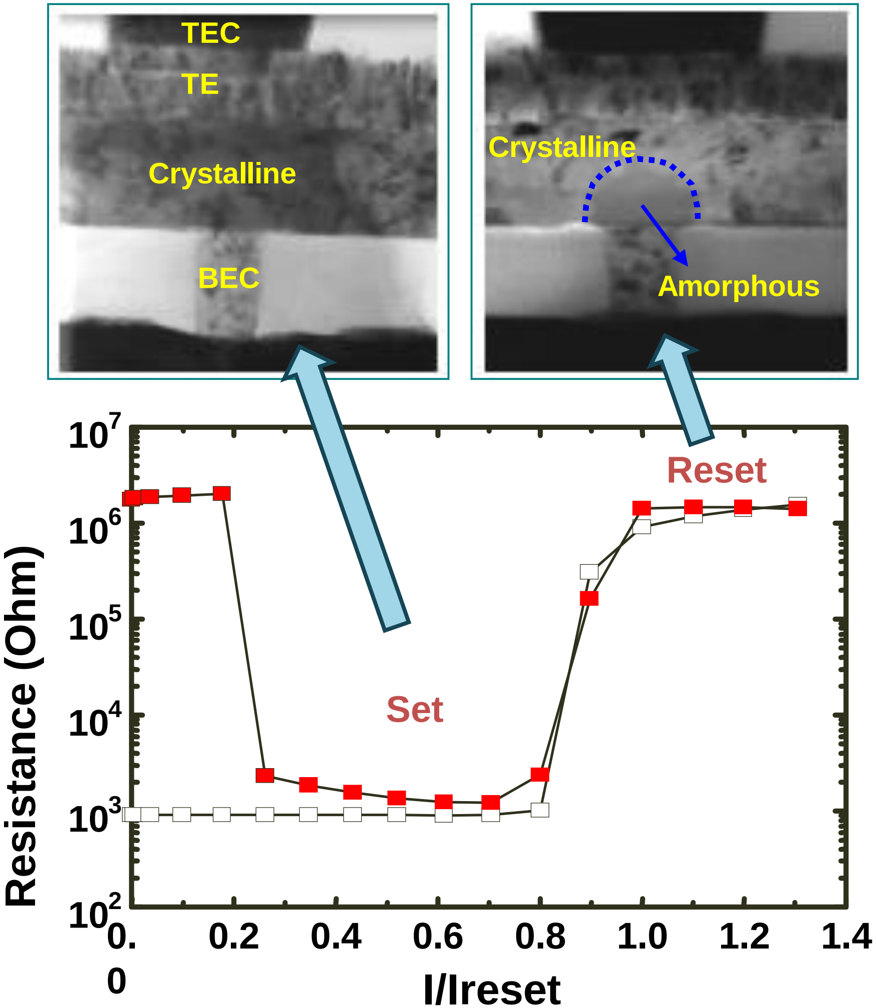
RESET state : “1”



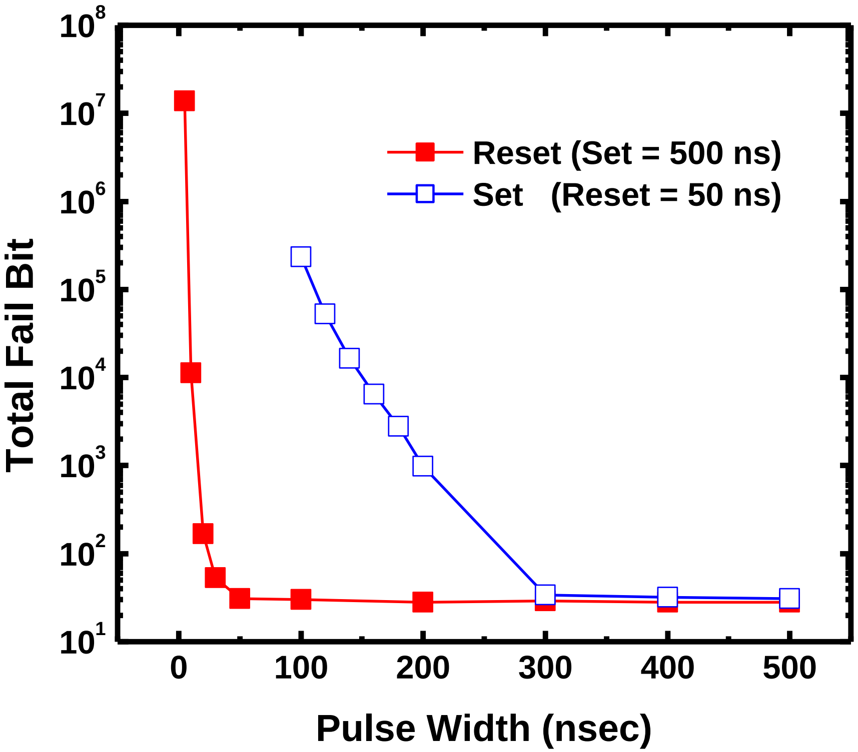


Switching Behavior of PRAM

- Set/Reset Transition



- Switching Speed

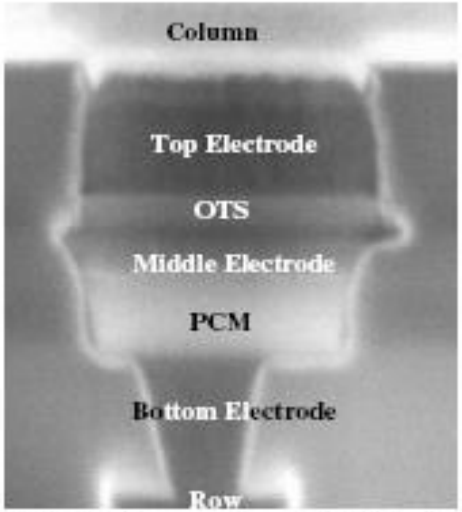


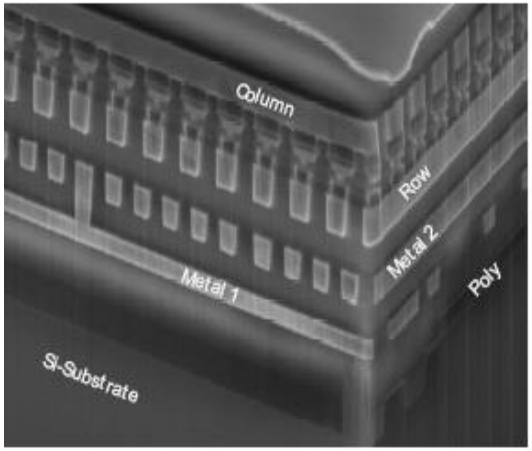
G. H. Koh, ISADPT(2003)

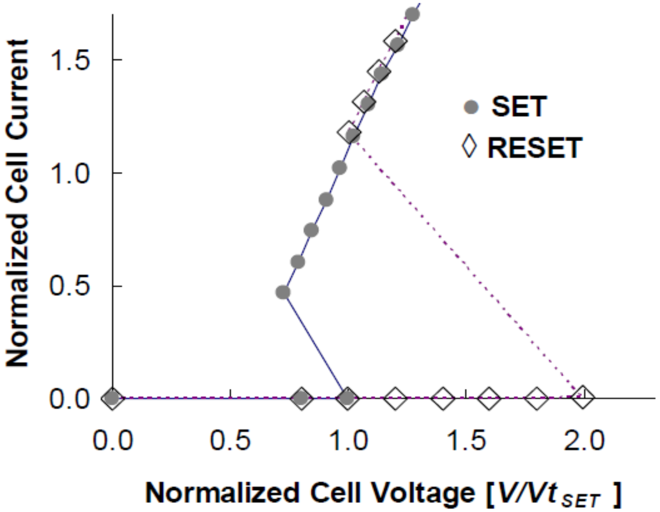
- Switching speed → Crystallization limit (transition to SET)
- Switching current → Melting limit (transition to RESET)

PRAM – 3D Stack

- **Cross-point cell structure**
  - Cell selector : OTS (Ovonic Threshold switching)
  - Cell storage : PCM (Phase change memory)





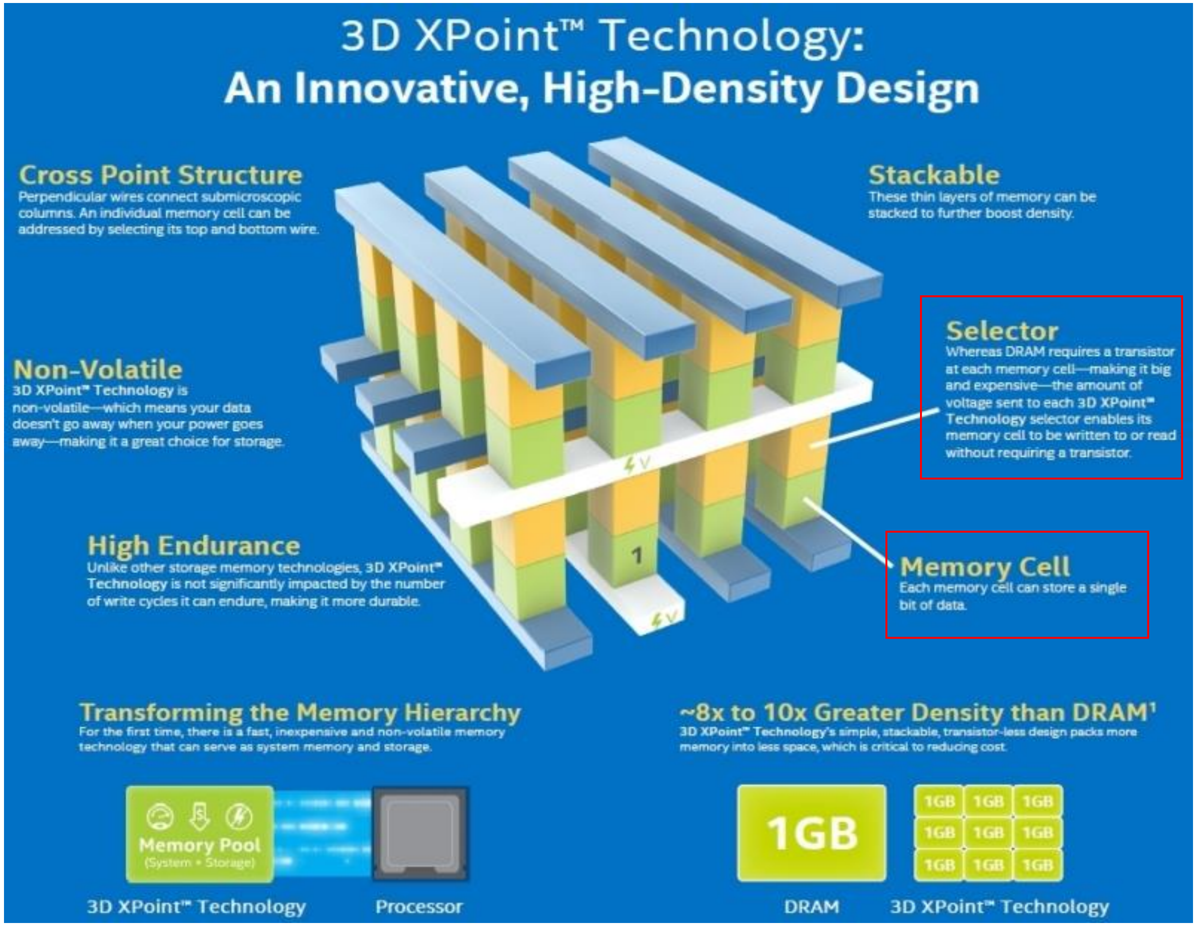


D. Kau, Intel/Numonyx, IEDM 2009

- Challenges :
  - Selector technology
  - Process integration & characteristic distribution control

PRAM - nowadays

3D-Xpoint Memory - Intel/Micron (2015)



3D XPoint™ Technology:
An Innovative, High-Density Design

Cross Point Structure
Perpendicular wires connect submicroscopic columns. An individual memory cell can be addressed by selecting its top and bottom wire.

Stackable
These thin layers of memory can be stacked to further boost density.

Non-Volatile
3D XPoint™ Technology is non-volatile—which means your data doesn't go away when your power goes away—making it a great choice for storage.

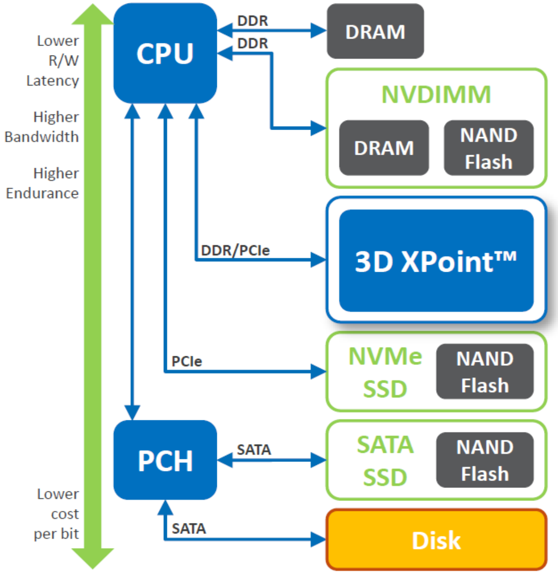
Selector
Whereas DRAM requires a transistor at each memory cell—making it big and expensive—the amount of voltage sent to each 3D XPoint™ Technology selector enables its memory cell to be written to or read without requiring a transistor.

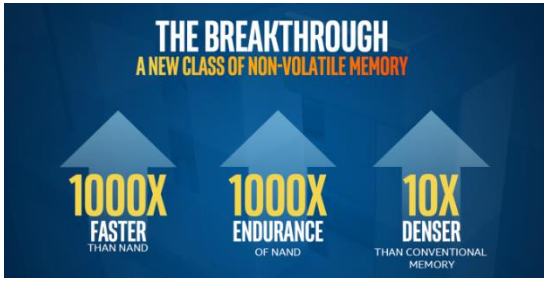
High Endurance
Unlike other storage memory technologies, 3D XPoint™ Technology is not significantly impacted by the number of write cycles it can endure, making it more durable.

Memory Cell
Each memory cell can store a single bit of data.

Transforming the Memory Hierarchy
For the first time, there is a fast, inexpensive and non-volatile memory technology that can serve as system memory and storage.

~8x to 10x Greater Density than DRAM[1]
3D XPoint™ Technology's simple, stackable, transistor-less design packs more memory into less space, which is critical to reducing cost.





PRAM – 3D VNAND-like Cell Structure

- Vertical Poly-Si Tr + Phase change material
- Thin channel Tr, Thin PCM → Memory hole size scaling

  (NAND 60nm → VCCPM 32nm)
- Vertical poly-Si diode : String Selector. Cell dimension $6F^2$ (Tr) → $4F^2$ (diode)

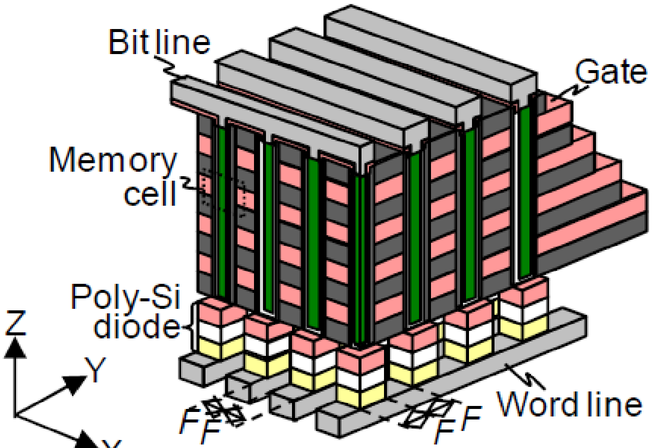


Figure 2. Device structure of VCCPM array

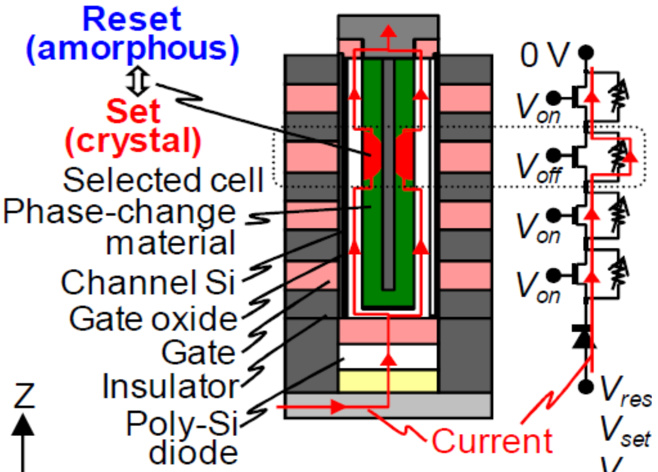


Figure 3. Device structure and operation of VCCPM

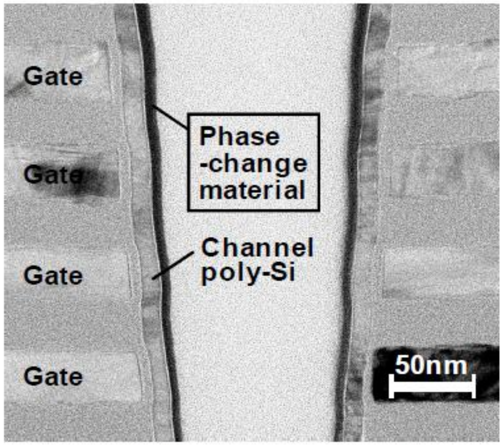
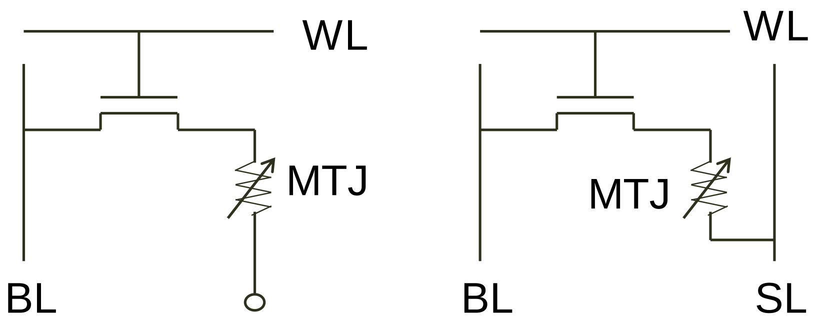
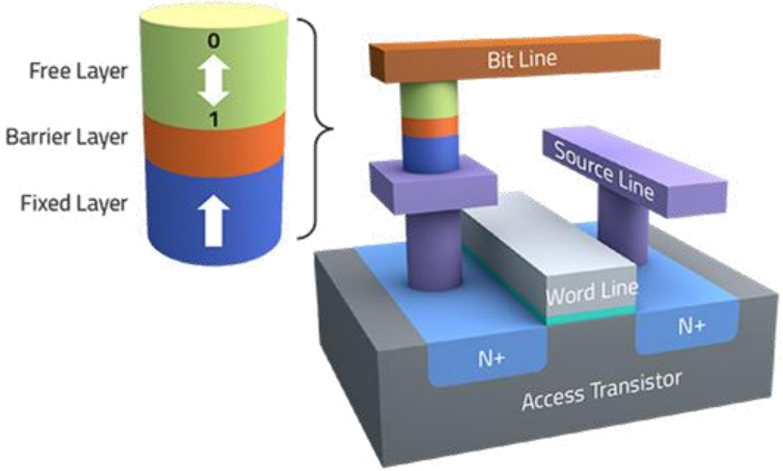


Figure 6. Cross-sectional view of VCCPM

M. Kinoshita, Hitachi, VLSI 201

MRAM (Magnetic RAM)

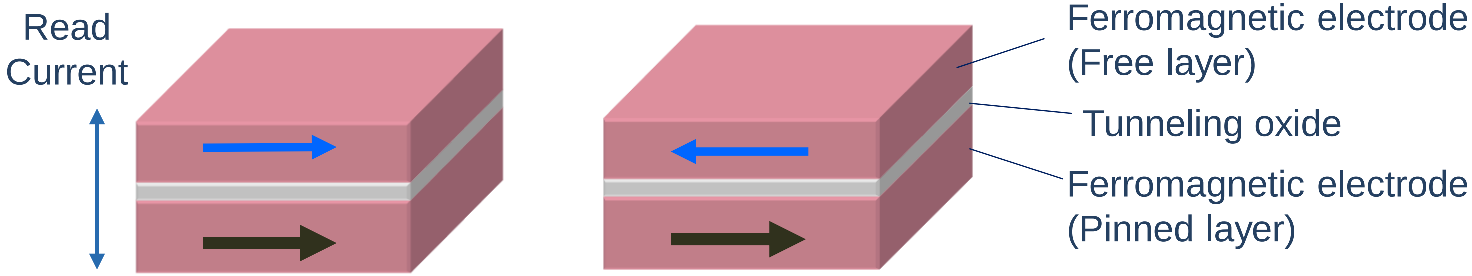




- **MTJ (Magnetic Tunnel Junction)**

  : Spin-dependent tunneling

  : Resistance change controlled by magnetization direction



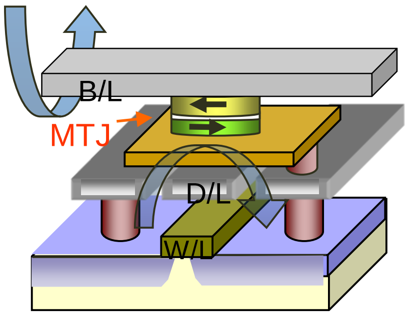
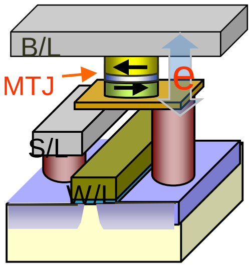
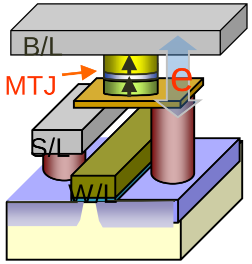
Parallel Magnetization
→ Low Resistance (R_p)

Anti-Parallel Magnetization
→ High Resistance (R_{ap})

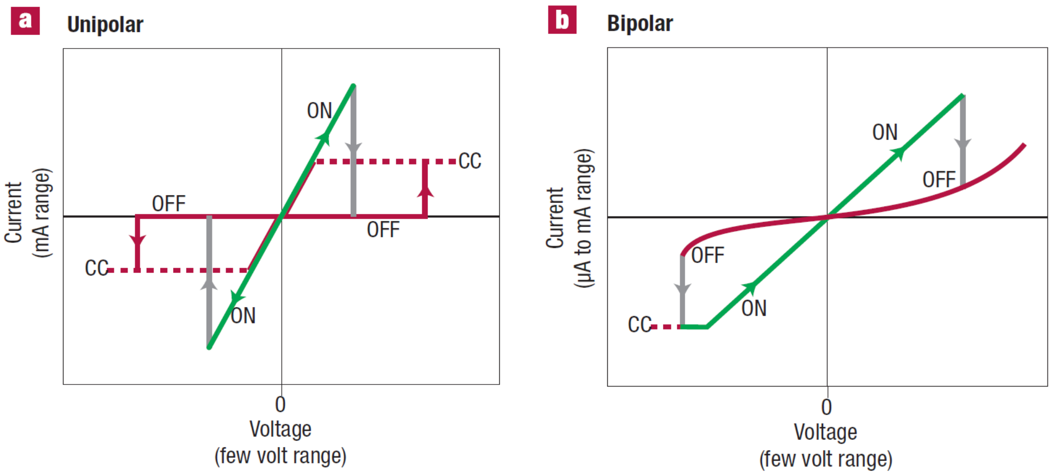
$$TMR = \frac{R_{AP} - R_P}{R_P}$$

TMR : Tunneling Magneto-resistance

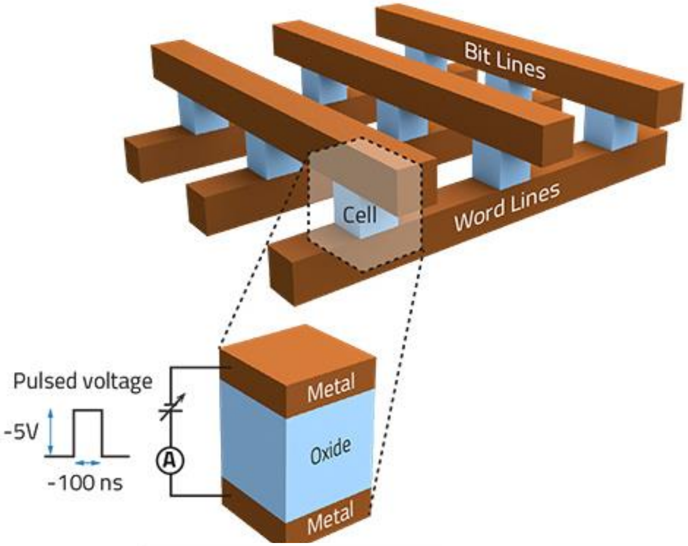
MRAM – Types and charateristics

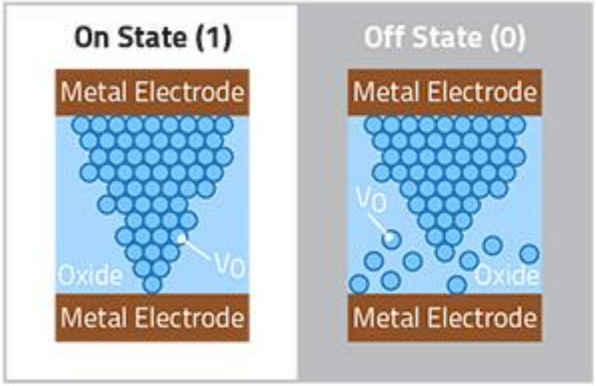
	Field -MRAM	STT-MRAM (in-plane mag.)	STT-MRAM (out-of-plane mag.)	
Operation Principle	**Field Switching** 	**STT Switching** 	**STT Switching** 	
Characteristic	- MTJ size decrease → I_{sw} increase - Disturb issue in half-selected cells	- MTJ size decrease → I_{sw} decrease - MTJ aspect ratio > 2:1	- MTJ size decrease → I_{sw} decrease - MTJ aspect ratio ~ 1:1	
Cell Area	> 22.5F^2	6~12F^2	4~12F^2	
Anisotropy	Shape K_u~10^4 erg/cc	Shape K_u~10^4 erg/cc	Interface K_u~5*10^6 erg/cc	Bulk K_u~10^7 erg/cc
Scalability Limit	**~ 90nm**	**30 ~ 40nm**	**10~20nm**	**5~10nm**

RRAM (Resistive RAM)



R. Waser, Nature Materials 2007

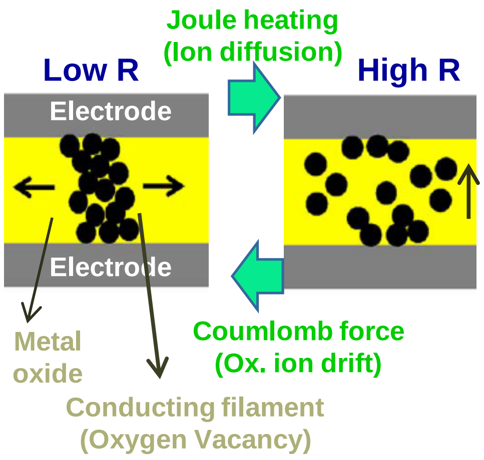
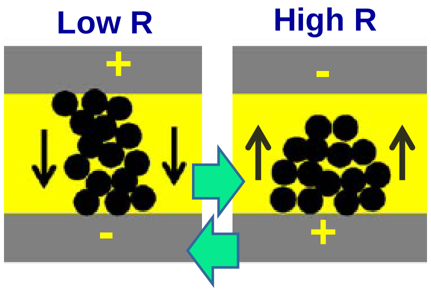
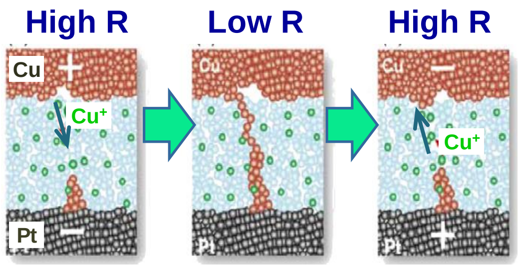
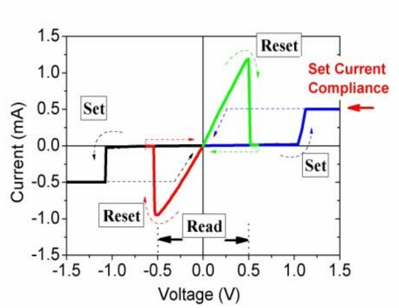
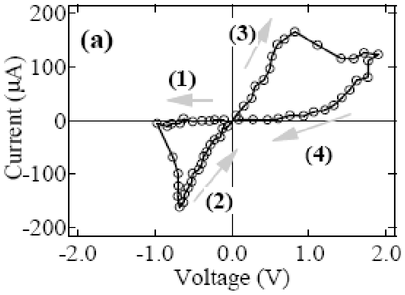
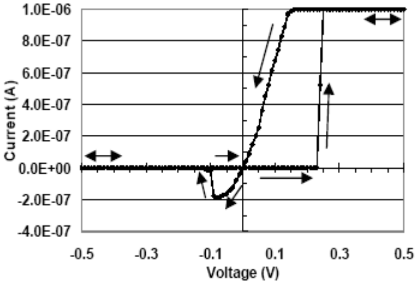




RRAM : R depends on the state of the film
Low Resistance (SET) & High resistance (RESET)

- Unipolar : SET & RESET switching occurs at the same polarity
- Bipolar : SET & RESET switching occurs at opposite polarity

RRAM - Types and Switching Mechanisms

	Filamentary (Unipolar)	Filamentary (Bipolar)	CBRAM (Bipolar)
Operating Principle	 **Joule heating (Ion diffusion)** **Low R** **High R** **Electrode** **Electrode** **Metal oxide** **Coulomb force (Ox. ion drift)** **Conducting filament (Oxygen Vacancy)** **O^{2-} ion Electro-migration + Thermal diffusion + red/ox**	 **Low R** **High R** **Coumlomb force (Ox. ion drift)** *D. Ielmini., T-ED, 2011* **O^{2-} ion Electro-migration + (local) red/ox**	 **High R** **Low R** **High R** **Coulomb force (Metal ion drift)** *I. Valov., J.Phys.D, 2013* **M^+ ion Electro-migration + red/ox**
Switching Curve			
Material	NiO, TiO_2, ZrO_2, HfO_2, … + Noble metal electrode	HfO_x, TiO_x, TaO_x, WO_x, Cu_2O, …	Solid electrolyte + metal ions (GeSe, ... + Ag, Cu...)