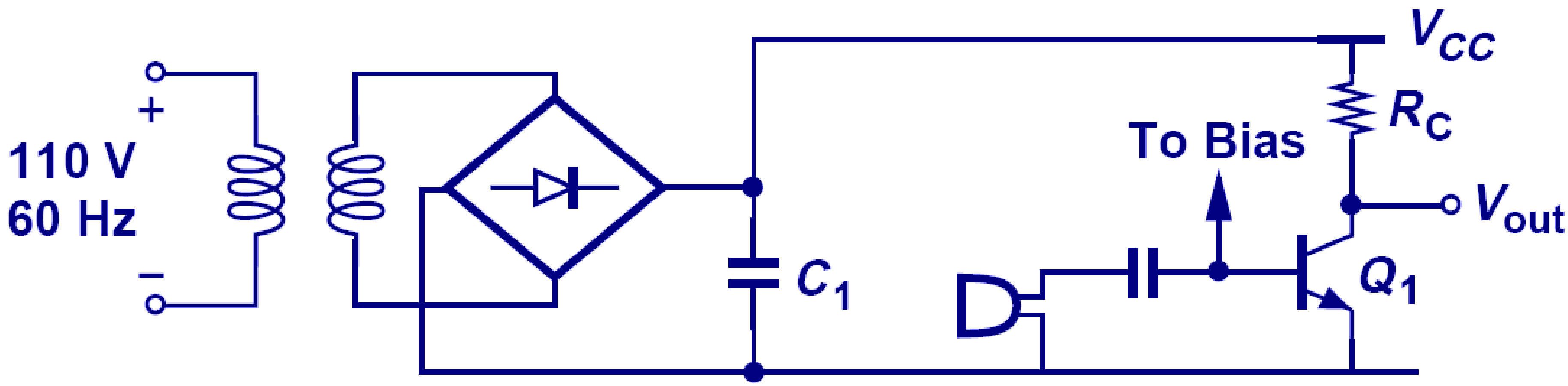
Chapter 10 Differential Amplifiers

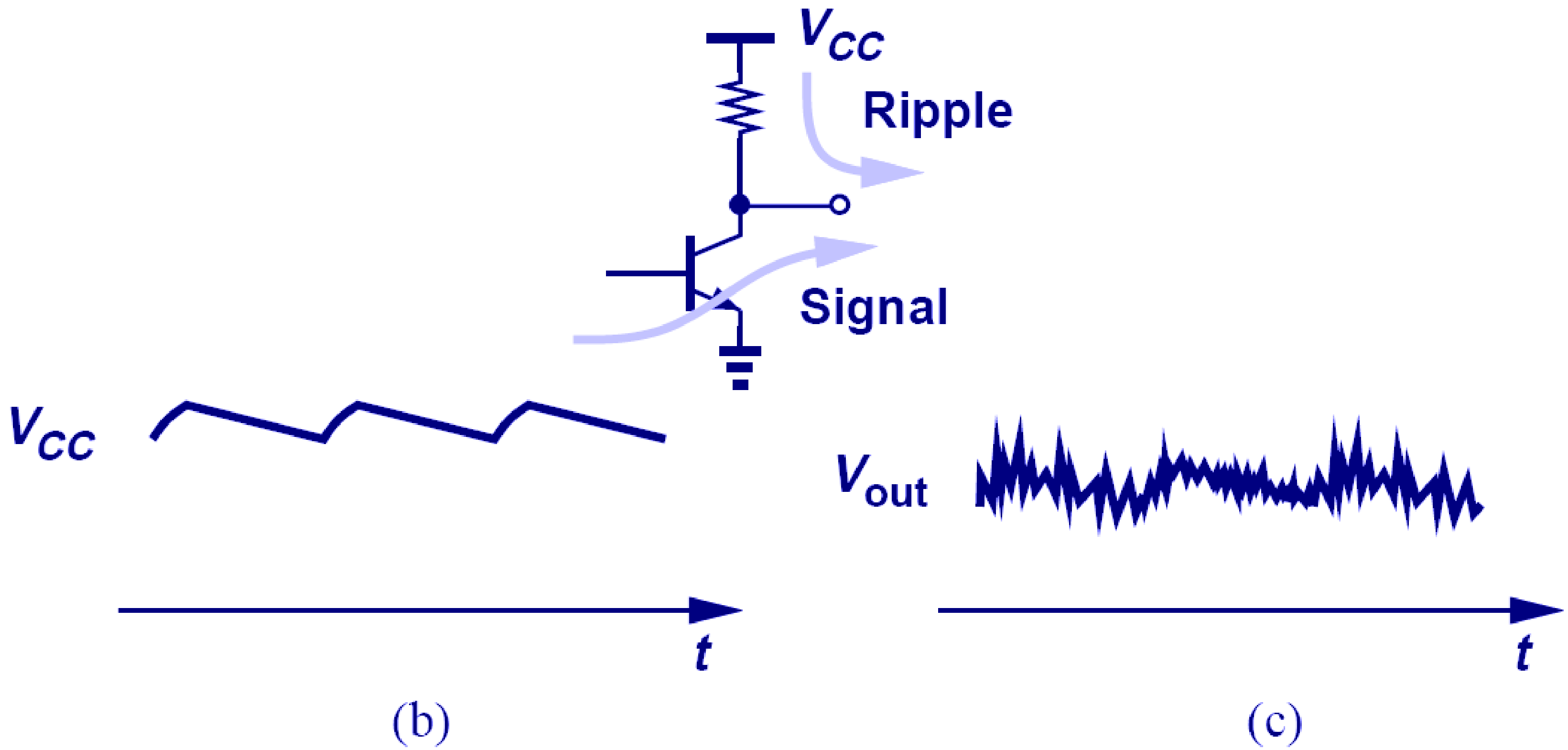
- 10.1 General Considerations
- 10.2 Bipolar Differential Pair
- 10.3 MOS Differential Pair
- 10.4 Cascode Differential Amplifiers
- 10.5 Common-Mode Rejection
- 10.6 Differential Pair with Active Load

Audio Amplifier Example



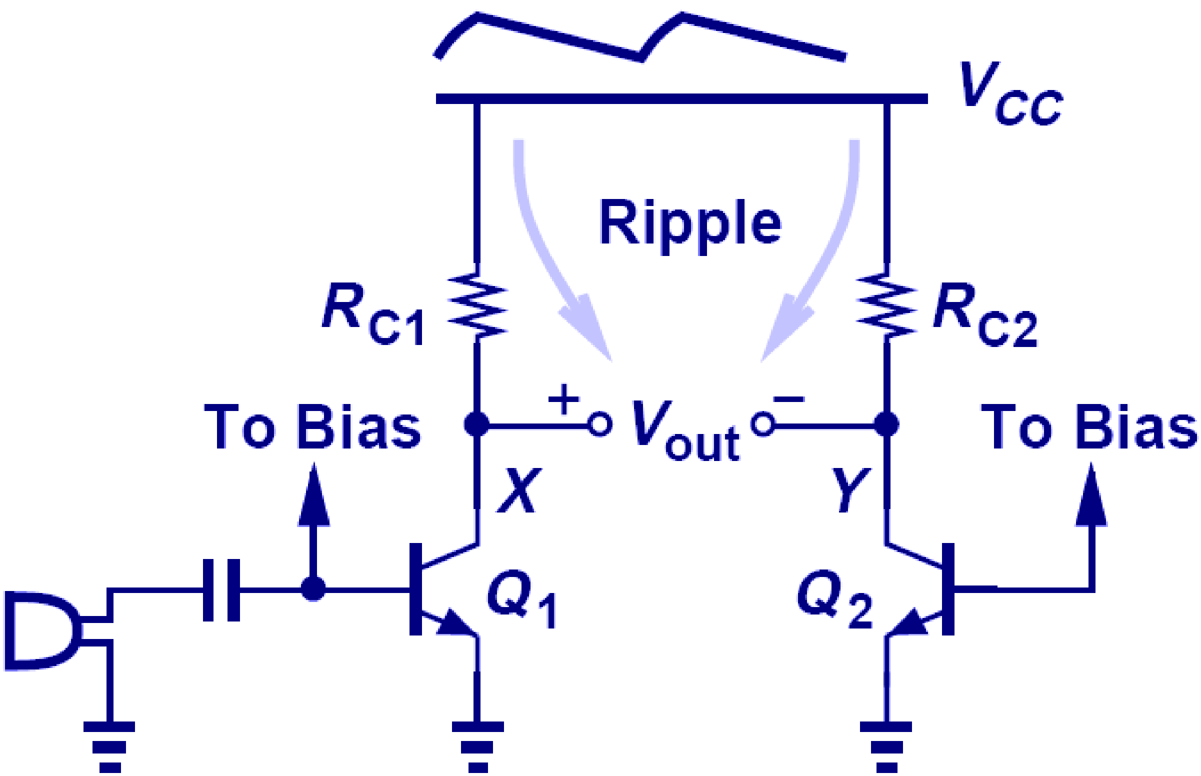
- An audio amplifier is constructed as above that takes a rectified AC voltage as its supply and amplifies an audio signal from a microphone.

"Humming" Noise in Audio Amplifier Example



- However, V_{CC} contains a ripple from rectification that leaks to the output and is perceived as a "humming" noise by the user.

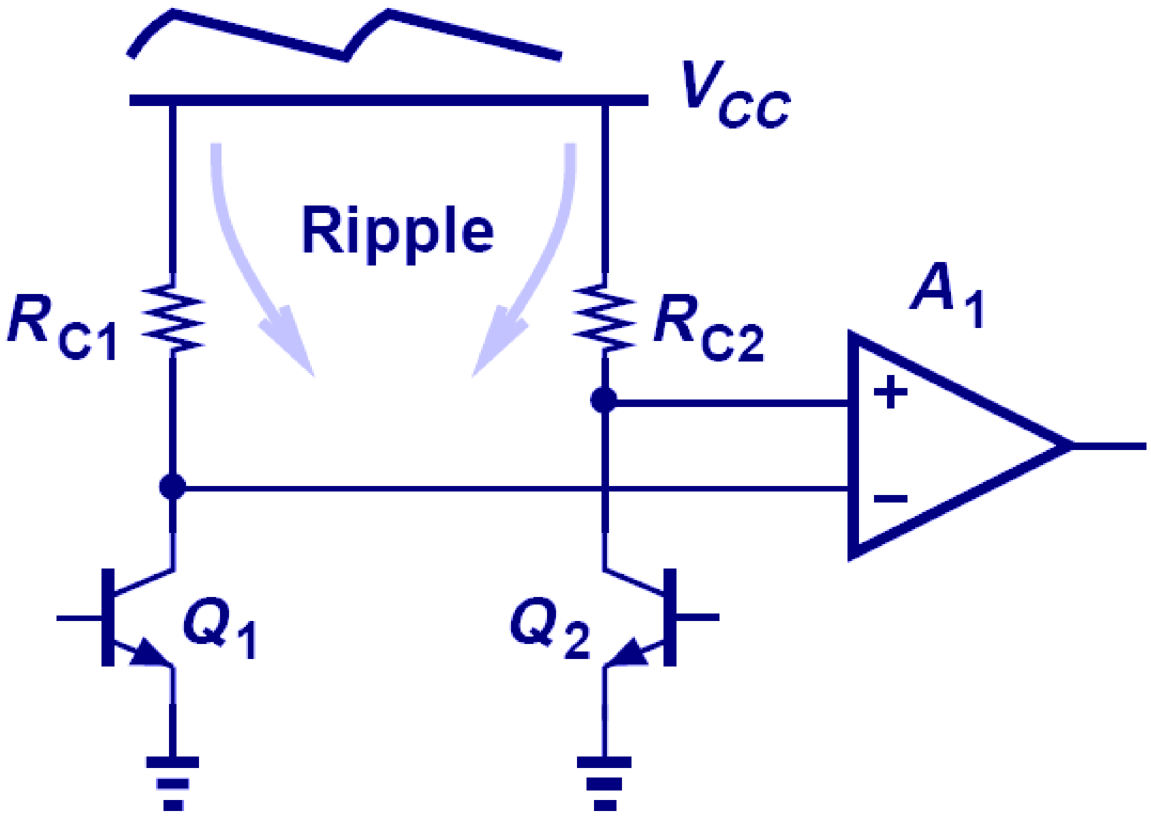
Supply Ripple Rejection



$$v_X = A_v v_{in} + v_r$$
$$v_Y = v_r$$
$$v_X - v_Y = A_v v_{in}$$

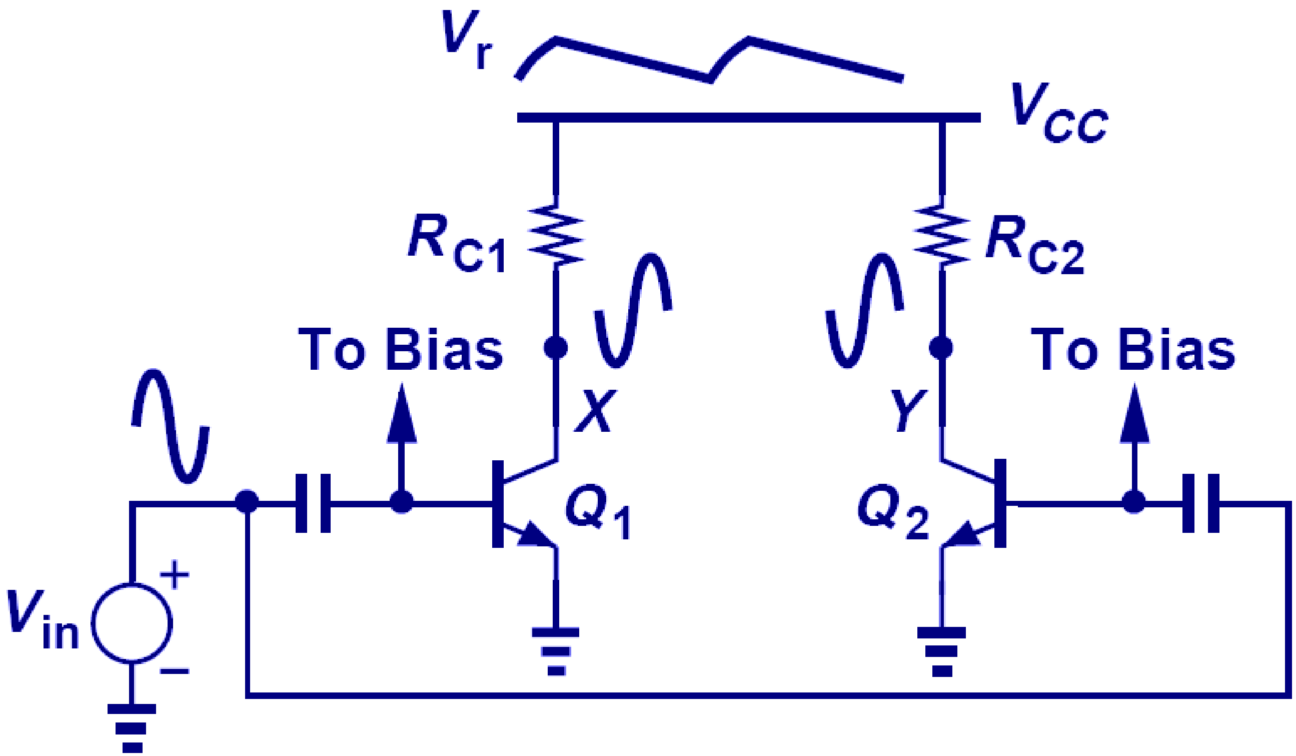
- **Since both node X and Y contain the same ripple, their difference will be free of ripple.**

Ripple-Free Differential Output



- **Since the signal is taken as a difference between two nodes, an amplifier that senses differential signals is needed.**

Common Inputs to Differential Amplifier



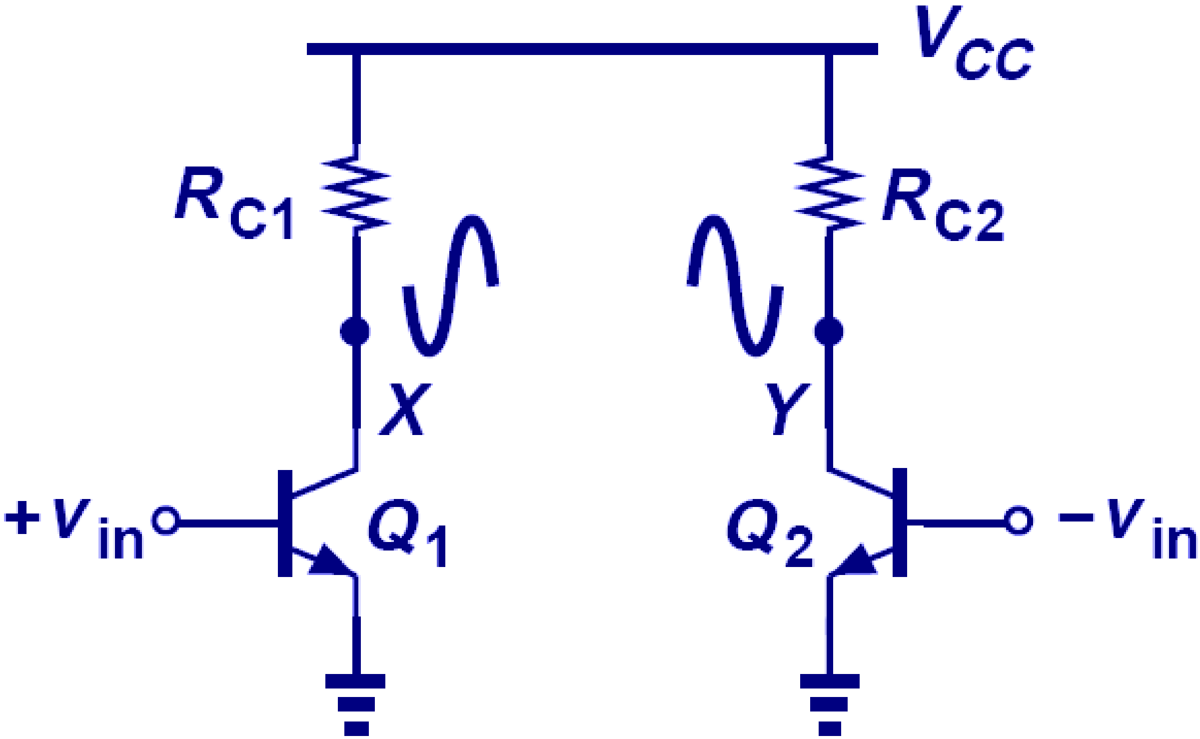
$$v_X = A_v v_{in} + v_r$$

$$v_Y = A_v v_{in} + v_r$$

$$v_X - v_Y = 0$$

- **Signals cannot be applied in phase to the inputs of a differential amplifier, since the outputs will also be in phase, producing zero differential output.**

Differential Inputs to Differential Amplifier



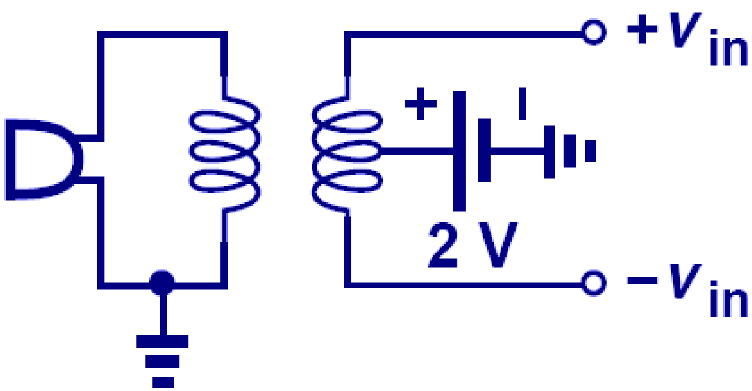
$$v_X = A_v v_{in} + v_r$$

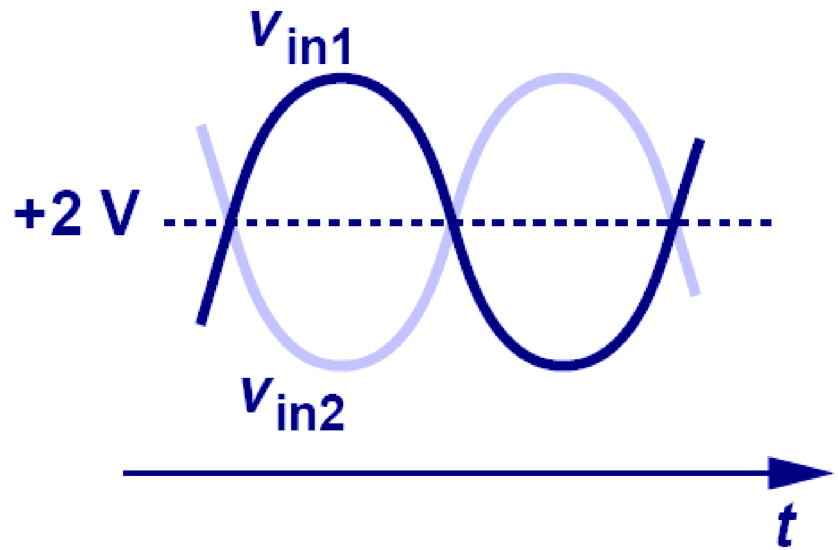
$$v_Y = -A_v v_{in} + v_r$$

$$v_X - v_Y = 2A_v v_{in}$$

- **When the inputs are applied differentially, the outputs are 180° out of phase; enhancing each other when sensed differentially.**

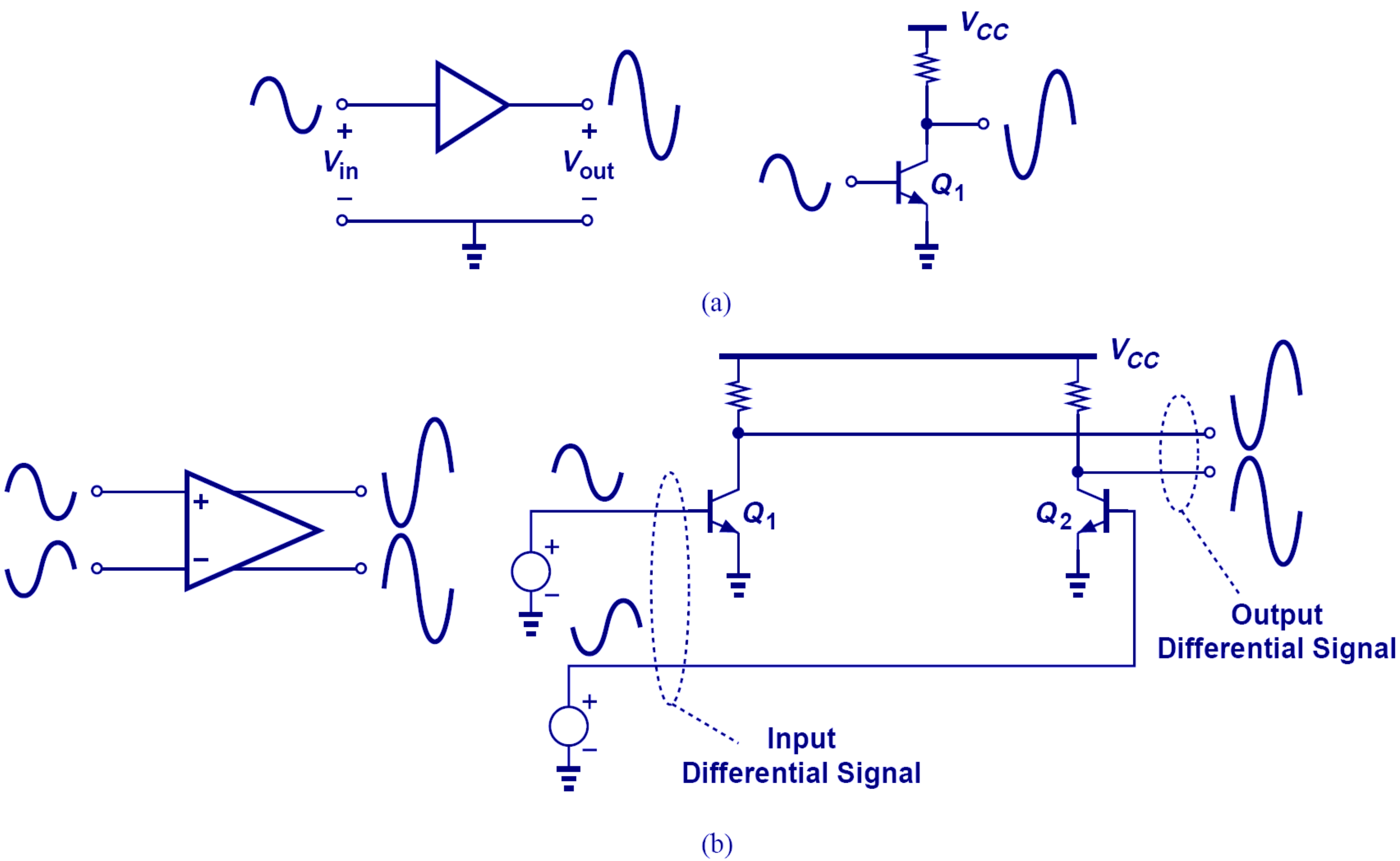
Differential Signals





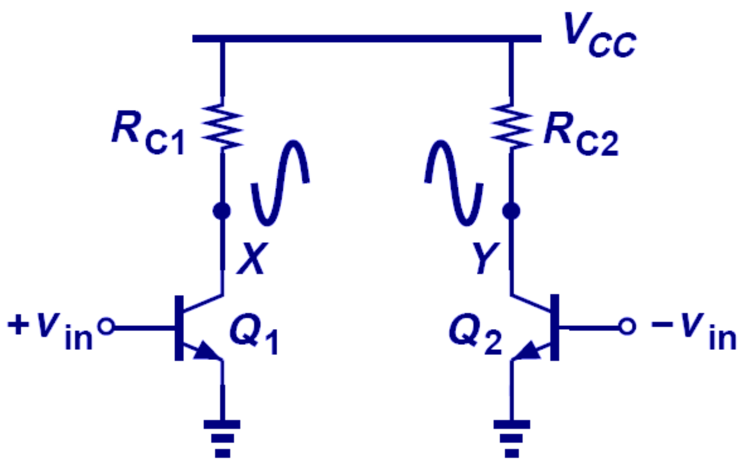
- A pair of differential signals can be generated, among other ways, by a transformer.
- Differential signals have the property that they share the same average value (DC) to ground and AC values are equal in magnitude but opposite in phase.

Single-ended vs. Differential Signals



Example 10.3

➢ **Determine the common-mode level at the output of the circuit shown in Fig. 10.3(b).**



In the absence of signals,

$$V_X = V_Y = V_{CC} - R_C I_C$$

where $R_C = R_{C1} = R_{C2}$ and

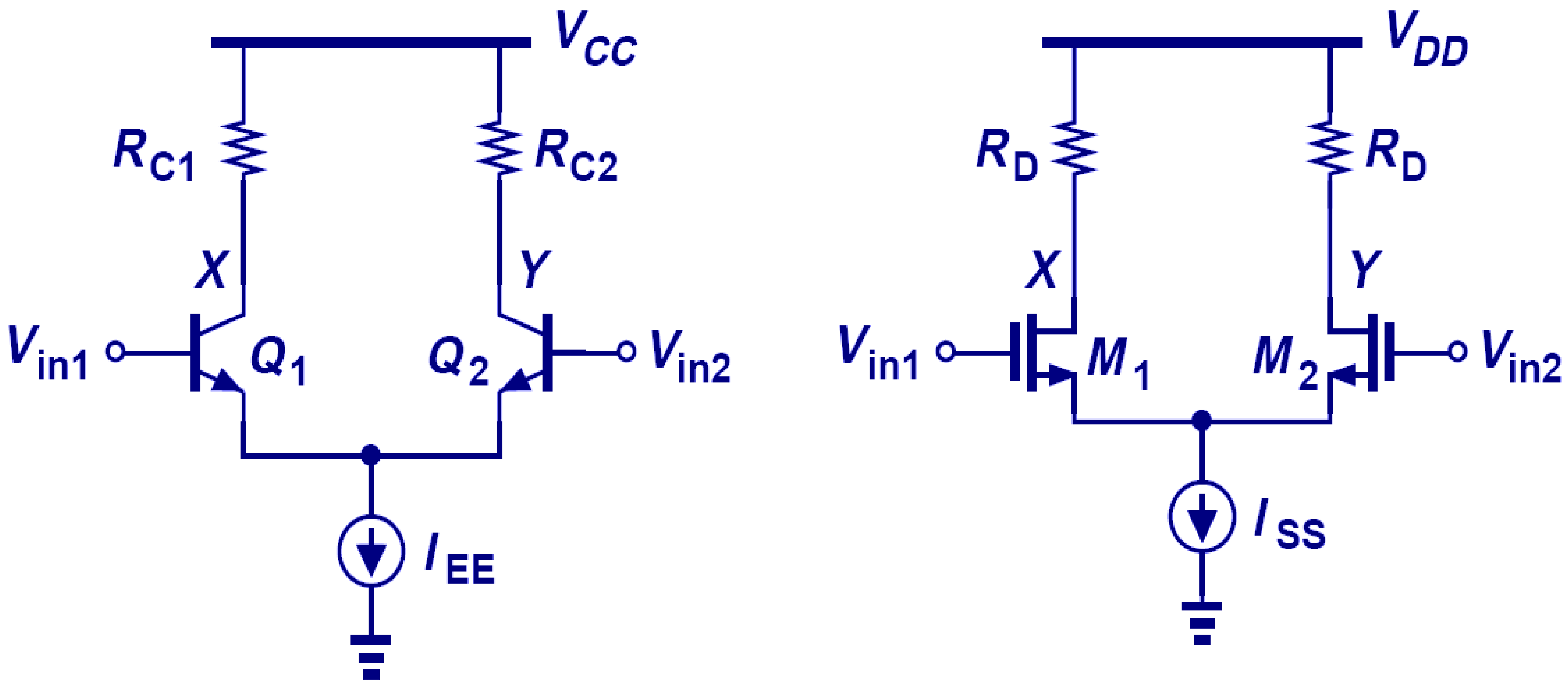
I_C denotes the bias current of Q_1 and Q_2

Thus, $V_{CM} = V_{CC} - R_C I_C$

Interestingly, the ripple affects V_{CM}

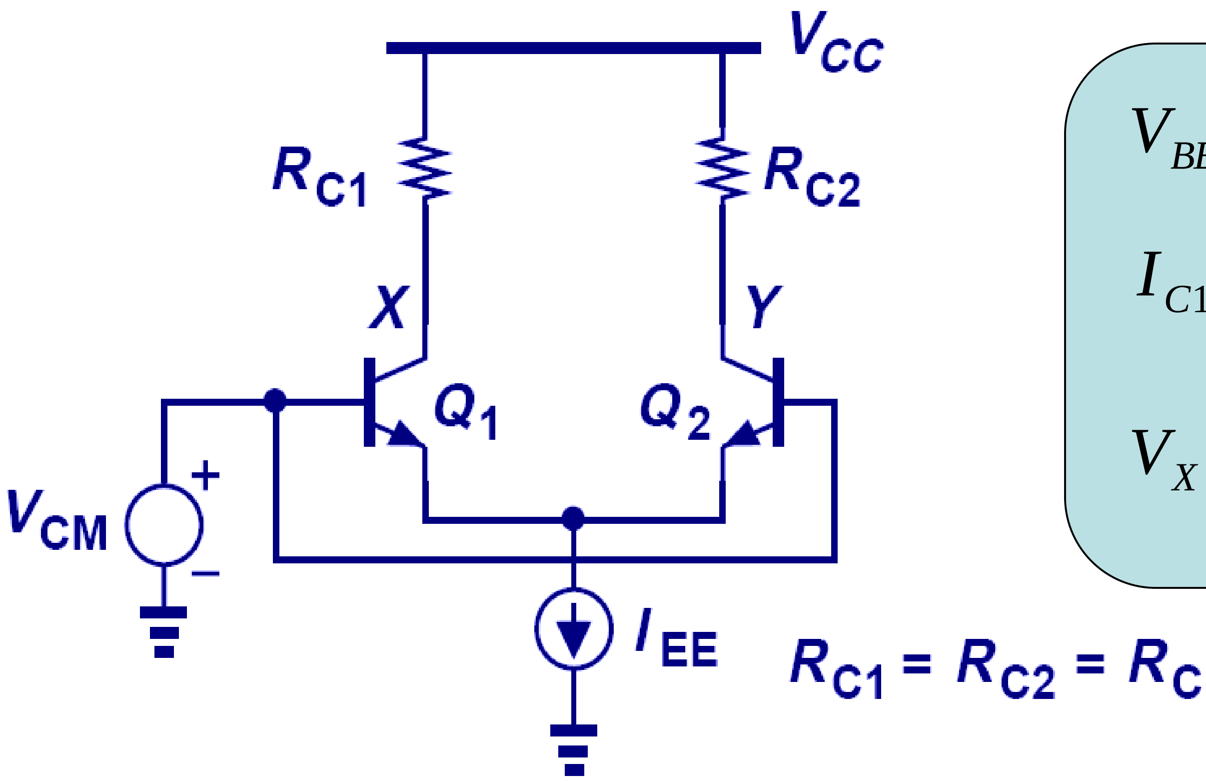
but not the differential output.

Differential Pair



- **With the addition of a tail current, the circuits above operate as an elegant, yet robust differential pair.**

Common-Mode Response



$$V_{BE1} = V_{BE2}$$

$$I_{C1} = I_{C2} = \frac{I_{EE}}{2}$$

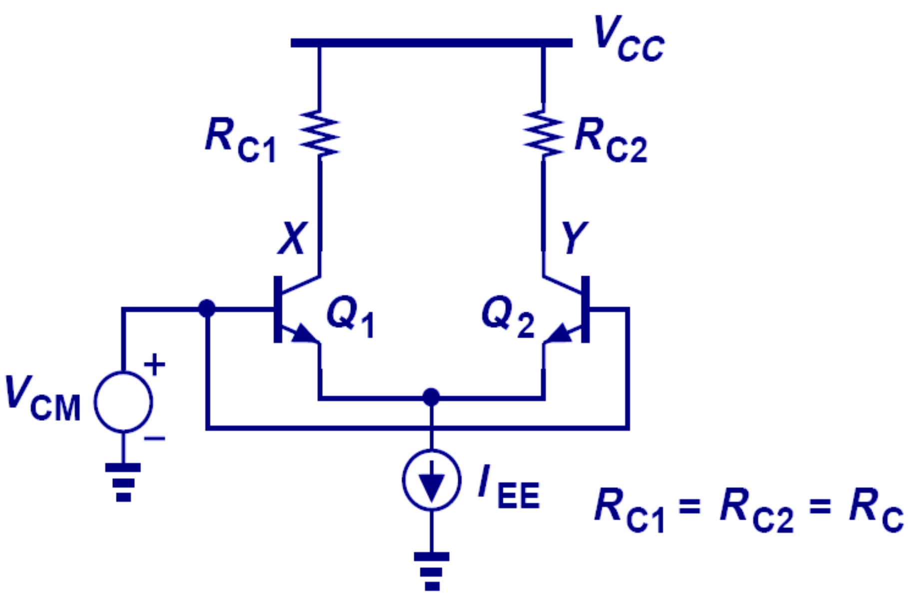
$$V_X = V_Y = V_{CC} - R_C \frac{I_{EE}}{2}$$

To avoid saturation, the collector voltages must not fall below the base voltages:

$$V_{CC} - R_C \frac{I_{EE}}{2} \geq V_{CM}$$

Example 10.4

- **A bipolar differential pair employs a load resistance of 1 kΩ and a tail current of 1 mA. How close to V_{CC} can V_{CM} be chosen?**

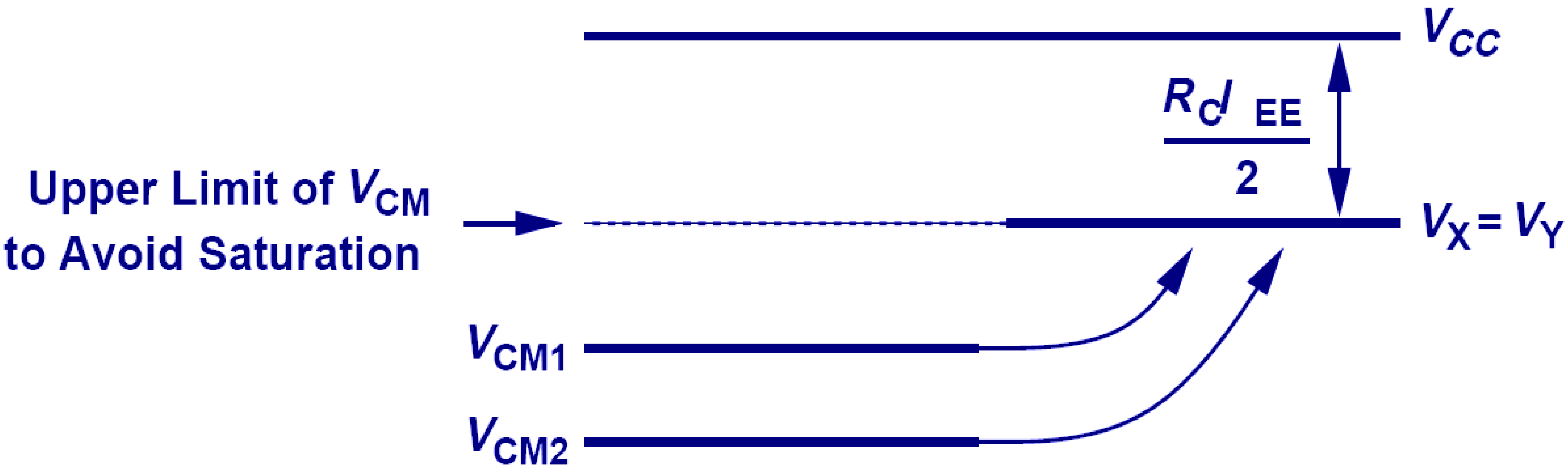


$$V_{CC} - V_{CM} \geq R_C \frac{I_{EE}}{2}$$

$$\geq 0.5\text{V}$$

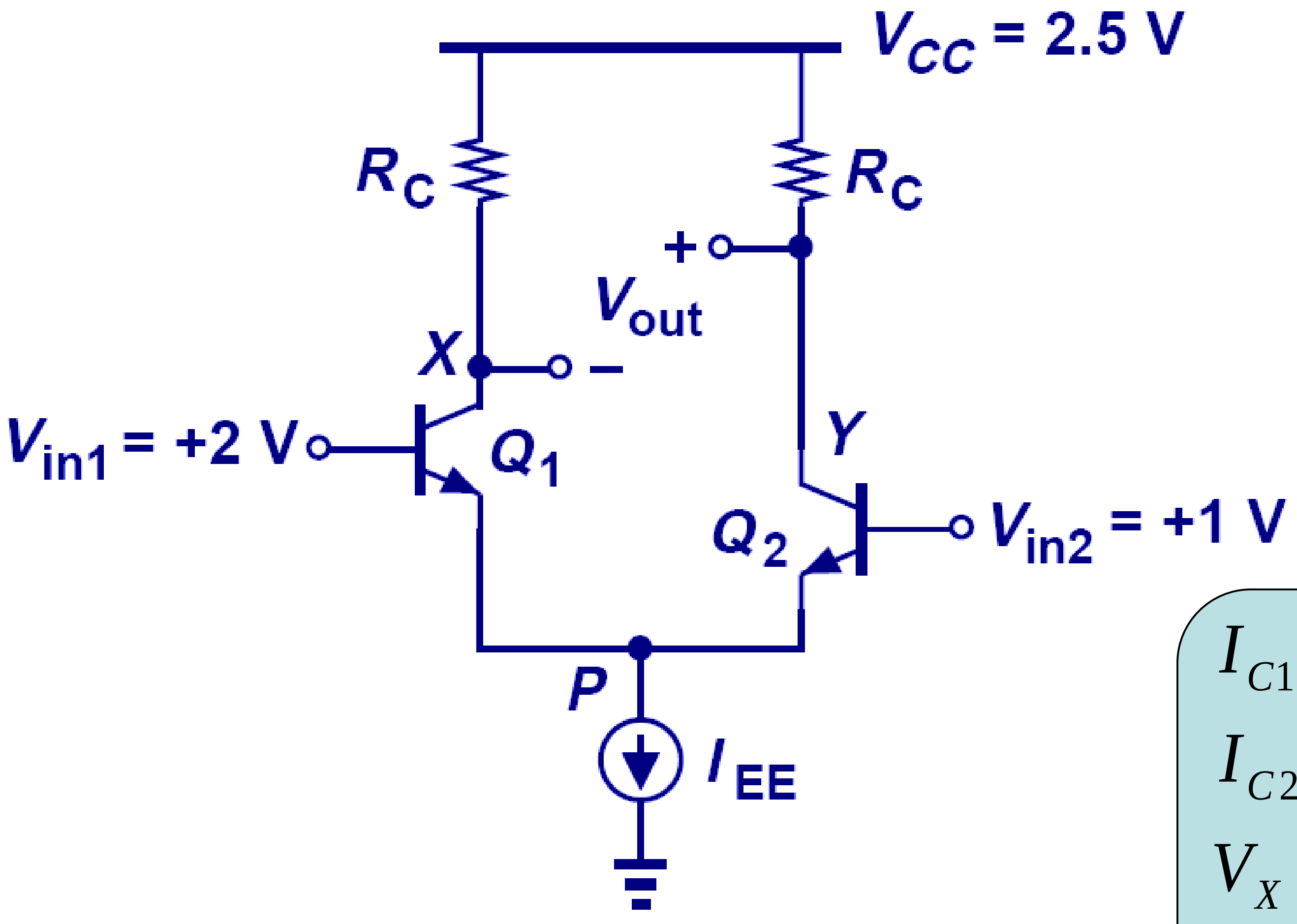
That is, V_{CM} must remain below V_{CC} by at least 0.5 V.

Common-Mode Rejection



- Due to the fixed tail current source, the input common-mode value can vary without changing the output common-mode value.

Differential Response I



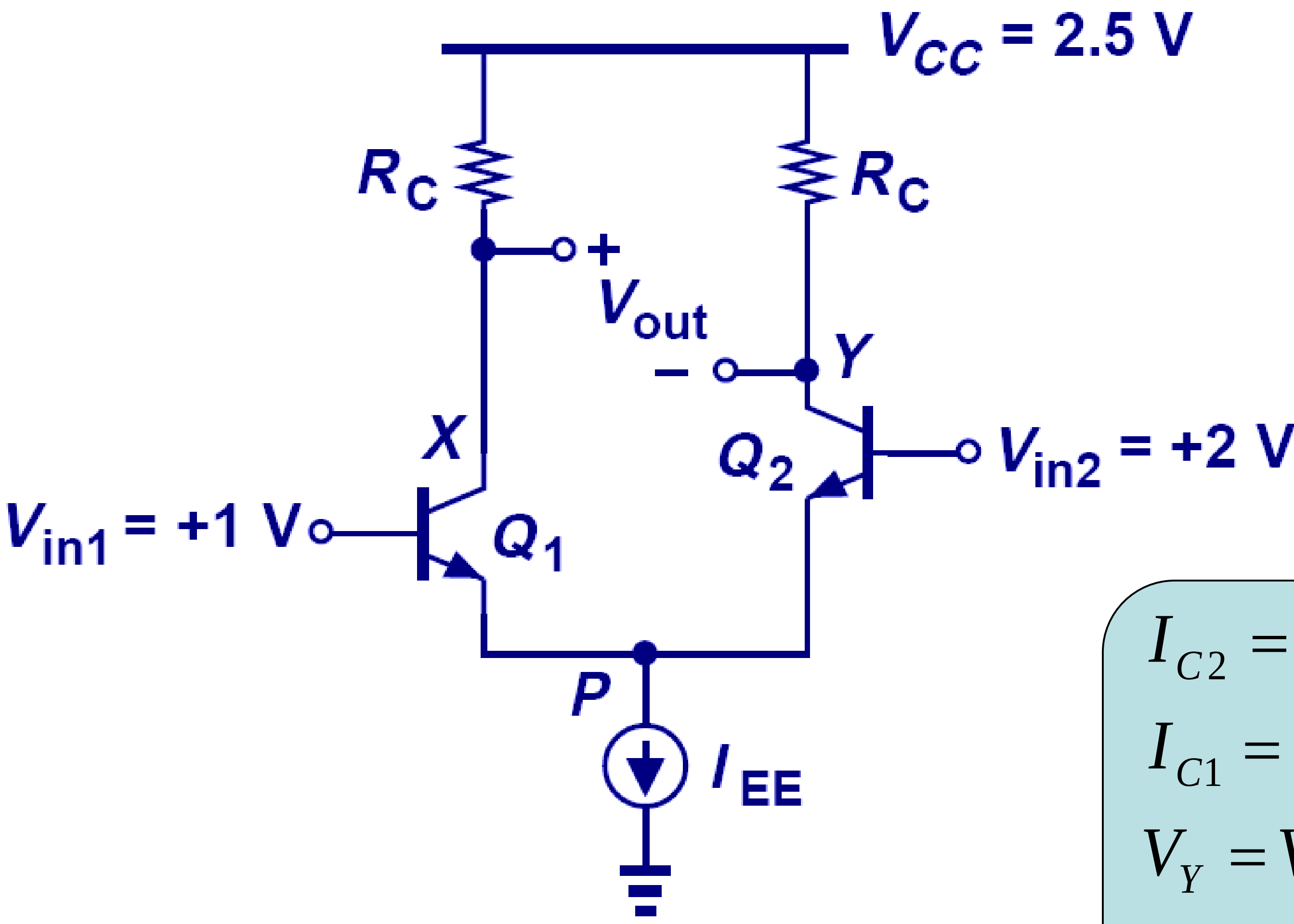
$$I_{C1} = I_{EE}$$

$$I_{C2} = 0$$

$$V_X = V_{CC} - R_C I_{EE}$$

$$V_Y = V_{CC}$$

Differential Response II



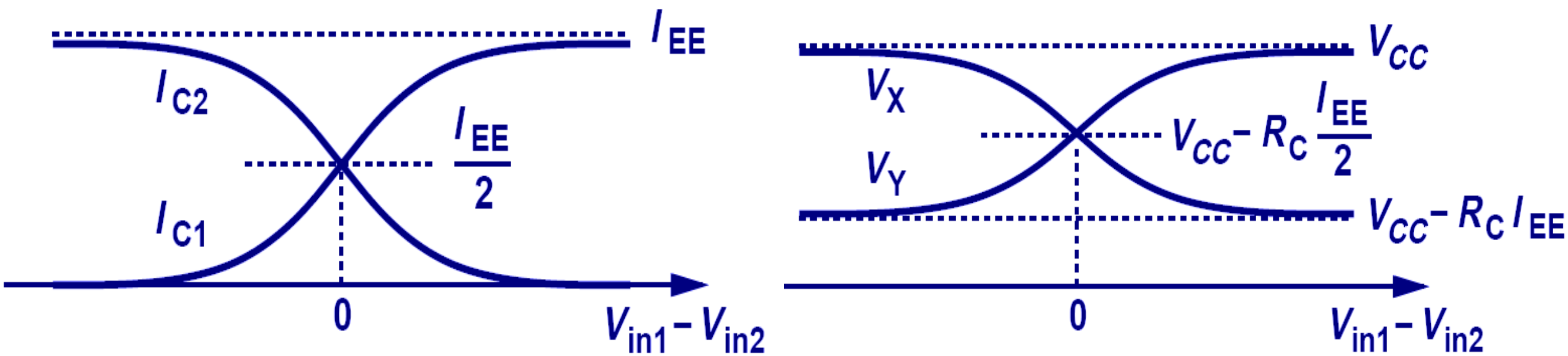
$$I_{C2} = I_{EE}$$

$$I_{C1} = 0$$

$$V_Y = V_{CC} - R_C I_{EE}$$

$$V_X = V_{CC}$$

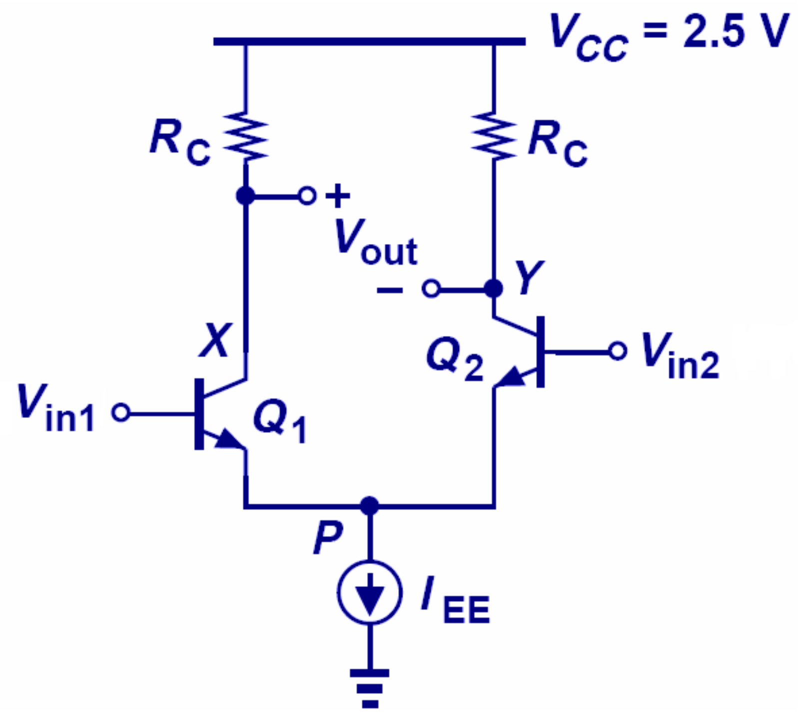
Differential Pair Characteristics



- **None-zero differential input produces variations in output currents and voltages, whereas common-mode input produces no variations.**

Example 10.5

- A bipolar differential pair employs a tail current of 0.5 mA and a collector resistance of 1 kΩ. What is the maximum allowable base voltage if the differential input is large enough to completely steer the tail current? Assume V_{CC}=2.5V.

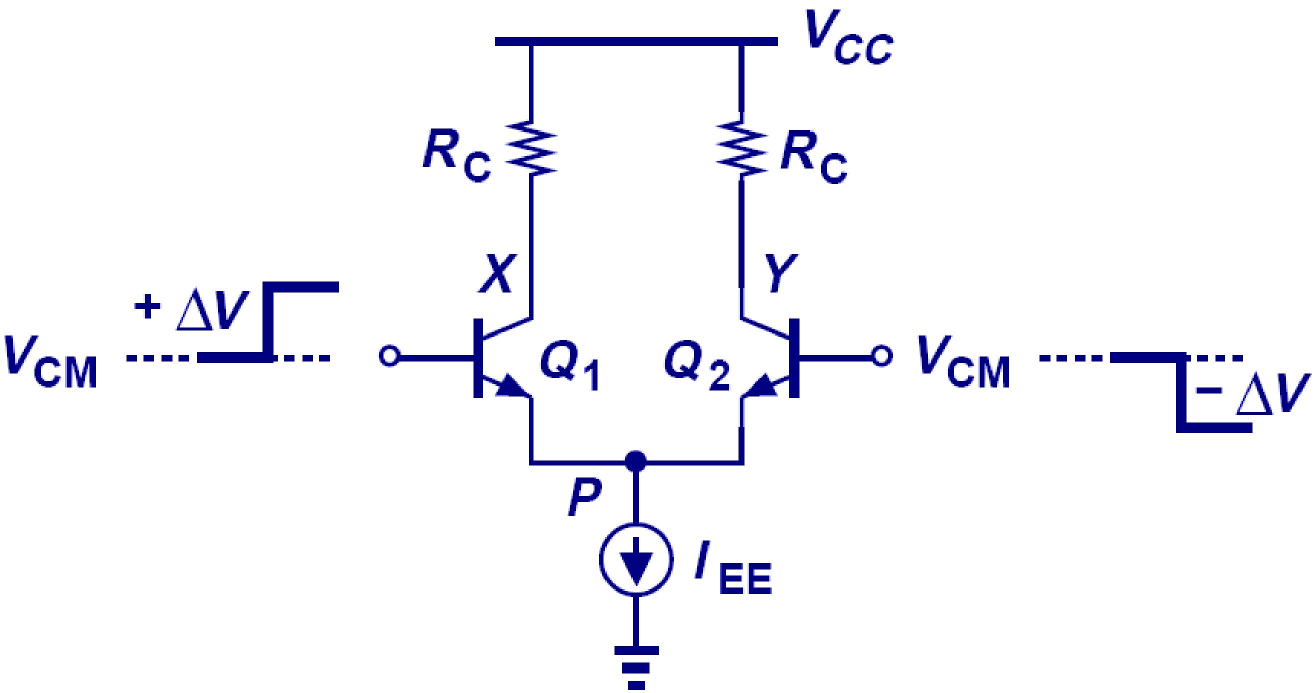


Because I_{EE} is completely steered,

$V_{CC} - R_C I_{EE} = 2\ V$ at one collector.

To avoid saturation, $V_B \leq 2\ V$.

Small-Signal Analysis

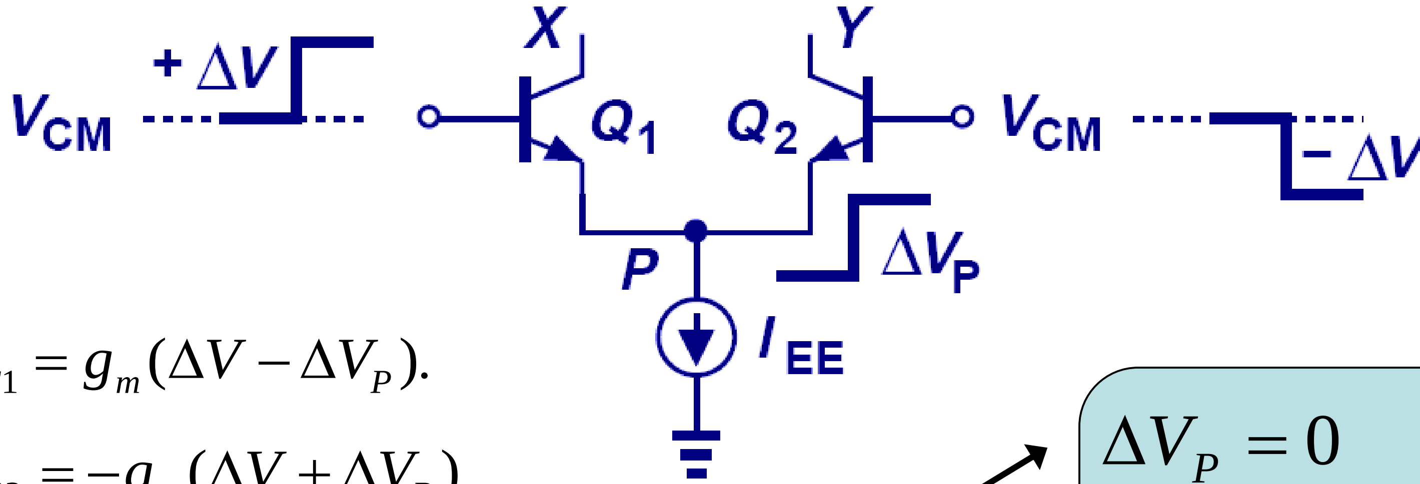


$$I_{C1} = \frac{I_{EE}}{2} + \Delta I$$

$$I_{C2} = \frac{I_{EE}}{2} - \Delta I$$

- Since the input to Q_1 and Q_2 rises and falls by the same amount, and their emitters are tied together, the rise in I_{C1} has the same magnitude as the fall in I_{C2}.

Virtual Ground



$$\Delta I_{C1} = g_m(\Delta V - \Delta V_P).$$

$$\Delta I_{C2} = -g_m(\Delta V + \Delta V_P).$$

$$\Delta I_{C2} + \Delta I_{C1} = 0$$

$$g_m(\Delta V - \Delta V_P) = g_m(\Delta V + \Delta V_P)$$

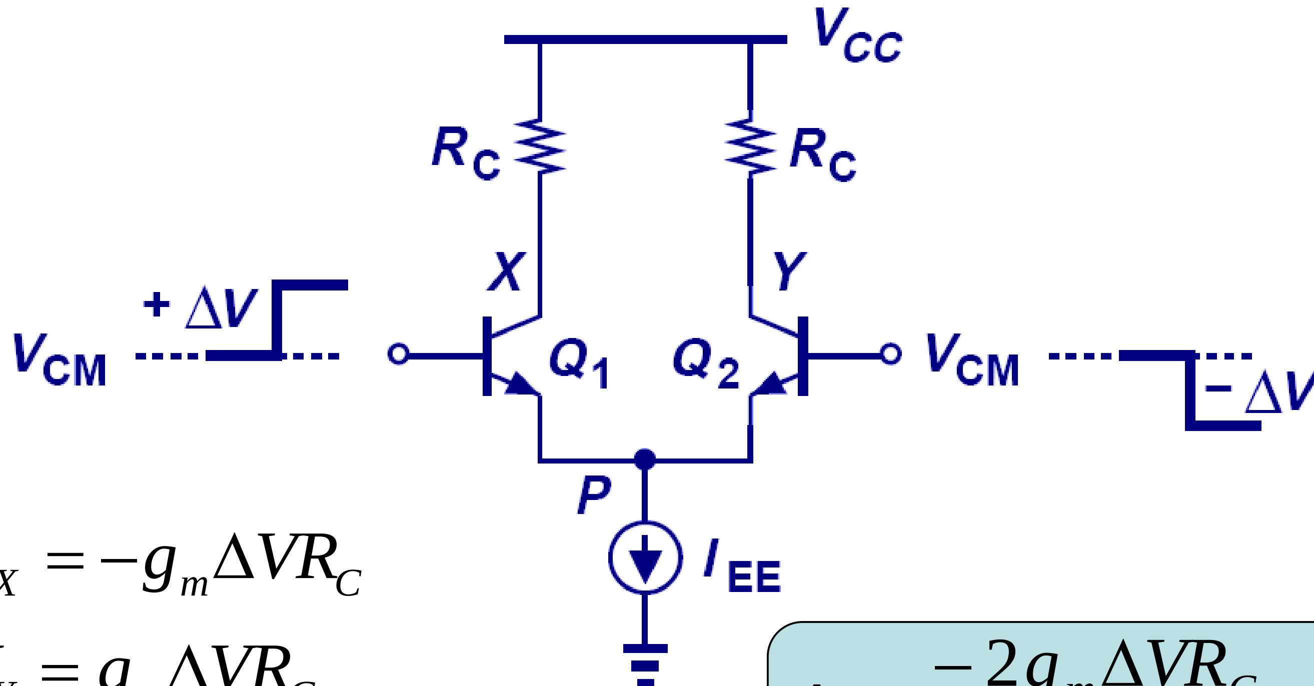
$$\Delta V_P = 0$$

$$\Delta I_{C1} = g_m \Delta V$$

$$\Delta I_{C2} = -g_m \Delta V$$

- **For small changes at inputs, the g_m's are the same, and the respective increase and decrease of I_{C1} and I_{C2} are the same, node P must stay constant to accommodate these changes. Therefore, node P can be viewed as AC ground.**

Small-Signal Differential Gain



$$\Delta V_X = -g_m \Delta V R_C$$

$$\Delta V_Y = g_m \Delta V R_C$$

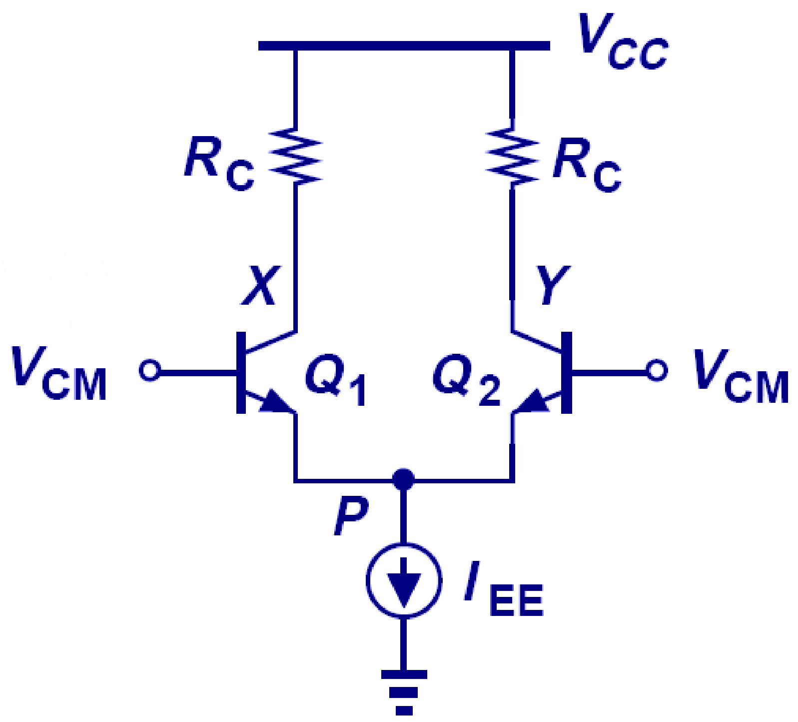
$$\Delta V_X - \Delta V_Y = -2 g_m \Delta V R_C$$

$$A_v = \frac{-2 g_m \Delta V R_C}{2\Delta V} = -g_m R_C$$

- **Since the output changes by $-2g_m\Delta VR_C$ and input by $2\Delta V$, the small signal gain is $-g_mR_C$, similar to that of the CE stage. However, to obtain same gain as the CE stage, power dissipation is doubled.**

Example 10.6

- Design a bipolar differential pair for a gain of 10 and a power budget of 1mW with a supply voltage of 2V.



$$V_{CC} = 2\text{ V}$$

$$\Rightarrow I_{EE} = \frac{1\text{ mW}}{2\text{ V}} = 0.5\text{ mA}$$

$$\Rightarrow g_m = \frac{I_C}{V_T} = \frac{I_{EE}/2}{V_T} = \frac{0.25\text{ mA}}{26\text{ mV}} = \frac{1}{104\ \Omega}$$

$$\Rightarrow R_C = \frac{|A_v|}{g_m} = 1040\ \Omega$$

Example 10.7

- Compare the power dissipation of a bipolar differential pair with that of a CE stage if both circuits are designed for equal voltage gains, collector resistances, and supply voltages.

Differential pair

$$|A_{V,\text{diff}}| = g_{m1,2}R_C$$

CE stage

$$|A_{V,CE}| = g_m R_C$$

$$g_{m1,2}R_C = g_m R_C$$

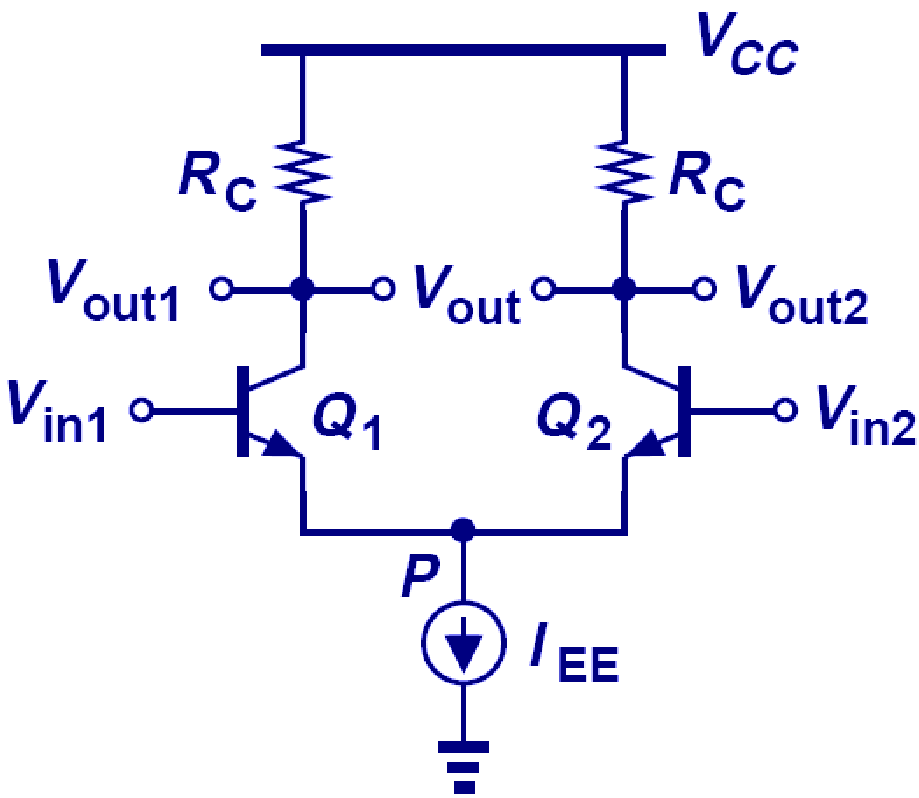
$$\frac{I_{EE}}{2V_T} = \frac{I_C}{V_T}$$

$$I_{EE} = 2I_C$$

$$P_{D,diff} = V_C I_{EE} = 2V_C I_C$$

$$P_{D,CE} = V_C I_C$$

Large Signal Analysis



$$V_{in1} - V_{in2} = V_{BE1} - V_{BE2}$$

$$= V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{C2}}{I_{S2}}$$

$$\text{and} \quad I_{C1} + I_{C2} = I_{EE}$$

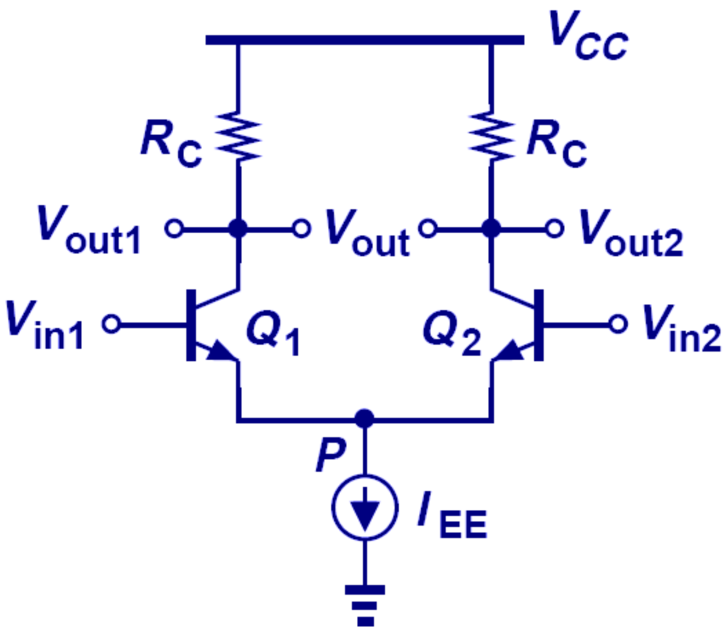
$$\Rightarrow I_{C2} \exp \frac{V_{in1} - V_{in2}}{V_T} + I_{C2} = I_{EE}$$

$$\Rightarrow I_{C2} = \frac{I_{EE}}{1 + \exp \frac{V_{in1} - V_{in2}}{V_T}}$$

$$\Rightarrow I_{C1} = \frac{I_{EE} \exp \frac{V_{in1} - V_{in2}}{V_T}}{1 + \exp \frac{V_{in1} - V_{in2}}{V_T}}$$

Example 10.8

- **Determine the differential input voltage that steers 98% of the tail current to one transistor.**



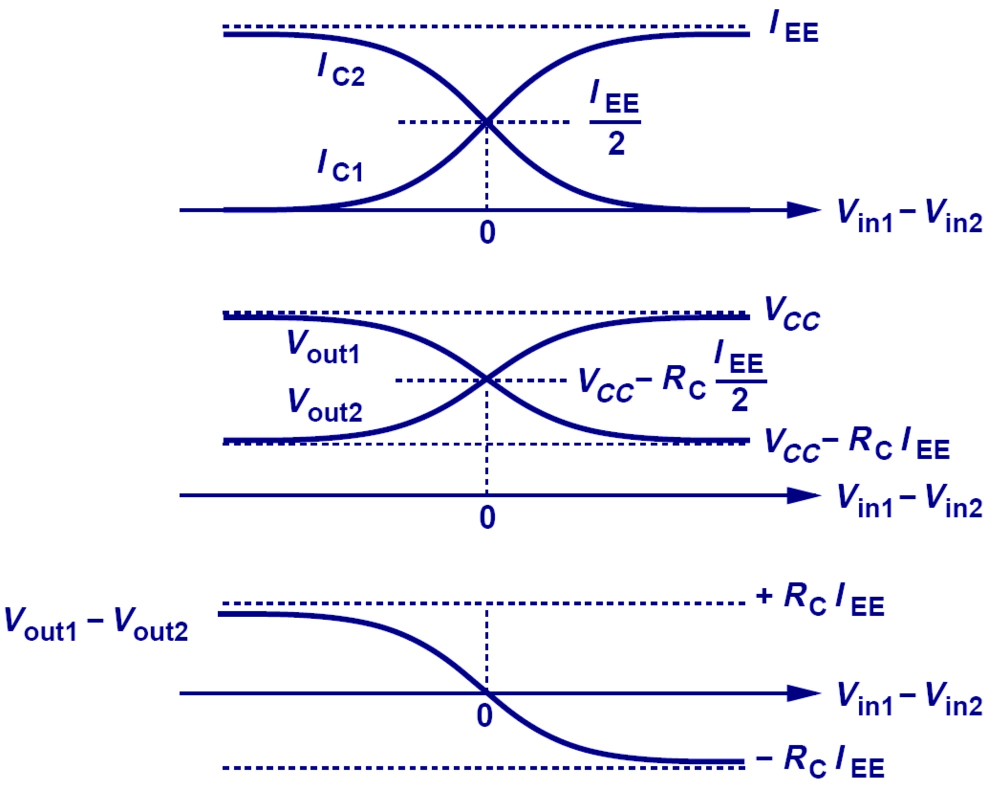
$$I_{C1} = 0.02 I_{EE}$$

$$\approx I_{EE} \exp \frac{V_{in1} - V_{in2}}{V_T}$$

$$V_{in1} - V_{in2} \approx -3.91 \cdot V_T.$$

We often say a differential input of $4 \cdot V_T$ is sufficient to turn one side of the bipolar pair nearly off.

Input/Output Characteristics



$$V_{out1} = V_{CC} - R_C I_{C1}$$

$$= V_{CC} - R_C \frac{I_{EE} \exp \frac{V_{in1} - V_{in2}}{V_T}}{1 + \exp \frac{V_{in1} - V_{in2}}{V_T}}$$

$$V_{out2} = V_{CC} - R_C I_{C2}$$

$$= V_{CC} - R_C \frac{I_{EE}}{1 + \exp \frac{V_{in1} - V_{in2}}{V_T}}$$

$$V_{out1} - V_{out2} = R_C I_{EE} \frac{1 - \exp \frac{V_{in1} - V_{in2}}{V_T}}{1 + \exp \frac{V_{in1} - V_{in2}}{V_T}}$$

$$= -R_C I_{EE} \tanh \frac{V_{in1} - V_{in2}}{2 \cdot V_T}$$

Example 10.9

- Sketch the output waveforms of the bipolar differential pair in Fig. 10.14(a) in response to the sinusoidal inputs shown in Figs. 10.14(b) and (c). Assume Q_1 and Q_2 remain in the forward active region.

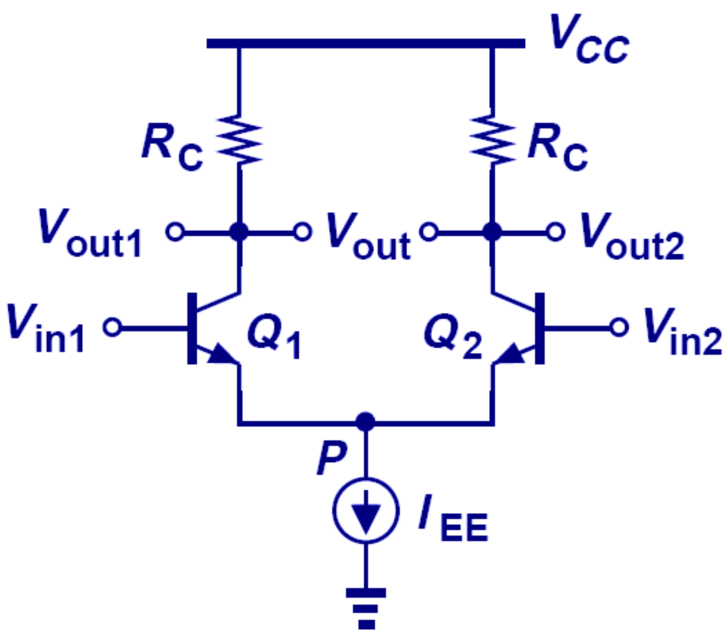
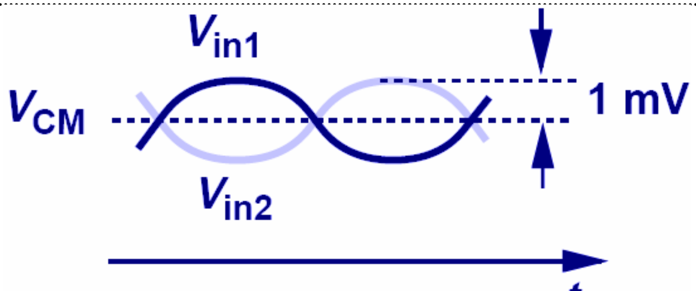
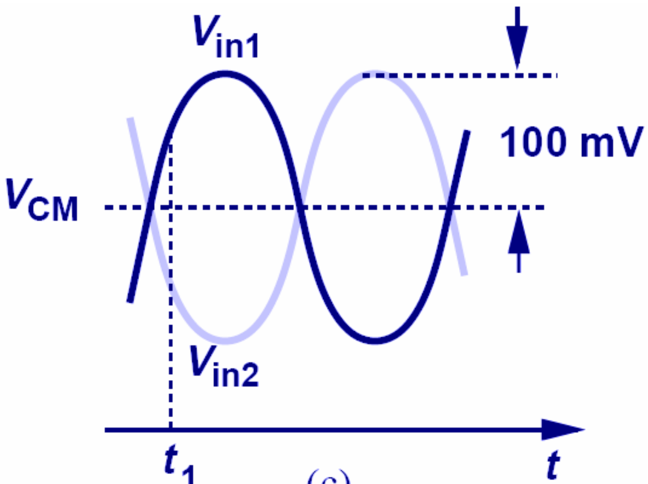


Figure10.14 (a)

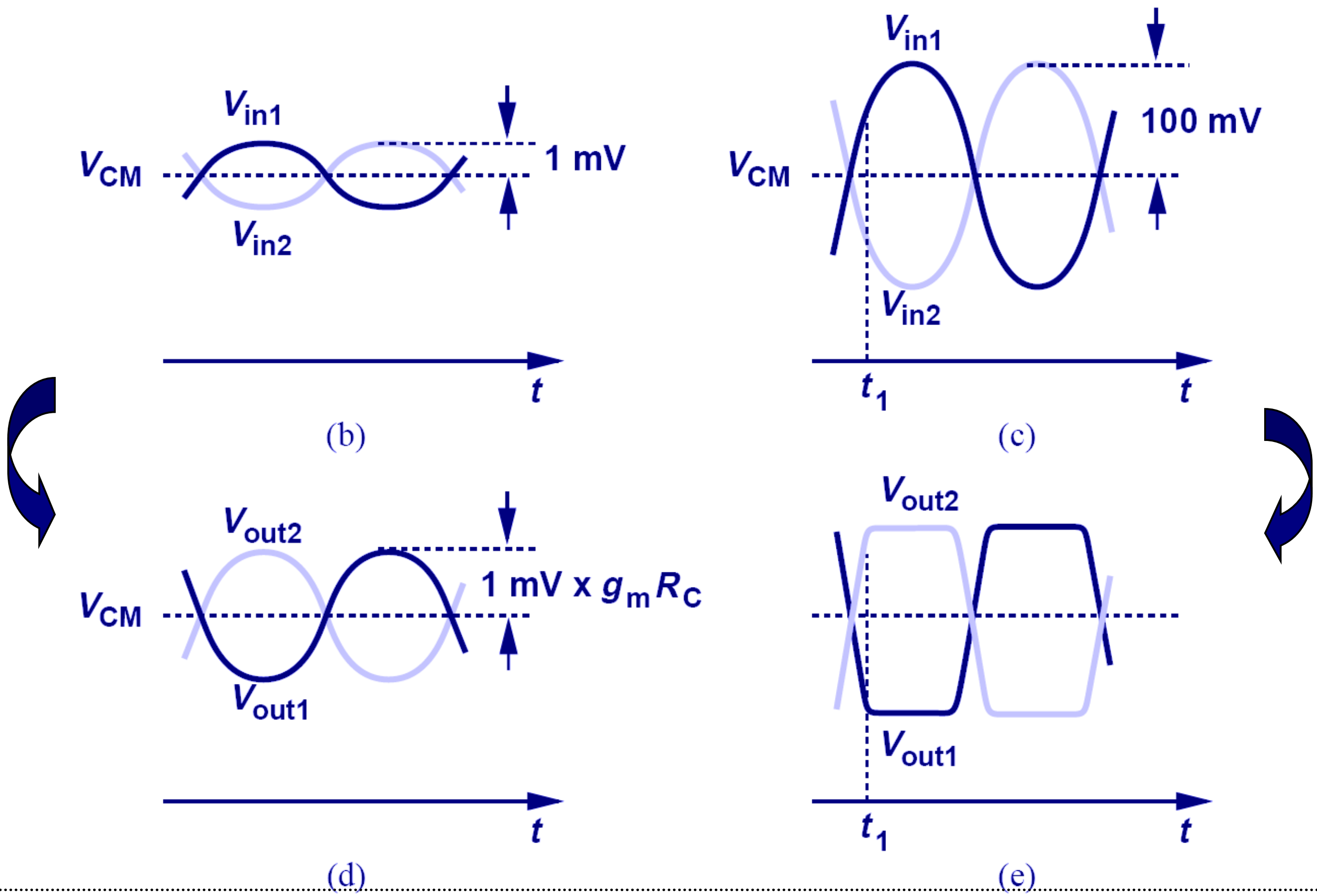


(b)



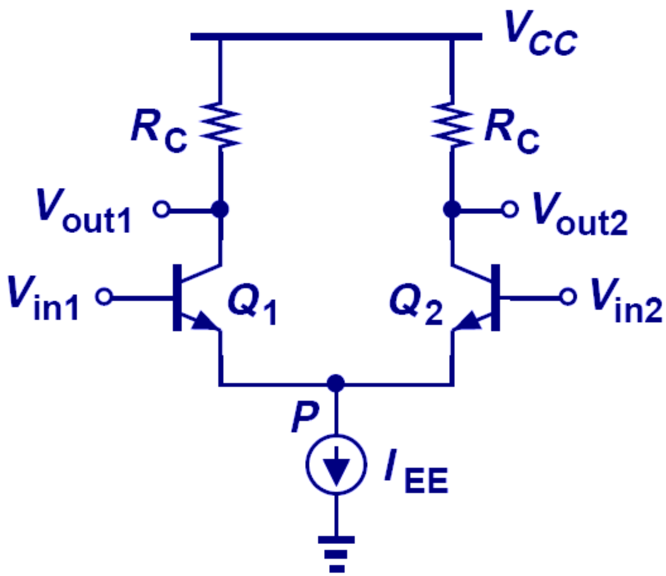
(c)

Example 10.9 (cont'd)



- **The left column operates in linear region (small-signal), whereas the right column operates in nonlinear region (large-signal).**

Small-Signal Model



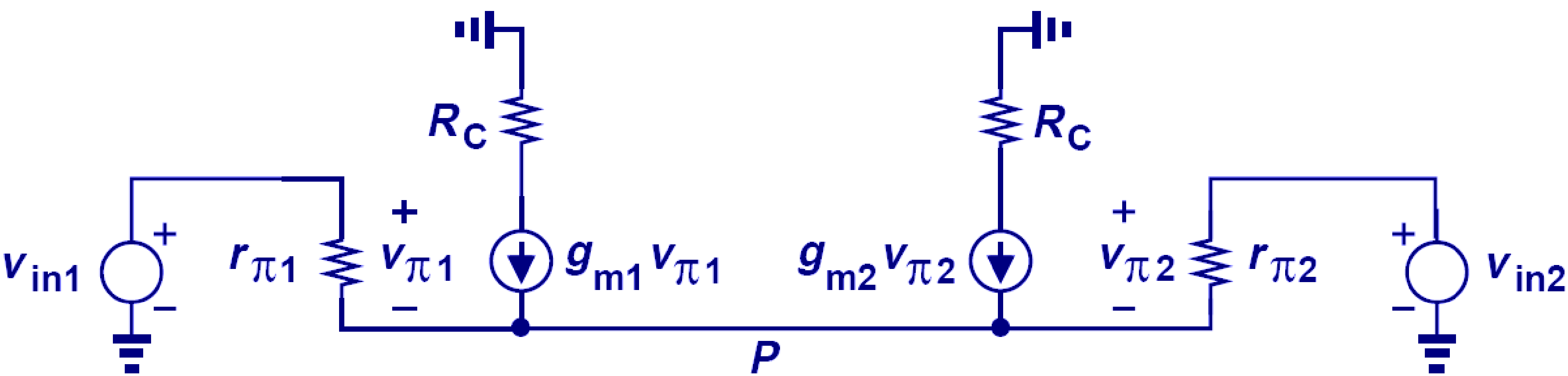
$$v_{in1} - v_{\pi 1} = v_P = v_{in2} - v_{\pi 2}$$

$$\frac{v_{\pi 1}}{r_{\pi 1}} + g_{m1} v_{\pi 1} + \frac{v_{\pi 2}}{r_{\pi 2}} + g_{m2} v_{\pi 2} = 0.$$

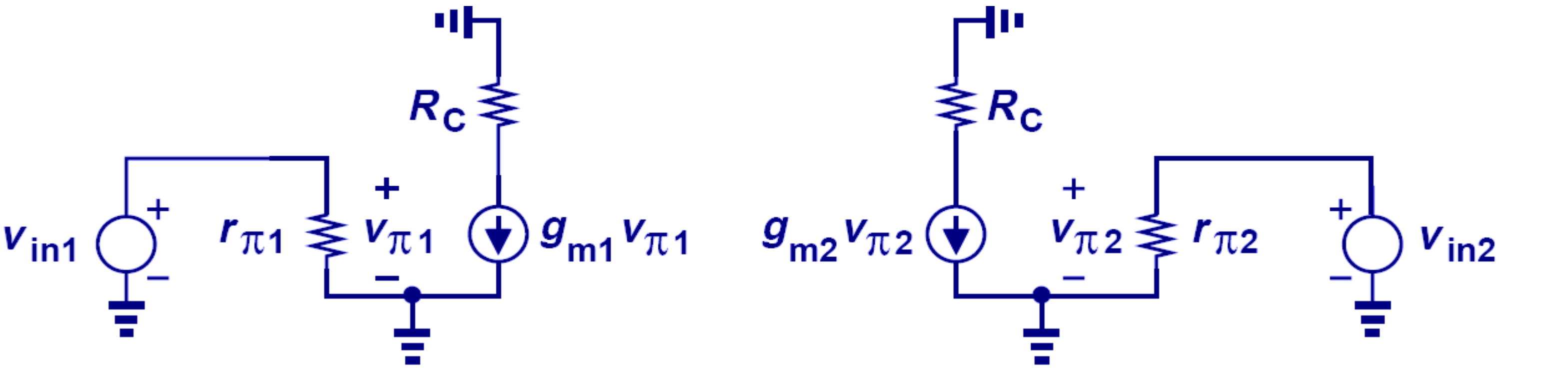
With $r_{\pi 1} = r_{\pi 2}$ and $g_{m1} = g_{m2}$ $\quad v_{\pi 1} = -v_{\pi 2}$

Since $v_{in1} = -v_{in2}$, $2v_{in1} = 2v_{\pi 1}$.

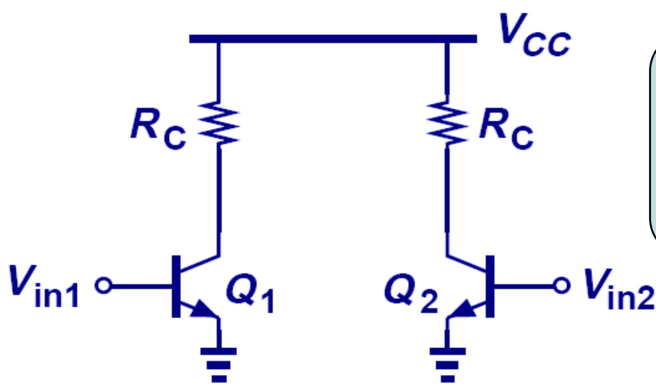
$$\therefore v_P = v_{in1} - v_{\pi 1} = 0$$



Half Circuits



(b)



(c)

$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m R_C$$

- **Since V_P is grounded, we can treat the differential pair as two CE "half circuits", with its gain equal to one half circuit's single-ended gain.**

Example 10.10

- Compute the differential gain of the circuit shown in Fig. 10.16(a), where ideal current sources are used as loads to maximize the gain.

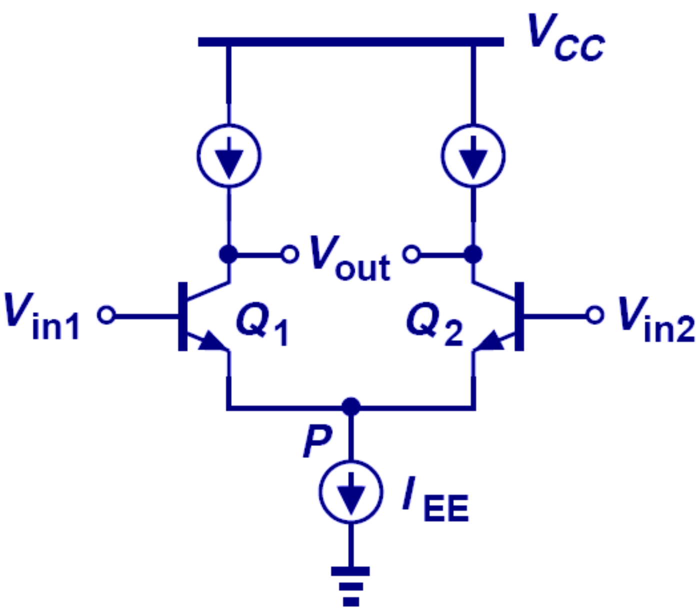
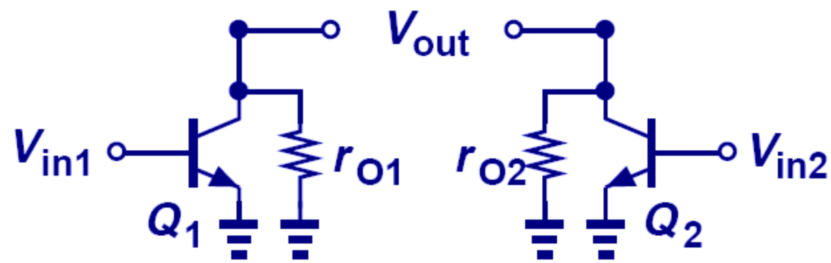


Figure10.16 (a)



$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m r_O$$

Example 10.11

- Figure 10.17(a) illustrates an implementation of the topology shown in Fig. 10.16(a). Calculate the differential voltage gain.

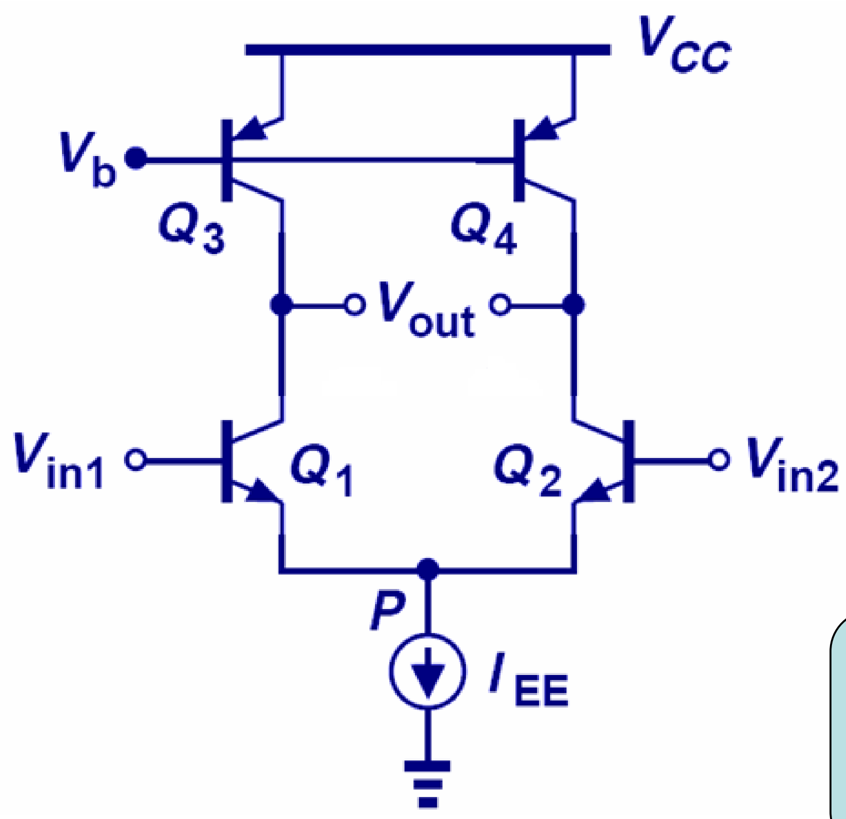
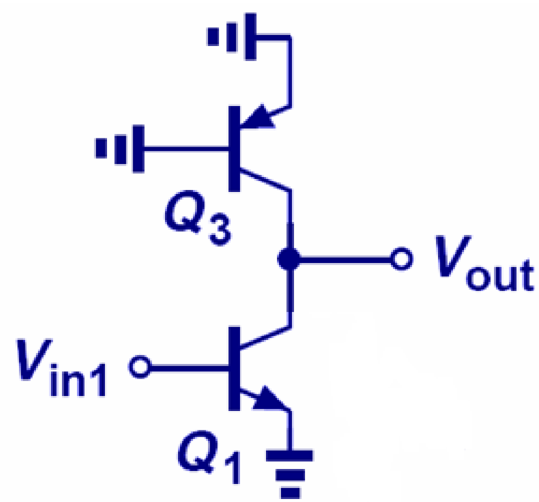
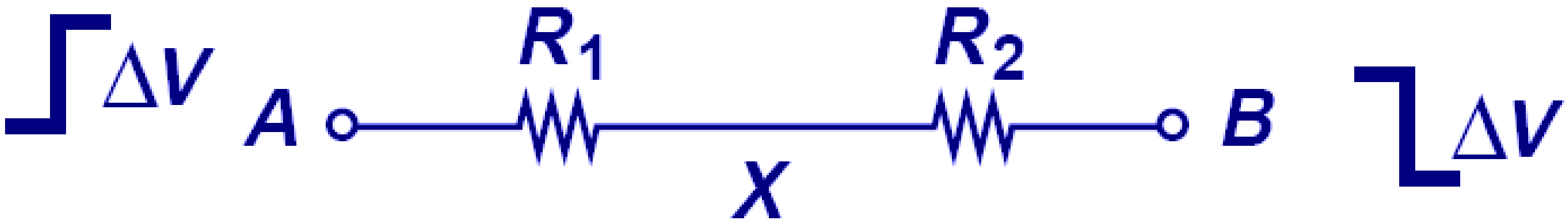


Figure10.17 (a)



$$\frac{v_{out1}-v_{out2}}{v_{in1}-v_{in2}}=-g_m\left(r_{ON}\|r_{OP}\right)$$

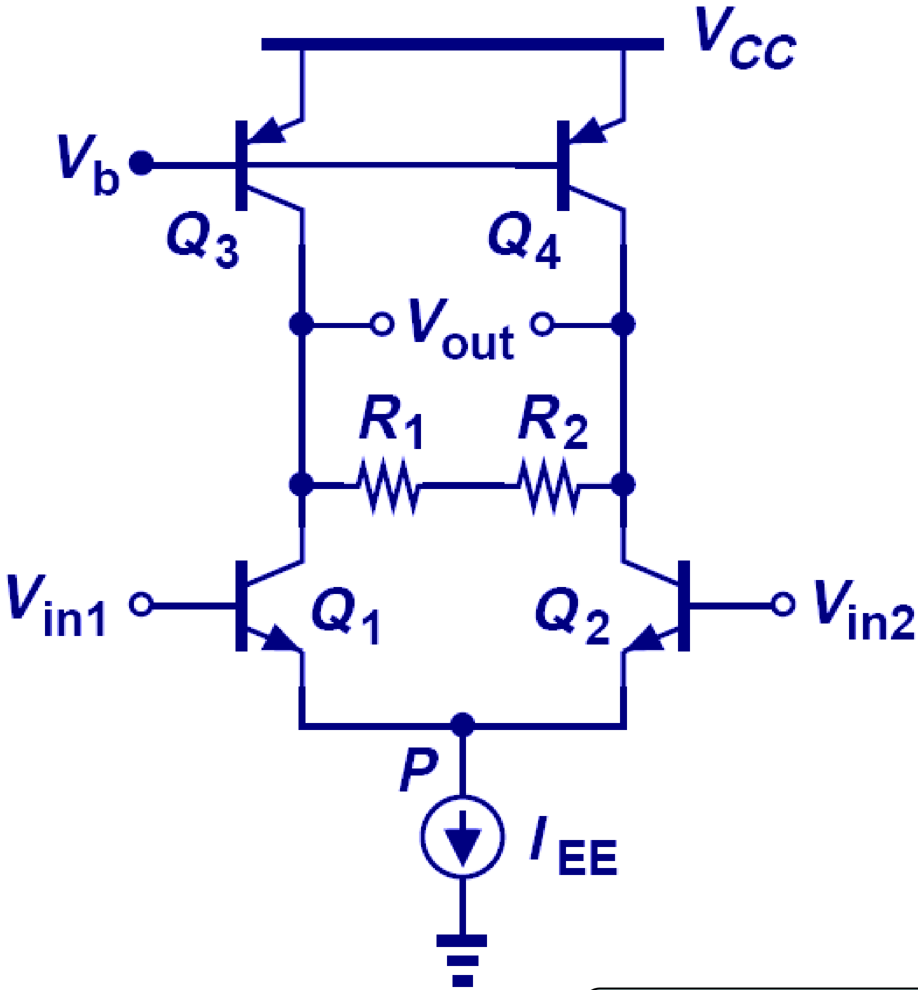
Extension of Virtual Ground

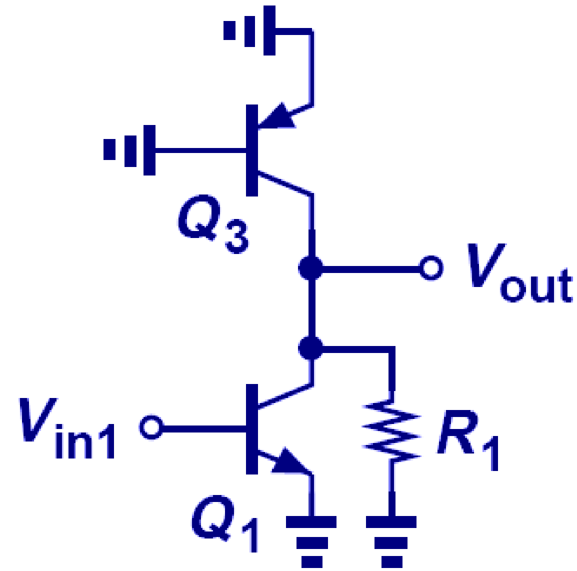


$$V_X = 0$$

- **It can be shown that if $R_1 = R_2$, and points A and B go up and down by the same amount respectively, V_X does not move. This property holds for any other node that appears on the axis of symmetry.**

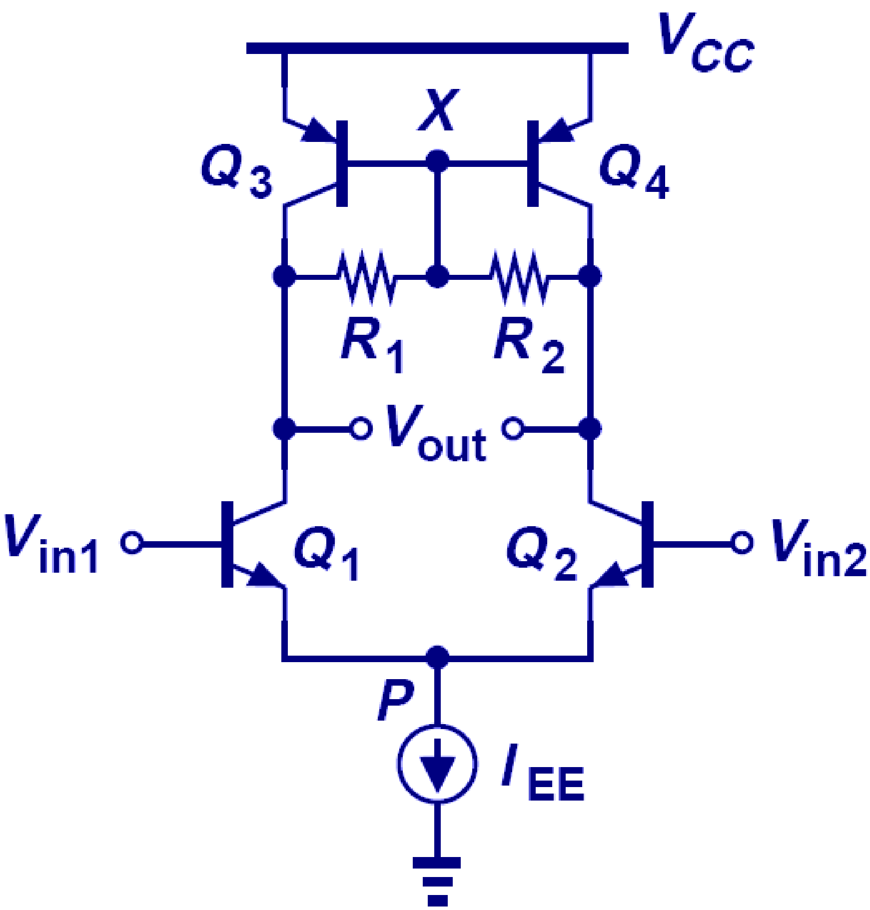
Half Circuit Example I

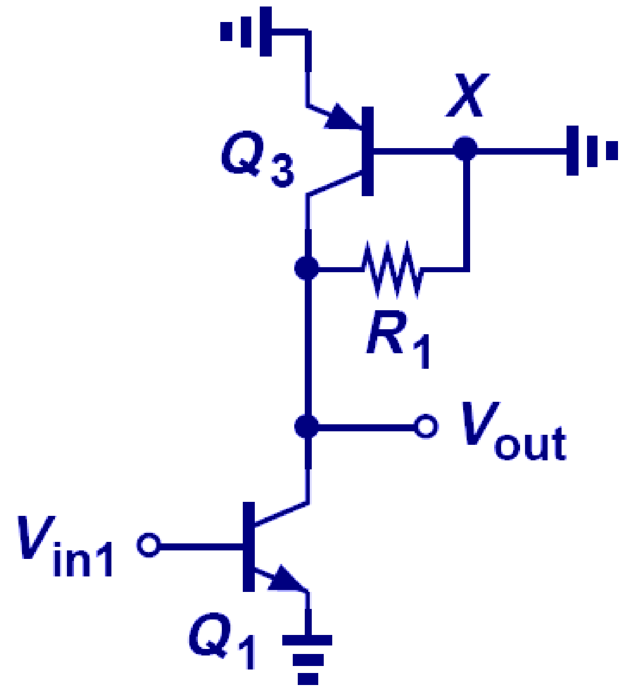




$$A_v = -g_{m1}\left(r_{O1} \,||\, r_{O3} \,||\, R_1\right)$$

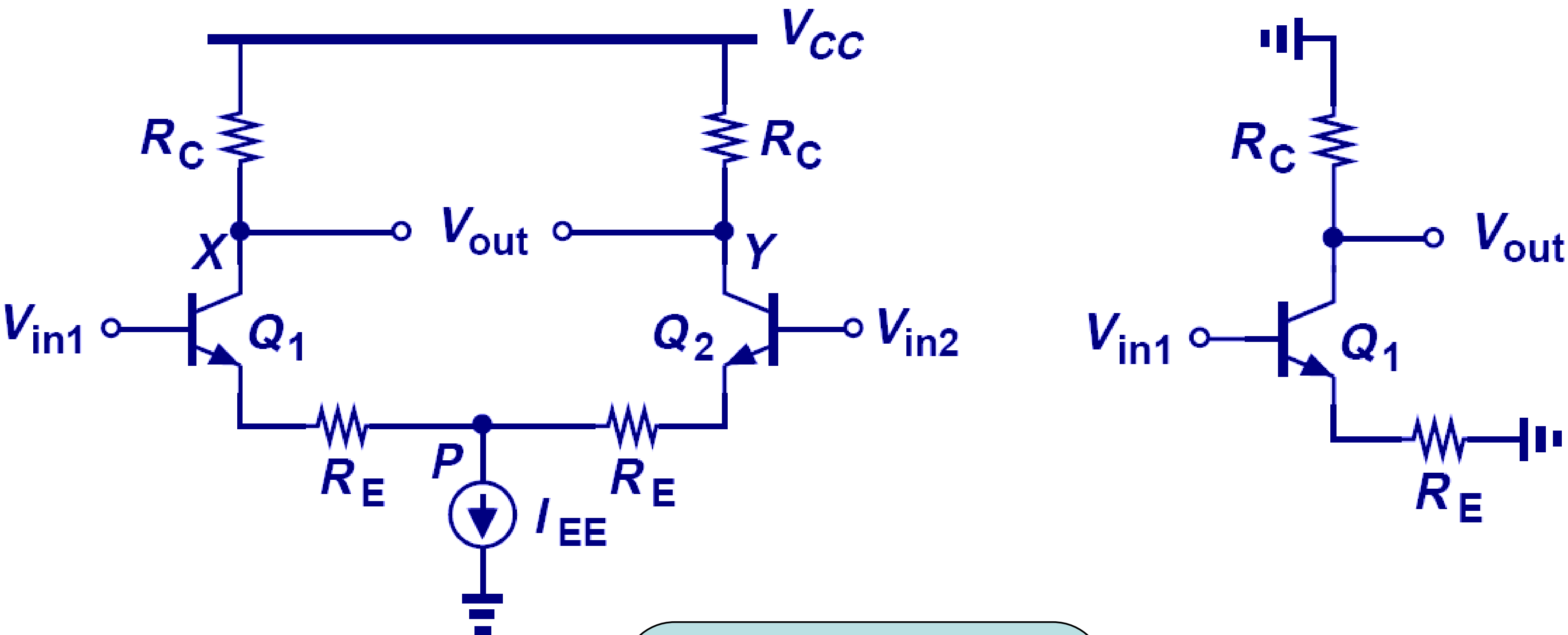
Half Circuit Example II





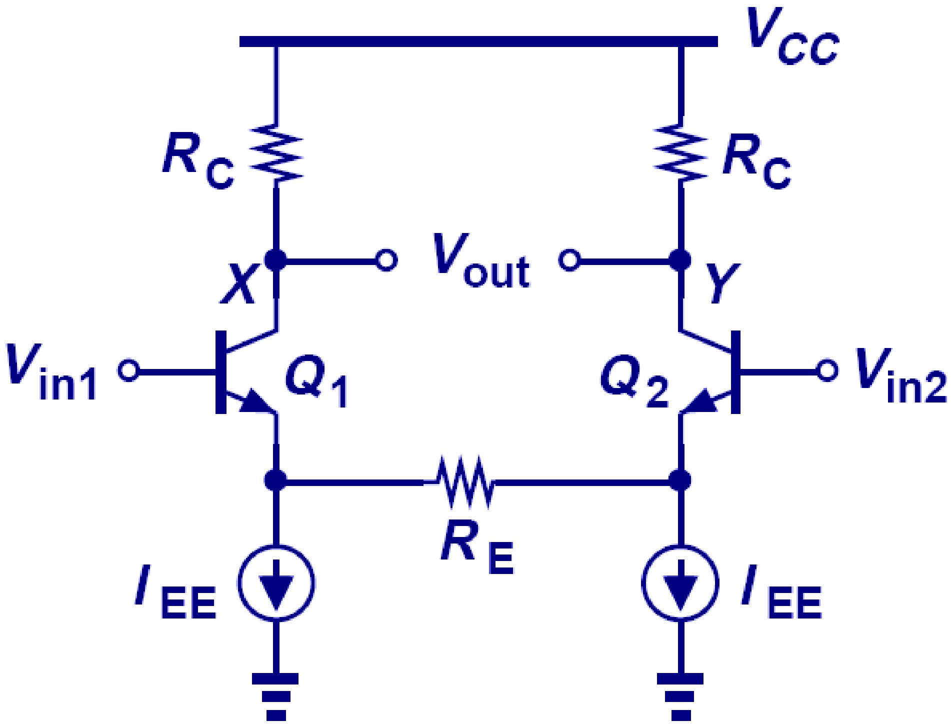
$$A_v = -g_{m1}\left(r_{O1} \| r_{O3} \| R_1\right)$$

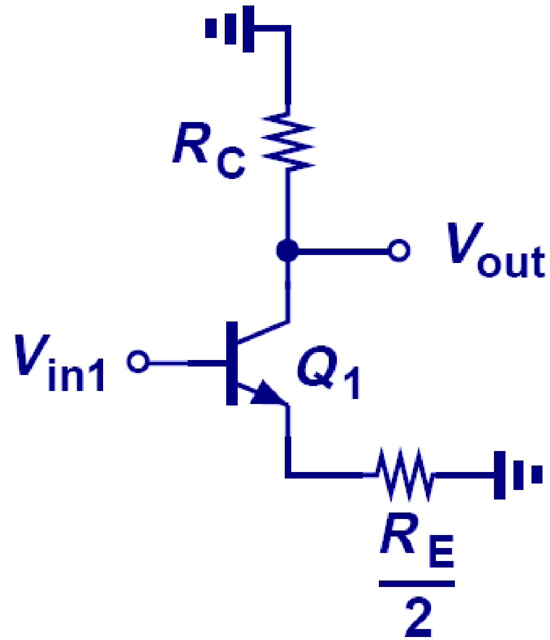
Half Circuit Example III



$$A_v = -\frac{R_C}{R_E + \frac{1}{g_m}}$$

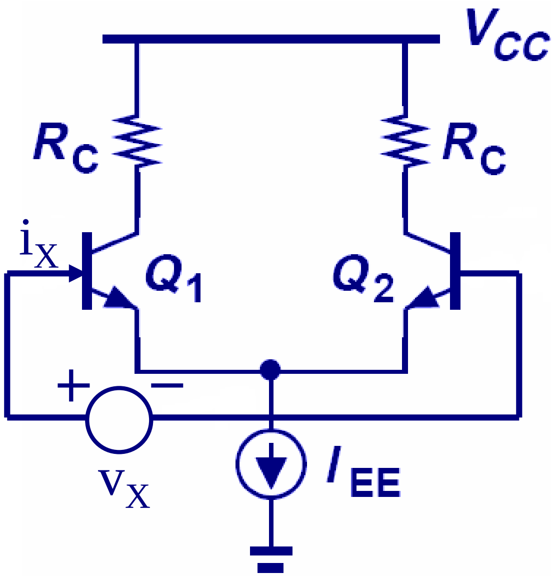
Half Circuit Example IV





$$A_v = -\frac{R_C}{\frac{R_E}{2} + \frac{1}{g_m}}$$

I/O Impedances

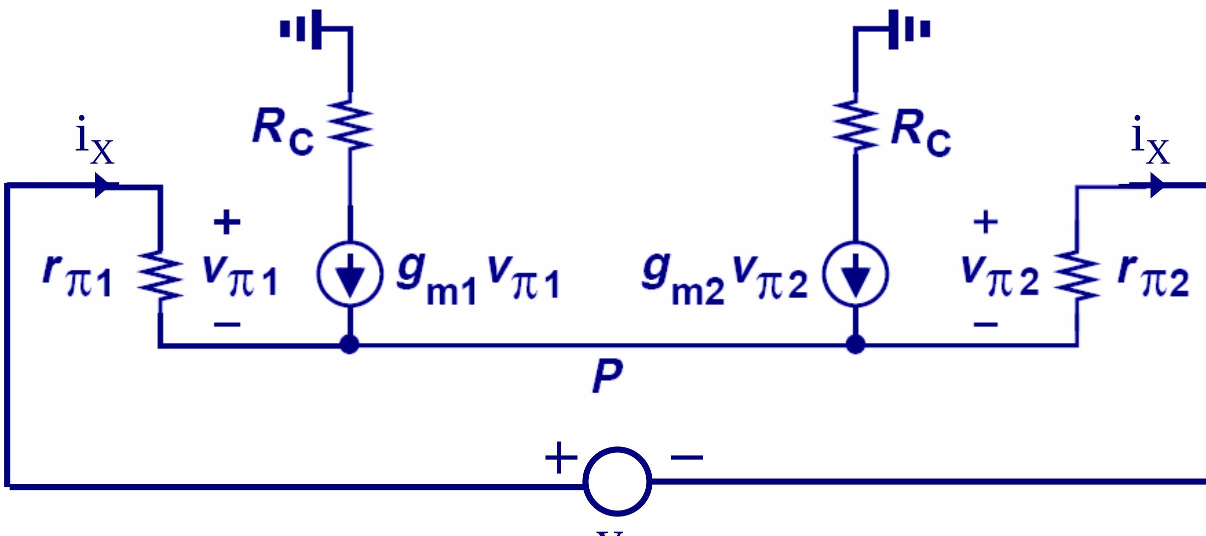


$$\frac{v_{\pi 1}}{r_{\pi 1}} = i_X = -\frac{v_{\pi 2}}{r_{\pi 2}}$$

$$v_X = v_{\pi 1} - v_{\pi 2}$$

$$= 2 r_{\pi 1} i_X$$

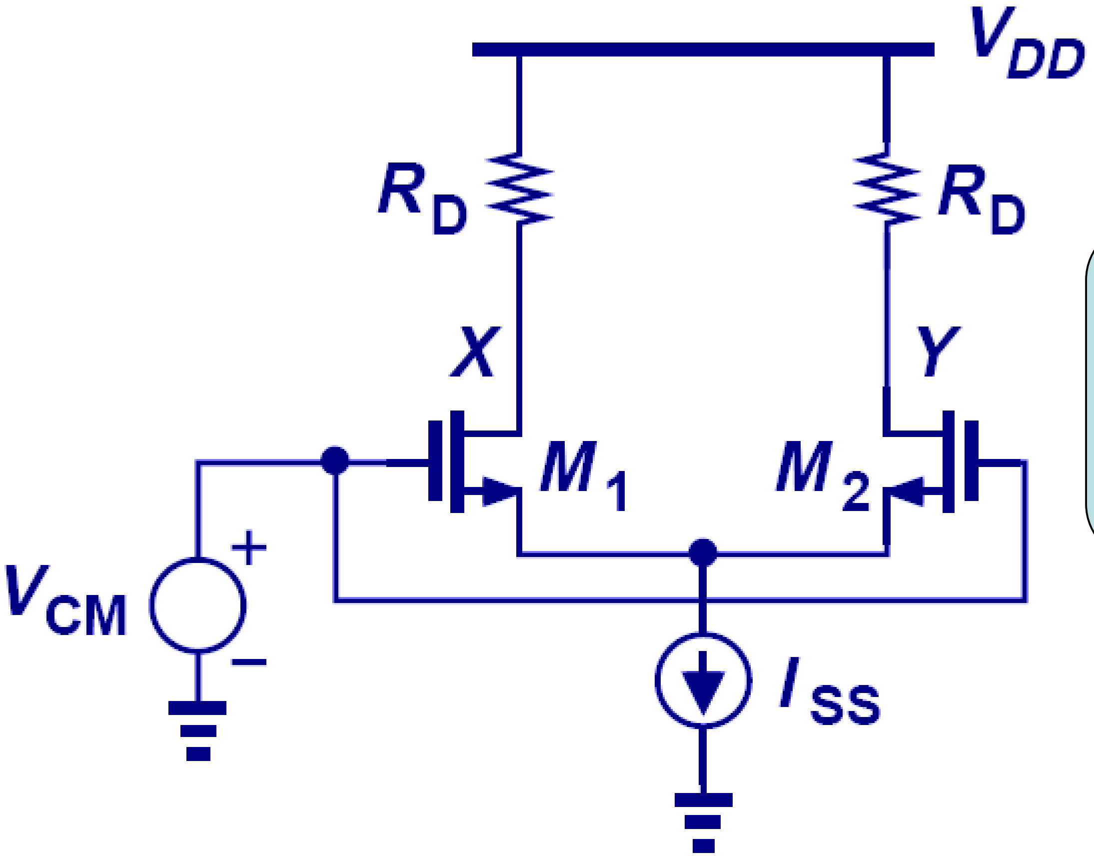
$$\Rightarrow R_{in} = \frac{v_X}{i_X} = 2 r_{\pi 1}$$



In a similar manner,

$$R_{out} = 2R_C$$

MOS Differential Pair's Common-Mode Response

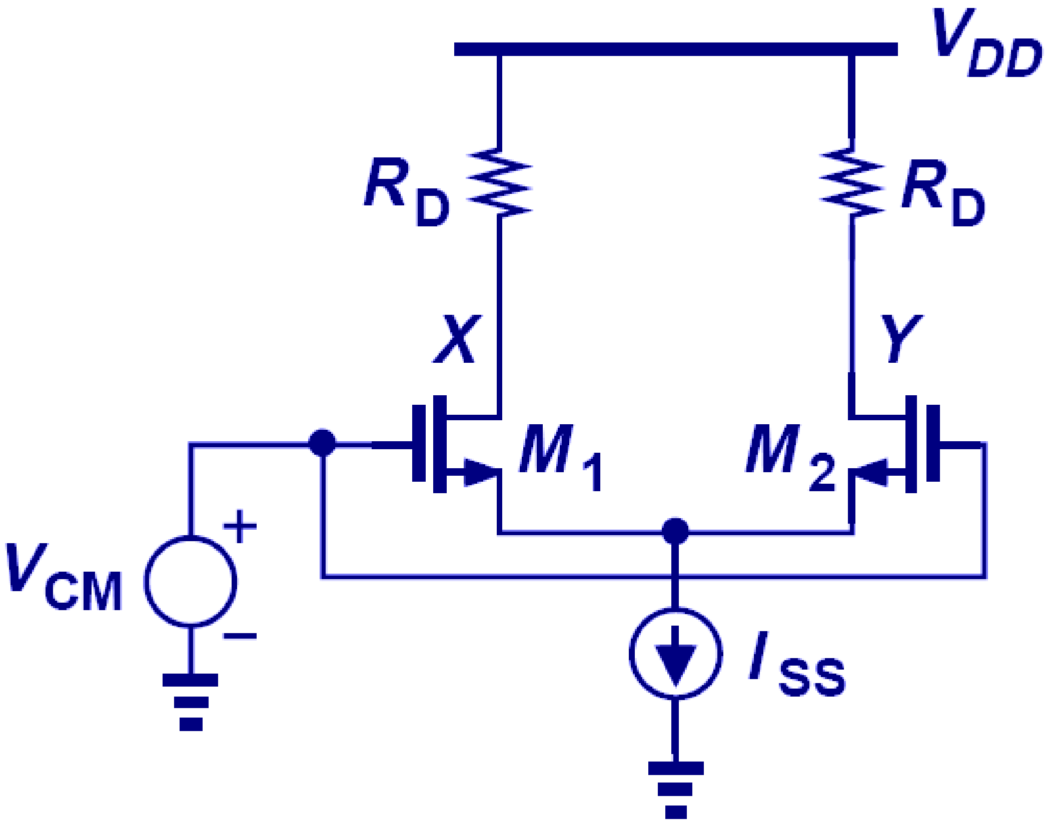


$$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

$$V_X = V_Y = V_{DD} - R_D \frac{I_{SS}}{2}$$

- **Similar to its bipolar counterpart, MOS differential pair produces zero differential output as V_{CM} changes.**

Equilibrium Overdrive Voltage



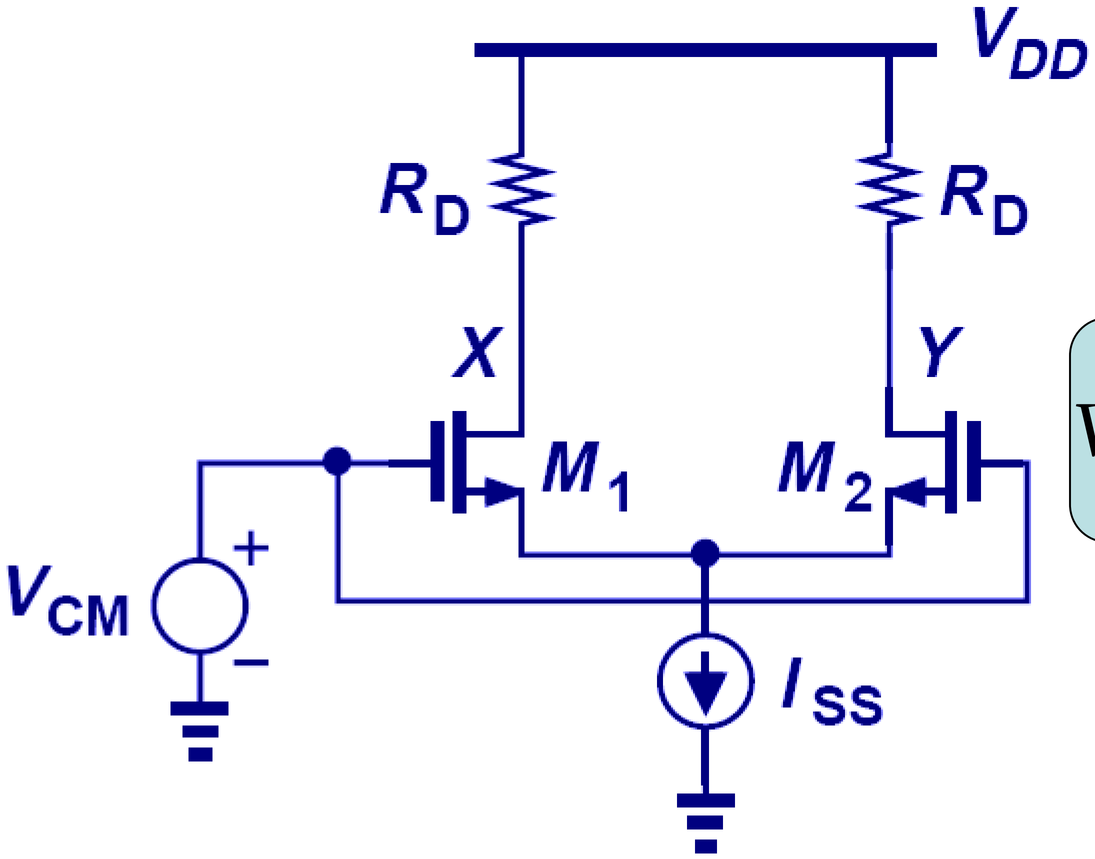
$$I_D = \frac{I_{SS}}{2}$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

$$\Rightarrow \left(V_{GS} - V_{TH}\right)_{equil} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

- **The equilibrium overdrive voltage is defined as the overdrive voltage seen by M_1 and M_2 when both of them carry a current of $I_{SS}/2$.**

Minimum Common-mode Output Voltage

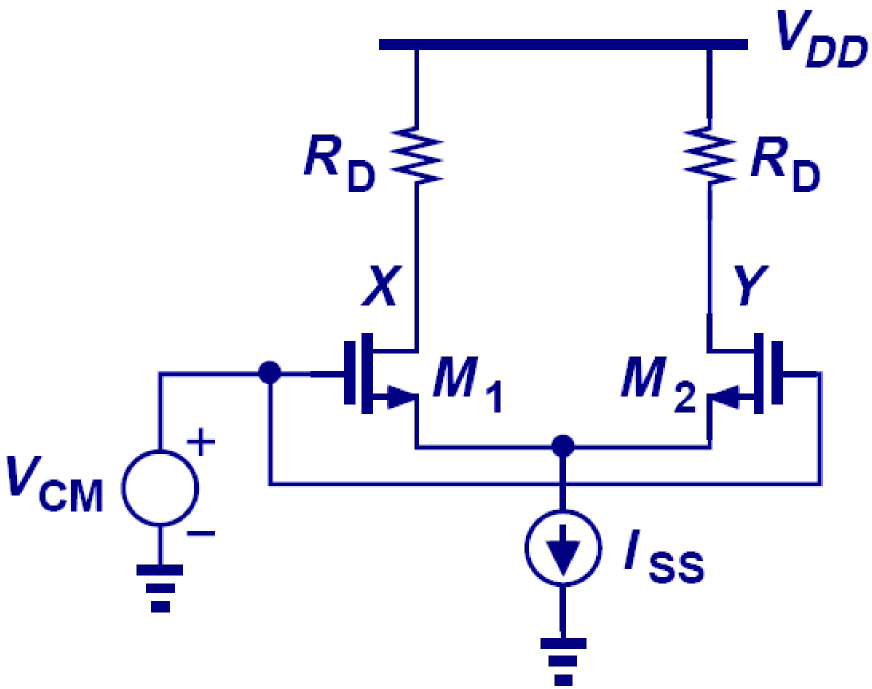


$$V_{DD} - R_D \frac{I_{SS}}{2} > V_{CM} - V_{TH}$$

- In order to maintain M_1 and M_2 in saturation, the common-mode output voltage cannot fall below the value above.
- This value usually limits voltage gain.

Example 10.15

- A MOS differential pair is driven with an input CM level of 1.6V. If I_{SS}=0.5mA, V_{TH}=0.5 V, and V_{DD}=1.8 V, what is the maximum allowable load resistance?

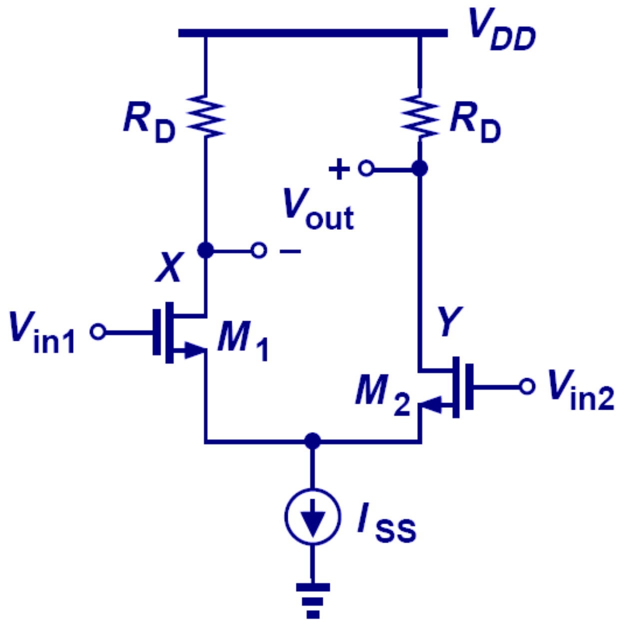


$$V_{DD} - R_D \frac{I_{SS}}{2} > V_{CM} - V_{TH}$$

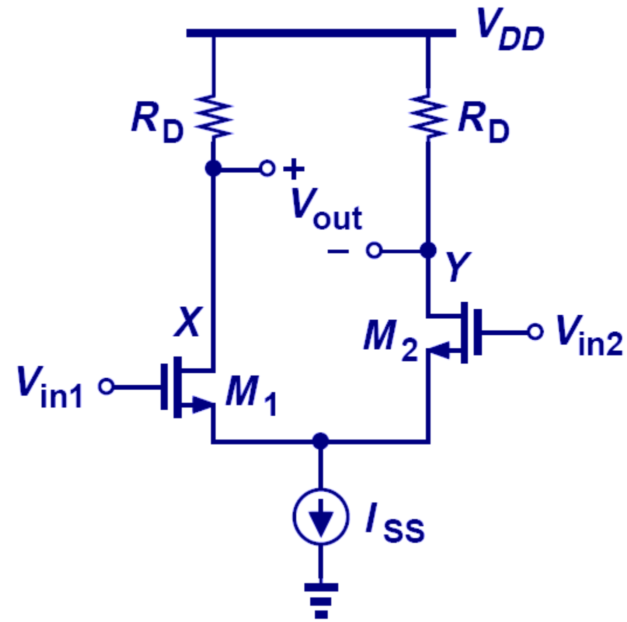
$$\Rightarrow R_D < 2\frac{V_{DD} - V_{CM} + V_{TH}}{I_{SS}}$$

$$< 2.8\ \text{k}\Omega$$

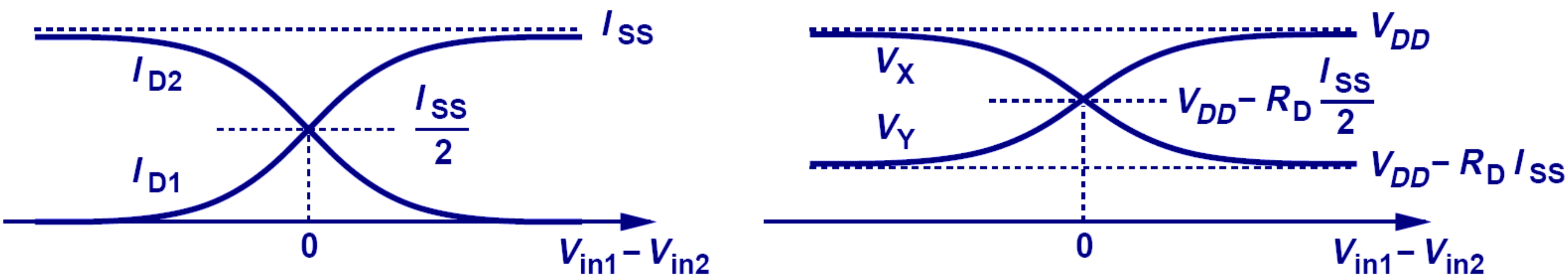
Differential Response



(a)

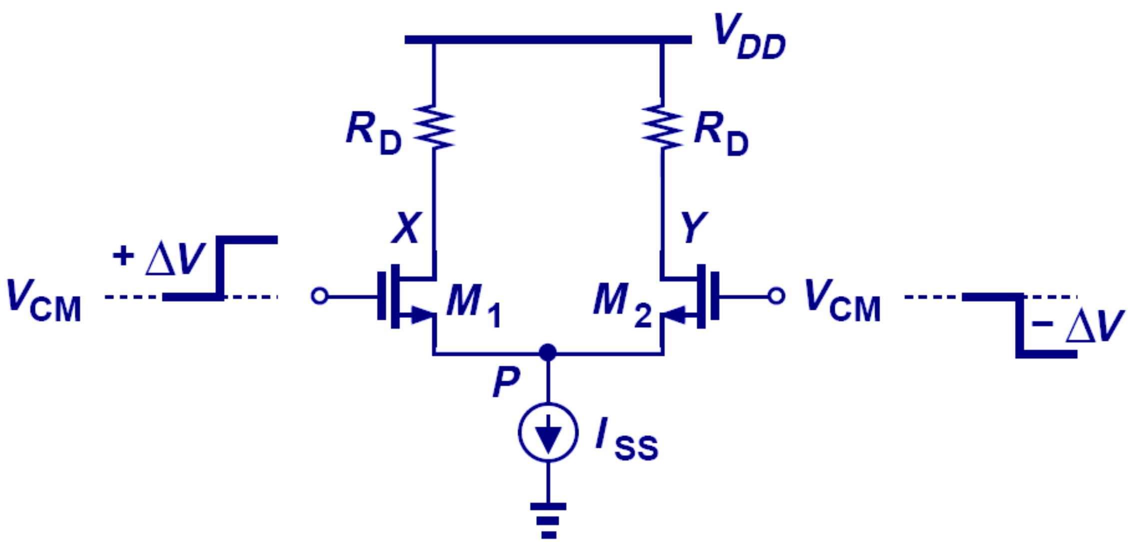


(b)



(c)

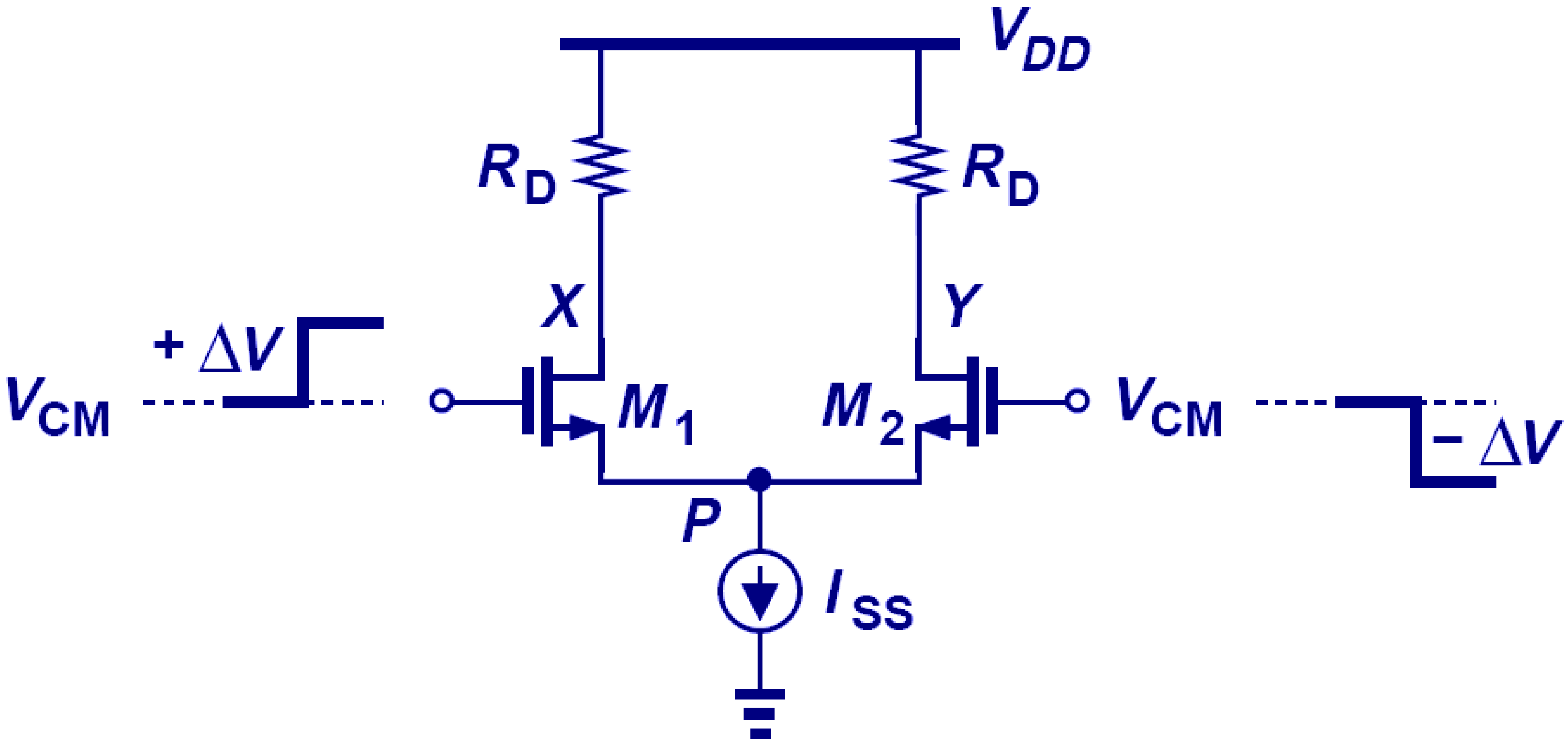
Small-Signal Response



$$\Delta V_P = 0$$
$$\Rightarrow \Delta I_{D1} = g_m \Delta V,$$
$$\Delta I_{D2} = -g_m \Delta V$$
$$\Rightarrow \Delta V_X - \Delta V_Y = -2 g_m R_D \Delta V$$
$$\therefore A_v = -g_m R_D$$

- Similar to its bipolar counterpart, the MOS differential pair exhibits the same virtual ground node and small signal gain.

Power and Gain Tradeoff

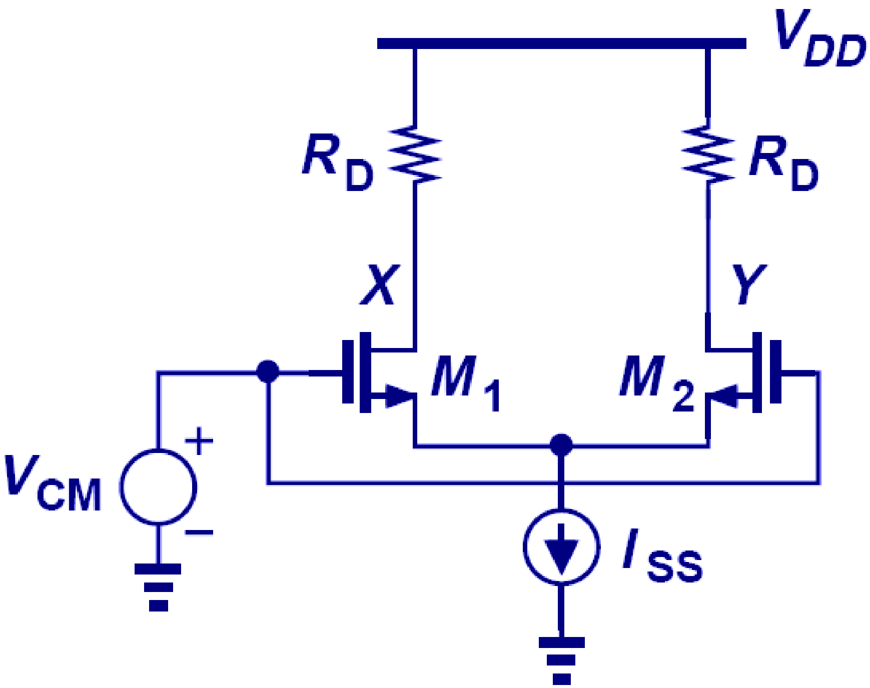


- In order to obtain the same gain as a CS stage, a MOS differential pair must dissipate twice the amount of current. This power and gain tradeoff is also echoed in its bipolar counterpart.

Example 10.16

- **Design an NMOS differential pair for a voltage gain of 5 and a power budget of 2 mW subject to the condition that the stage following the differential pair requires an output CM level of at least 1.6V. Assume $\mu_n C_{ox}$=100 μA/V², λ=0, and V_{DD}= 1.8 V.**

Textbook Error!



$$I_{SS} = \frac{2\ \text{mW}}{1.8\ \text{V}} = 1.11\ \text{mA}$$

$$V_{CM,out} = V_{DD} - R_D \frac{I_{SS}}{2} \geq 1.6\ \text{V}$$

$$\Rightarrow R_D \leq 360\ \Omega$$

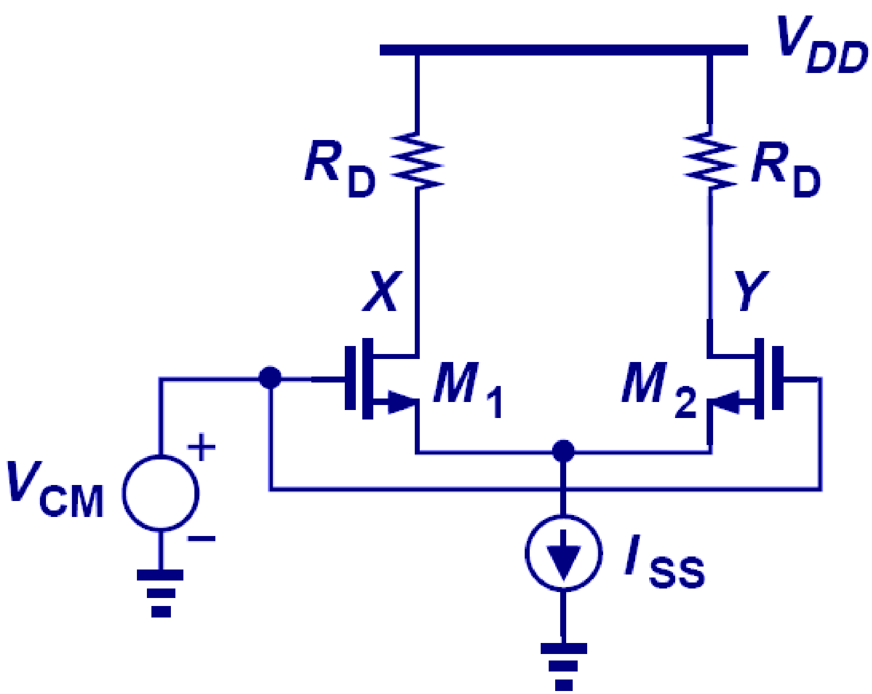
For $R_D = 360\ \Omega$,

$$g_m = \frac{A_v}{R_D} = \frac{5}{360\ \Omega} = \sqrt{2\mu_n C_{ox} \frac{W}{L} \frac{I_{SS}}{2}}$$

$$\Rightarrow \frac{W}{L} = 1738$$

Example 10.17

- **What is the maximum allowable input CM level in the previous example if V_{TH}=0.4 V?**



To guarantee that M_1 and M_2 operate in saturation,

$$V_{CM,in} < V_{DD} - R_D \frac{I_{SS}}{2} + V_{TH}$$

$$< V_{CM,out} + V_{TH}.$$

Thus,

$$V_{CM,in} < 2\text{ V}$$

Example 10.18

- The common-source stage and the differential pair shown in Fig. 10.28 incorporate equal load resistors. If the two circuits are designed for the same voltage gain and the same supply voltage, discuss the choice of (a) transistor dimensions for a given power budget, (b) power dissipation for given transistor dimensions.

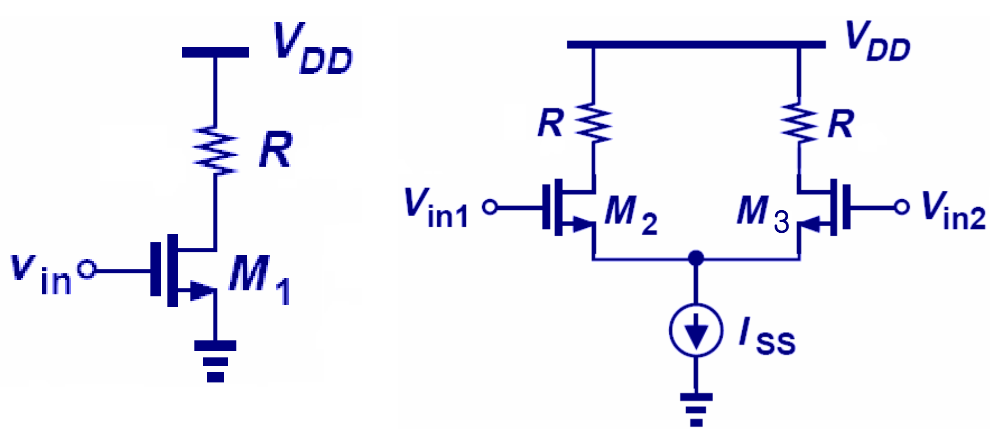


Figure10.28

(a) for same power budget,

$$I_{D1} = I_{SS} = 2I_{D2} = 2I_{D3}$$

$$\Rightarrow \frac{W_1}{L_1} = \frac{1}{2}\frac{W_2}{L_2} = \frac{1}{2}\frac{W_3}{L_3}$$

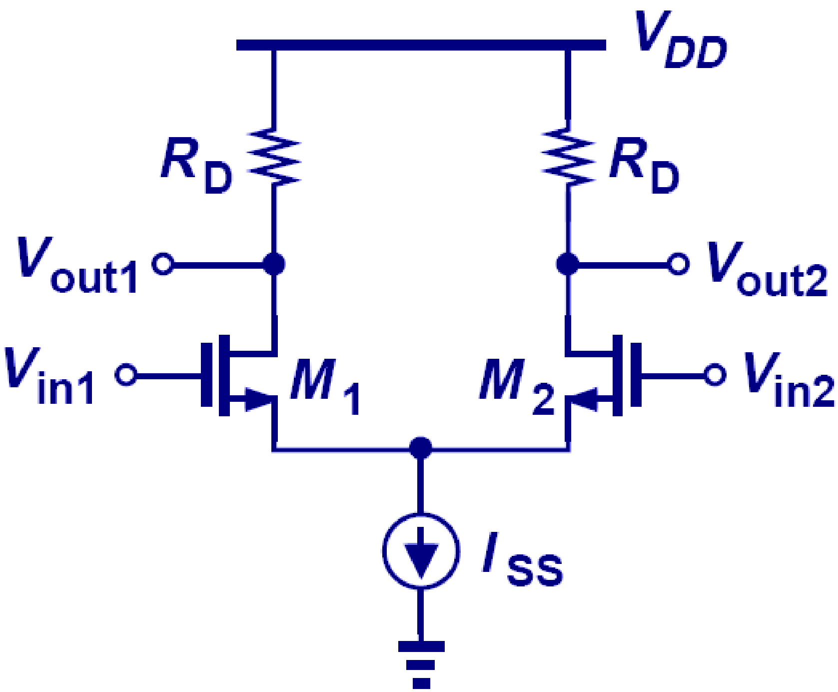
$$\left(\because g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \right)$$

(b) for same transistor dimensions,

$$I_{SS} = 2I_{D1}$$

$$\Rightarrow P_{diff} = 2P_{CS}$$

MOS Differential Pair's Large-Signal Response



Goal is to obtain I_{D1} - I_{D2}

$$V_{in1} - V_{GS1} = V_{in2} - V_{GS2}.$$

$$I_{D1} + I_{D2} = I_{SS}.$$

$$I_D = (1/2)\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})^2.$$

$$\Rightarrow V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}}.$$

$$\Rightarrow V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

$$= \sqrt{\frac{2}{\mu_n C_{ox}\frac{W}{L}}}(\sqrt{I_{D1}} - \sqrt{I_{D2}}).$$

MOS Differential Pair's Large-Signal Response (cont'd)

$$(V_{in1}-V_{in2})^2=\frac{2}{\mu_n C_{ox}\frac{W}{L}}(I_{D1}+I_{D2}-2\sqrt{I_{D1}I_{D2}})$$

$$=\frac{2}{\mu_n C_{ox}\frac{W}{L}}(I_{SS}-2\sqrt{I_{D1}I_{D2}}).$$

$$\Rightarrow 4\sqrt{I_{D1}I_{D2}}=2I_{SS}-\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2$$

$$\Rightarrow 16I_{D1}I_{D2}=\left[2I_{SS}-\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2\right]^2$$

$$\Rightarrow 16I_{D1}(I_{SS}-I_{D1})=\left[2I_{SS}-\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2\right]^2$$

MOS Differential Pair's Large-Signal Response (cont'd)

$$\Rightarrow 16I_{D1}^2 - 16I_{SS}I_{D1} + \left[2I_{SS} - \mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2\right]^2 = 0$$

$$\Rightarrow I_{D1} = \frac{I_{SS}}{2} \pm \frac{1}{4}\sqrt{4I_{SS}^2 - \left[\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - 2I_{SS}\right]^2}$$

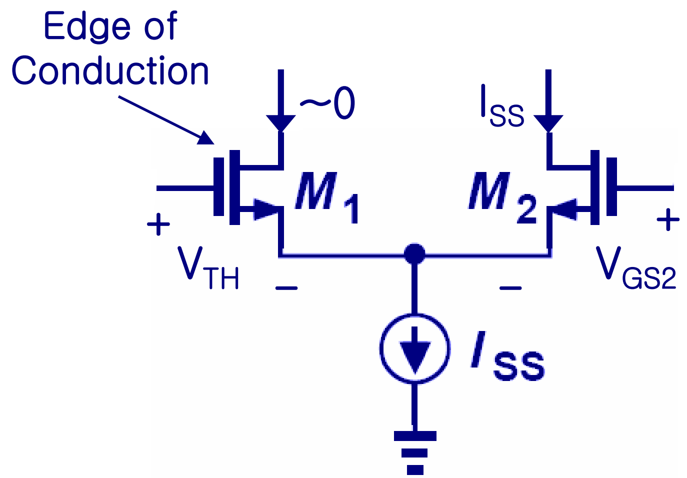
$$= \frac{I_{SS}}{2} + \frac{V_{in1} - V_{in2}}{4}\sqrt{\mu_n C_{ox}\frac{W}{L}\left[4I_{SS} - \mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2\right]}$$

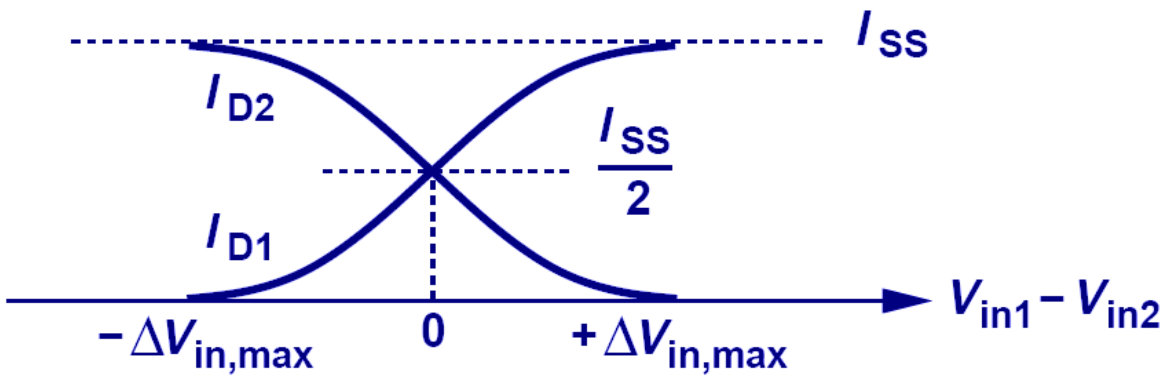
$$\Rightarrow I_{D2} = \frac{I_{SS}}{2} + \frac{V_{in2} - V_{in1}}{4}\sqrt{\mu_n C_{ox}\frac{W}{L}\left[4I_{SS} - \mu_n C_{ox}\frac{W}{L}(V_{in2} - V_{in1})^2\right]}$$

($\because$ the symmetry of the circuit)

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{in1} - V_{in2}\right)\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \left(V_{in1} - V_{in2}\right)^2}$$

Maximum Differential Input Voltage





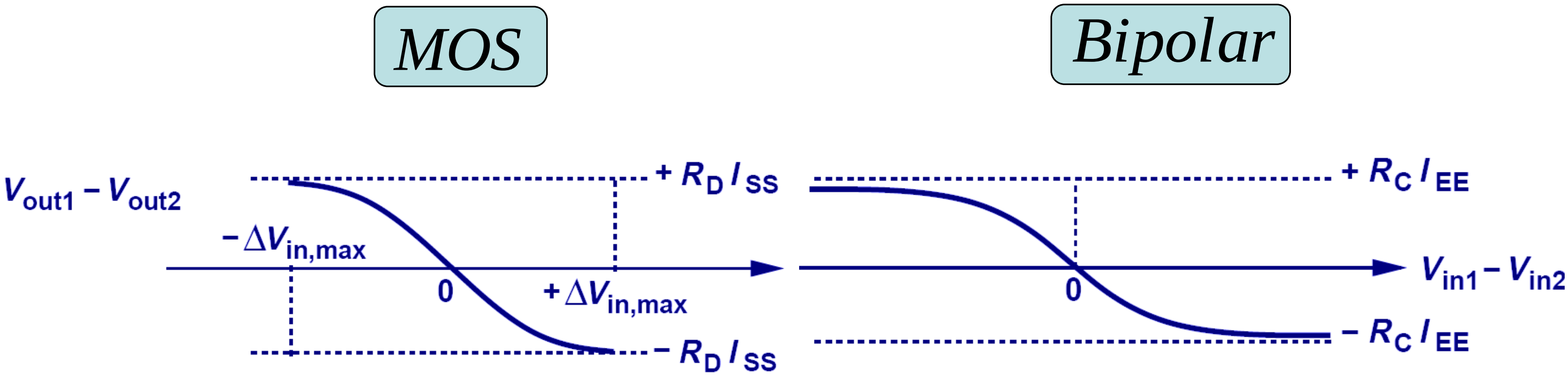
$$V_{GS1} = V_{TH}$$

$$V_{GS2} = V_{TH} + \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

$$\left| V_{in1} - V_{in2} \right|_{\max} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = \sqrt{2} \left(V_{GS} - V_{TH} \right)_{equil}$$

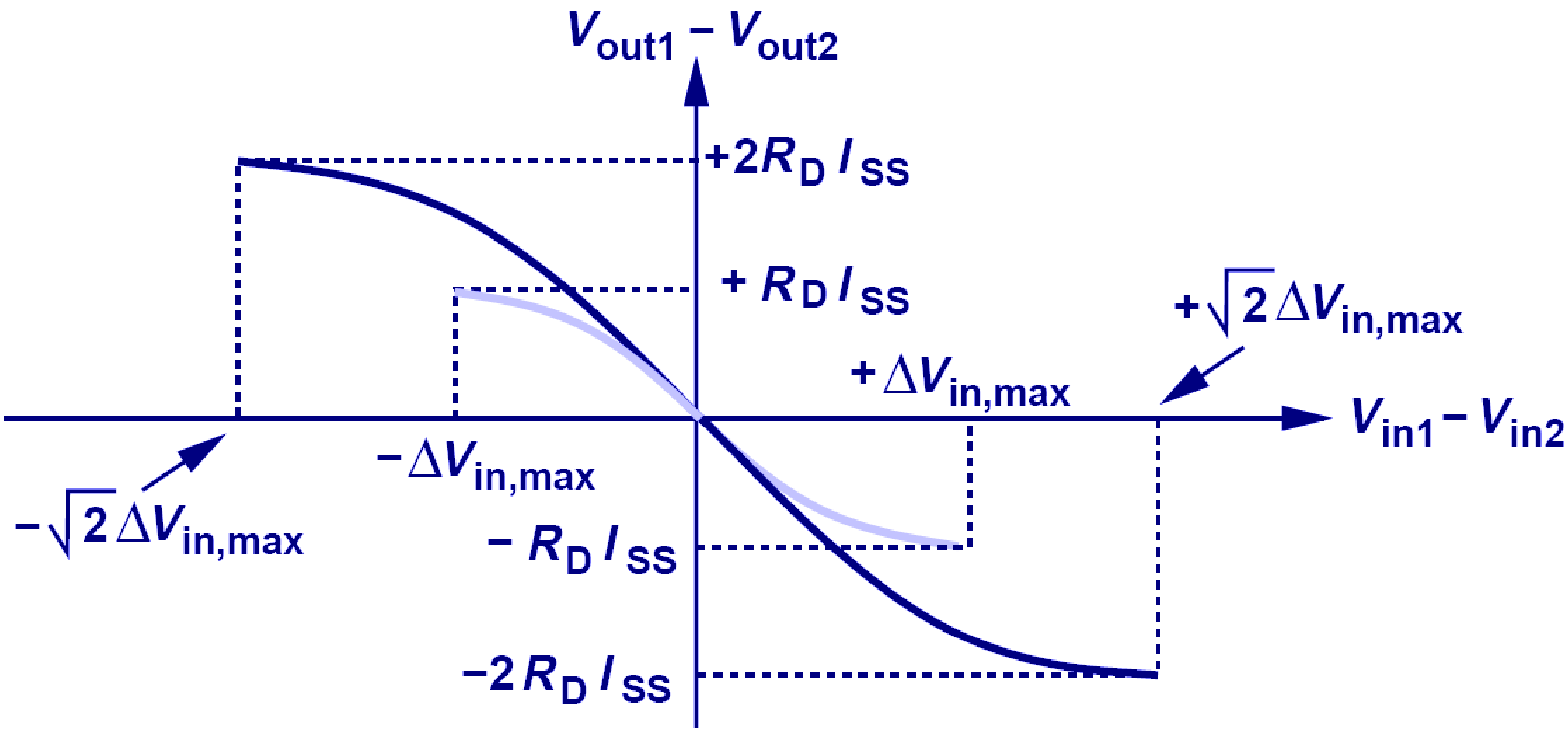
- **There exists a finite differential input voltage that completely steers the tail current from one transistor to the other. This value is known as the maximum differential input voltage.**

Contrast Between MOS and Bipolar Differential Pairs



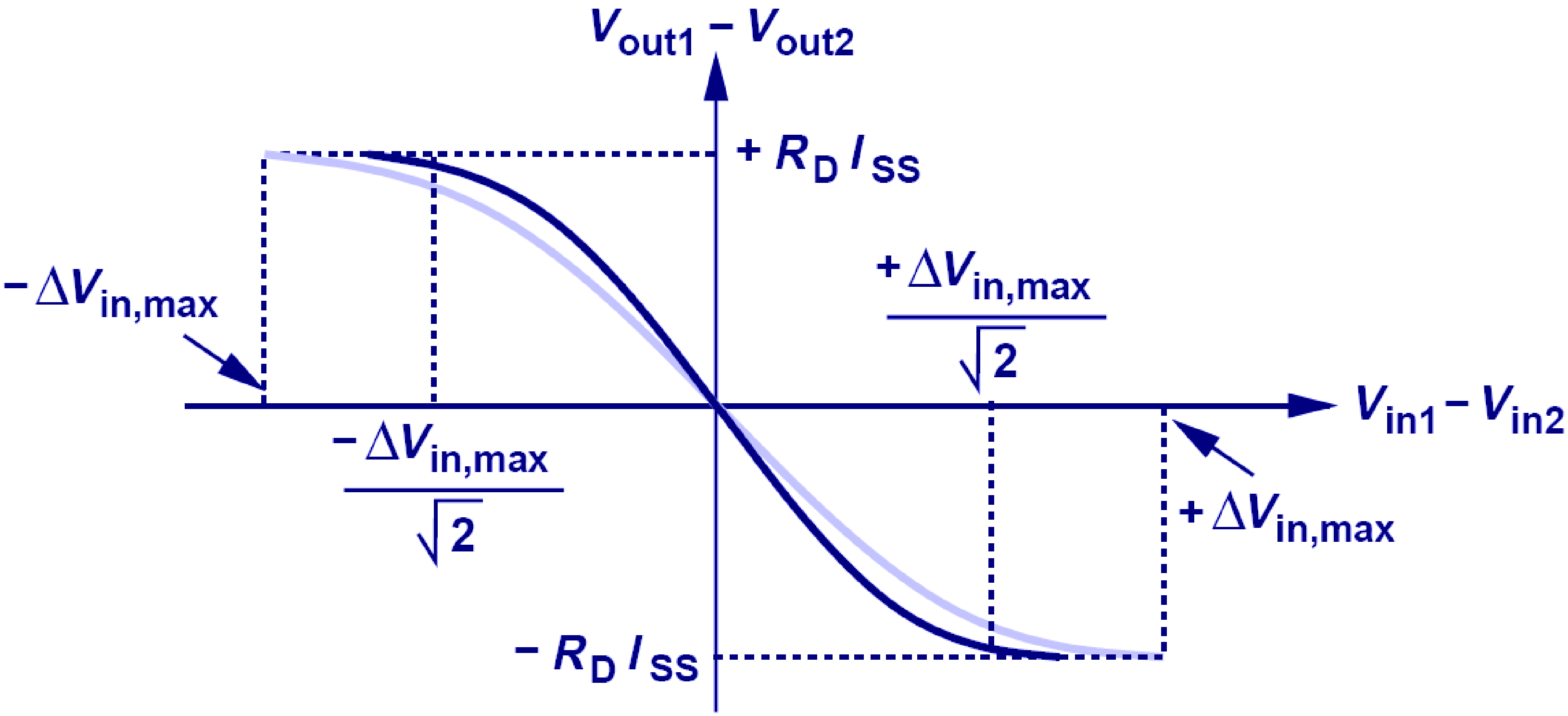
- **In a MOS differential pair, there exists a finite differential input voltage to completely switch the current from one transistor to the other, whereas, in a bipolar pair that voltage is infinite.**

The effects of Doubling the Tail Current



- Since I_{SS} is doubled and W/L is unchanged, the equilibrium overdrive voltage for each transistor must increase by $\sqrt{2}$ to accommodate this change, thus $\Delta V_{in,max}$ increases by $\sqrt{2}$ as well. Moreover, since I_{SS} is doubled, the differential output swing will double.

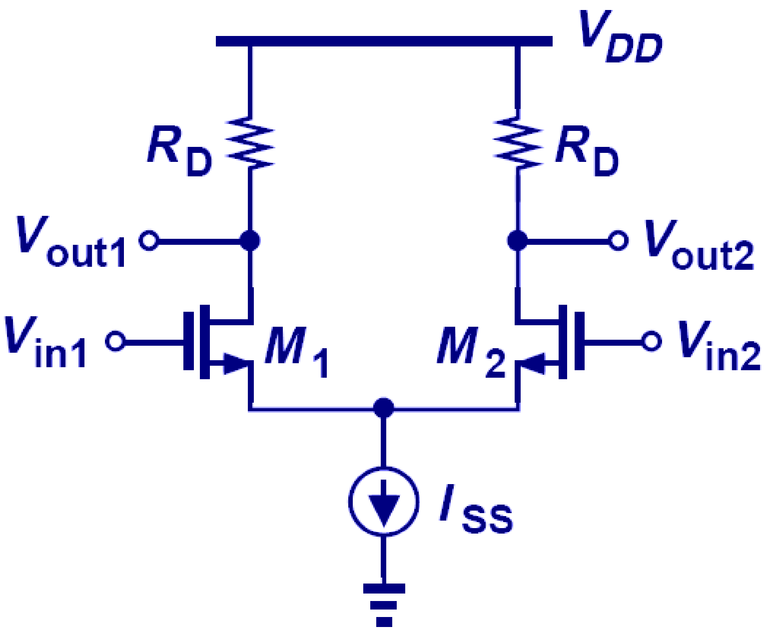
The effects of Doubling W/L



- **Since W/L is doubled and the tail current remains unchanged, the equilibrium overdrive voltage will be lowered by $\sqrt{2}$ to accommodate this change, thus $\Delta V_{in,max}$ will be lowered by as well. Moreover, the differential output swing will remain unchanged since neither I_{SS} nor R_D has changed**

Example 10.20

- Design an NMOS differential pair for a power budget of 3 mW and $\Delta V_{in,max}$=500 mV. Assume $\mu_n C_{ox}$=100 μA/V² and V_{DD}=1.8 V.



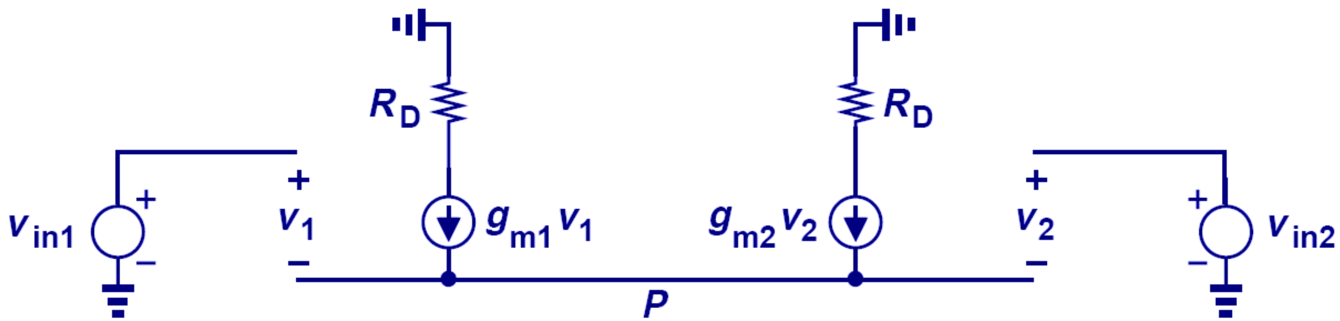
$$I_{SS} = \frac{3\text{ mW}}{1.8\text{ V}} = 1.67\text{ mA}$$

From $$\left|V_{in1} - V_{in2}\right|_{\max} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$\frac{W}{L} = \frac{2I_{SS}}{\mu_n C_{ox} \Delta V_{in,\max}^2} = 133.6$$

R_D is determined by the required voltage gain.

Small-Signal Analysis of MOS Differential Pair



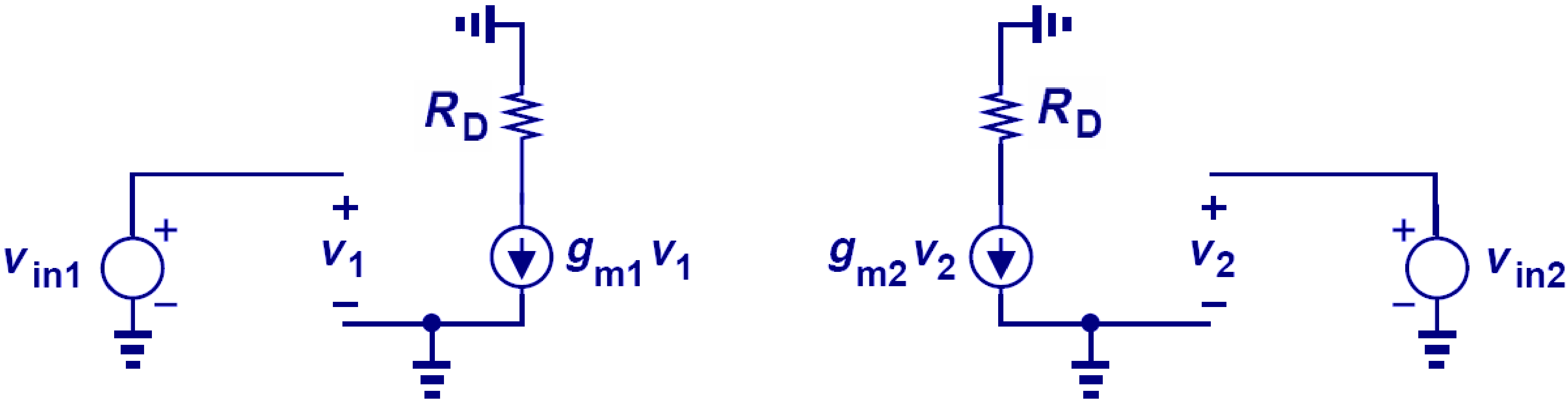
$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

$$\approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$= \sqrt{\mu_n C_{ox}\frac{W}{L}I_{SS}}\,(V_{in1} - V_{in2})$$

- **When the input differential signal is small compared to $[4I_{SS}/\mu_n C_{ox}(W/L)]^{1/2}$, the output differential current is linearly proportional to it, and small-signal model can be applied.**

Virtual Ground and Half Circuit

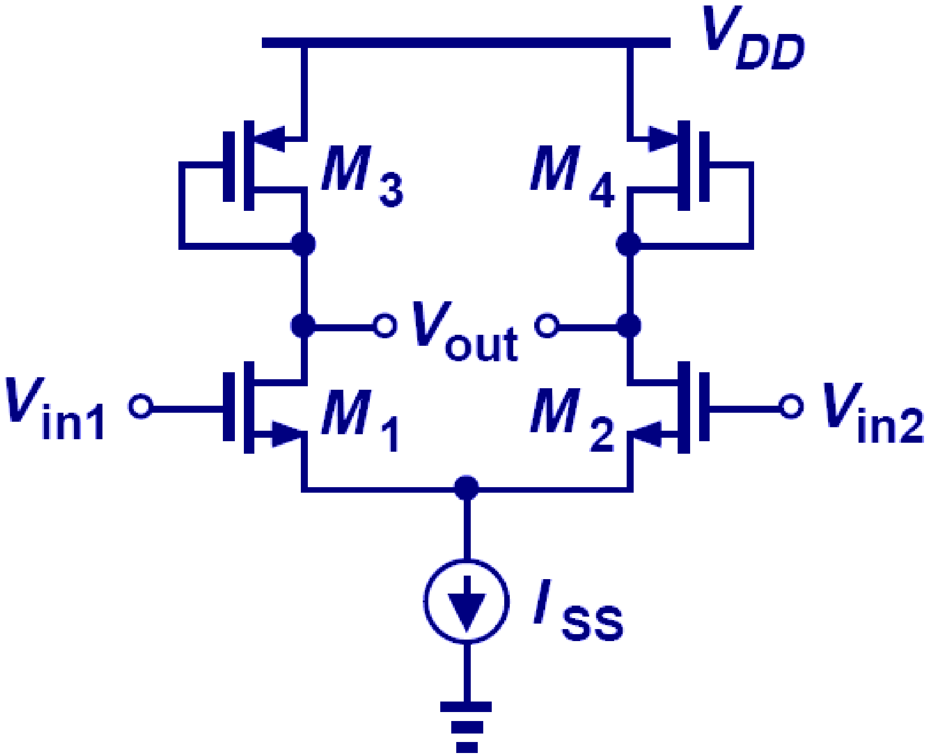


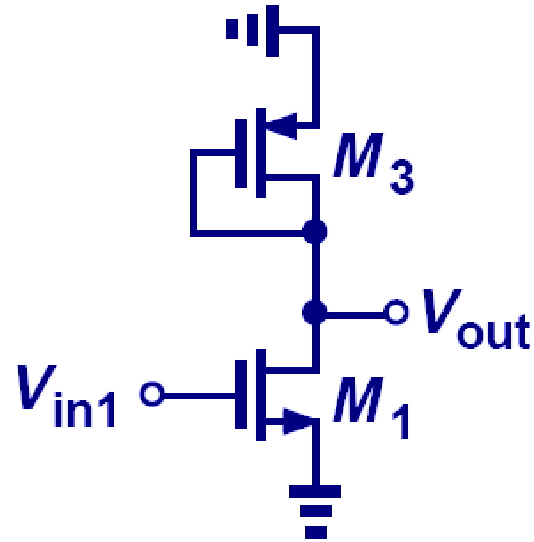
$$\Delta V_P = 0$$

$$A_v = -g_m R_D$$

- Applying the same analysis as the bipolar case, we will arrive at the same conclusion that node P will not move for small input signals and the concept of half circuit can be used to calculate the gain.

MOS Differential Pair Half Circuit Example I

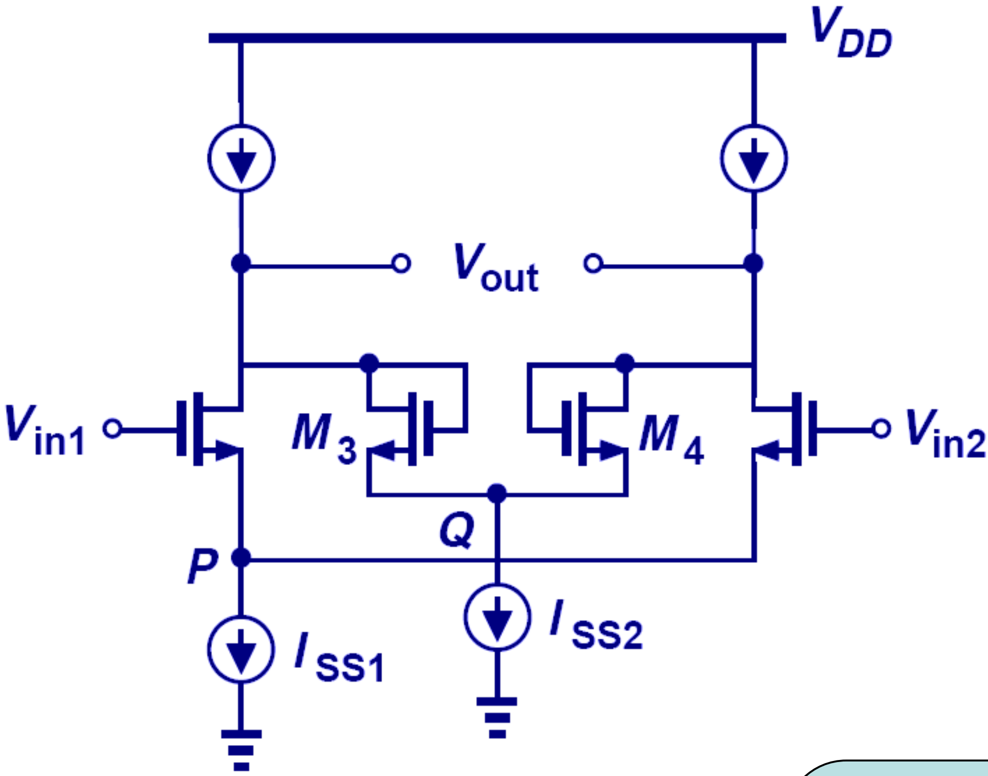


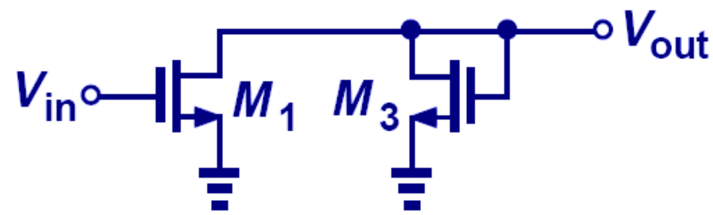


$$\lambda \neq 0$$

$$A_v = -g_{m1}\left(\frac{1}{g_{m3}} \parallel r_{O3} \parallel r_{O1}\right)$$

MOS Differential Pair Half Circuit Example II

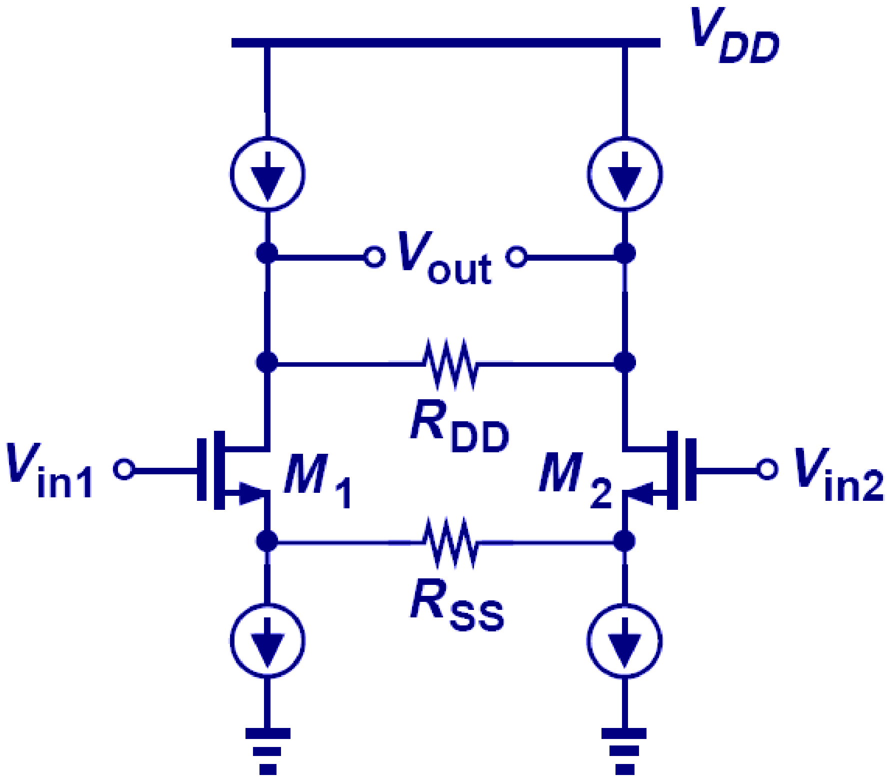


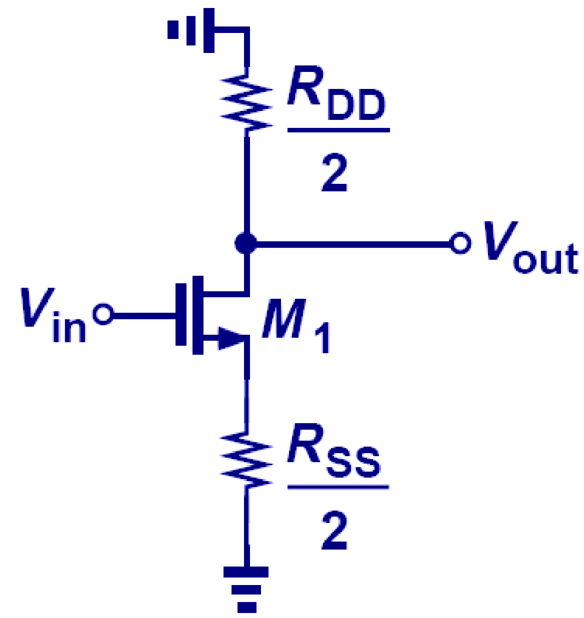


$$\lambda = 0$$

$$A_v = -\frac{g_{m1}}{g_{m3}}$$

MOS Differential Pair Half Circuit Example III

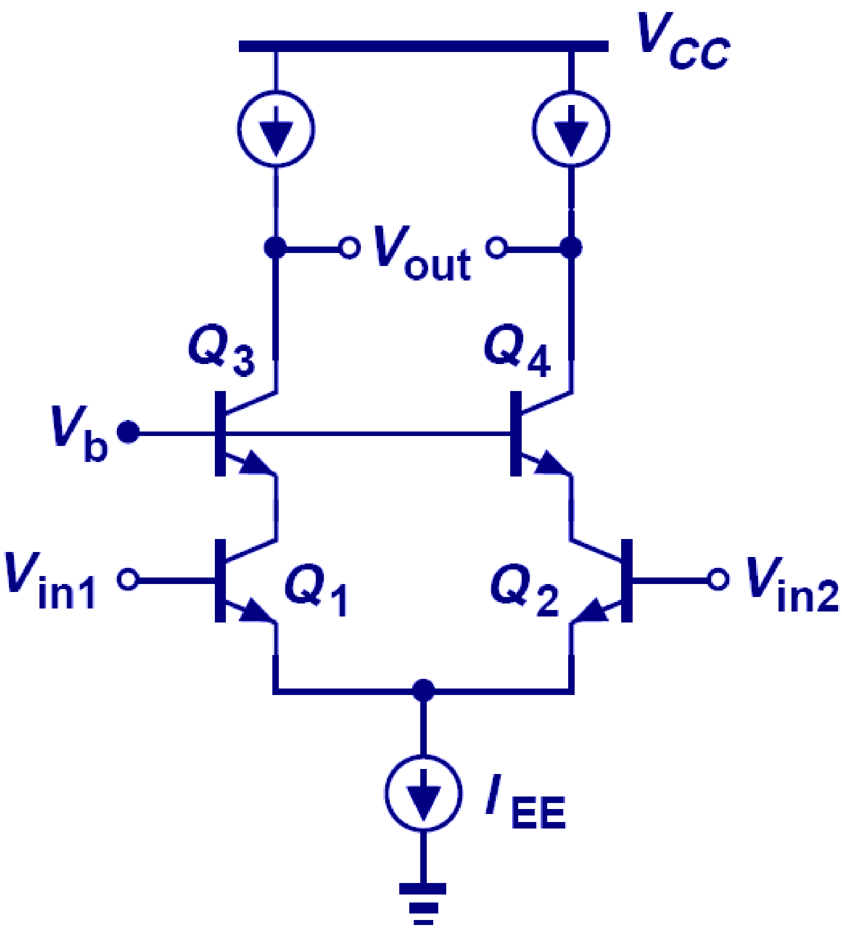


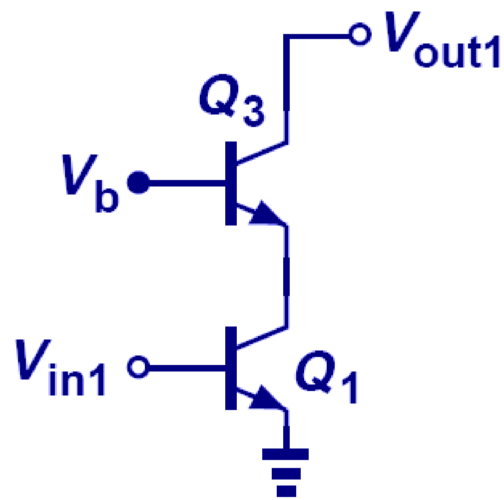


$$\lambda = 0$$

$$A_v = -\frac{R_{DD}/2}{R_{SS}/2 + 1/g_m}$$

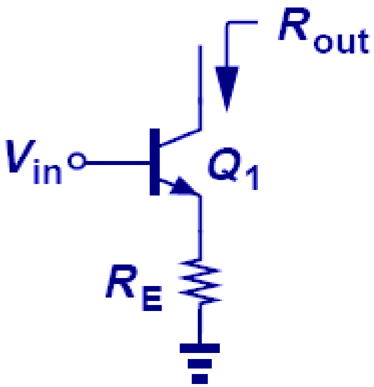
Bipolar Cascode Differential Pair



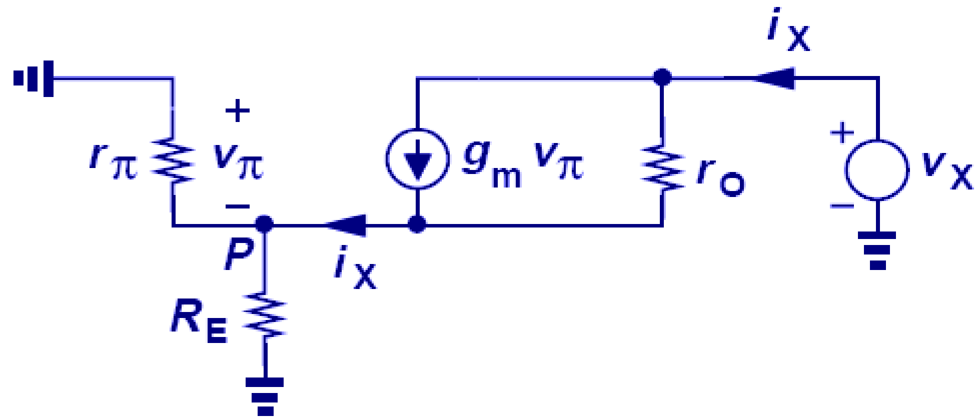


$$A_v = -g_{m1}\left[g_{m3}\left(r_{O1} \,||\, r_{\pi 3}\right) r_{O3} + r_{O1} \,||\, r_{\pi 3}\right]$$

Output Impedance of CE Stage with Degeneration



(a)



(b)

$$v_X = (i_X - g_m v_\pi) r_O - v_\pi$$

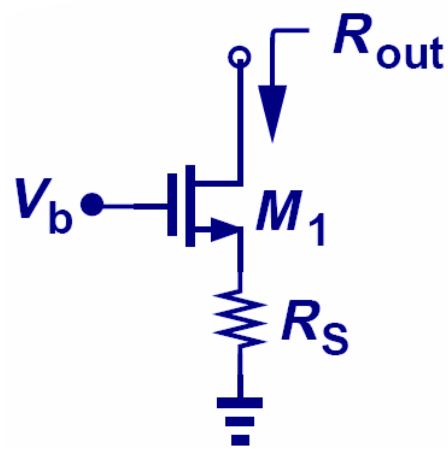
$$= \left[i_X + g_m i_X (R_E \| r_\pi) \right] r_O + i_X (R_E \| r_\pi)$$

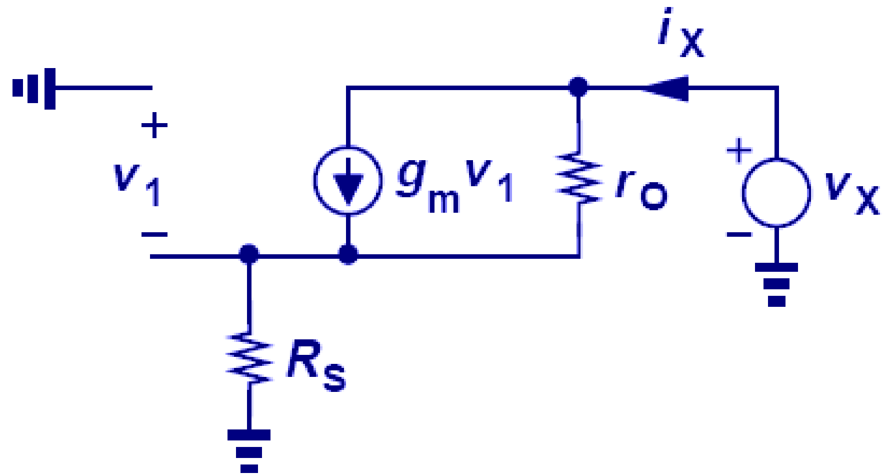
$$\therefore R_{out} = \left[1 + g_m (R_E \| r_\pi) \right] r_O + R_E \| r_\pi$$

$$= r_O + (g_m r_O + 1)(R_E \| r_\pi)$$

$$\approx r_O \left[1 + g_m (R_E \| r_\pi) \right]$$

Output Impedance of CS Stage with Degeneration





$$i_X - g_m v_1 = i_X - g_m\left(-i_X R_S\right) = i_X + g_m i_X R_S$$

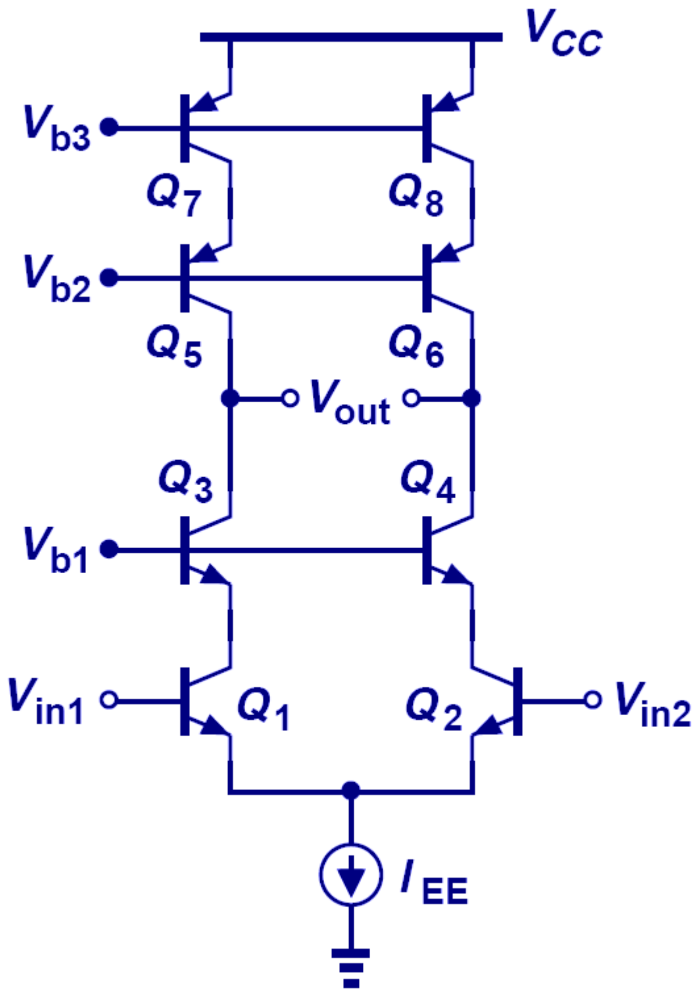
$$\Rightarrow r_O\left(i_X + g_m i_X R_S\right) + i_X R_S = v_X$$

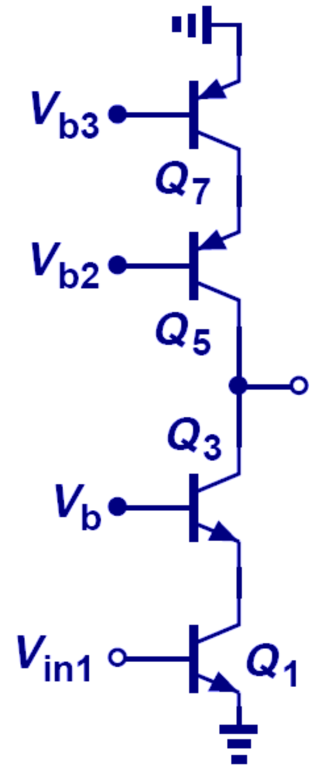
$$\therefore R_{out} = r_O\left(1 + g_m R_S\right) + R_S$$

$$= \left(1 + g_m r_O\right) R_S + r_O$$

$$\approx g_m r_O R_S + r_O$$

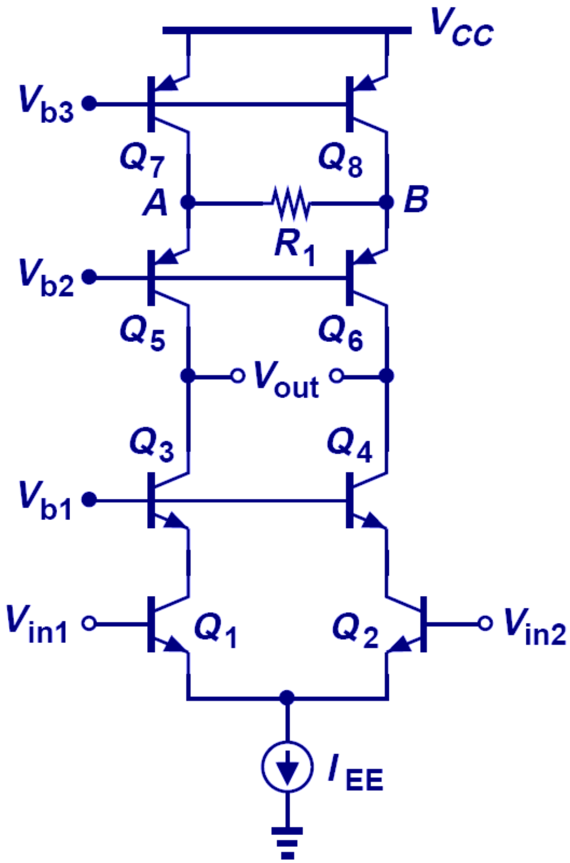
Bipolar Telescopic Cascode

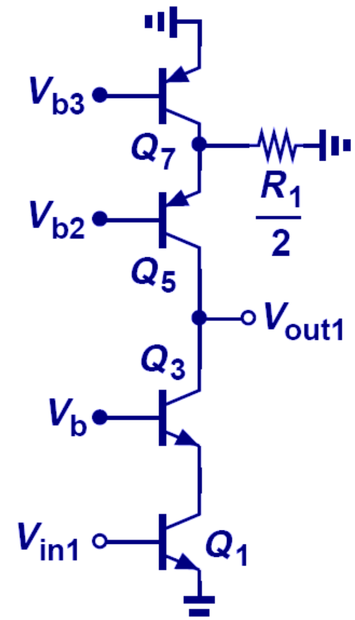




$$A_v \approx -g_{m1}[g_{m3}r_{O3}(r_{O1} \parallel r_{\pi 3})] \parallel [g_{m5}r_{O5}(r_{O7} \parallel r_{\pi 5})]$$

Example: Bipolar Telescopic Parasitic Resistance

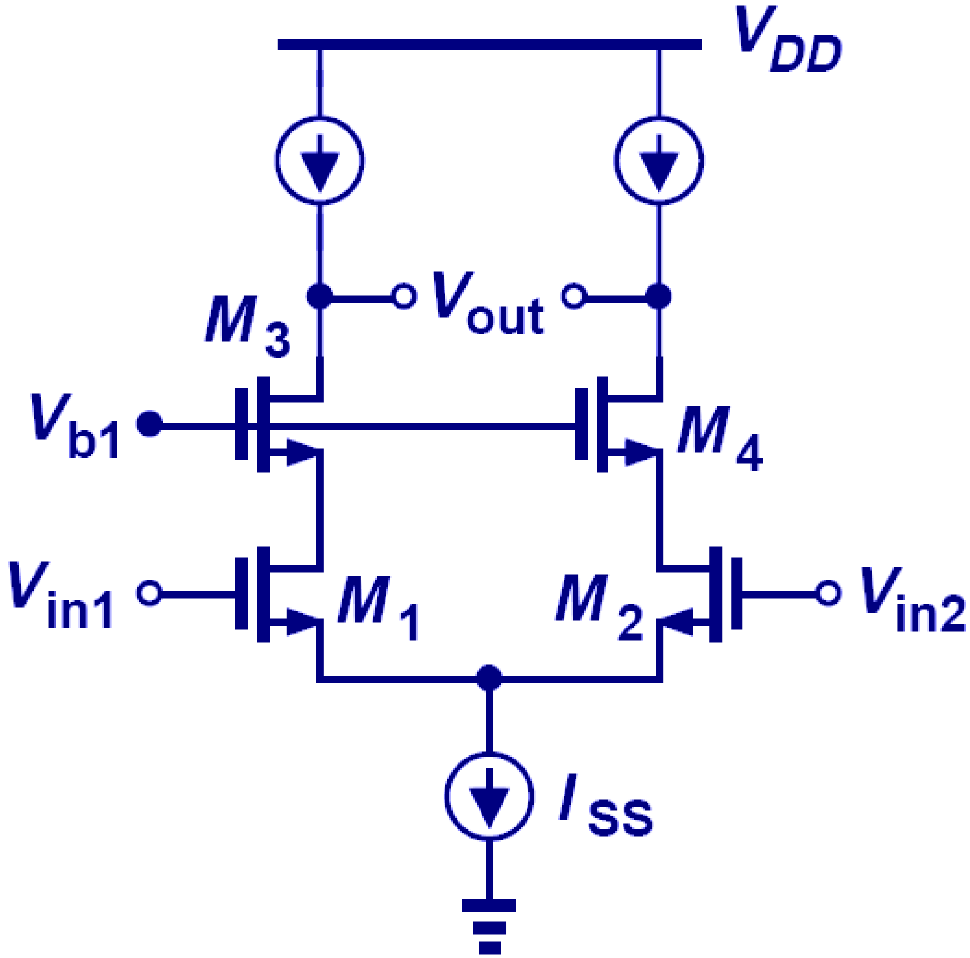


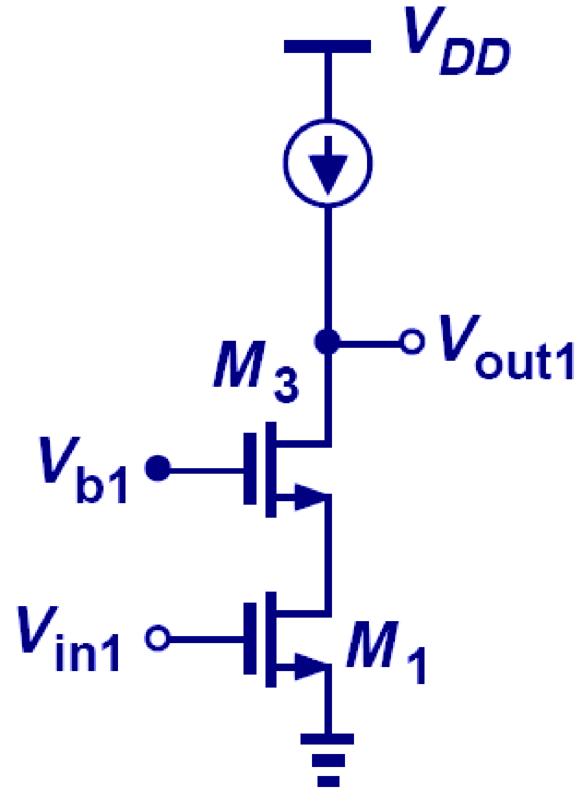


$$R_{op} = r_{O5}\left[1 + g_{m5}\left(r_{O7} \parallel r_{\pi 5} \parallel \frac{R_1}{2}\right)\right] + r_{O7} \parallel r_{\pi 5} \parallel \frac{R_1}{2}$$

$$A_v = -g_{m1}\left[\{g_{m3} r_{O3}(r_{O1} \parallel r_{\pi 3})\} \parallel R_{op}\right]$$

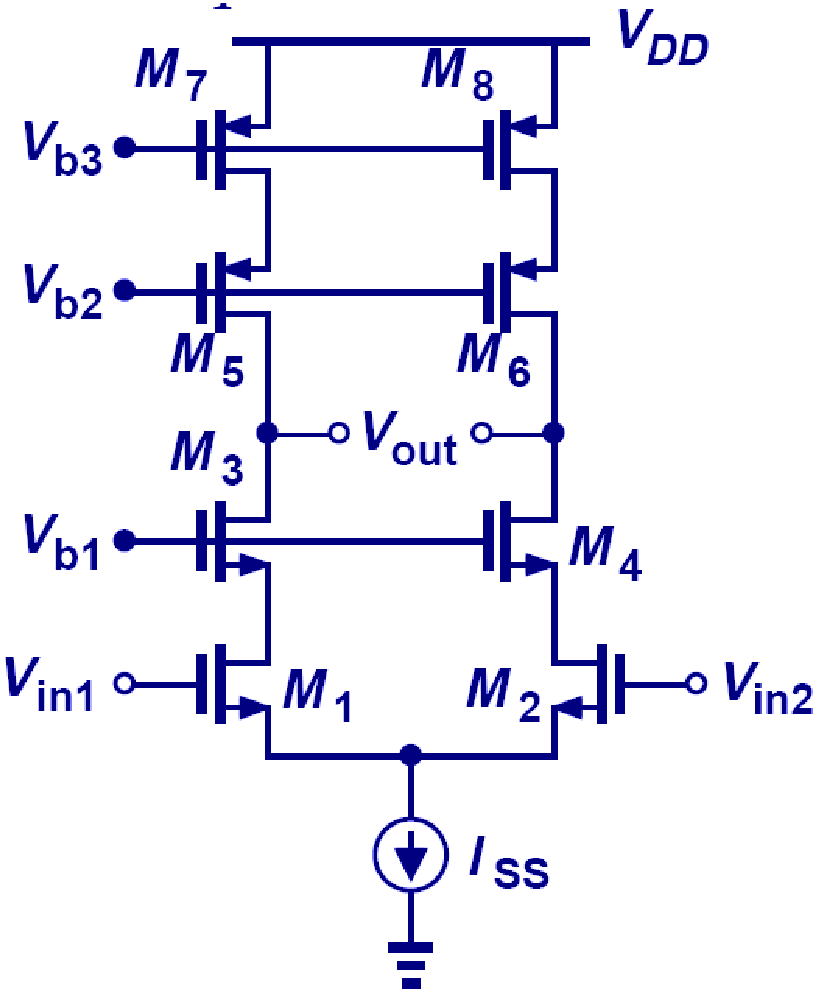
MOS Cascode Differential Pair

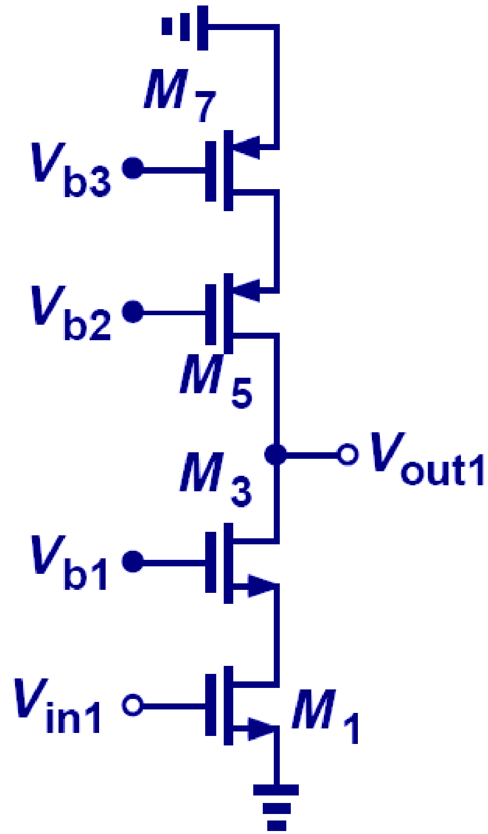




$$A_v \approx -g_{m1} r_{O3} g_{m3} r_{O1}$$

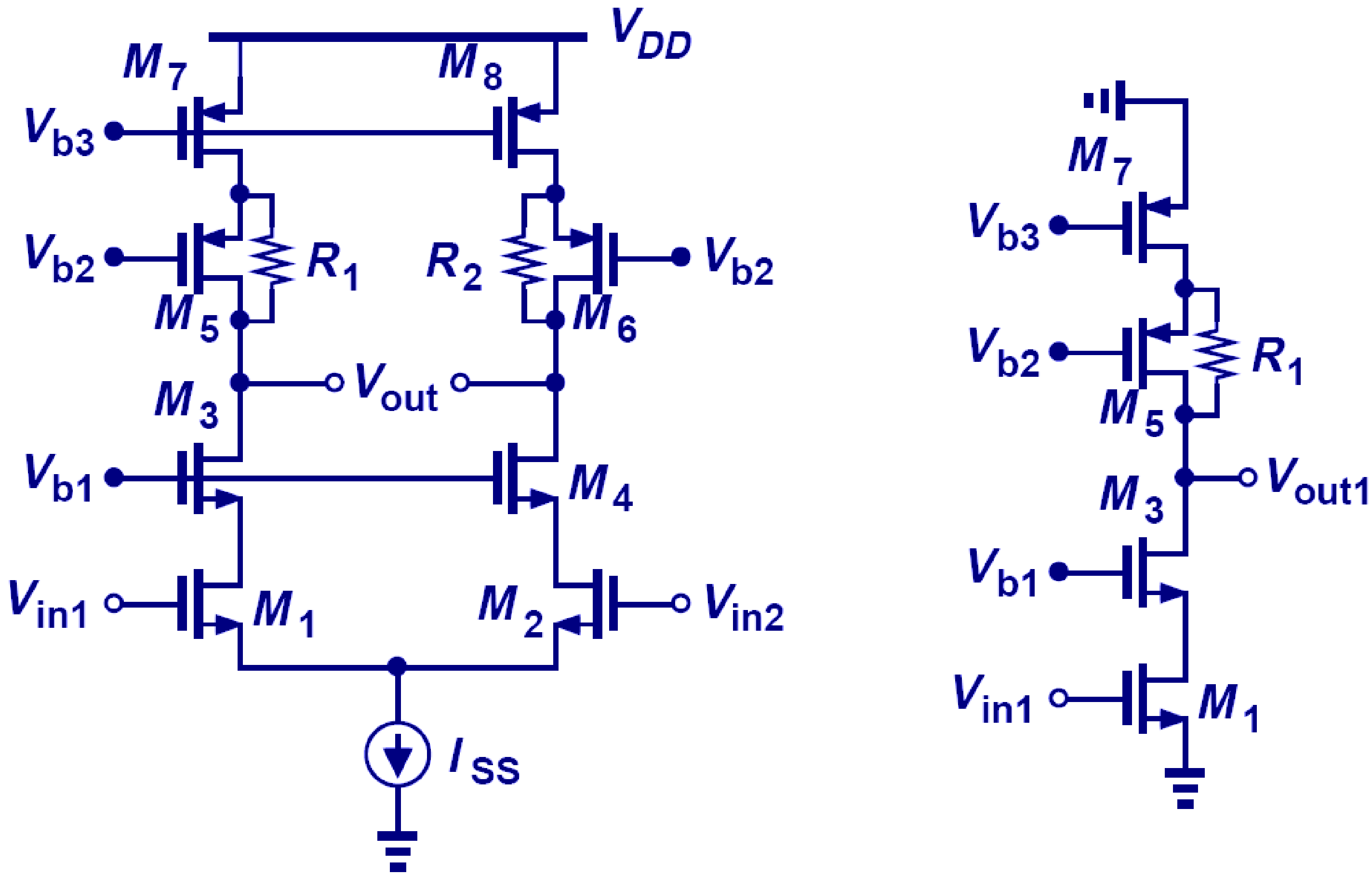
MOS Telescopic Cascode





$$A_v \approx -g_{m1}\left[\left(g_{m3}r_{O3}r_{O1}\right) \| \left(g_{m5}r_{O5}r_{O7}\right)\right]$$

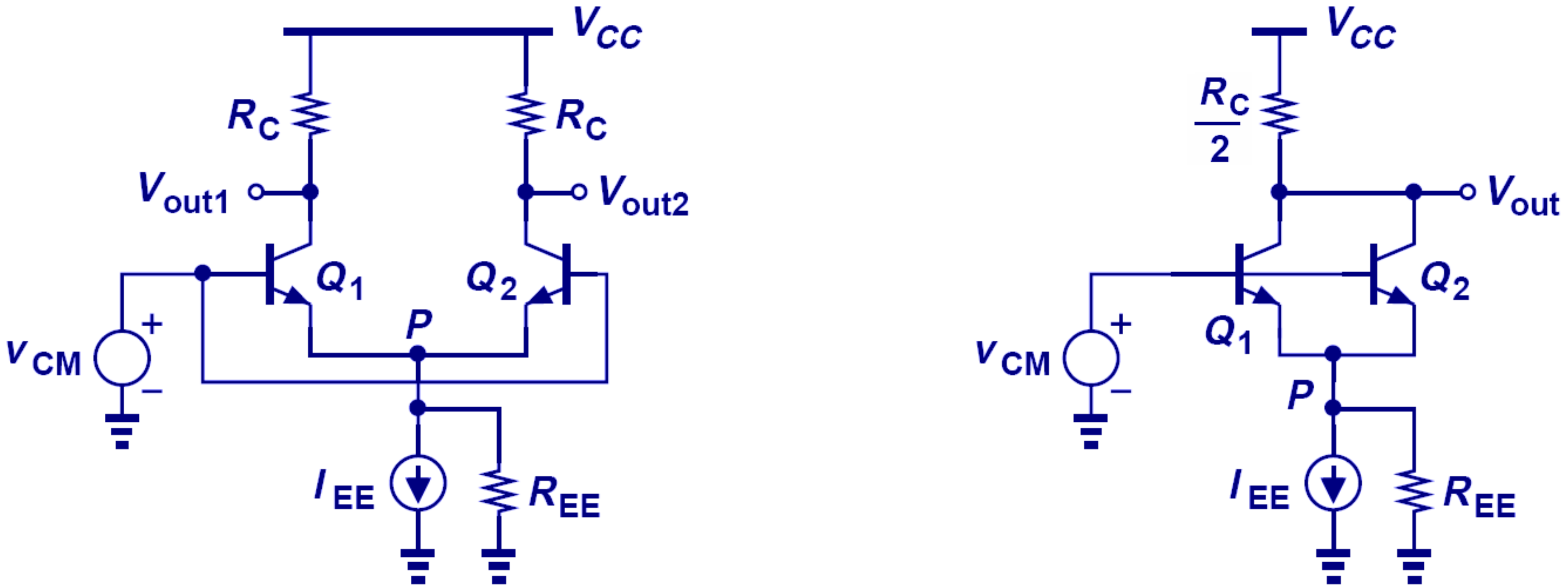
Example: MOS Telescopic Parasitic Resistance



$$R_{op} = \left[1 + g_{m5}\left(r_{O5} \parallel R_1\right)\right] r_{O7} + r_{O5} \parallel R_1$$

$$A_v \approx -g_{m1}\left(R_{op} \parallel r_{O3} g_{m3} r_{O1}\right)$$

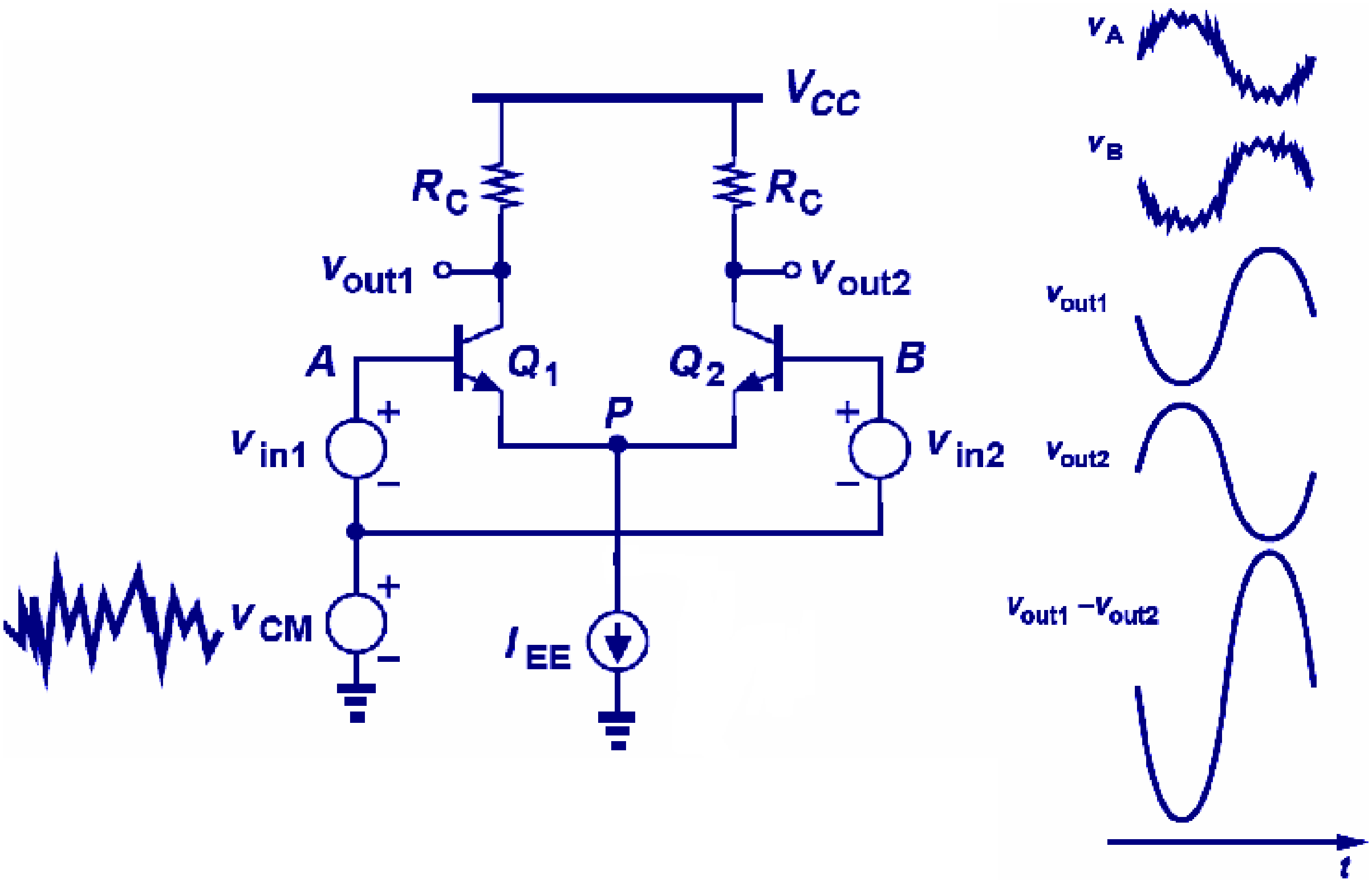
Effect of Finite Tail Impedance



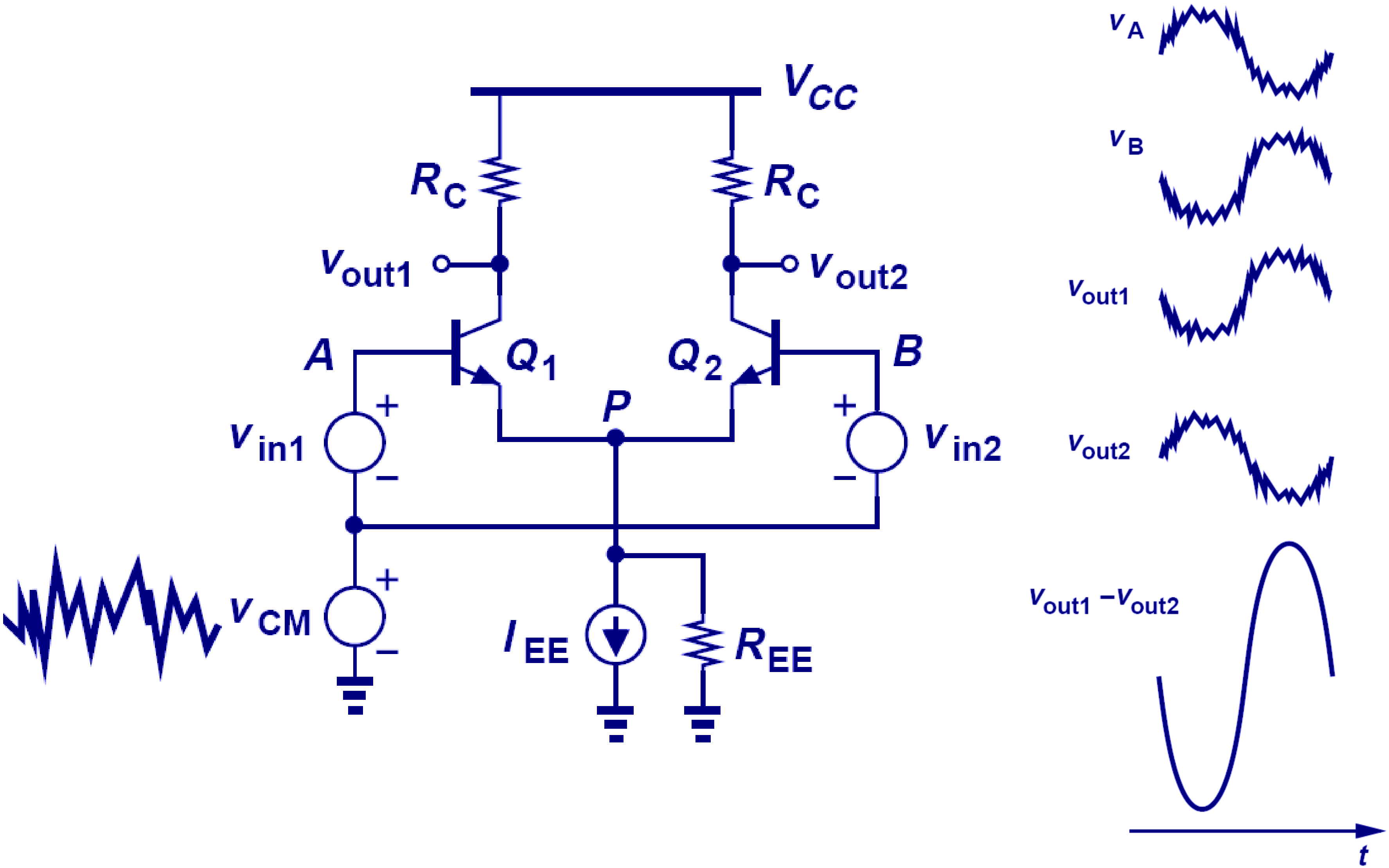
$$\frac{\Delta V_{out,CM}}{\Delta V_{in,CM}} = -\frac{R_C / 2}{R_{EE} + 1/2g_m}$$

- **If the tail current source is not ideal, then when a input CM voltage is applied, the currents in Q_1 and Q_2 and hence output CM voltage will change.**

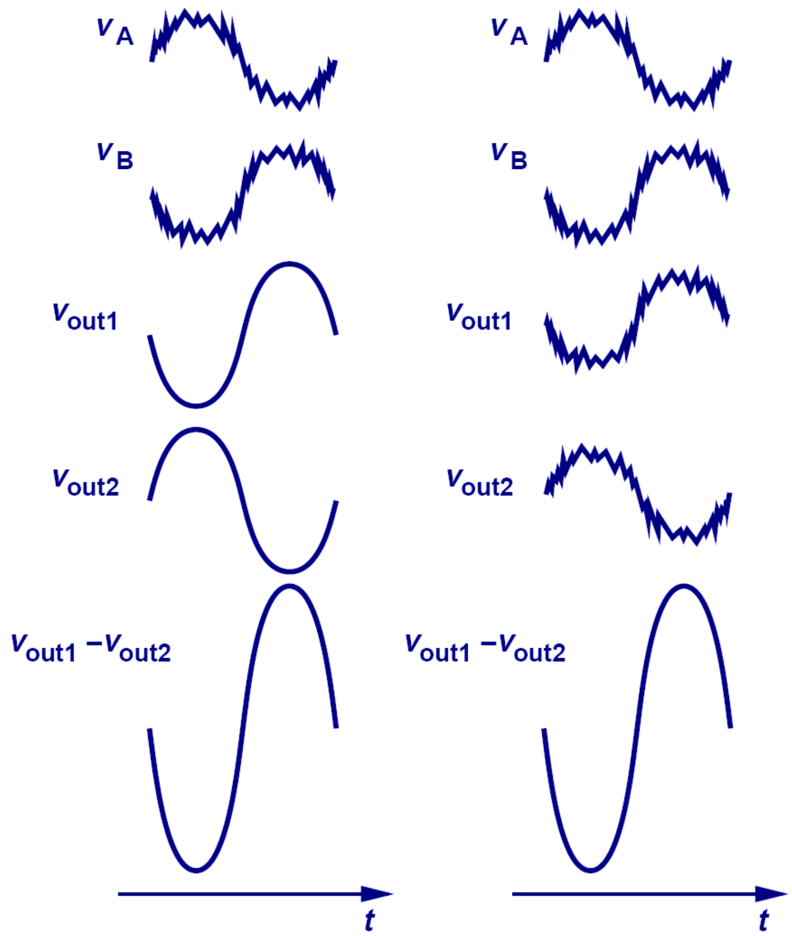
Input CM Noise with Ideal Tail Current



Input CM Noise with Non-ideal Tail Current

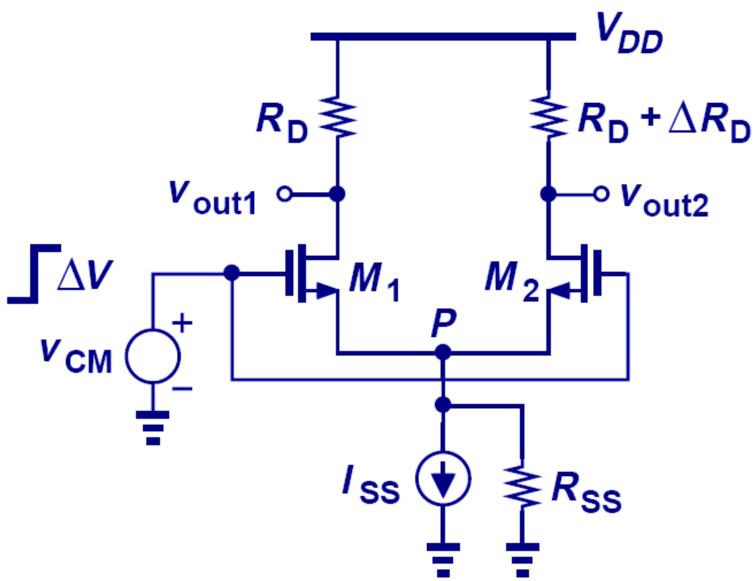


Comparison



- **As it can be seen, the differential output voltages for both cases are the same. So for small input CM noise, the differential pair is not affected.**

CM to DM Conversion, $A_{CM\text{-}DM}$



$$\Delta V_{CM} = \Delta V_{GS} + 2\Delta I_D R_{SS}$$

$$= \Delta I_D \left(\frac{1}{g_m} + 2R_{SS} \right), \quad \because \Delta V_{GS} = \frac{\Delta I_D}{g_m}$$

$$\Rightarrow \Delta I_D = \frac{\Delta V_{CM}}{\frac{1}{g_m} + 2R_{SS}}$$

$$\therefore \Delta V_{out} = \Delta V_{out1} - \Delta V_{out2}$$

$$= -\Delta I_D R_D + \Delta I_D \left(R_D + \Delta R_D \right)$$

$$= \Delta I_D \Delta R_D$$

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$$= \frac{\Delta V_{CM}}{1/g_m + 2R_{SS}} \Delta R_D$$

$$\Rightarrow \boxed{\left| \frac{\Delta V_{out}}{\Delta V_{CM}} \right| = \frac{\Delta R_D}{1/g_m + 2R_{SS}} \approx \frac{\Delta R_D}{2R_{SS}}}$$

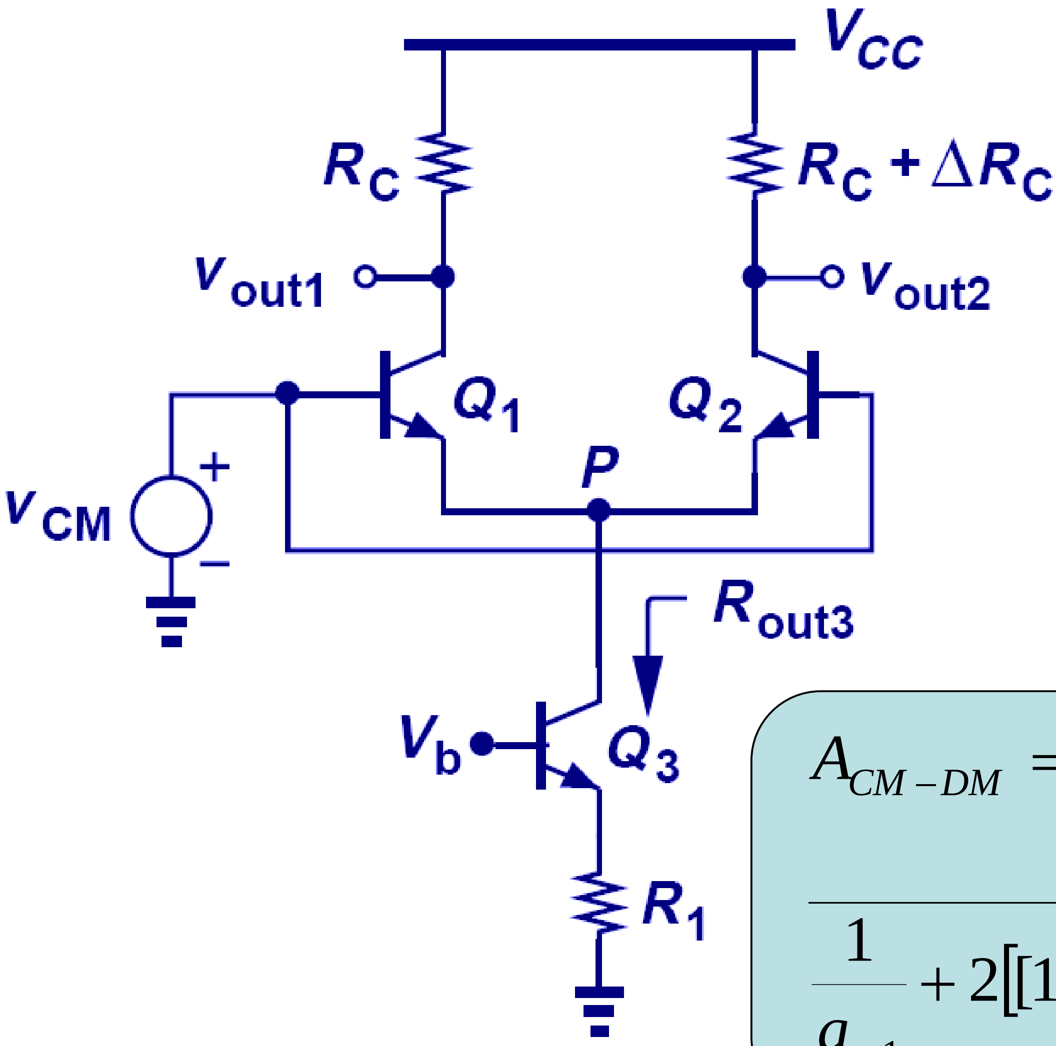
$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{GS1} - V_{TH} \right)^2$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{GS2} - V_{TH} \right)^2$$

$$I_{D1} = I_{D2} \ \ \& \ \ \Delta I_{D1} = \Delta I_{D2}, \quad \because V_{GS1} = V_{GS2}$$

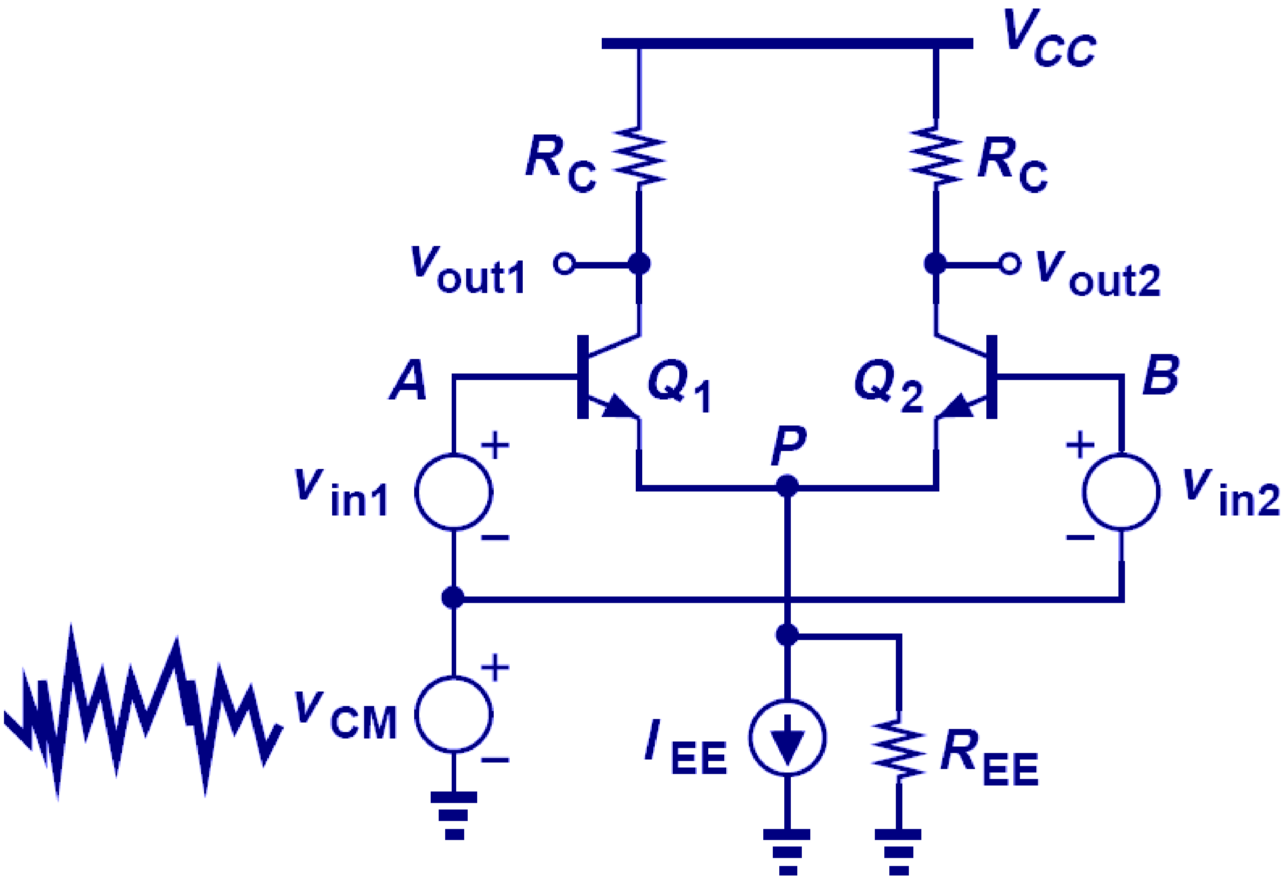
- If finite tail impedance and asymmetry are both present, then the differential output signal will contain a portion of input common-mode signal.

Example: A_{CM-DM}



$$A_{CM-DM} = \frac{\Delta R_C}{\frac{1}{g_{m1}} + 2\left[\left[1 + g_{m3}(R_1 \| r_{\pi 3})\right] r_{O3} + R_1 \| r_{\pi 3}\right]}$$

CMRR



$$CMRR = \frac{A_{DM}}{A_{CM-DM}}$$

- **CMRR defines the ratio of wanted amplified differential input signal to unwanted converted input common-mode noise that appears at the output.**

Example 10.28

- Calculate the CMRR of the circuit in Fig. 10.46.

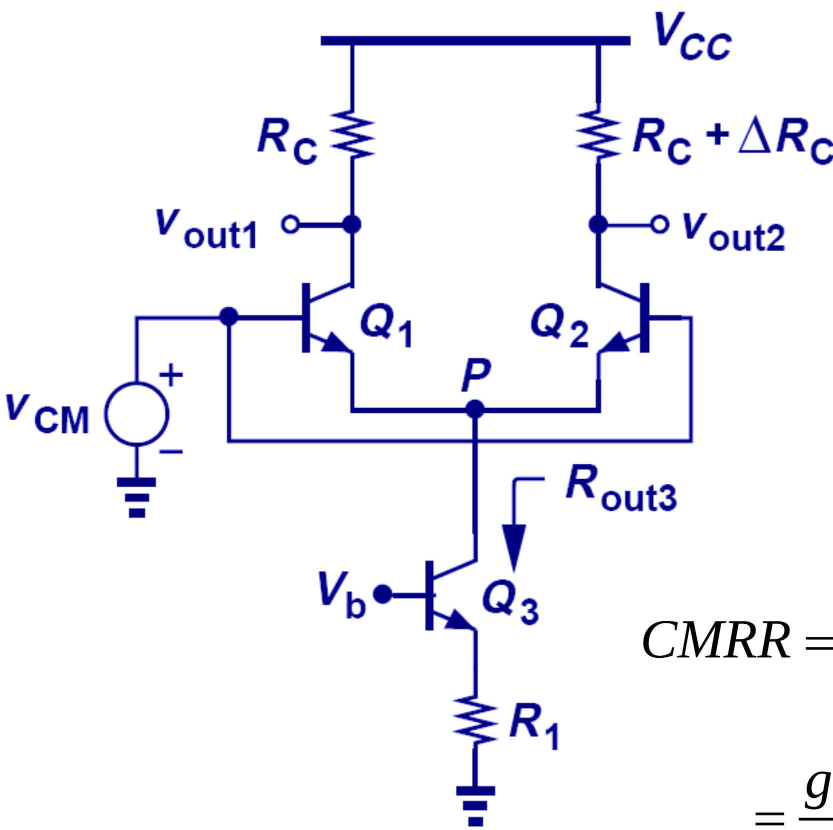
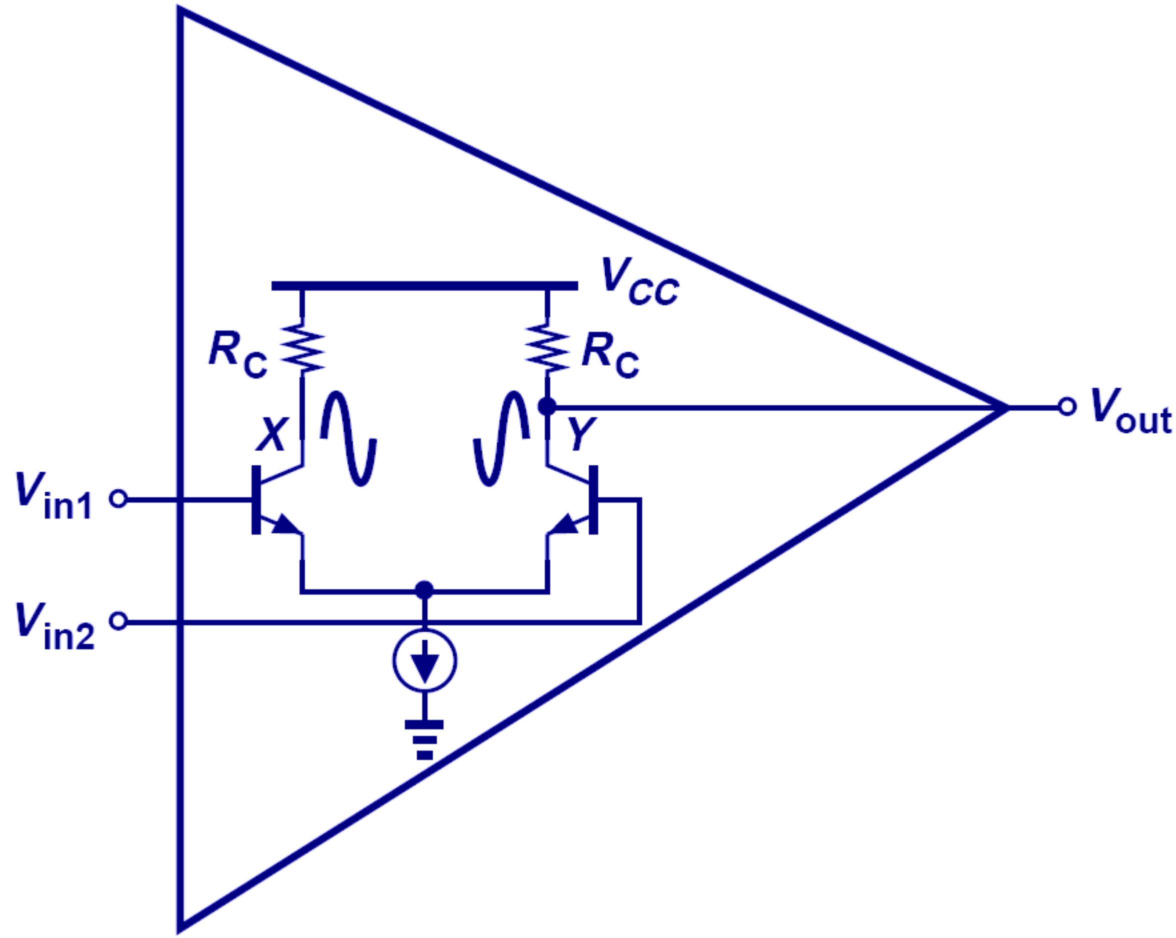


Figure10.46

$$CMRR = \frac{A_{DM}}{A_{CM-DM}} = \frac{g_{m1} R_C}{A_{CM-DM}}$$

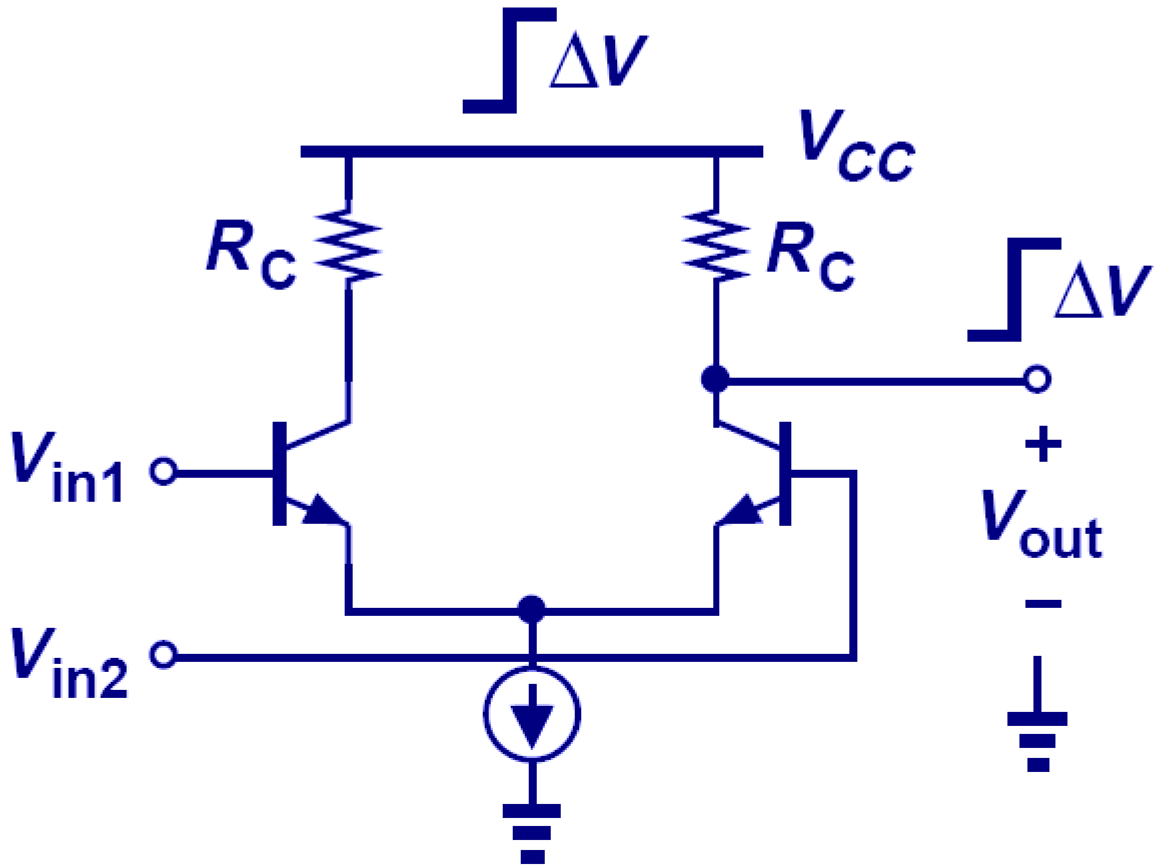
$$= \frac{g_{m1} R_C}{\Delta R_C} \left\{ \frac{1}{g_{m1}} + 2\left[\left[1 + g_{m3}(R_1 \| r_{\pi 3})\right] r_{O3} + R_1 \| r_{\pi 3}\right] \right\}$$

Differential to Single-ended Conversion



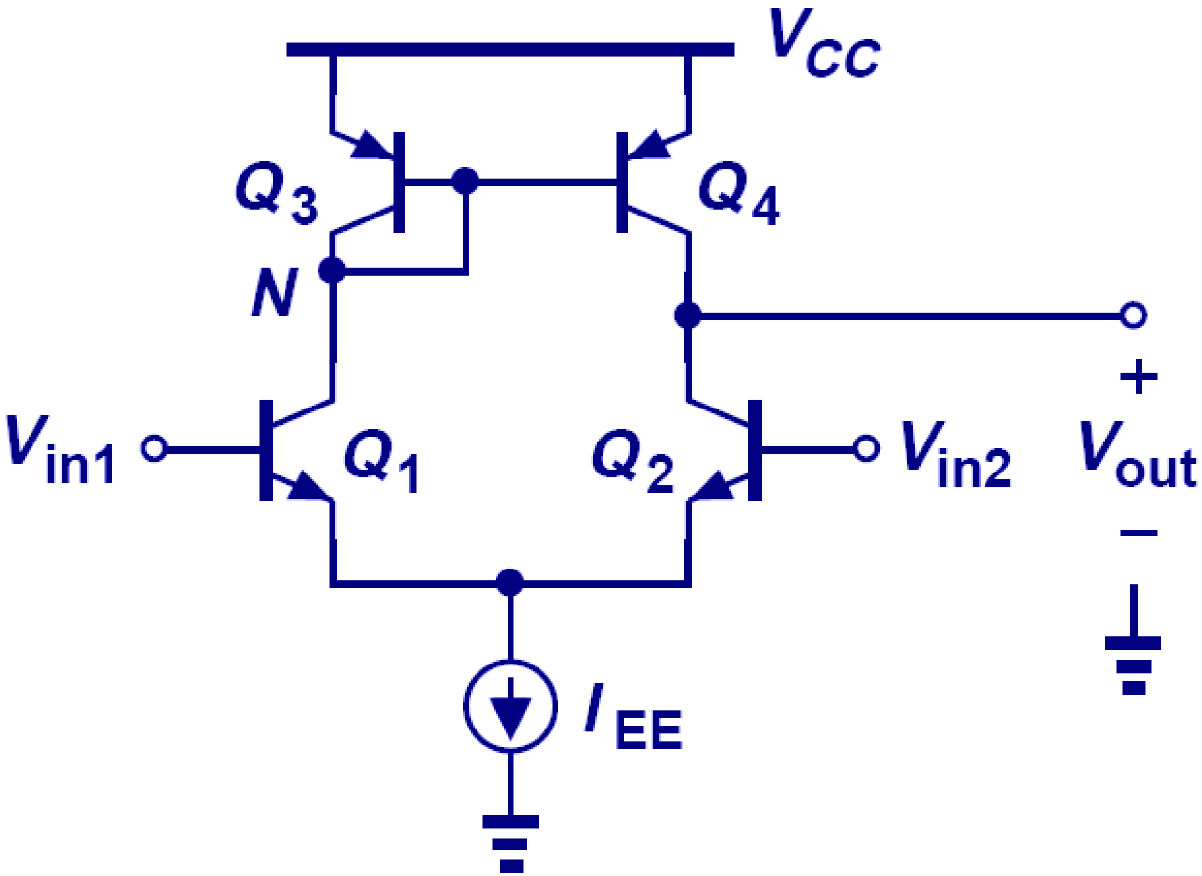
- Many circuits require a differential to single-ended conversion, however, the above topology is not very good.

Supply Noise Corruption



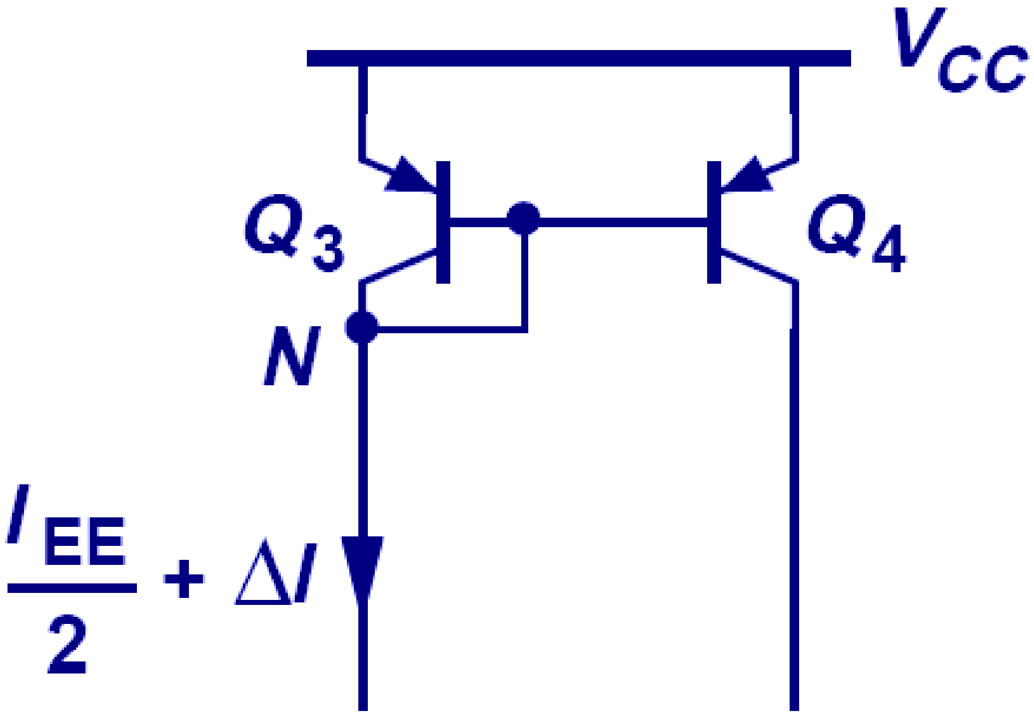
- The most critical drawback of this topology is supply noise corruption, since no common-mode cancellation mechanism exists. Also, we lose half of the signal.

Better Alternative



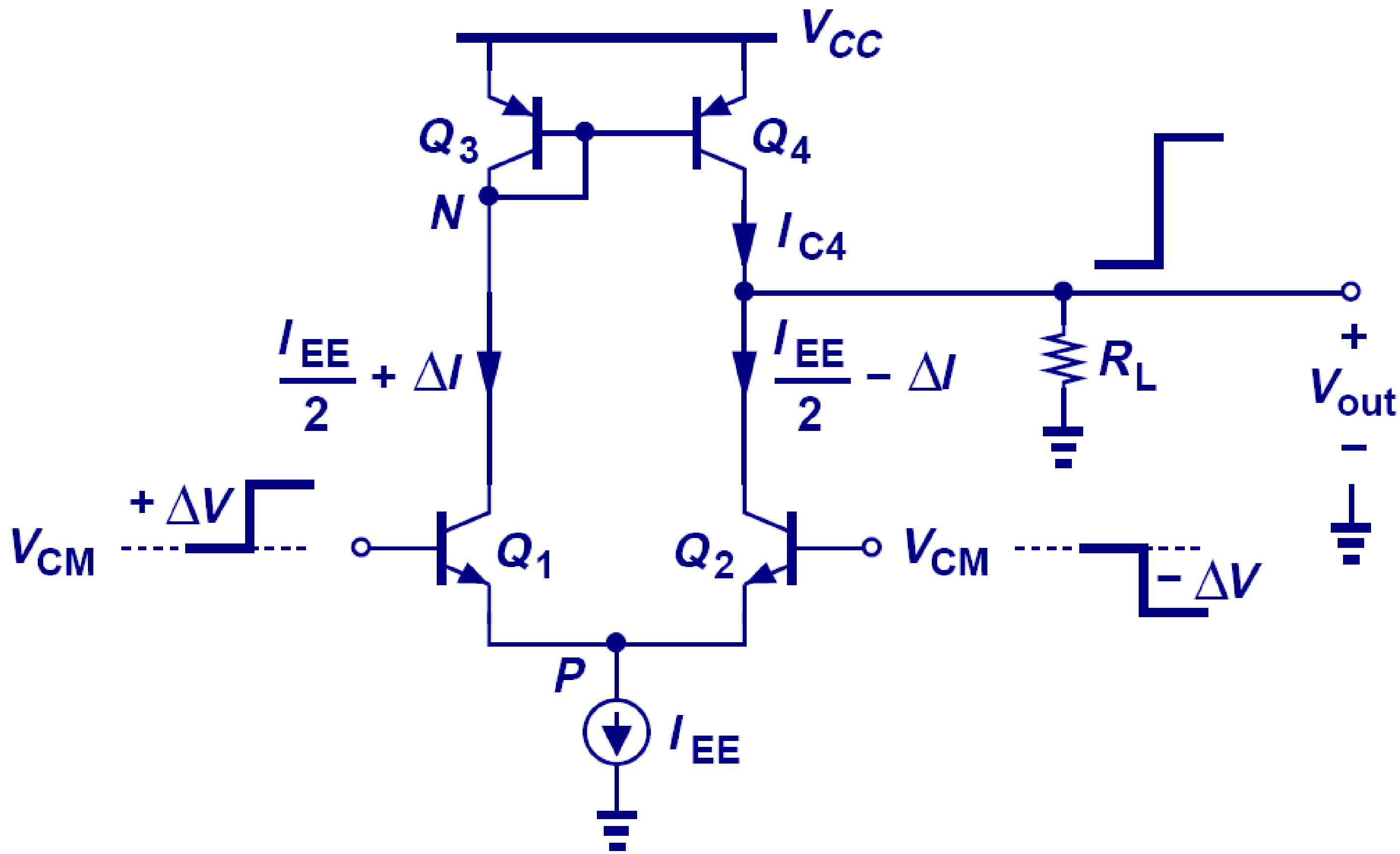
➢ **This circuit topology performs differential to single-ended conversion with no loss of gain.**

Active Load



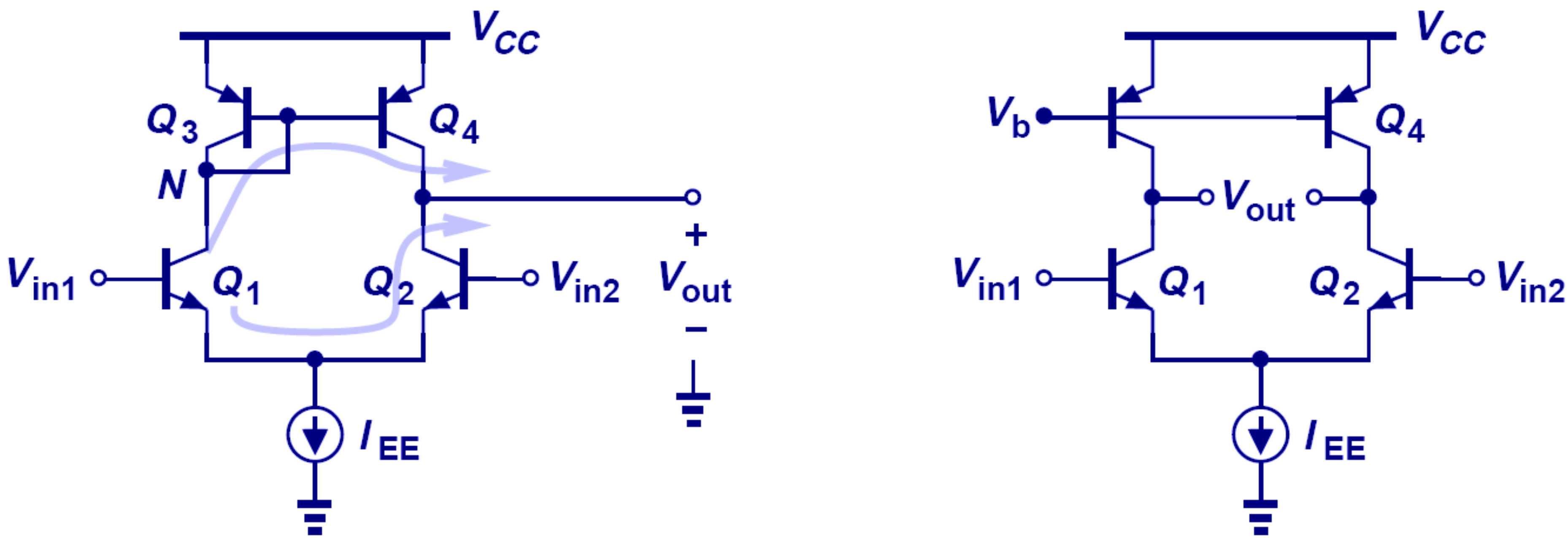
- With current mirror used as the load, the signal current produced by the Q_1 can be replicated onto Q_4.
- This type of load is different from the conventional "static load" and is known as an "active load".

Differential Pair with Active Load



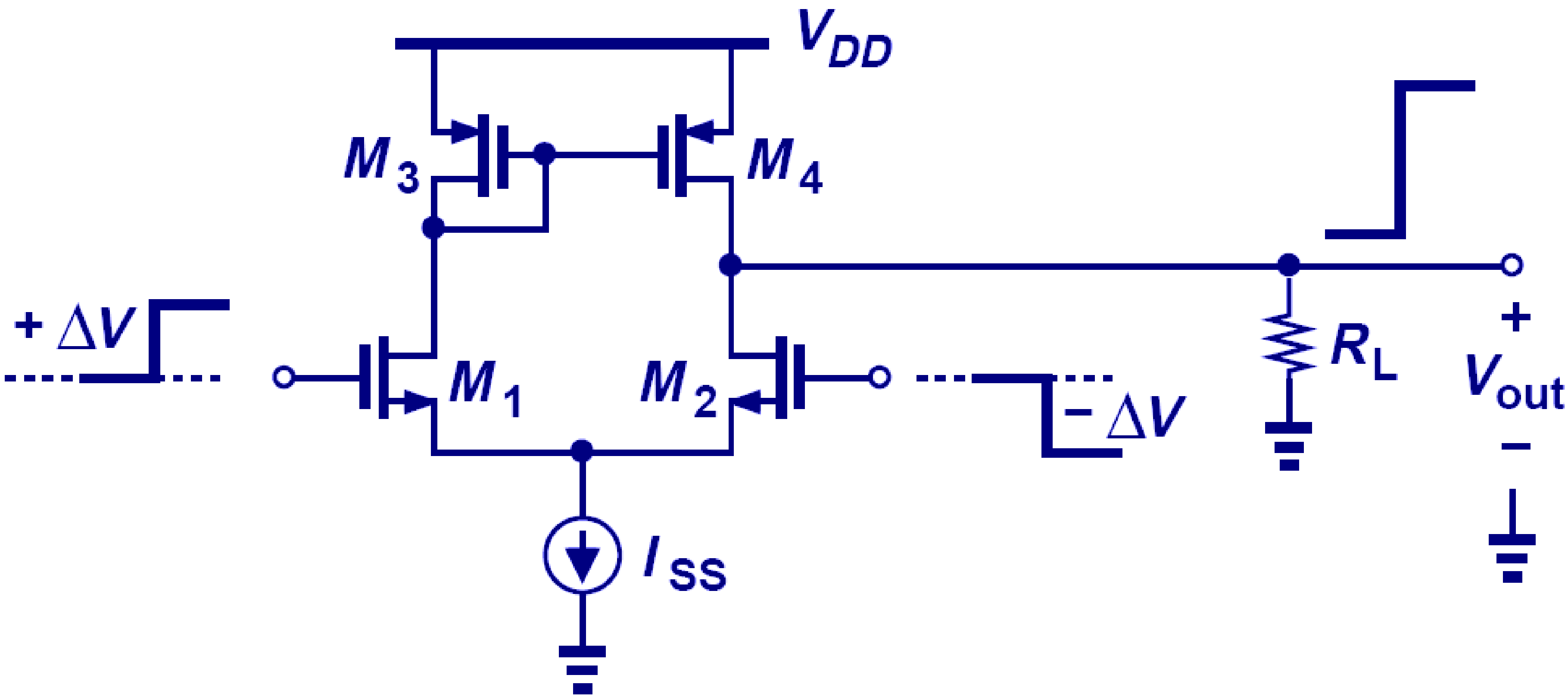
- The input differential pair decreases the current drawn from R_L by ΔI and the active load pushes an extra ΔI into R_L by current mirror action; these effects enhance each other.

Active Load vs. Static Load



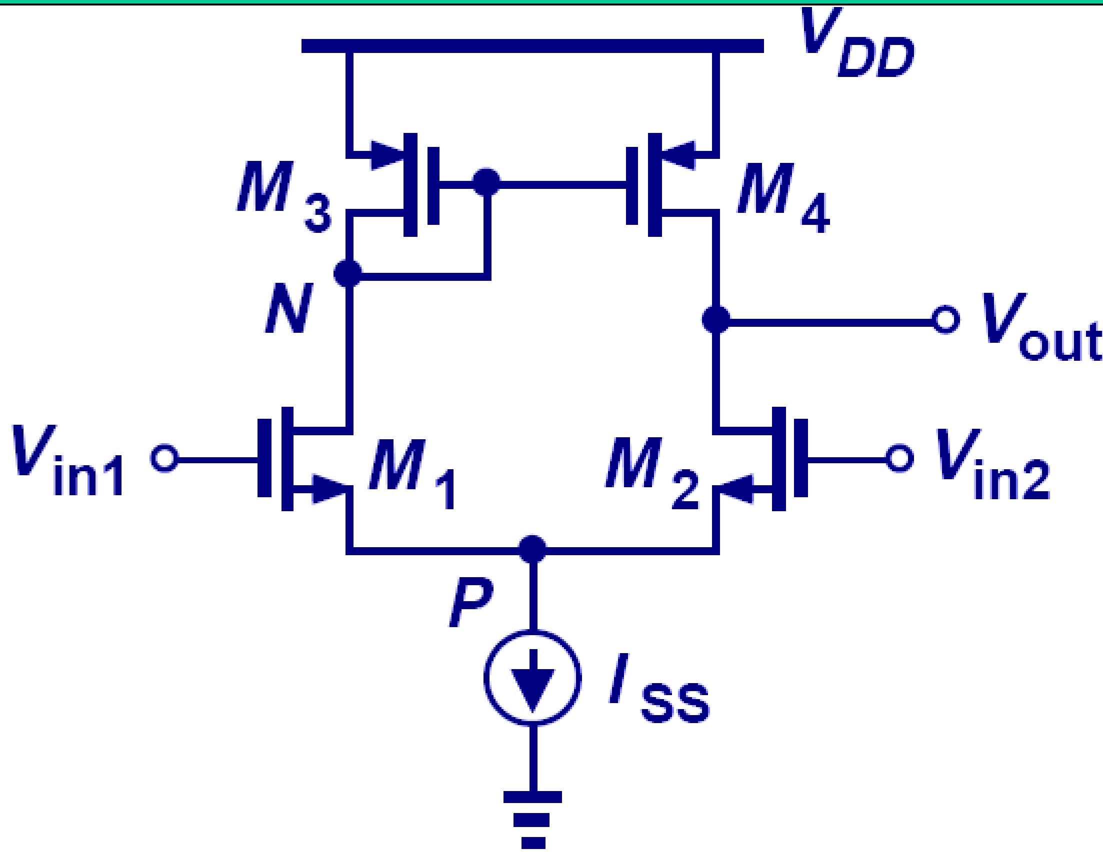
- **The load on the left responds to the input signal and enhances the single-ended output, whereas the load on the right does not.**

MOS Differential Pair with Active Load



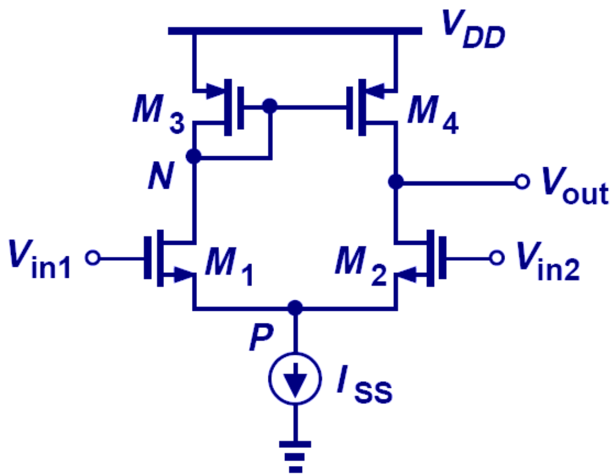
- Similar to its bipolar counterpart, MOS differential pair can also use active load to enhance its single-ended output.

Asymmetric Differential Pair



- Because of the vastly different resistance magnitude at the drains of M_1 and M_2, the voltage swings at these two nodes are different and therefore node P cannot be viewed as a virtual ground when $V_{in2}=-V_{in1}$.

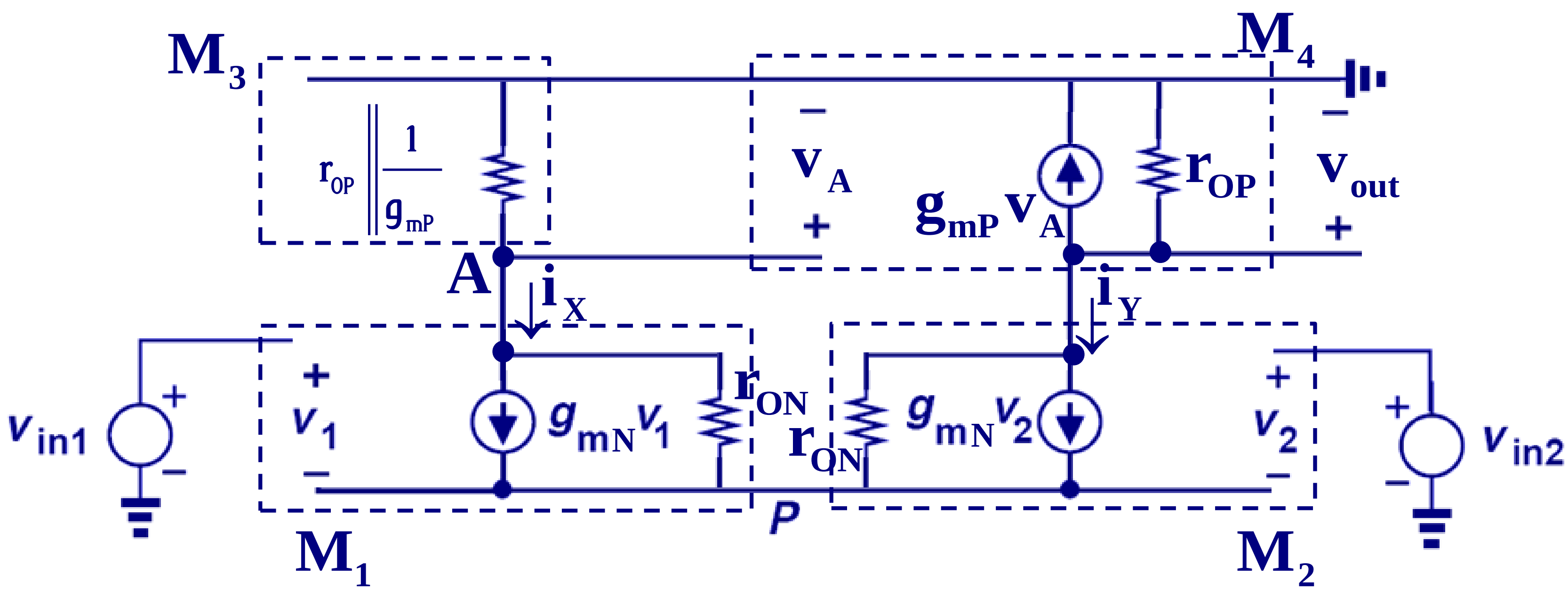
Quantitative Analysis - Approach 1



$$i_X = -i_Y \quad \& \quad v_A = -i_X \left(g_{mP}^{-1} \| r_{OP} \right)$$

$$-i_Y = \frac{v_{out}}{r_{OP}} + g_{mP} v_A = \frac{v_{out}}{r_{OP}} - g_{mP} i_X \left(g_{mP}^{-1} \| r_{OP} \right) = i_X$$

$$\Rightarrow i_X = \frac{v_{out}}{r_{OP}\left[1 + g_{mP}\left(g_{mP}^{-1} \| r_{OP} \right)\right]}$$



Quantitative Analysis - Approach 1 – cont'd

$$-v_A + \left(i_X - g_{mN} v_1\right) r_{ON} - \left(i_Y - g_{mN} v_2\right) r_{ON} + v_{out} = 0$$

$$\Rightarrow -v_A + 2 i_X r_{ON} - g_{mN} r_{ON} \left(v_{in1} - v_{in2}\right) + v_{out} = 0$$

$$\because v_1 - v_2 = v_{in1} - v_{in2} \quad \& \quad i_X = -i_Y$$

Substituting for v_A and i_X,

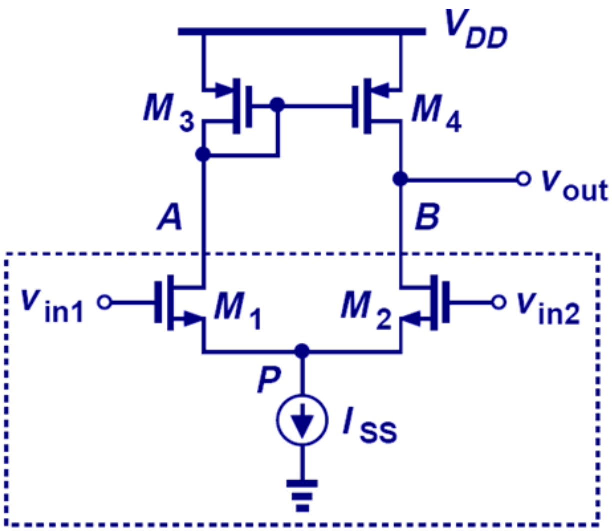
$$\frac{v_{out}}{r_{OP}\left[1 + g_{mP}\left(g_{mP}^{-1} \| r_{OP}\right)\right]}\left(g_{mP}^{-1} \| r_{OP}\right) + 2 r_{ON} \frac{v_{out}}{r_{OP}\left[1 + g_{mP}\left(g_{mP}^{-1} \| r_{OP}\right)\right]}$$

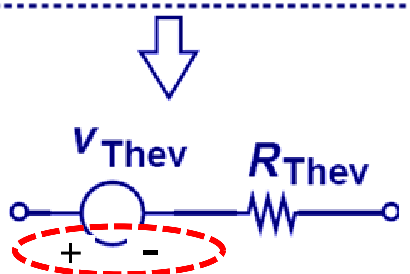
$$+ v_{out} = g_{mN} r_{ON} \left(v_{in1} - v_{in2}\right)$$

$$\Rightarrow \frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN} r_{ON} \frac{r_{OP}\left[1 + g_{mP}\left(g_{mP}^{-1} \| r_{OP}\right)\right]}{2 r_{ON} + 2 r_{OP}}$$

$$\approx g_{mN} \left(r_{ON} \| r_{OP}\right)$$

Quantitative Analysis - Approach 2





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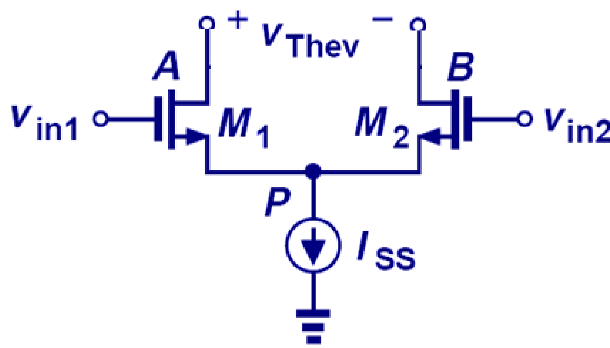

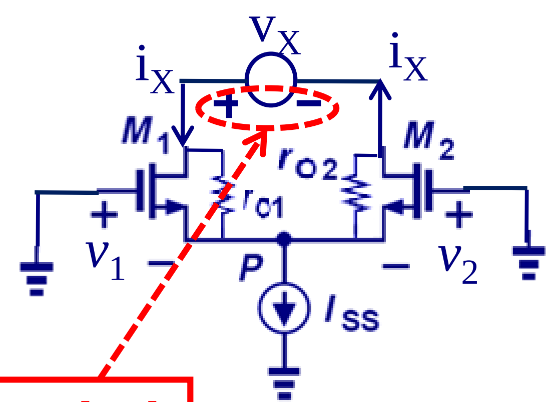

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$$v_{Thev} = -g_{mN} r_{oN} (v_{in1} - v_{in2})$$

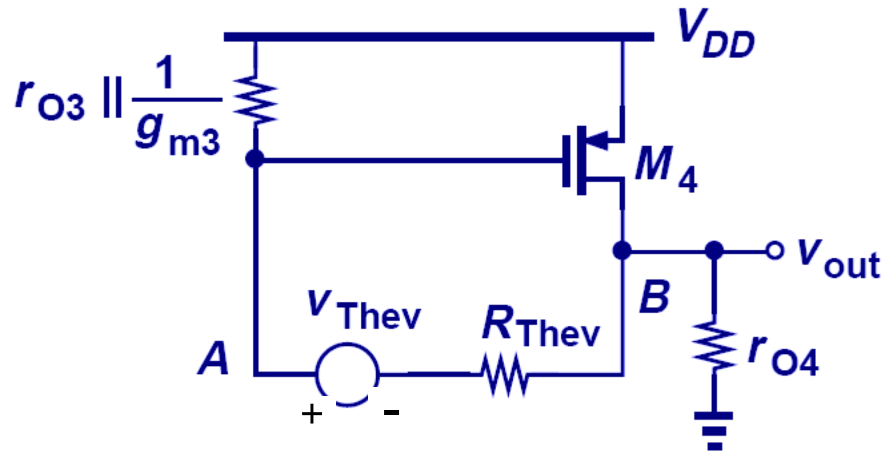
$$R_{Thev} = 2r_{oN}$$

$$\because v_1 = v_2 \;\; \& \;\; (i_X - g_{m1} v_1) r_{O1} + (i_X + g_{m2} v_2) r_{O2} = v_X$$

Quantitative Analysis - Approach 2 – cont'd

$$v_A = \frac{\frac{1}{g_{m3}} \| r_{O3}}{\frac{1}{g_{m3}} \| r_{O3} + R_{Thev}} \left(v_{out} + v_{Thev} \right)$$

$$g_{m4} v_A + \frac{v_{out}}{r_{O4}} + \frac{v_{out} + v_{Thev}}{\frac{1}{g_{m3}} \| r_{O3} + R_{Thev}} = 0$$



$$\Rightarrow \left(g_{m4} \frac{\frac{1}{g_{m3}} \| r_{O3}}{\frac{1}{g_{m3}} \| r_{O3} + R_{Thev}} + \frac{1}{\frac{1}{g_{m3}} \| r_{O3} + R_{Thev}} \right) \left(v_{out} + v_{Thev} \right) + \frac{v_{out}}{r_{O4}} = 0$$

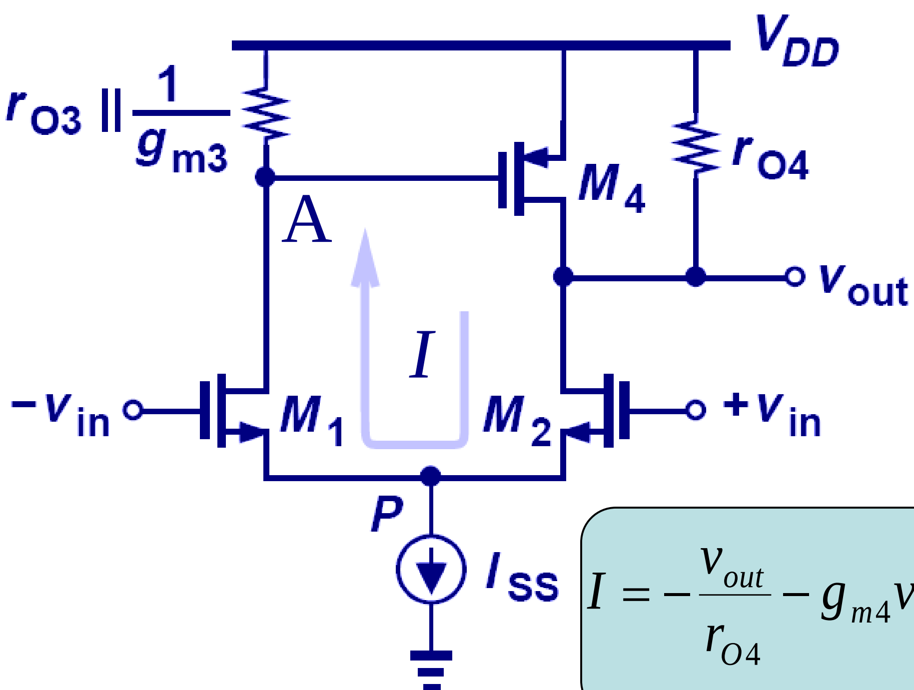
$$\Rightarrow \frac{2}{R_{Thev}} \left(v_{out} + v_{Thev} \right) + \frac{v_{out}}{r_{O4}} = 0 \ \left(\because \frac{1}{g_{m3}} \| r_{O3} << R_{Thev} \text{ and } g_{m3} = g_{m4} \right)$$

$$\Rightarrow v_{out} \left(\frac{1}{r_{ON}} + \frac{1}{r_{OP}} \right) = \frac{g_{mN} r_{ON} \left(v_{in1} - v_{in2} \right)}{r_{ON}}$$

$$\Rightarrow \frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN} \left(r_{ON} \| r_{OP} \right)$$

Example 10.29

- Prove that the voltage swing at node A is much less than that at the output.



$$I = -\frac{v_{out}}{r_{O4}} - g_{m4}v_A$$

$$v_A = -\left(\frac{v_{out}}{r_{O4}} + g_{m4}v_A\right)\left(\frac{1}{g_{m3}} \| r_{O3}\right)$$

$$\approx -\left(\frac{v_{out}}{r_{O4}} + g_{m4}v_A\right)\frac{1}{g_{m3}}$$

$$\Rightarrow v_A \approx -\frac{v_{out}}{r_{O4}g_{m3}} - v_A$$

$$\Rightarrow v_A \approx -\frac{v_{out}}{2r_{O4}g_{m3}}$$