Topics in IC (Wireline Transceiver Design)

Dept. of Electrical and Computer Engineering
Seoul National University

Fall 2020

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Key words: VCOs, ILOs, PLLs, DLLs, CDRs, PAM4, equalization

Course Overview:

The class covers various topics in integrated circuit design for high-speed wireline transceiver design. After a brief introduction to timing jitter representation, various topics on timing and signaling circuits such as VCOs, ILOs, PLLs, DLLs, CDRs, PAM4 signaling, timing recovery, equalization, and bandwidth extension techniques are discussed including their architecture, circuits, stability, performance, and so on. A few design examples are shown as a case study. At the end of the semester, a class project will be performed on the topic of the student's own choice. The topic must include practical problems faced by typical high-speed transceiver designers.

Class Web Page: http://isdl.snu.ac.kr

Class Room and Hours: 301-821, Mon, Wed 11:00AM-12:15PM

Prerequisites: Digital IC Design (undergraduate)

Textbooks and References:

Collection of papers and presentation materials

Grading:

Midterm Exam 20%, Final Exam 20%, Homework 30%, Design Project 30%

HWs - zero score on copied HWs, two grades down in final grade

Exams - final grade F on cheating

Design Project - final grade F on plagiarism, falsification, or fabrication

Topics Covered and Course Schedule (Tentative)

1. Timing Conventions (1.5 weeks)
    A. Skew and Jitter
    B. Phase Noise
2. Phase-Locked Loops (1.5 weeks)
    A. Building Blocks (PD, PFD, LF, VCO, CP, and so on)
    B. Stability
    C. Frequency Synthesizers
    D. All-Digital PLLs
3. Delay-Locked Loops (1.5 weeks)
    A. Building Blocks (PD, LF, DCDL, and so on)
    B. Stability
    C. All-Digital DLLs
4. Clock and Data Recovery (1.5 weeks)
    A. Building Blocks
    B. Stability
    C. Jitter Tolerance
5. Injection Locked Oscillators (1.5 weeks)
    A. Theory
    B. Frequency Tuning
    C. Injection techniques
6. Channels and Equalizers (1.5 weeks)
    A. Pre-emphasis
    B. Continuous-Time Linear Equalizers
    C. DFE
7. Samplers and Drivers (1.5 weeks)
    A. Samplers and Meta-stability
    B. Offset Cancellation
    C. Drivers and Termination
    D. PAM4 signaling
8. Bandwidth extension techniques (1 week)
    A. Inductor peaking
    B. T-Coil
9. LDO and bandgap reference (1 week)
10. Design Examples (1 week)
    A. DDR5
    B. PCIe
    C. Display Port

Mid-Term Exam: 10/26/2020

Final Exam: 12/9/2020

Term Project Proposal Submission: 11/4/2020

Term Project Presentation and Final Report Submission: 12/14/2020

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